General Description

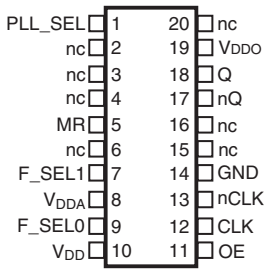
The ICS874001I-05 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874001I-05 has a bandwidth of 6MHz with <1dB peaking, easily meeting PCI Express Gen2 PLL requirements.

The ICS874001I-05 uses IDT's 3RD Generation FemtoClock® PLL technology to achieve the lowest possible phase noise. The device is packaged in a small 20-pin TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

Features

- One differential LVDS output pair
- One differential clock input
- CLK, nCLK supports the following input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 640MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 50ps (maximum)
- Full 3.3V operating supply
- PCI Express (2.5Gb/s) and Gen 2 (5 Gb/s) jitter compliant
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



ICS874001I-05
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body
G Package
Top View

Block Diagram

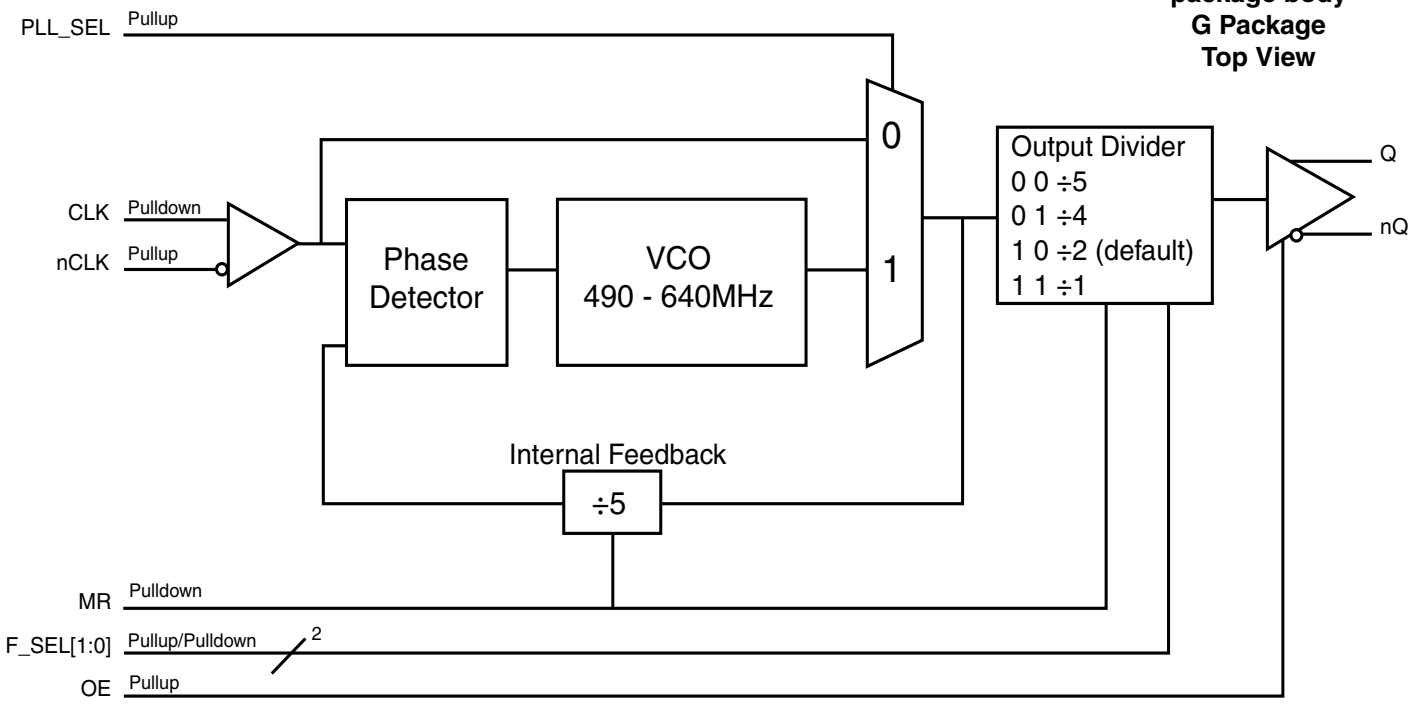


Table 1. Pin Descriptions

Number	Name	Type		Description
1	PLL_SEL	Input	Pullup	PLL select pin. When LOW, bypasses the PLL. When HIGH selects the PLL. LVCMOS/LVTTL interface levels. See Table 3B.
2, 3, 4, 6, 15, 16, 20	nc	Unused		No connect.
5	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go LOW and the inverted output nQ to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	F_SEL1	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3C.
8	V_{DDA}	Power		Analog supply pin.
9	F_SEL0	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3C.
10	V_{DD}	Power		Core supply pin.
11	OE	Input	Pullup	Output enable. When HIGH, outputs are enabled. When LOW, forces outputs to a High-Impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
17, 18	nQ, Q	Output		Differential output pair. LVDS interface levels.
19	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Inputs	Outputs
OE	**Q, nQ**
0	High-Impedance
1 (default)	Enabled

Table 3B. PLL_SEL Control Table

Inputs	
PLL_SEL	**Function**
0	Bypass
1	VCO (default)

Table 3C. F_SELx Function Table

Inputs			
F_SEL1	**F_SEL0**	**Output Divider**	**Output Frequency (MHz)**
0	0	÷5	98 - 128
0	1	÷4	122.5 - 160
1	0	÷2	245 - 320 (default)
1	1	÷1	490 - 640

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				75	mA
I_{DDA}	Analog Supply Current				13	mA
I_{DDO}	Output Supply Current				25	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PLL_SEL, F_SEL1, OE	$V_{DD} = V_{IN} = 3.6V$			5	µA
		F_SEL0, MR	$V_{DD} = V_{IN} = 3.6V$			150	µA
I_{IL}	Input Low Current	PLL_SEL, F_SEL1, OE	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-150			µA
		F_SEL0, MR	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-5			µA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.6V$			150	µA
		nCLK	$V_{DD} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-5			µA
		nCLK	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275	375	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.20	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

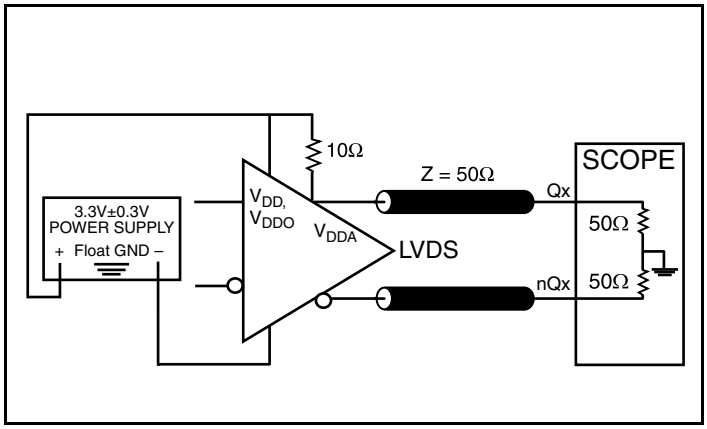
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

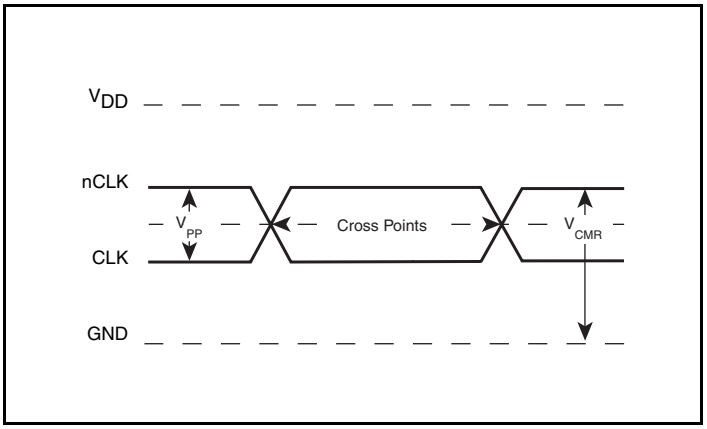
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98		640	MHz
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1				50	ps
T_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 2, 4	100MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		16.14		ps
		125MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		15.64		ps
		250MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		13.16		ps
		500MHz, (1.2MHz –21.9MHz), Evaluation Band: 0Hz - Nyquist (clock frequency/2)		12.17		ps
$T_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 3, 4	100MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.4		ps
		125MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.39		ps
		250MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.18		ps
		500MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.11		ps
$T_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 3, 4	100MHz output, Low Band: 10kHz - 1.5MHz		0.33		ps
		125MHz output, Low Band: 10kHz - 1.5MHz		0.22		ps
		250MHz output, Low Band: 10kHz - 1.5MHz		0.22		ps
		500MHz output, Low Band: 10kHz - 1.5MHz		0.22		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle	F_SEL[10] ≠ 11	48		52	%
		F_SEL[10] = 11	42		58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 3: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 4: Guaranteed only when input clock source is PCI Express and PCI Express Gen 2 compliant.

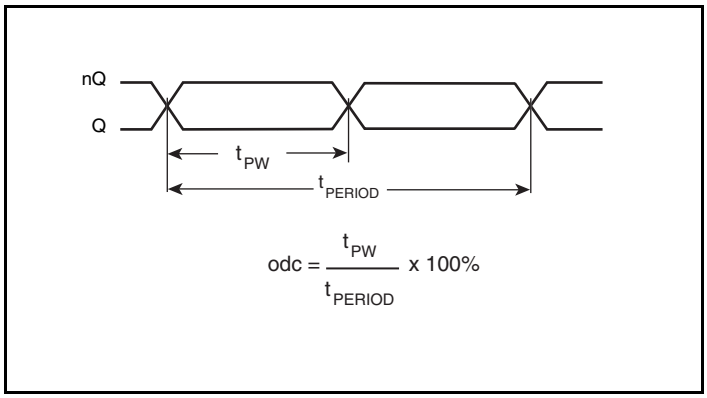
Parameter Measurement Information



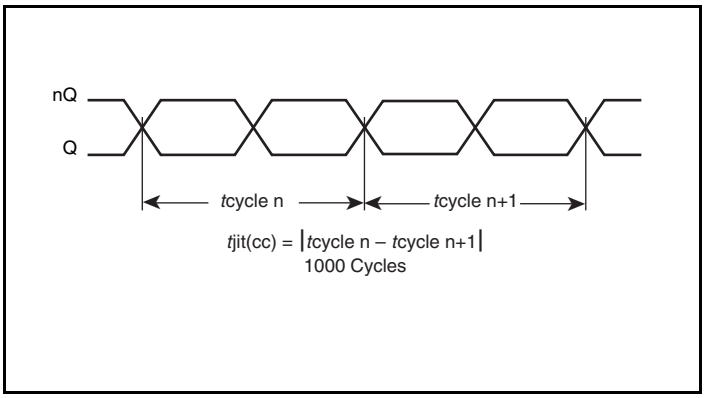
3.3V LVDS Output Load AC Test Circuit



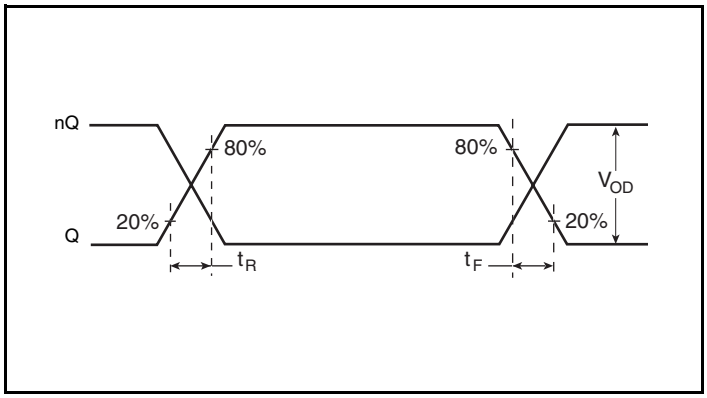
Differential Input Level



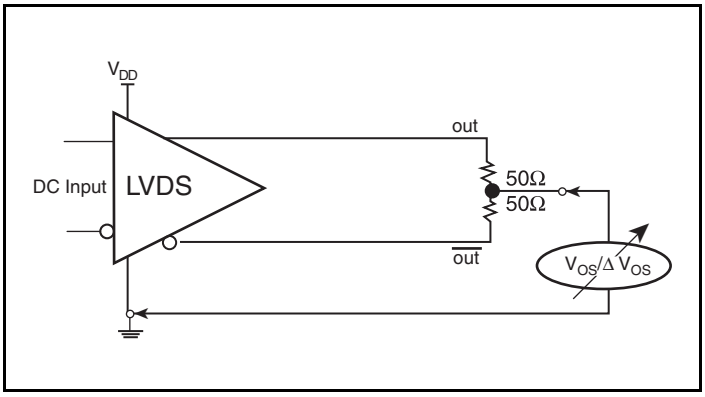
Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter

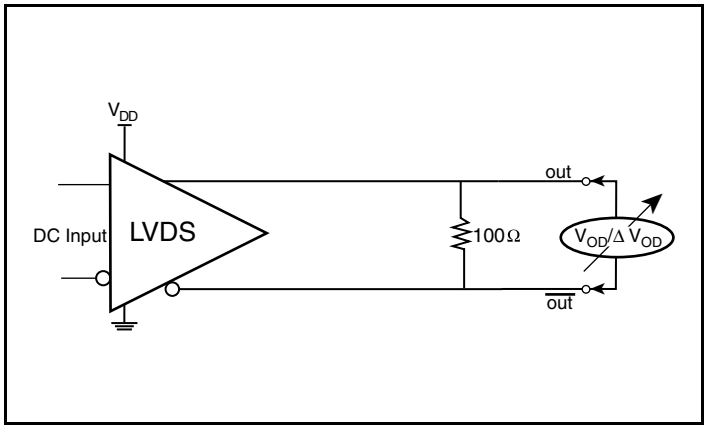


Output Rise/Fall Time



Offset Voltage Setup

Parameter Measurement Information, continued



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

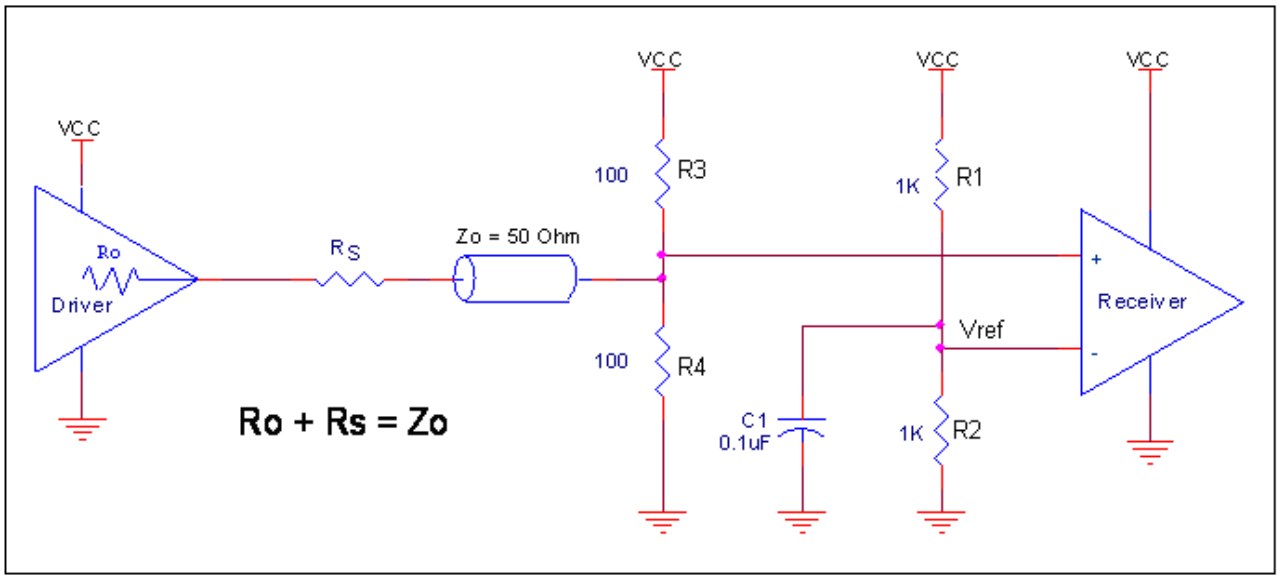
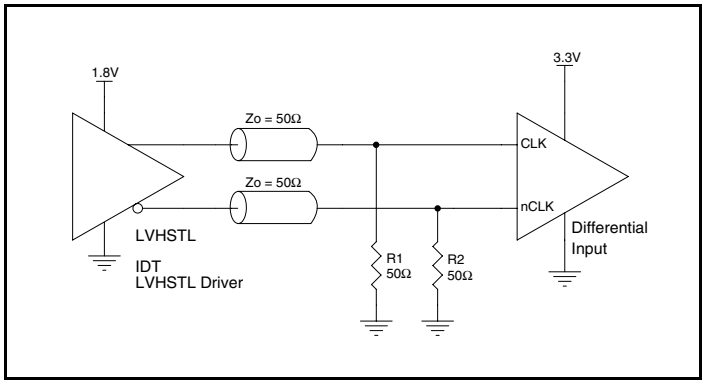


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

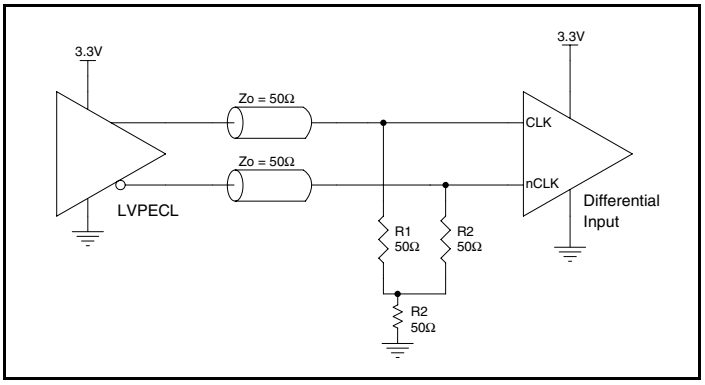


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

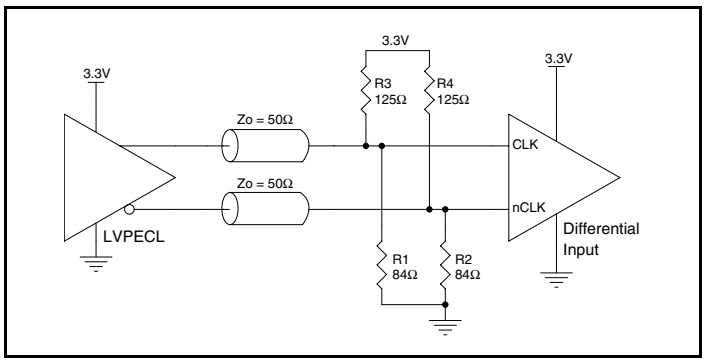


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

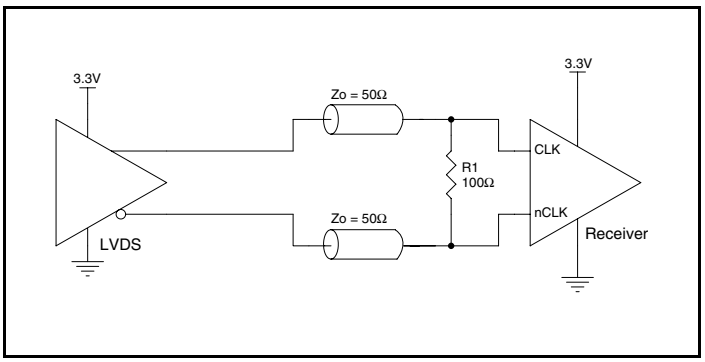


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

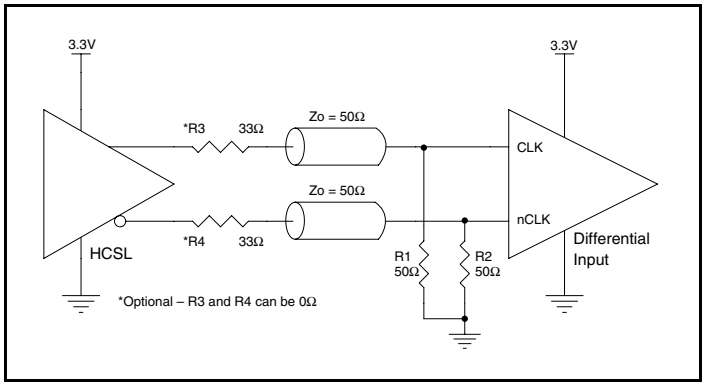


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

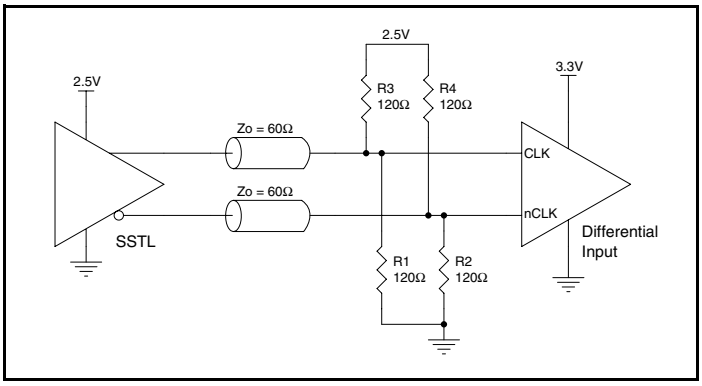


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 3 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

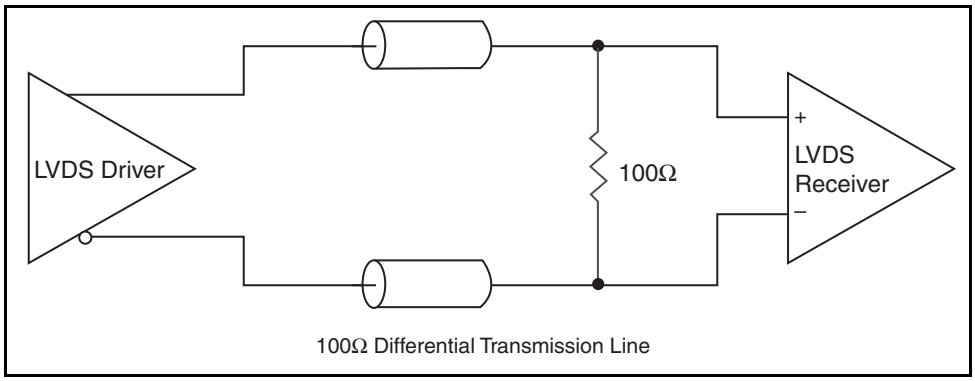


Figure 3. Typical LVDS Driver Termination

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

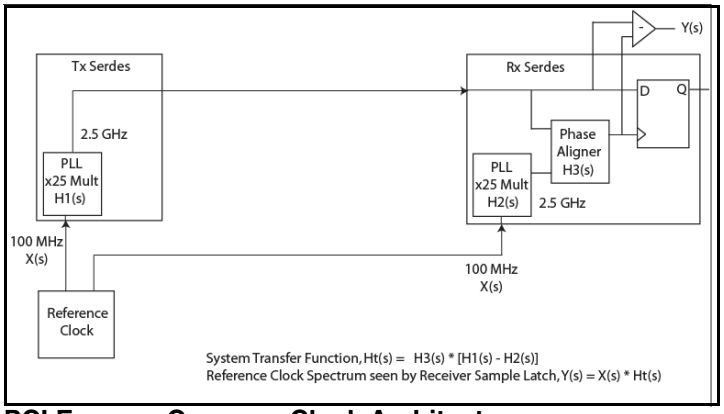
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

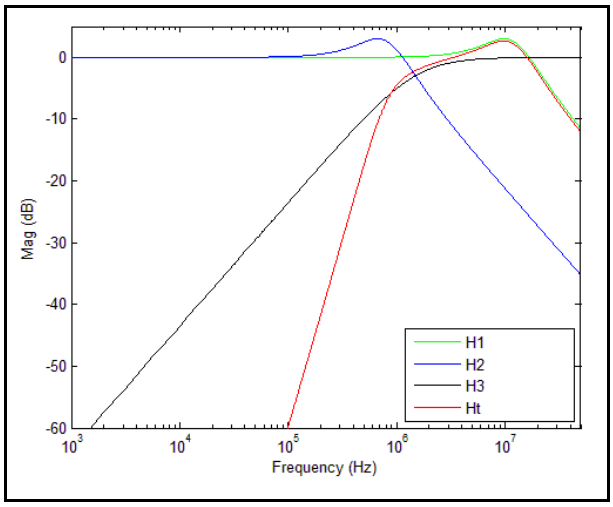
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



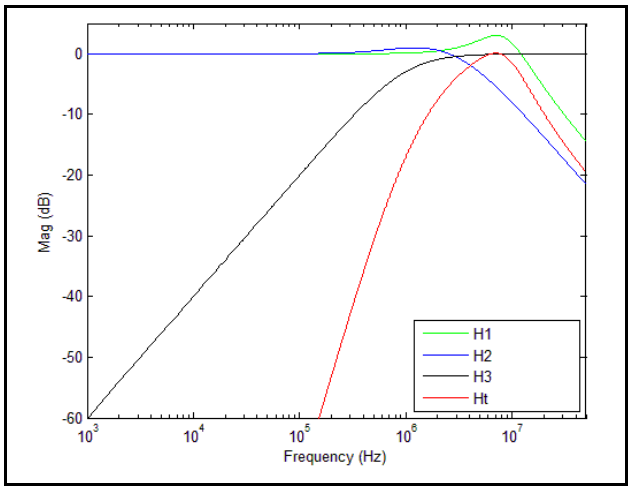
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

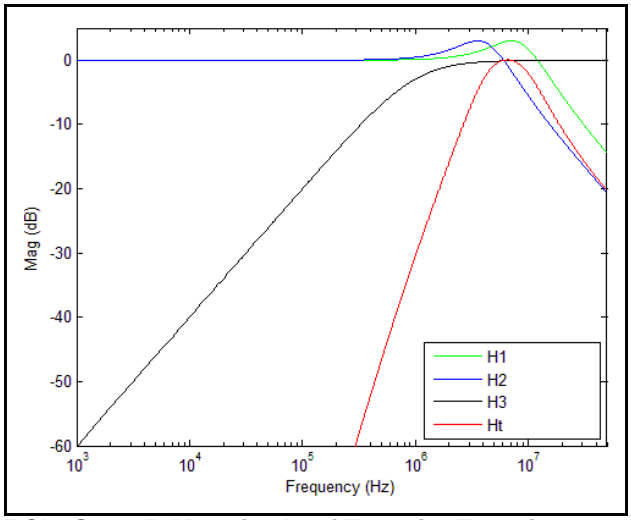


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Schematic Layout

Figure 4 shows an example of ICS874001I-05 application schematic. In this example, the device is operated at $V_{DD} = V_{DDA} = V_{DDO} = 3.3V$. The input is driven by a 3.3V LVPECL driver.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The ICS74001I-05 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

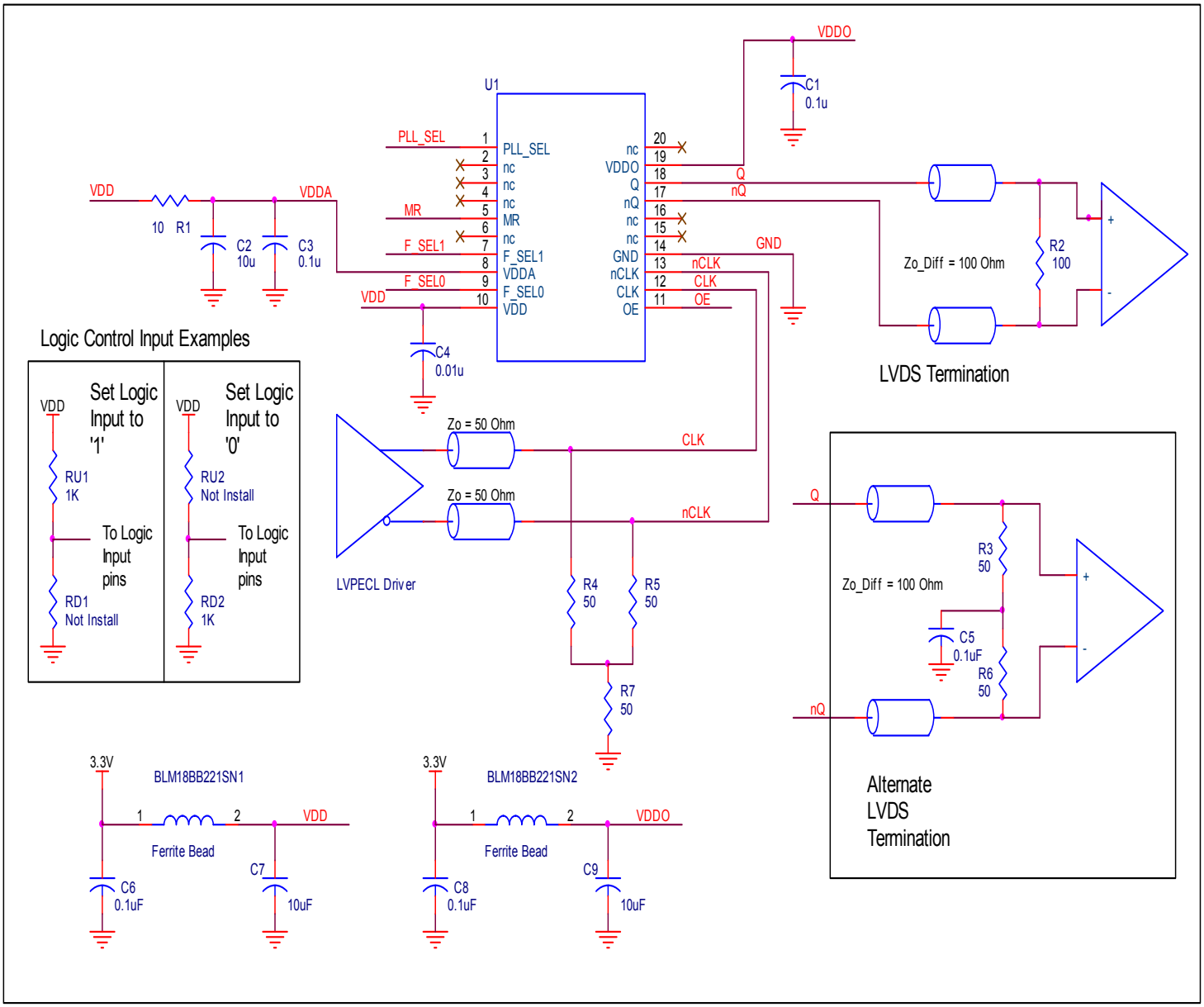


Figure 4. ICS874001I-05 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for theICS874001I-05.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS874001I-05 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.6V * (75mA + 13mA) = **316.8mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.6V * 25mA = **90mW**

Total Power$_{\_MAX}$ = 316.8mW + 90mW = **406.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.407W * 86.7°C/W = 120.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for ICS874001I-05 is: 1,608

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

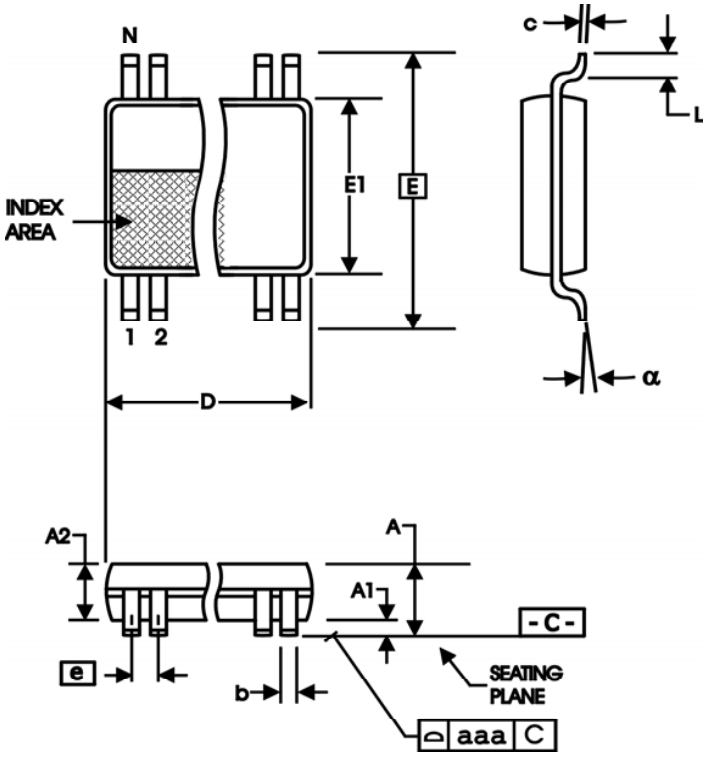


Table 8 Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874001AGI-05LF	ICS4001AI05L	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
874001AGI-05LFT	ICS4001AI05L	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T5	6	Updated HCSL notes.	1/14/11
		9	Deleted *Power Supply Filtering Techniques* application note (see schematic application). Updated *Wiring the Differential Input to Accept Single-ended Levels* application note.	
		11	Updated *LVDS Driver Termination* application note.	
		12	Update *PCI Express Application Note.*	
		13	Updated *Schematic Layout* application Note and diagram.	
			Converted datasheet format.	

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(Rev.1.0 Mar 2020)

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