Description

The 8T49N242 has one fractional-feedback PLL that can be used as a jitter attenuator and frequency translator. It is equipped with four integer output dividers, allowing the generation of up to four different output frequencies, ranging from 8kHz to 1GHz. These frequencies are completely independent of the input reference frequencies, and the crystal reference frequency. The device places virtually no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error. The outputs may select among LVPECL, LVDS, HCSL or LVCMOS output levels.

This makes it ideal to be used in any frequency synthesis application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates.

The 8T49N242 accepts up to two differential or single-ended input clocks and a fundamental-mode crystal input. The internal PLL can lock to either of the input reference clocks or just to the crystal to behave as a frequency synthesizer. The PLL can use the second input for redundant backup of the primary input reference, but in this case, both input clock references must be related in frequency.

The device supports hitless reference switching between input clocks. The device monitors both input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The 8T49N242 supports holdover. The holdover has an initial accuracy of ±50ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for the PLL that may be returned to in holdover at a limited phase slope.

The PLL has a register-selectable loop bandwidth from 0.2Hz to 6.4kHz.

The device supports Output Enable & Clock Select inputs and Lock, Holdover & LOS status outputs.

The device is programmable through an I^2C interface. It also supports I^2C master capability to allow the register configuration to be read from an external EEPROM.

Programming with IDT's *Timing Commander* software is recommended for optimal device performance. Factory pre-programmed devices are also available.

Typical Applications

- OTN or SONET / SDH equipment
- Gigabit and Terabit IP switches / routers including Synchronous Ethernet
- Video broadcast

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- 0.35ps RMS Typical Jitter (including spurs): 12kHz to 20MHz
- Operating Modes: Synthesizer, Jitter Attenuator
- Operates from a 10MHz to 50MHz fundamental-mode crystal or a 10MHz to 125MHz external oscillator
- Initial holdover accuracy of ±50ppb.
- Accepts up to 2 LVPECL, LVDS, LVHSTL or LVCMOS input clocks
  - Accepts frequencies ranging from 8kHz to 875MHz
  - Auto and manual clock selection with hitless switching
  - Clock input monitoring including support for gapped clocks
- Phase-slope limiting and fully hitless switching options to control output clock phase transients
- Generates four LVPECL / LVDS / HCSL or eight LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (differential)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
  - Integer divider ranging from ÷4 to ÷786,420 for each output
- Programmable loop bandwidth settings from 0.2Hz to 6.4kHz
  - Optional fast-lock function
- Four General Purpose I/O pins with optional support for status & control:
  - Two Output Enable control inputs provide control over the four clocks
  - Manual clock selection control input
  - Lock, Holdover and Loss-of-Signal alarm outputs
- Open-drain Interrupt pin
- Register programmable through I^2C or via external I^2C EEPROM
- Full 2.5V or 3.3V supply modes, 1.8V support for LVCMOS outputs, GPIO and control pins
- -40°C to 85°C ambient operating temperature
- Package: 40-VFQFPN, lead-free (RoHS 6)

8T49N242 Block Diagram

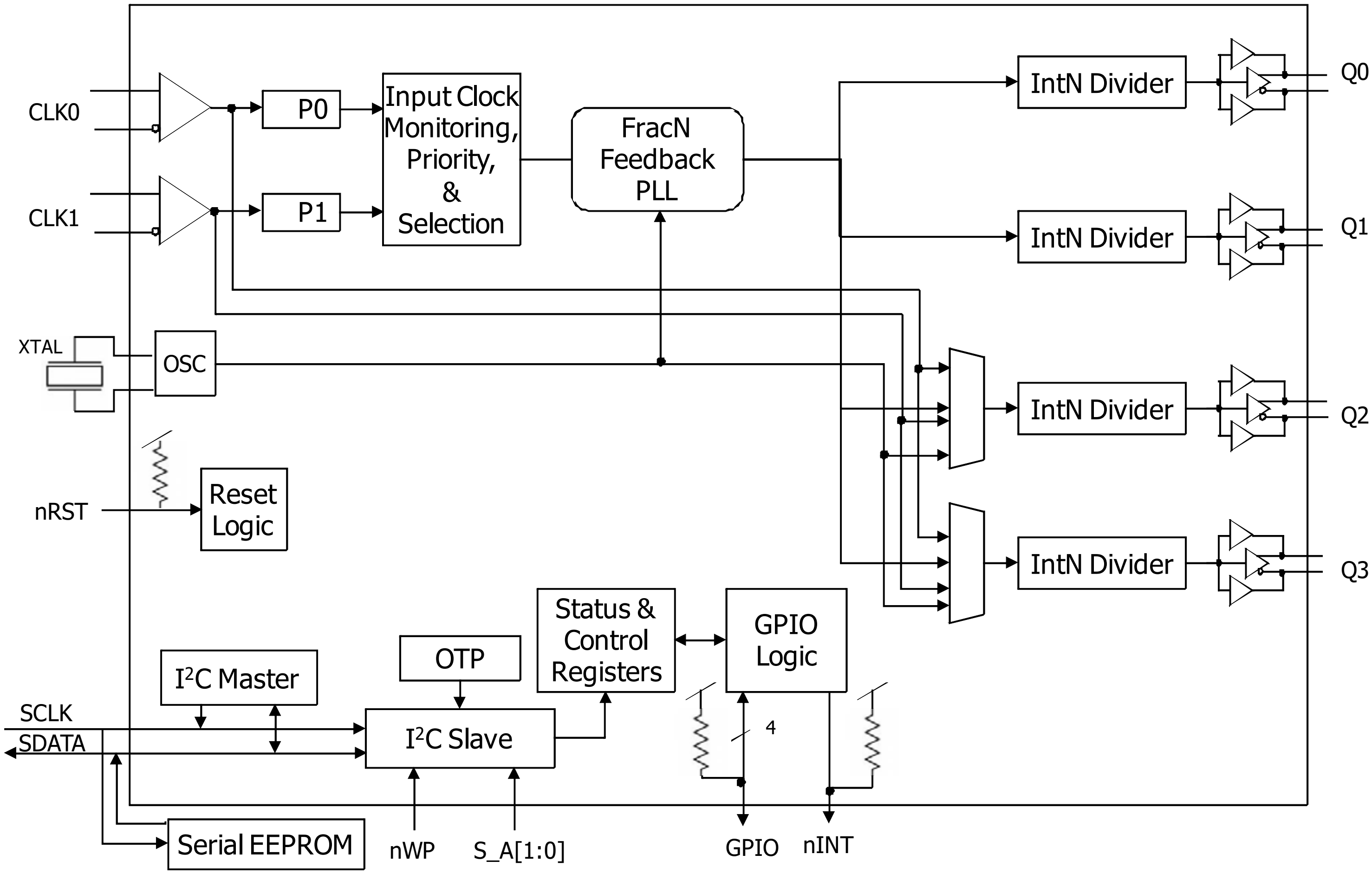


Figure 1. 8T49N242 Block Diagram

Pin Assignment

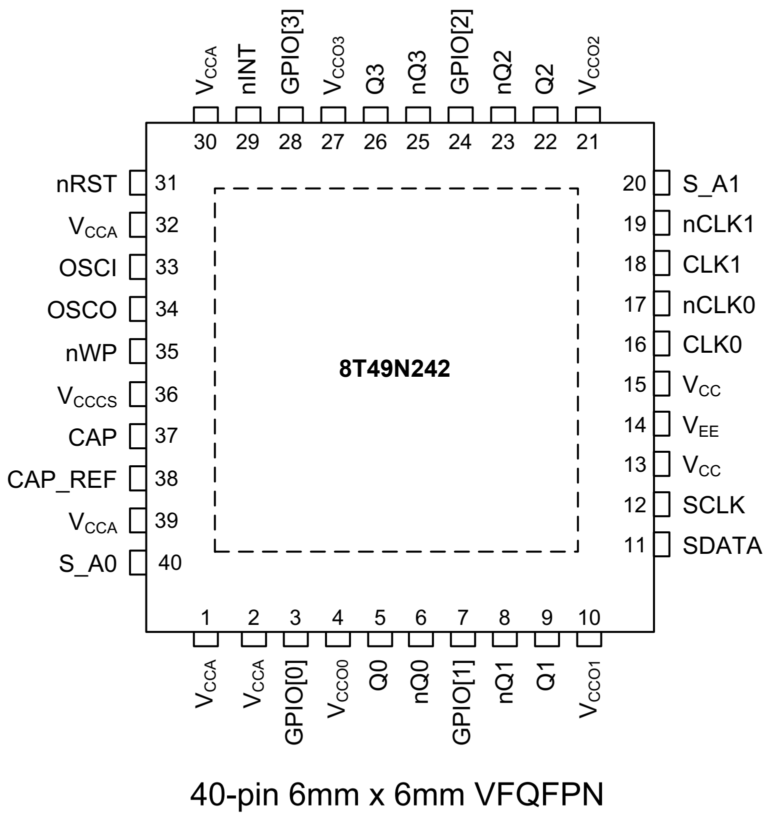


Figure 2. 8T49N242 Pin Assignments

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type[1]		Description
1	V_{CCA}	Power		Analog function supply for core analog functions. 2.5V or 3.3V supported.
2	V_{CCA}	Power		Analog function supply for analog functions associated with the PLL. 2.5V or 3.3V supported.
3	GPIO[0]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
4	V_{CCO0}	Power		High-speed output supply for output pair Q0, nQ0. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
5	Q0	O	Universal	Output Clock 0. Please refer to the Output Drivers for more details.
6	nQ0	O	Universal	Output Clock 0. Please refer to the Output Drivers for more details.
7	GPIO[1]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
8	nQ1	O	Universal	Output Clock 1. Please refer to the Output Drivers for more details.
9	Q1	O	Universal	Output Clock 1. Please refer to the Output Drivers for more details.
10	V_{CCO1}	Power		High-speed output supply for output pair Q1, nQ1. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
11	SDATA	I/O	Pullup	I^2C interface bi-directional data.
12	SCLK	I/O	Pullup	I^2C interface bi-directional clock.
13	V_{CC}	Power		Core digital function supply. 2.5V or 3.3V supported.
14	V_{EE}	Power		Negative supply voltage. All V_{EE} pins and EPAD must be connected before any positive supply voltage is applied.
15	V_{CC}	Power		Core digital function supply. 2.5V or 3.3V supported.
16	CLK0	I	Pulldown	Non-inverting differential clock input 0.
17	nCLK0	I	Pullup / Pulldown	Inverting differential clock input 0. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors)
18	CLK1	I	Pulldown	Non-inverting differential clock input 1.
19	nCLK1	I	Pullup / Pulldown	Inverting differential clock input 1. V_{CC} / 2 when left floating (set by internal pullup / pulldown resistors).
20	S_A1	I	Pulldown	I^2C Address Bit A1
21	V_{CCO2}	Power		High-speed output supply voltage for output pair Q2, nQ2. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
22	Q2	O	Universal	Output Clock 2. Please refer to the Output Drivers for more details.
23	nQ2	O	Universal	Output Clock 2. Please refer to the Output Drivers for more details.
24	GPIO[2]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
25	nQ3	O	Universal	Output Clock 3. Please refer to the Output Drivers for more details.
26	Q3	O	Universal	Output Clock 3. Please refer to the Output Drivers for more details.
27	V_{CCO3}	Power		High-speed output supply voltage for output pair Q3, nQ3. 2.5V or 3.3V supported for differential output types. LVCMOS outputs also support 1.8V.
28	GPIO[3]	I/O	Pullup	General-purpose input-output. LVTTL / LVCMOS Input levels.
29	nINT	O	Open-drain with pullup	Interrupt output.

Number	Name	Type[1]		Description
30	V_{CCA}	Power		Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
31	nRST	I	Pullup	Master Reset input. LVTTL / LVCMOS interface levels: 0 = All registers and state machines are reset to their default values 1 = Device runs normally
32	V_{CCA}	Power		Analog function supply for core analog functions. 2.5V or 3.3V supported.
33	OSCI	I		Crystal Input. Accepts a 10MHz – 50MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal. For proper device functionality, a crystal or external oscillator must be connected to this pin.
34	OSCO	O		Crystal Output. This pin must be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.
35	nWP	I	Pullup	Write Protect input. LVTTL / LVCMOS interface levels. 0 = Write operations on the serial port will complete normally, but will have no effect except on interrupt registers.
36	V_{CCCS}	Power		Output supply for Control & Status pins: GPIO[3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST 1.8V, 2.5V or 3.3V supported
37	CAP	Analog		PLL External Capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
38	CAP_REF	Analog		PLL External Capacitance. A 0.1µF capacitance value across CAP and CAP_REF pins is recommended.
39	V_{CCA}	Power		Analog function supply for analog functions associated with PLL. 2.5V or 3.3V supported.
40	S_A0	I	Pulldown	I^2C Address Bit A0.
ePAD	Exposed Pad	Power		Negative supply voltage. All V_{EE} pins and ePAD must be connected before any positive supply voltage is applied.

NOTE 1: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics, $V_{CC} = V_{CCOX} = 3.3V\pm5\%$ or $2.5V\pm5\%$[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance[2]				3.5		pF
C_{XTAL}	Crystal Pins (OSCI, OSCO) Internal Capacitance				14		pF
R_{PULLUP}	Input Pullup Resistor	GPIO[3:0], nRST, nWP, SDATA, SCLK			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	S_A0, S_A1			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS	$V_{CCOX} = 3.465V$		11.5		pF
		LVCMOS	$V_{CCOX} = 2.625V$		10.5		pF
		LVCMOS	$V_{CCOX} = 1.89V$		11		pF
		LVDS, HCSL or LVPECL	$V_{CCOX} = 3.465V$ or $2.625V$		2.5		pF
R_{OUT}	Output Impedance	GPIO[3:0]	$V_{CCCS} = 3.3V$		26		Ω
			$V_{CCCS} = 2.5V$		30		
			$V_{CCCS} = 1.8V$		42		
		LVCMOS Q[3:0], nQ[3:0]	$V_{CCOX} = 3.3V$		18		Ω
			$V_{CCOX} = 2.5V$		22		
			$V_{CCOX} = 1.8V$		30		

NOTE 1: V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2} or V_{CCO3}.

NOTE 2: This specification does not apply to the OSCI or OSCO pins.

Principles of Operation

The 8T49N242 can be locked to either of the input clocks and generate a wide range of synchronized output clocks.

It could be used for example in either the transmit or receive path of Synchronous Ethernet equipment.

The 8T49N242 accepts up to two differential or single-ended input clocks ranging from 8kHz up to 875MHz. It generates up to four output clocks ranging from 8kHz up to 1.0GHz.

The PLL path within the 8T49N242 supports three states: Lock, Holdover and Free-run. Lock & holdover status may be monitored on register bits and pins. The PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. The PLL within the 8T49N242 has an initial holdover frequency offset of ±50ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, the PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N242 continuously monitors each input for activity (signal transitions). If no input references are provided, the device will remain locked to the crystal in Free-run state and will generate output frequencies as a synthesizer.

When an input clock has been validated the PLL will transition to the Lock state. In automatic reference switching, if the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into Holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the 8T49N242 will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive. Manual switchover is also available with switchover only occurring on user command, either via register bit or via the Clock Select input function of the GPIO[3:0] pins.

The device supports conversion of any input frequencies to four different output frequencies: one independent output frequency on Q0 and three more integer-related frequencies on Q[1:3].

The 8T49N242 has a programmable loop bandwidth from 0.2Hz to 6.4kHz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device is programmable through an I^2C and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I^2C EEPROM.

Crystal Input

The crystal input on the 8T49N242 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency range of 10MHz – 50MHz.

The oscillator input also supports being driven by a single-ended crystal oscillator or reference clock.

The initial holdover frequency offset is set by the device, but the long term drift depends on the quality of the crystal or oscillator attached to this port.

This device provides the ability to double the crystal frequency input into the PLL for improved close-in phase noise performance. Refer to Figure 3.

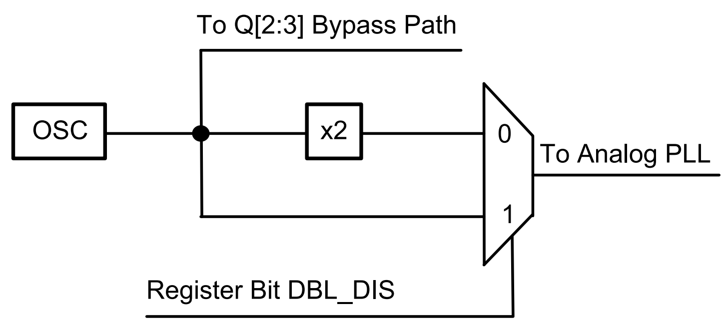


Figure 3. Doubler Block Diagram

Bypass Path

The crystal input, CLK0 or CLK1 may be used directly as a clock source for the Q[2:3] output dividers. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The 8T49N242 accepts up to two input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels.

In Manual mode, only one of the inputs may be chosen and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIO[2] must be used as a Clock Select input (CSEL). CSEL = 0 will select the CLK0 input and CSEL = 1 will select the CLK1 input.

In addition, the crystal frequency may be passed directly to the output dividers Q[2:3] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ±100ppm or better, except where gapped clock inputs are used.

If the PLL is working in automatic mode, then one of the input reference sources is assigned as the higher priority. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see Input Clock Monitor for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control bit.

Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of the PLL's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL tracking will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and is validated. Validation occurs once 8 rising edges have been received on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation period starts over.

Each LOS flag may also be reflected on one of the GPIO[3:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Holdover

The 8T49N242 supports a small initial holdover frequency offset in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for two LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The 8T49N242 can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When the PLL loses all valid input references, it will enter the holdover state. In fast average mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings. This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the VCO band
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in the *AC Characteristics Table,* Table 11.
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3dB attenuation point corresponding to nominal a period of 20 minutes. The accuracy is shown in the *AC Characteristics Table,* Table 11.

When entering holdover, the PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While the PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) will have drifted outside of the limits of the holdover state and be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the 8T49N242 cannot know or influence when that transition occurs.

Input to Output Clock Frequency

The 8T49N242 is designed to accept any frequency within its input range and generate four different output frequencies that are integer-related to the PLL frequency and hence to each other, but not to the input frequencies. The internal architecture of the device ensures that most translations will result in the exact output frequency specified. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may act as a frequency synthesizer with the PLL generating its operating frequency from just the crystal input. By setting the SYN_MODE register bit and setting the STATE[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

When operating as a synthesizer, the precision of the output frequency will be < 1ppb for any supported configuration.

Loop Filter and Bandwidth

The 8T49N242 uses one external capacitor of fixed value to support its loop bandwidth. When operating in Synthesizer mode a fixed loop bandwidth of approximately 200kHz is provided.

When not operating as a synthesizer, the 8T49N242 will support a range of loop bandwidths: 0.2Hz, 0.4Hz, 0.8Hz, 1.6Hz, 3.2Hz, 6.4Hz, 12Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz, 800Hz, 1.6kHz or 6.4kHz.

The device supports two different loop bandwidth settings: acquisition and locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to “fast-lock”. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times.

Output Dividers

The 8T49N242 supports four integer output dividers. Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. In addition, the Q[2:3] first stage dividers may be bypassed if CLK0, CLK1 or the crystal are used as the clock source for them. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in Table 3.

An output synchronization via the PLL_SYN bit is necessary after programming the output dividers to ensure that the outputs are synchronized.

Table 3. Output Divide Ratios

1st-Stage Divide	2nd-Stage Divide	Total Divide	Minimum F_{OUT} MHz	Maximum F_{OUT} MHz
4	1	4	750	1000
5	1	5	600	800
6	1	6	500	666.7
4	2	8	375	500
5	2	10	300	400
6	2	12	250	333.3
4	4	16	187.5	250
5	4	20	150	200
6	4	24	125	166.7
...				
4	131,070	524,280	0.0057	0.0076
5	131,070	655,350	0.0046	0.0061
6	131,070	786,420	0.0038	0.0051

Output Divider Frequency Sources

Output dividers associated with the Q[0:1] outputs take their input frequency directly from the PLL.

Output dividers associated with the Q[2:3] outputs can take their input frequencies from the PLL, CLK0 or CLK1 input reference frequency or the crystal frequency.

Output Phase Control on Switchover

There are two options on how the output phase can be controlled when the 8T49N242 enters or leaves the holdover state, or the PLL switches between input references. Phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODE bit selects which behavior is to be followed.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used. Fully hitless switching should not be used unless all input references are in the same clock domain. Note that use of this mode may prevent an output frequency and phase from being able to trace its alignment back to a primary reference source.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEW[1:0] bits. Phase-slope limiting should be used if all input references are not in the same clock domain or users wish to retain traceability to a primary reference source.

Output Drivers

The Q0 to Q3 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO}.

Each output may be enabled or disabled by register bits and/or GPIO pins.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q & nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions can be disabled via register programming:

- Any unused output, including all output divider logic, can be individually powered-off.
- Any unused input, including the clock monitoring logic can be individually powered-off.
- The digital PLL can be powered-off when running in synthesizer mode.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

The status and control signals for the device, may be operated at 1.8V, 2.5V or 3.3V as determined by the voltage applied to the V_{CCCS} pins. All signals will share the same voltage levels.

Signals involved include: nWP, nINT, nRST, GPIO[3:0], S_A0, S_A1, SCLK and SDATA. The voltage used here is independent of the voltage chosen for the digital and analog core voltages and the output voltages selected for the clock outputs.

General-Purpose I/Os & Interrupts

The 8T49N242 provides four General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as either an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in Table 4. Note that the default state prior to configuration being loaded from internal OTP will be to set each GPIO to input direction to function as an Output Enable.

Table 4. GPIO Configuration[1]

	Configured as Input		Configured as Output	
GPIO Pin	Fixed Function (default)	General Purpose	Fixed Function	General Purpose
3	-	GPI[3]	LOL	GPO[3]
2	CSEL	GPI[2]	LOS[0]	GPO[2]
1	OSEL[1]	GPI[1]	LOS[1]	GPO[1]
0	OSEL[0]	GPI[0]	HOLD	GPO[0]

NOTE 1:

GPI[x]: General Purpose Input. Logic state on GPIO[x] pin is directly reflected in GPI[x] register.

LOL: Loss-of-Lock Status Flag for Digital PLL. Logic-high indicates digital PLL not locked.

GPO[x]: General Purpose Output. Logic state is determined by value written in register GPO[x].

OSEL[n]: Output Enable Control Signals for Outputs Qx, nQx. Refer to Output Enable Operation section.

LOS[x]: Loss-of-Signal Status Flag for Input Reference x. Logic-high indicates input reference failure.

CSEL: Manual Clock Select Input for PLL. Logic-high selects differential clock input 1 (CLK1).

HOLD: Holdover Status Flag for Digital PLL. Logic-high indicates digital PLL in holdover status.

Refer to Register Descriptions for additional details.

If used in the Fixed Function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in Table 4.

The LOL alarm will support two modes of operation:

- De-asserts once PLL is locked, or
- De-asserts after PLL is locked and all internal synchronization operations that may destabilize output clocks are completed.

Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock status (LOL), PLL in holdover status (HOLD) and Loss-of-Signal status for each input (LOS[1:0]). Those Status Flags are set whenever there is an alarm on their respective functions. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Device Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status Flag and nINT output pin are asserted if any of the enabled interrupt Status Flags are set.

Output Enable Operation

When GPIO[1:0] are used as Output Enable control signals, the function of the pins is to select one of four register-based maps that indicate which outputs should be enabled or disabled.

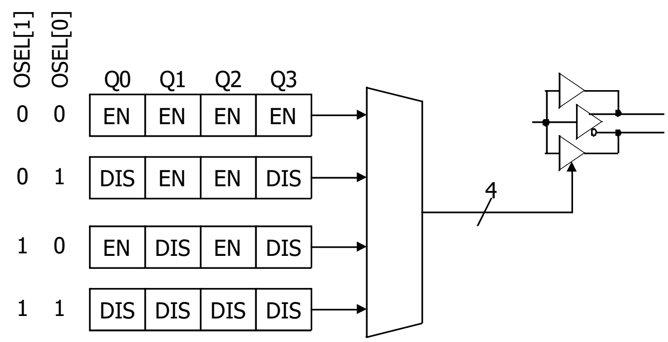


Figure 4. Output Enable Map Operation

Device Hardware Configuration

The 8T49N242 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with one complete device configuration. Some or all of this pre-programmed configuration will be loaded into the device's registers on power-up or reset.

These default register settings can be over-written using the serial programming interface once reset is complete. Any configuration written via the serial programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up and Reset Behavior

The 8T49N242 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it is common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as Output Enable inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the later of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N242 will check the register settings to see if it should load the remainder of its configuration from an external I^{2}C EEPROM at a defined address or continue loading from OTP, or both. See I2C Boot-up Initialization Mode for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the crystal and begin operation. Once the PLL is locked, all the outputs derived from it will be synchronized and output phase adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I^{2}C compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

The device has the additional capability of becoming a master on the I^{2}C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I^{2}C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I^{2}C bus or pre-programmed into the device prior to assembly.

I^{2}C Mode Operation

The I^{2}C interface is designed to fully support v2.1 of the I^{2}C Specification for Normal and Fast mode operation. The device acts as a slave device on the I^{2}C bus at 100kHz or 400kHz using the address defined in the Serial Interface Control register (0006h), as modified by the S_A0 & S_A1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

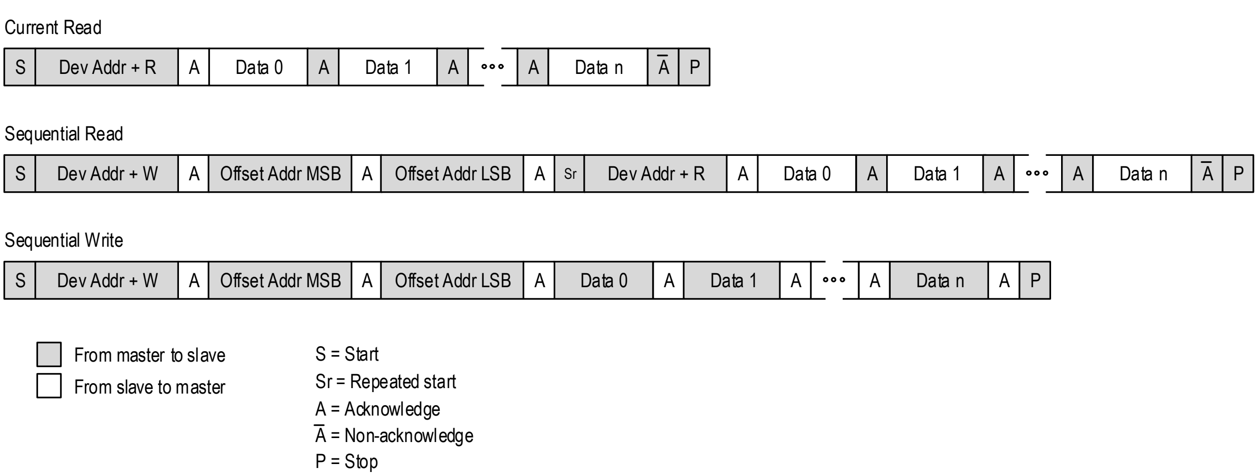


Figure 5. I^{2}C Slave Read and Write Cycle Sequencing

I²C Master Mode

When operating in I²C mode, the 8T49N242 has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the 8T49N242 will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (84h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1- or 2-byte addressing mode
- Master arbitration with programmable number of retries
- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out

The 8T49N242 will not support the following functions:

- I²C General Call
- Slave clock stretching
- I²C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

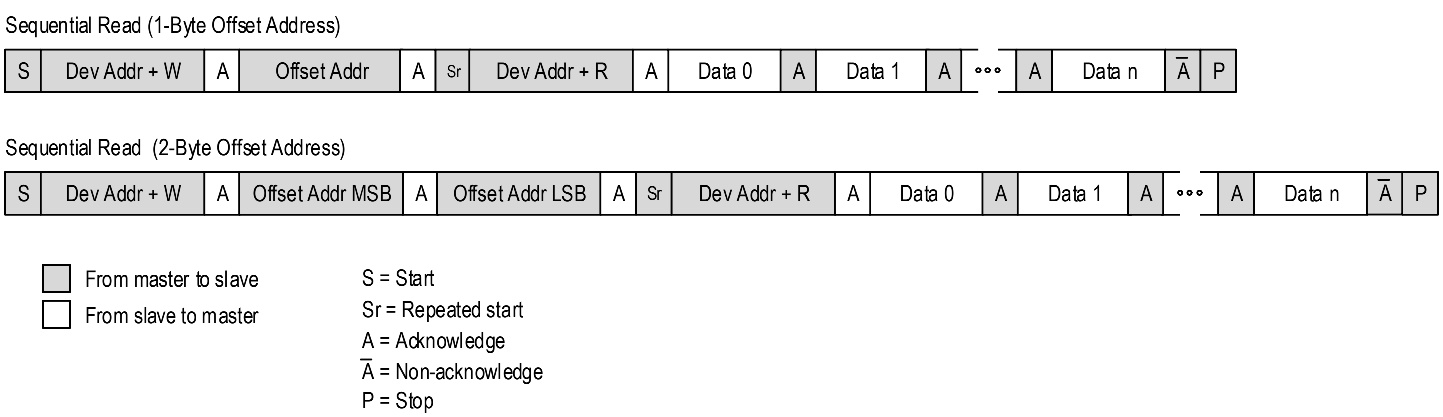


Figure 6. I²C Master Read Cycle Sequencing

I^2C Boot-up Initialization Mode

If enabled (via the BOOT_EEP bit in the Startup register), once the nRST input has been de-asserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I^2C bus to read its initial register settings from a memory location on the I^2C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address 84h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit in the Global Interrupt Status register (0210h) will also be set in this event.

Contents of the EEPROM should be as shown in Table 5.

Table 5. External Serial EEPROM Contents

EEPROM Offset (Hex)	Contents							
	D7	D6	D5	D4	D3	D2	D1	D0
00	1	1	1	1	1	1	1	1
01	1	1	1	1	1	1	1	1
02	1	1	1	1	1	1	1	1
03	1	1	1	1	1	1	1	1
04	1	1	1	1	1	1	1	1
05	1	1	1	1	1	1	1	Serial EEPROM Speed Select 0 = 100kHz 1 = 400kHz
06	1	8T49N242 Device I^2C Address [6:2]					1	1
07	0	0	0	0	0	0	0	0
08 - 83	Desired contents of Device Registers 08h - 83h							
84	Serial EEPROM CRC							
85 - FF	Unused							

Register Descriptions

Table 6. Register Blocks

Register Ranges Offset (Hex)	Register Block Description
0000 - 0001	Startup Control Registers
0002 - 0005	Device ID Control Registers
0006 - 0007	Serial Interface Control Registers
0008 - 002F	Digital PLL Control Registers
0030 - 0038	GPIO Control Registers
0039 - 003E	Output Driver Control Registers
003F - 004A	Output Divider Control Registers
004B - 0056	Reserved
0057 - 0062	Reserved
0063 - 0067	Output Divider Source Control Registers
0068- 006B	Analog PLL Control Registers
006C - 0070	Power-Down & Lock Alarm Control Registers
0071 - 0078	Input Monitor Control Registers
0079	Interrupt Enable Register
007A - 007B	Factory Setting Registers
007C - 01FF	Reserved
0200 - 0201	Interrupt Status Registers
0202 - 020B	Reserved
020C	General-Purpose Input Status Register
020D - 0212	Global Interrupt and Boot Status Register
0213 - 03FF	Reserved

Table 7A. Startup Control Register Bit Field Locations and Descriptions

Startup Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0000	EEP_RTY[4:0]					Rsvd	nBOOT_OTP	nBOOT_EEP
0001	EEP_A15	EEP_ADDR[6:0]						

Startup Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
EEP_RTY[4:0]	R/W	1h	Select number of times arbitration for the I^{2}C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try.
nBOOT_OTP	R/W	NOTE[1]	Internal One-Time Programmable (OTP) memory usage on power-up: 0 = Load power-up configuration from OTP 1 = Only load 1st eight bytes from OTP
nBOOT_EEP	R/W	NOTE[1]	External EEPROM usage on power-up: 0 = Load power-up configuration from external serial EEPROM (overwrites OTP values) 1 = Don't use external EEPROM
EEP_A15	R/W	NOTE[1]	Serial EEPROM supports 15-bit addressing mode (multiple pages).
EEP_ADDR[6:0]	R/W	NOTE[1]	I^{2}C base address for serial EEPROM.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock® NG Universal Frequency Translator Ordering Product Information guide or custom datasheet addendum for more details.

Table 7B. Device ID Control Register Bit Field Locations and Descriptions

Device ID Register Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0002	REV_ID[3:0]				DEV_ID[15:12]			
0003	DEV_ID[11:4]							
0004	DEV_ID[3:0]				DASH_CODE [10:7]			
0005	DASH_CODE [6:0]							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REV_ID[3:0]	R/W	0h	Device revision.
DEV_ID[15:0]	R/W	0607h	Device ID code.
DASH CODE [10:0]	R/W	NOTE[1]	Device Dash code. Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Please refer to the FemtoClock® NG Universal Frequency Translator Ordering Product Information guide or custom datasheet addendum for more details.

Table 7C. Serial Interface Control Register Bit Field Locations and Descriptions

Serial Interface Control Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0006	0	UFTADD[6:2]					UFTADD[1]	UFTADD[0]
0007	Rsvd							1

Device ID Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
UFTADD[6:2]	R/W	NOTE[1]	Configurable portion of I^2C base (bits 6:2) address for this device.
UFTADD[1]	R/O	0b	I^2C base address bit 1. This address bit reflects the status of the S_A1 external input pin. See Table 1.
UFTADD[0]	R/O	0b	I^2C base address bit 0. This address bit reflects the status of the S_A0 external input pin. See Table 1.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Generic dash codes -900 through -903, -998 and -999 are available and programmed with the default I^2C address of 1111100b (1101100b for -999). Please refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* for more details.

Table 7D. Digital PLL Input Control Register Bit Field Locations and Descriptions

Digital PLL Input Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0008	REFSEL[2:0]			FBSEL[1:0]			RVRT	SWMODE
0009	Rsvd							REF_PRI
000A	Rsvd		REFDIS1	REFDIS0	Rsvd	Rsvd	STATE[1:0]	
000B	Rsvd			PRE0[20:16]				
000C	PRE0[15:8]							
000D	PRE0[7:0]							
000E	Rsvd			PRE1[20:16]				
000F	PRE1[15:8]							
0010	PRE1[7:0]							

Digital PLL Input Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
REFSEL[2:0]	R/W	000b	Input reference selection for Digital PLL: 000 = Automatic selection 001 = Manual selection by GPIO input 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = Do not use 111 = Do not use
FBSEL[2:0]	R/W	000b	Feedback mode selection for Digital PLL: 000 through 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = do not use 111 = do not use
RVRT	R/W	1b	Automatic switching mode for Digital PLL: 0 = non-revertive switching 1 = revertive switching
SWMODE	R/W	1b	Controls how Digital PLL adjusts output phase when switching between input references: 0 = Absorb any phase differences between old & new input references 1 = Track to follow new input reference's phase using phase-slope limiting
REF_PRI	R/W	0b	Switchover priority for Input References when used by Digital PLL: 0 = CLK0 is primary input reference 1 = CLK1 is primary input reference
REFDIS0	R/W	0b	Input Reference 0 Switching Selection Disable for Digital PLL: 0 = Input Reference 0 is included in the switchover sequence 1 = Input Reference 0 is not included in the switchover sequence
REFDIS1	R/W	0b	Input Reference 1 Switching Selection Disable for Digital PLL: 0 = Input Reference 1 is included in the switchover sequence 1 = Input Reference 1 is not included in the switchover sequence

Digital PLL Input Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
STATE[1:0]	R/W	00b	Digital PLL State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode. 10 = Force NORMAL state 11 = Force HOLDOVER state
PRE0[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 0 when used by Digital PLL.
PRE1[20:0]	R/W	000000h	Pre-divider ratio for Input Reference 1 when used by Digital PLL.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7E. Digital PLL Feedback Control Register Bit Field Locations and Descriptions

Digital PLL Feedback Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0011	M1_0[23:16]							
0012	M1_0[15:8]							
0013	M1_0[7:0]							
0014	M1_1[23:16]							
0015	M1_1[15:8]							
0016	M1_1[7:0]							
0017	LCKBW[3:0]				ACQBW[3:0]			
0018	LCKDAMP[2:0]			ACQDAMP[2:0]			PLLGAIN[1:0]	
0019	Rsvd			Rsvd	Rsvd			Rsvd
001A	Rsvd							
001B	Rsvd							
001C	Rsvd							Rsvd
001D	Rsvd							
001E	Rsvd							
001F	FFh							
0020	FFh							
0021	FFh							
0022	FFh							
0023	SLEW[1:0]		Rsvd	HOLD[1:0]		Rsvd	HOLDAVG	FASTLCK
0024	LOCK[7:0]							
0025	Rsvd							DSM_INT[8]
0026	DSM_INT[7:0]							
0027	Rsvd							
0028	Rsvd			DSMFRAC[20:16]				
0029	DSMFRAC[15:8]							
002A	DSMFRAC[7:0]							
002B	Rsvd							
002C	01h							
002D	Rsvd							
002E	Rsvd							
002F	DSM_ORD[1:0]		DCXOGAIN[1:0]		Rsvd	DITHGAIN[2:0]		

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
M1_0[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL.
M1_1[23:0]	R/W	070000h	M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL.
LCKBW[3:0]	R/W	0111b	Digital PLL Loop Bandwidth while locked: 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved
ACQBW[3:0]	R/W	0111b	Digital PLL Loop Bandwidth while in acquisition (not-locked): 0000 = 0.2Hz 0001 = 0.4Hz 0010 = 0.8Hz 0011 = 1.6Hz 0100 = 3.2Hz 0101 = 6.4Hz 0110 = 12Hz 0111 = 25Hz 1000 = 50Hz 1001 = 100Hz 1010 = 200Hz 1011 = 400Hz 1100 = 800Hz 1101 = 1.6kHz 1110 = 6.4kHz 1111 = Reserved
LCKDAMP[2:0]	R/W	011b	Damping factor for Digital PLL while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
ACQDAMP[2:0]	R/W	011b	Damping factor for Digital PLL while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved
PLLGAIN[1:0]	R/W	01b	Digital Loop Filter Gain Settings for Digital PLL: 00 = 0.5 01 = 1 10 = 1.5 11 = 2
SLEW[1:0]	R/W	00b	Phase-slope control for Digital PLL: 00 = no limit - controlled by loop bandwidth of Digital PLL 01 = 64us/s 10 = 11us/s 11 = Reserved
HOLD[1:0]	R/W	00b	Holdover Averaging mode selection for Digital PLL: 00 = Instantaneous mode - uses historical value 100ms prior to entering holdover 01 = Fast Average Mode 10 = Reserved 11 = Return to Center of VCO Tuning Range
HOLDAVG	R/W	0b	Holdover Averaging Enable for Digital PLL: 0 = Holdover averaging disabled 1 = Holdover averaging enabled as defined in HOLD[1:0]
FASTLCK	R/W	0b	Enables Fast Lock operation for Digital PLL: 0 = Normal locking using LCKBW & LCKDAMP fields in all cases 1 = Fast Lock mode using ACQBW & ACQDAMP when not phase locked and LCKBW & LCKDAMP once phase locked
LOCK[7:0]	R/W	3Fh	Lock window size for Digital PLL. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.
DSM_INT[8:0]	R/W	02Dh	Integer portion of the Delta-Sigma Modulator value.
DSMFRAC[20:0]	R/W	000000h	Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{21} to determine the actual fraction.
DSM_ORD[1:0]	R/W	11b	Delta-Sigma Modulator Order for Digital PLL: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation

Digital PLL Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
DCXOGAIN[1:0]	R/W	01b	Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL: 00 = 0.5 01 = 1 10 = 2 11 = 4
DITHGAIN[2:0]	R/W	000b	Dither Gain setting for Digital PLL: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7F. GPIO Control Register Bit Field Locations and Descriptions

The values observed on any GPIO pins that are used as general purpose inputs are visible in the GPI[3:0] register that is located at location 0x020C near a number of other read-only registers.

GPIO Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0030	Rsvd				GPIO_DIR[3:0]			
0031	Rsvd				GPI3SEL[2]	GPI2SEL[2]	GPI1SEL[2]	GPI0SEL[2]
0032	Rsvd				GPI3SEL[1]	GPI2SEL[1]	GPI1SEL[1]	GPI0SEL[1]
0033	Rsvd				GPI3SEL[0]	GPI2SEL[0]	GPI1SEL[0]	GPI0SEL[0]
0034	Rsvd				GPO3SEL[2]	GPO2SEL[2]	GPO1SEL[2]	GPO0SEL[2]
0035	Rsvd				GPO3SEL[1]	GPO2SEL[1]	GPO1SEL[1]	GPO0SEL[1]
0036	Rsvd				GPO3SEL[0]	GPO2SEL[0]	GPO1SEL[0]	GPO0SEL[0]
0037	Rsvd							
0038	Rsvd				GPO[3:0]			

GPIO Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
GPIO_DIR[3:0]	R/W	0000b	Direction control for General-Purpose I/O Pins GPIO[3:0]: 0 = input mode 1 = output mode
GPI0SEL[2:0]	R/W	001b	Function of GPIO[0] pin when set to input mode by GPIO_DIR[0] register bit: 000 = General Purpose Input (value on GPIO[0] pin directly reflected in GPI[0] register bit) 001 = Output Enable control bit 0: OSEL[0], (Refer to Figure 4 for more details.) 010 = reserved 011 = reserved 100 through 111 = reserved
GPI1SEL[2:0]	R/W	001b	Function of GPIO[1] pin when set to input mode by GPIO_DIR[1] register bit: 000 = General Purpose Input (value on GPIO[1] pin directly reflected in GPI[1] register bit) 001 = Output Enable control bit 1: OSEL[1], (Refer to Figure 4 for more details.) 010 through 111 = reserved
GPI2SEL[2:0]	R/W	001b	Function of GPIO[2] pin when set to input mode by GPIO_DIR[2] register bit: 000 = General Purpose Input (value on GPIO[2] pin directly reflected in GPI[2] register bit) 001 = CSEL: Manual Clock Select Input for PLL 010 = reserved 011 = reserved 100 = reserved 101 through 111 = reserved
GPI3SEL[2:0]	R/W	001b	Function of GPIO[3] pin when set to input mode by GPIO_DIR[3] register bit: 000 = General Purpose Input (value on GPIO[3] pin directly reflected in GPI[3] register bit) 001 = reserved 010 = reserved 011 = reserved 100 through 111 = reserved

GPIO Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
GPO0SEL[2:0]	R/W	000b	Function of GPIO[0] pin when set to output mode by GPIO_DIR[0] register bit: 000 = General Purpose Output (value in GPO[0] register bit driven on GPIO[0] pin 001 = Holdover Status Flag for Digital PLL reflected on GPIO[0] pin 010 = reserved 011 = reserved 100 = reserved 101 = reserved 110 through 111 = reserved
GPO1SEL[2:0]	R/W	000b	Function of GPIO[1] pin when set to output mode by GPIO_DIR[1] register bit: 000 = General Purpose Output (value in GPO[1] register bit driven on GPIO[1] pin 001 = Loss-of-Signal Status Flag for Input Reference 1 reflected on GPIO[1] pin 010 = reserved 011 = reserved 100 = reserved 101 = reserved 110 = reserved 111 = reserved
GPO2SEL[2:0]	R/W	000b	Function of GPIO[2] pin when set to output mode by GPIO_DIR[2] register bit: 000 = General Purpose Output (value in GPO[2] register bit driven on GPIO[2] pin 001 = Loss-of-Signal Status Flag for Input Reference 0 reflected on GPIO[2] pin 010 = reserved 011 = reserved 100 = reserved 101 through 111 = reserved
GPO3SEL[2:0]	R/W	000b	Function of GPIO[3] pin when set to output mode by GPIO_DIR[3] register bit: 000 = General Purpose Output (value in GPO[3] register bit driven on GPIO[3] pin 001 = Loss-of-Lock Status Flag for Digital PLL reflected on GPIO[3] pin 010 = reserved 011 = reserved 100 through 111 = reserved
GPO[3:0]	R/W	0000b	Output Values reflect on pin GPIO[3:0] when General-Purpose Output Mode selected.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7G. Output Driver Control Register Bit Field Locations and Descriptions

Output Driver Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0039	Rsvd				OUTEN[3:0]			
003A	Rsvd				POL_Q[3:0]			
003B	Rsvd							
003C	Rsvd							
003D	OUTMODE3[2:0]			SE_MODE3	OUTMODE2[2:0]			SE_MODE2
003E	OUTMODE1[2:0]			SE_MODE1	OUTMODE0[2:0]			SE_MODE0

Output Driver Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
OUTEN[3:0]	R/W	0000b	Output Enable control for Clock Outputs Q[3:0], nQ[3:0]: 0 = Qn is in a high-impedance state 1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field
POL_Q[3:0]	R/W	0000b	Polarity of Clock Outputs Q[3:0], nQ[3:0]: 0 = Qn is normal polarity 1 = Qn is inverted polarity
OUTMODEm[2:0]	R/W	001b	Output Driver Mode of Operation for Clock Output Pair Qm, nQm: 000 = High-impedance 001 = LVPECL 010 = LVDS 011 = LVCMOS 100 = HCSL 101 - 111 = reserved
SE_MODEm	R/W	0b	Behavior of Output Pair Qm, nQm when LVCMOS operation is selected: (Must be 0 if LVDS or LVPECL output style is selected) 0 = Qm and nQm are both the same frequency but inverted in phase 1 = Qm and nQm are both the same frequency and phase
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7H. Output Divider Control Register Bit Field Locations and Descriptions

Output Divider Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
003F	Rsvd						NS1_Q0[1:0]	
0040	NS2_Q0[15:8]							
0041	NS2_Q0[7:0]							
0042	Rsvd						NS1_Q1[1:0]	
043	NS2_Q1[15:8]							
0044	NS2_Q1[7:0]							
0045	Rsvd						NS1_Q2[1:0]	
0046	NS2_Q2[15:8]							
0047	NS2_Q2[7:0]							
0048	Rsvd						NS1_Q3[1:0]	
0049	NS2_Q3[15:8]							
004A	NS2_Q3[7:0]							

Output Divider Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
NS1_Qm[1:0]	R/W	10b	1st Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 2, 3): 00 = /5 01 = /6 10 = /4 11 = /1 (Do not use this selection if PLL is the source since the 2nd-stage divider has a limit of 1GHz).
NS2_Qm[15:0]	R/W	0002h	2nd Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 2, 3). Actual divider ratio is 2x the value written here. A value of 0 in this register will bypass the second stage of the divider.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7I. Output Clock Source Control Register Bit Field Locations and Descriptions

Output Clock Source Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0063	PLL_SYN	Rsvd	CLK_SEL3[1:0]		Rsvd	Rsvd	CLK_SEL2[1:0]	
0064	Rsvd							
0065	Rsvd							
0066	Rsvd		Rsvd		Rsvd		Rsvd	
0067	10b		10b		00b		Rsvd	

Output Clock Source Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PLL_SYN	R/W	0b	Output Synchronization Control for Outputs Derived from PLL. Setting this bit from 0->1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1->0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0.
CLK_SELm[1:0]	R/W	00b	Clock Source Selection for output pair Qm: nQm (m = 2, 3): Do not select Input Reference 0 or 1 if that input is faster than 250MHz: 00 = PLL 01 = Input Reference 0 (CLK0) 10 = Input Reference 1 (CLK1) 11 = Crystal input
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7J. Analog PLL Control Register Bit Field Locations and Descriptions

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

Analog PLL Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0068	CPSET[2:0]			RS[1:0]		CP[1:0]		WPOST
0069	Rsvd		Rsvd	TDC_DIS	SYN_MODE	Rsvd	DLCNT	DBITM
006A	VCOMAN[2:0]			DBIT[4:0]				
006B	001b			Rsvd				

Analog PLL Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
CPSET[2:0]	R/W	100b	Charge Pump Current Setting for Analog PLL: 000 = 110µA 001 = 220µA 010 = 330µA 011 = 440µA 100 = 550µA 101 = 660µA 110 = 770µA 111 = 880µA
RS[1:0]	R/W	01b	Internal Loop Filter Series Resistor Setting for Analog PLL: 00 = 330Ω 01 = 640Ω 10 = 1.2kΩ 11 = 1.79kΩ
CP[1:0]	R/W	01b	Internal Loop Filter Parallel Capacitor Setting for Analog PLL: 00 = 40pF 01 = 80pF 10 = 140pF 11 = 200pF
WPOST	R/W	1b	Internal Loop Filter 2nd-Pole Setting for Analog PLL: 0 = Rpost = 497Ω, Cpost = 40pF 1 = Rpost = 1.58kΩ, Cpost = 40pF
TDC_DIS	R/W	0b	TDC Disable Control for PLL: 0 = TDC Enabled 1 = TDC Disabled
SYN_MODE	R/W	0b	Frequency Synthesizer Mode Control for PLL: 0 = PLL jitter attenuates and translates one or more input references 1 = PLL synthesizes output frequencies using only the crystal as a reference Note that the STATE[1:0] field in the Digital PLL Control Register must be set to Force Freerun state.
DLCNT	R/W	1b	Digital Lock Count Setting for Analog PLL: 0 = Counter is a 20-bit accumulator 1 = Counter is a 16-bit accumulator
DBITM	R/W	0b	Digital Lock Manual Override Setting for Analog PLL: 0 = Automatic Mode 1 = Manual Mode

Analog PLL Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
VCOMAN[2:0]	R/W	001b	Manual Lock Mode VCO Selection Setting for Analog PLL: 000 = VCO0 001 = VCO1 010 - 111 = Reserved
DBIT[4:0]	R/W	01011b	Manual Mode Digital Lock Control Setting for VCO in Analog PLL.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7K. Power Down Control Register Bit Field Locations and Descriptions

Power Down Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
006C	Rsvd						LCKMODE	DBL_DIS
006D	Rsvd						CLK1_DIS	CLK0_DIS
006E	Rsvd							
006F	Rsvd				Q3_DIS	Q2_DIS	Q1_DIS	Q0_DIS
0070	Rsvd					DPLL_DIS	DSM_DIS	CALRST

Power Down Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
LCKMODE	R/W	0b	Controls the behavior of the LOL alarm de-assertion: 0 = LOL alarm de-asserts once PLL is locked 1 = LOL alarm de-asserts once PLL is locked and output clocks are stable
DBL_DIS	R/W	0b	Controls whether crystal input frequency is doubled before being used in PLL: 0 = 2x Actual Crystal Frequency Used 1 = Actual Crystal Frequency Used
CLKm_DIS	R/W	0b	Disable Control for Input Reference m (m = 0, 1): 0 = Input Reference m is Enabled 1 = Input Reference m is Disabled
Qm_DIS	R/W	0b	Disable Control for Output Qm, nQm (m = 0, 1, 2, 3): 0 = Output Qm, nQm functions normally 1 = All logic associated with Output Qm, nQm is Disabled & Driver in High-Impedance state
DPLL_DIS	R/W	0b	Disable Control for Digital PLL: 0 = Digital PLL Enabled 1 = Digital PLL Disabled
DSM_DIS	R/W	0b	Disable Control for Delta-Sigma Modulator for Analog PLL: 0 = DSM Enabled 1 = DSM Disabled
CALRST	R/W	0b	Reset Calibration Logic for Analog PLL: 0 = Calibration Logic for Analog PLL Enabled 1 = Calibration Logic for Analog PLL Disabled
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7L. Input Monitor Control Register Bit Field Locations and Descriptions

Input Monitor Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0071	Rsvd							LOS_0[16]
0072	LOS_0[15:8]							
0073	LOS_0[7:0]							
0074	Rsvd							LOS_1[16]
0075	LOS_1[15:8]							
0076	LOS_1[7:0]							
0077	Rsvd							
0078	Rsvd							

Input Monitor Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LOS_m[16:0]	R/W	1FFFFh	Number of Input Monitoring clock periods before Input Reference m (m = 0, 1) is considered to be missed (soft alarm). Minimum setting is 3.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7M. Interrupt Enable Control Register Bit Field Locations and Descriptions

Interrupt Enable Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0079	Rsvd	LOL_EN	Rsvd	HOLD_EN	Rsvd		LOS1_EN	LOS0_EN

Interrupt Enable Control Register Block Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
LOL_EN	R/W	0b	Interrupt Enable Control for Loss-of-Lock Interrupt Status Bit: 0 = LOL_INT register bit will not affect status of nINT output signal 1 = LOL_INT register bit will affect status of nINT output signal
HOLD_EN	R/W	0b	Interrupt Enable Control for Holdover Interrupt Status Bit: 0 = HOLD_INT register bit will not affect status of nINT output signal 1 = HOLD_INT register bit will affect status of nINT output signal
LOSm_EN	R/W	0b	Interrupt Enable Control for Loss-of-Signal Interrupt Status Bit for Input Reference m: 0 = LOSm_INT register bit will not affect status of nINT output signal 1 = LOSm_INT register bit will affect status of nINT output signal
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7N. Factory Setting Register Bit Field Locations

Factory Setting Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
007A	27h							
007B	000b			1b	0b	1b	0b	0b

Table 7O. Interrupt Status Register Bit Field Locations and Descriptions

This register contains "sticky" bits for tracking the status of the various alarms. Whenever an alarm occurs, the appropriate Interrupt Status bit will be set. The Interrupt Status bit will remain asserted even after the original alarm goes away. The Interrupt Status bits remain asserted until explicitly cleared by a write of a '1' to the bit over the serial port. This type of functionality is referred to as Read / Write-1-to-Clear (R/W1C).

Interrupt Status Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0200	Rsvd	LOL_INT	Rsvd	HOLD_INT	Rsvd		LOS1_INT	LOS0_INT
0201	Rsvd							

Interrupt Status Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
LOL_INT	R/W1C	0b	Interrupt Status Bit for Loss-of-Lock: 0 = No Loss-of-Lock alarm flag on PLL has occurred since the last time this register bit was cleared 1 = At least one Loss-of-Lock alarm flag on PLL has occurred since the last time this register bit was cleared
HOLD_INT	R/W1C	0b	Interrupt Status Bit for Holdover: 0 = No Holdover alarm flag has occurred since the last time this register bit was cleared 1 = At least one Holdover alarm flag has occurred since the last time this register bit was cleared
LOSm_INT	R/W1C	0b	Interrupt Status Bit for Loss-of-Signal on Input Reference m: 0 = No Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared 1 = At least one Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7P. General Purpose Input Status Register Bit Field Locations and Descriptions

Global Interrupt Status Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
020C	Rsvd				GPI[3]	GPI[2]	GPI[1]	GPI[0]

General Purpose Input Status Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
GPI[3:0]	R/O	-	Shows current values on GPIO[3:0] pins that are configured as General-Purpose Inputs.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Table 7Q. Global Interrupt Status Register Bit Field Locations and Descriptions

Global Interrupt Status Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
020D	Rsvd		Rsvd		Rsvd			INT
020E	Rsvd				Rsvd			
020F	Rsvd			Rsvd				
0210	Rsvd					Rsvd	EEP_ERR	BOOTFAIL
0211	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	EEPDONE
0212	Rsvd							

Global Interrupt Status Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
INT	R/O	-	Device Interrupt Status: 0 = No Interrupt Status bits that are enabled are asserted (nINT pin released) 1 = At least one Interrupt Status bit that is enabled is asserted (nINT pin asserted low)
EEP_ERR	R/O	-	CRC Mismatch on EEPROM Read. Once set this bit is only cleared by reset.
BOOTFAIL	R/O	-	Reading of Serial EEPROM failed. Once set this bit is only cleared by reset.
EEPDONE	R/O	-	Serial EEPROM Read cycle has completed. Once set this bit is only cleared by reset.
Rsvd	R/W	-	Reserved. Always write 0 to this bit location. Read values are not defined.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I OSCI Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, V_O (Q[3:0], nQ[3:0])	-0.5V to V_{CCOX}[1] + 0.5V
Outputs, V_O (GPIO, SCLK, SDATA, nINT)	-0.5V to V_{CCCS} + 0.5V
Outputs, I_O (Q[3:0], nQ[3:0]) Continuous Current Surge Current	 40mA 65mA
Outputs, I_O (GPIO[3:0], SCLK, SDATA, nINT) Continuous Current Surge Current	 8mA 13mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE 1: V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

Supply Voltage Characteristics

Table 8A. Power Supply DC Characteristics, V_{CC} = 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	V_{CC}	V
V_{CCCS}	Control and Status Supply Voltage		1.71		V_{CC}	V
I_{CC}	Core Supply Current[1]			42	47	mA
I_{CCCS}	Control and Status Supply Current[2]			3	5	mA
I_{CCA}	Analog Supply Current[1]			93	119	mA
I_{EE}	Power Supply Current[3]	Q[3:0] Configured for LVPECL Logic Levels; Outputs Unloaded[4]		256	320	mA
I_{EE}	Power Supply Current[3]	Q[3:0] Configured for LVPECL, Outputs Disabled; Logic Levels; Outputs Unloaded[5]		236	309	mA

NOTE 1: I_{CC}, I_{CCA} and I_{CCCS} are included in I_{EE} when Q[3:0] configured for LVPECL logic levels.
NOTE 2: GPIO [3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST pins are floating.
NOTE 3: Internal dynamic switching current at maximum f_{OUT} is included.
NOTE 4: Outputs enabled.
NOTE 5: Outputs disabled.

Table 8B. Power Supply DC Characteristics, V_{CC} = 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	V_{CC}	V
V_{CCCS}	Control and Status Supply Voltage		1.71		V_{CC}	V
I_{CC}	Core Supply Current[1]			42	47	mA
I_{CCCS}	Control and Status Supply Current[2]			3	5	mA
I_{CCA}	Analog Supply Current[1]			90	116	mA
I_{EE}	Power Supply Current[3]	Q[3:0] Configured for LVPECL Logic Levels. Outputs Unloaded[4]		240	300	mA
I_{EE}	Power Supply Current[3]	Q[3:0] Configured for LVPECL, Outputs Disabled; Logic Levels. Outputs Unloaded[5]		228	294	mA

NOTE 1: I_{CC}, I_{CCA} and I_{CCCS} are included in I_{EE} when Q[3:0] configured for LVPECL logic levels.

NOTE 2: GPIO [3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST pins are floating.GPIO [3:0], SDATA, SCLK, S_A1, S_A0, nINT, nWP, nRST pins are floating.

NOTE 3: Internal dynamic switching current at maximum f_{OUT} is included.

NOTE 4: Outputs enabled.

NOTE 5: Outputs disabled.

Table 8C. Maximum Output Supply Current, V_{CC} = V_{CCCS} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[1] = 3.3V ±5%				V_{CCOx}[1] = 2.5V ±5%				V_{CCOx}[1] = 1.8V±5%	Units
			LVPECL	LVDS	HCSL	LVCMOS	LVPECL	LVDS	HCSL	LVCMOS	LVCMOS	
I_{CCO0}[2]	Q0, nQ0 Output Supply Current	Outputs Unloaded[3]	45	53	44	45	34	42	33	36	30	mA
		Outputs Unloaded[4]	39	38	38	34	31	31	31	28	26	mA
I_{CCO1}[2]	Q1, nQ1 Output Supply Current	Outputs Unloaded[3]	45	53	44	45	34	42	33	35	30	mA
		Outputs Unloaded[4]	38	38	38	34	32	30	30	27	25	mA
I_{CCO2}[2]	Q2, nQ2 Output Supply Current	Outputs Unloaded[3]	47	56	46	49	36	44	36	38	33	mA
		Outputs Unloaded[4]	41	40	40	36	34	33	33	30	28	mA
I_{CCO3}[2]	Q3, nQ3 Output Supply Current	Outputs Unloaded[3]	45	53	44	45	36	44	36	38	33	mA
		Outputs Unloaded[4]	38	38	38	34	34	32	32	30	28	mA

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: Internal dynamic switching current at maximum f_{OUT} is included.

NOTE 3: Outputs enabled.

NOTE 4: Outputs disabled.

DC Electrical Characteristics

Table 8E. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	nWP, nRST, GPIO[3:0], SDATA, SCLK, S_A1, S_A0	V_{CCCS} = 3.3V	2.1		V_{CCCS} +0.3	V
			V_{CCCS} = 2.5V	1.7		V_{CCCS} +0.3	V
			V_{CCCS} = 1.8V	1.4		V_{CCCS} +0.3	V
V_{IL}	Input Low Voltage	nWP, nRST, GPIO[3:0], SDATA, SCLK, S_A1, S_A0	V_{CCCS} = 3.3V	-0.3		0.8	V
			V_{CCCS} = 2.5V	-0.3		0.6	V
			V_{CCCS} = 1.8V	-0.3		0.4	V
I_{IH}	Input High Current	S_A1, S_A0	V_{CCCS} = V_{IN} = 3.465V, 2.625V, 1.89V			150	µA
		nRST, nWP, SDATA, SCLK	V_{CCCS} = V_{IN} = 3.465V, 2.625V, 1.89V			5	µA
		GPIO[3:0]	V_{CCCS} = V_{IN} = 3.465V, 2.625V, 1.89V			1	mA
I_{IL}	Input Low Current	S_A1, S_A0	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-5			µA
		nRST, nWP, SDATA, SCLK	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-150			µA
		GPIO[3:0]	V_{CCCS} = 3.465V, 2.625V, 1.89V, V_{IN} = 0V	-1			mA
V_{OH}	Output High Voltage	SDATA[1], SCLK[1], nINT[1]	V_{CCCS} = 3.3V ±5%, I_{OH} = -5µA	2.6			V
		GPIO[3:0]	V_{CCCS} = 3.3V ±5%, I_{OH} = -50µA	2.6			V
		SDATA[1], SCLK[1], nINT[1]	V_{CCCS} = 2.5V ±5%, I_{OH} = -5µA	1.8			V
		GPIO[3:0]	V_{CCCS} = 2.5V ±5%, I_{OH} = -50µA	1.8			V
		SDATA[1], SCLK[1], nINT[1]	V_{CCCS} = 1.8V ±5%, I_{OH} = -5µA	1.3			V
		GPIO[3:0]	V_{CCCS} = 1.8V ±5%, I_{OH} = -50µA	1.3			V
V_{OL}	Output Low Voltage	SDATA[1], SCLK[1], nINT[1]	V_{CCCS} = 3.3V ±5%, 2.5V±5%, or 1.8V±5% I_{OL} = 5mA			0.5	V
		GPIO[3:0]	V_{CCCS} = 3.3V ±5%, 2.5V±5%, or 1.8V±5% I_{OL} = 5mA			0.5	V

NOTE 1: Use of external pull-up resistors is recommended.

Table 8F. Differential Input DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKx,[1] nCLKx[1]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLKx[1]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLKx[1]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage[2]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[2, 3]			V_{EE}		V_{CC} -1.2	V

NOTE 1: CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

NOTE 2: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.

NOTE 3: Common mode voltage is defined as the cross-point.

Table 8G. LVPECL DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[1] = 3.3V±5%			V_{CCOx}[1] = 2.5V±5%			Units
			Minimum	Typical	Maximum	Minimum	Typical	Maximum	
V_{OH}	Output High Voltage[2]		V_{CCOX} - 1.3		V_{CCOX} - 0.8	V_{CCOX} - 1.4		V_{CCOX} - 0.9	V
V_{OL}	Output Low Voltage[2]		V_{CCOX} - 1.95		V_{CCOX} - 1.75	V_{CCOX} - 1.95		V_{CCOX} - 1.75	V

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: Outputs terminated with 50Ω to V_{CCOx} – 2V.

Table 8H. LVDS DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOX} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200		400	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: Terminated with 100Ω across Qx and nQx.

Table 8I. LVCMOS DC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[1] = 3.3V±5%			V_{CCOx}[1] = 2.5V±5%			V_{CCOx}[1] = 1.8V ±5%			Units
			Minimum	Typical	Maximum	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
V_{OH}	Output High Voltage	I_{OH} = -8mA	2.6			1.8			1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.5			0.5			0.5	V

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

Table 9. Input Frequency Characteristics, V_{CC} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency[1]	OSCI, OSCO	Using a Crystal (See Table 10 for Crystal Characteristics)	10		50	MHz
			Over-driving Crystal Input Doubler Logic Enabled[2]	10		62.5	MHz
			Over-driving Crystal Input Doubler Logic Disabled[2]	10		125	MHz
		CLKx,[3] nCLKx[3]		0.008		875	MHz
f_{PD}	Phase Detector Frequency[4]			0.008		8	MHz
f_{SCLK}	Serial Port Clock SCLK (slave mode)	I^2C Operation		100		400	kHz

NOTE 1: For the input reference frequency, the divider values must be set for the VCO to operate within its supported range.

NOTE 2: For optimal noise performance, the use of a quartz crystal is recommended. Refer to Overdriving the XTAL Interface in the Applications Information section.

NOTE 3: CLKx denotes CLK0, CLK1; nCLKx denotes nCLK0, nCLK1.

NOTE 4: Pre-dividers must be used to divide the CLKx frequency down to a f_{PD} valid frequency range.

Table 10. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		50	MHz
Equivalent Series Resistance (ESR)			15	30	Ω
Load Capacitance (C_L)			12		pF
Frequency Stability (total)		-100		100	ppm

AC Electrical Characteristics

Table 11. AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[1, 2]

Symbol	Parameter			Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Operating Frequency				3000		4000	MHz
f_{OUT}	Output Frequency	LVPECL, LVDS, HCSL			0.008		1000	MHz
		LVCMOS			0.008		250	MHz
t_R / t_F	Output Rise and Fall Times		LVPECL	20% to 80%		320	520	ps
			LVDS	20% to 80%, V_{CCOx} = 3.3V		160	320	ps
				20% to 80%, V_{CCOx} = 2.5V		200	400	ps
			HCSL	20% to 80%		280	470	ps
			LVCMOS[3, 4]	20% to 80%, V_{CCOx} = 3.3V		240	310	ps
				20% to 80%, V_{CCOx} = 2.5V		260	330	ps
				20% to 80%, V_{CCOx} = 1.8V		350	550	ps
SR	Output Slew Rate	LVPECL		Differential Waveform, Measured ±150mV from Center	1		5	V/ns
		LVDS		Differential Waveform, Measured ±150mV from Center, V_{CCOx} = 2.5V	0.5		4	V/ns
				Differential Waveform, Measured ±150mV from Center, V_{CCOx} = 3.3V	0.5		5	V/ns
		HCSL		Measured on Differential Waveform, ±150mV from Center, V_{CCOx} = 2.5V, f_{OUT} ≤ 156.25MHz	1.5		5	V/ns
				Measured on Differential Waveform, ±150mV from Center, V_{CCOx} = 3.3V, f_{OUT} ≤ 156.25MHz	2.5		6.5	V/ns
*t*sk(b)	Bank Skew	LVPECL	Q0, nQ0, Q1, nQ1	NOTE[5, 6, 7, 8]			50	ps
			Q2, nQ2, Q3, nQ3	NOTE[5, 6, 7, 8]			50	ps
		LVDS	Q0, nQ0, Q1, nQ1	NOTE[5, 6, 7, 8]			50	ps
			Q2, nQ2, Q3, nQ3	NOTE[5, 6, 7, 8]			50	ps
		HCSL	Q0, nQ0, Q1, nQ1	NOTE[5, 6, 7, 8]			50	ps
			Q2, nQ2, Q3, nQ3	NOTE[5, 6, 7, 8]			50	ps
		LVCMOS	Q0, nQ0, Q1, nQ1	NOTE[3, 5, 6, 8, 9]			50	ps
			Q2, nQ2, Q3, nQ3	NOTE[3, 5, 6, 8, 9]			65	ps
odc	Output Duty Cycle[10]		LVPECL, LVDS, HCSL		45	50	55	%
			LVCMOS		40	50	60	%

Table 11. AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[1, 2] **(Continued)**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
∆SPO	Static Phase Offset Variation[11]		f_{IN} = f_{OUT} = 156.25MHz, V_{CC} = V_{CCOX} = 2.5V±5% or 3.3V±5%	-250		250	ps
	Initial Frequency Offset[12, 13, 14]		Switchover or Entering / Leaving Holdover State	-50		50	ppb
	Output Phase Change in Fully Hitless Switching[13, 14, 15]		Switchover or Entering / Leaving Holdover State		2		ns
Φ_{SSB}(1k)	Single Sideband Phase Noise[16]	1kHz	122.88MHz Output		-102		dBc/Hz
Φ_{SSB}(10k)		10kHz	122.88MHz Output		-126		dBc/Hz
Φ_{SSB}(100k)		100kHz	122.88MHz Output		-133		dBc/Hz
Φ_{SSB}(1M)		1MHz	122.88MHz Output		-145		dBc/Hz
Φ_{SSB}(10M)		10MHz	122.88MHz Output		-155		dBc/Hz
Φ_{SSB}(30M)		≥30MHz	122.88MHz Output		-156		dBc/Hz
	Spurious Limit at Offset[17]	≥800kHz	122.88MHz LVPECL Output		-77		dBc
$t_{startup}$	Startup Time	Internal OTP Startup[13]	From V_{CC} >80% to First Output Clock Edge		110	150	ms
		External EEPROM Startup[13, 18]	From V_{CC} >80% to First Output Clock Edge (0 retries) I^2C Frequency = 100kHz		120	200	ms
			From V_{CC} >80% to First Output Clock Edge (0 retries) I^2C Frequency = 400kHz		110	150	ms
			From V_{CC} >80% to First Output Clock Edge (31 retries) I^2C Frequency = 100kHz		610	1200	ms
			From V_{CC} >80% to First Output Clock Edge (31 retries) I^2C Frequency = 400kHz		270	500	ms

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 3: Appropriate SE_MODE bit must be configured to select phase-aligned or phase-inverted operation.

NOTE 4: All Q and nQ outputs in phase-inverted operation.

NOTE 5: This parameter is guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7: Measured at the output differential cross point.

NOTE 8: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 9: Measured at $V_{CCOx}/2$ of the rising edge. All Qx and nQx outputs phase-aligned.

NOTE 10: Characterized in PLL Mode. Duty cycle of bypassed signals (input reference clocks or crystal input) is not adjusted by the device.

NOTE 11: This parameter was measured using CLK0 as the reference input and CLK1 as the external feedback input. Characterized with 8T49N242-902.

NOTE 12: Tested in fast-lock operation after >20 minutes of locked operation to ensure holdover averaging logic is stable.

NOTE 13: This parameter is guaranteed by design.

NOTE 14: Using internal feedback mode configuration.

NOTE 15: Device programmed with SWMODE = 0 (absorbs phase differences).

NOTE 16: Characterized with 8T49N242-900.

NOTE 17: Tested with all outputs operating at 122.88MHz.

NOTE 18: Assuming a clear I^2C bus.

Table 12. HCSL AC Characteristics, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-back Voltage Margin[3, 4]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed[3, 4]		500			ps
V_{MAX}	Absolute Max. Output Voltage[5, 6]				1150	mV
V_{MIN}	Absolute Min. Output Voltage[5, 7]		-300			mV
V_{CROSS}	Absolute Crossing Voltage[8, 9]		200		500	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} Over all Edges[8, 10]				140	mV

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 3: Measurement taken from differential waveform.

NOTE 4: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

NOTE 5: Measurement taken from single ended waveform.

NOTE 6: Defined as the maximum instantaneous voltage including overshoot.

NOTE 7: Defined as the minimum instantaneous voltage including undershoot.

NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

NOTE 10: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in V_{CROSS} for any particular system.

Table 13A. Typical RMS Phase Jitter, V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{CCOx} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5% (1.8V only supported for LVCMOS outputs), T_A = -40°C to 85°C[1]

Symbol	Parameter	Test Conditions	LVPECL	LVDS	HCSL	LVCMOS	Units
tjit(φ)	RMS Phase Jitter[2] (Random)	f_{OUT} = 122.88MHz, Integration Range: 12kHz - 20MHz[3, 4]	323	350	340	349	fs
		f_{OUT} = 156.25MHz, Integration Range: 12kHz - 20MHz[3, 5]	328	359	364	328	fs
		f_{OUT} = 622.08MHz, Integration Range: 12kHz - 20MHz[3, 6]	292	277	276	N/A[7]	fs

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: It is recommended to use IDT's *Timing Commander* software to program the device for optimal jitter performance.

NOTE 3: Tested with all outputs operating at the same output frequency.

NOTE 4: Characterized with 8T49N242-900.

NOTE 5: Characterized with 8T49N242-901.

NOTE 6: Characterized with 8T49N242-902.

NOTE 7: This frequency is not supported for LVCMOS operation.

Table 13B. PCI Express Jitter Specifications, V_{CC} = V_{CCOx} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter	Test Conditions[3]	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak[4, 5]	*ƒ* = 100MHz, 40MHz Crystal Input Evaluation Band: 0Hz - Nyquist (Clock Frequency/2)		6.99	16	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS[5, 6]	*ƒ* = 100MHz, 40MHz Crystal Input High Band: 1.5MHz - Nyquist (Clock Frequency/2)		0.51	1.5	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS[5, 6]	*ƒ* = 100MHz, 40MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.20	1.5	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS[5, 7]	*ƒ* = 100MHz, 40MHz Crystal Input Evaluation Band: 0Hz - Nyquist (Clock Frequency/2)		0.13	0.5	0.8	ps

NOTE 1: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}.

NOTE 2: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 3: Outputs configured in HCSL mode. FOX #277LF-40-18 crystal used with doubler logic enabled.

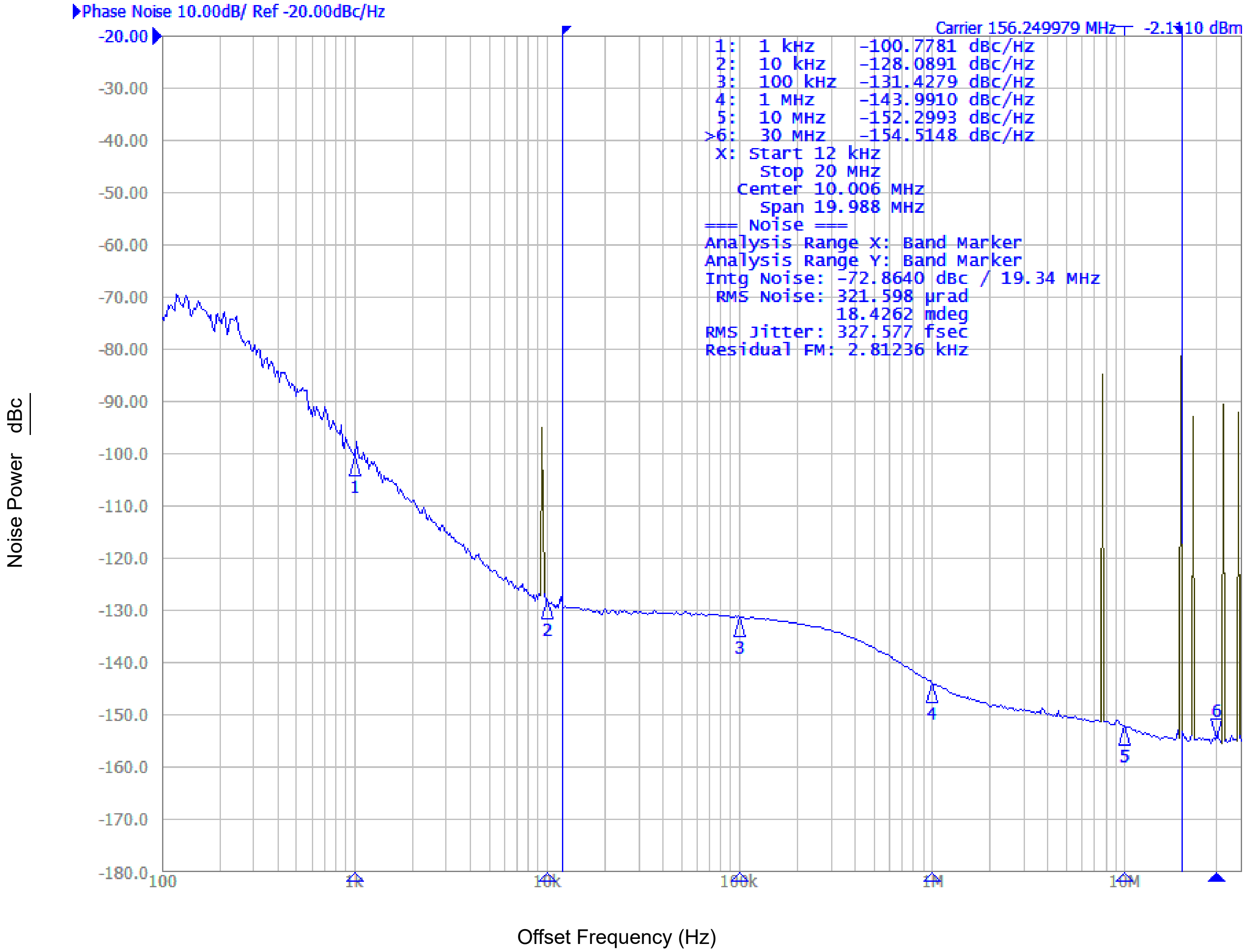
NOTE 4: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1

NOTE 5: This parameter is guaranteed by characterization. Not tested in production.

NOTE 6: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).

NOTE 7: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

Typical Phase Noise at 156.25MHz



Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Input

For applications not requiring the use of one or more reference clock inputs, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx not be driven with active signals when not selected.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

Any unused LVDS output pair can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached.

HCSL Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 7A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 7B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSCI input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

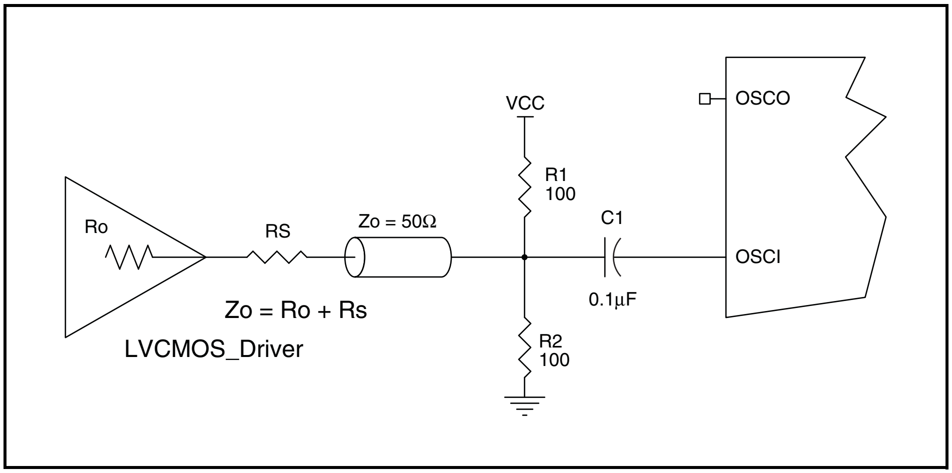


Figure 7A. General Diagram for LVCMOS Driver to XTAL Input Interface

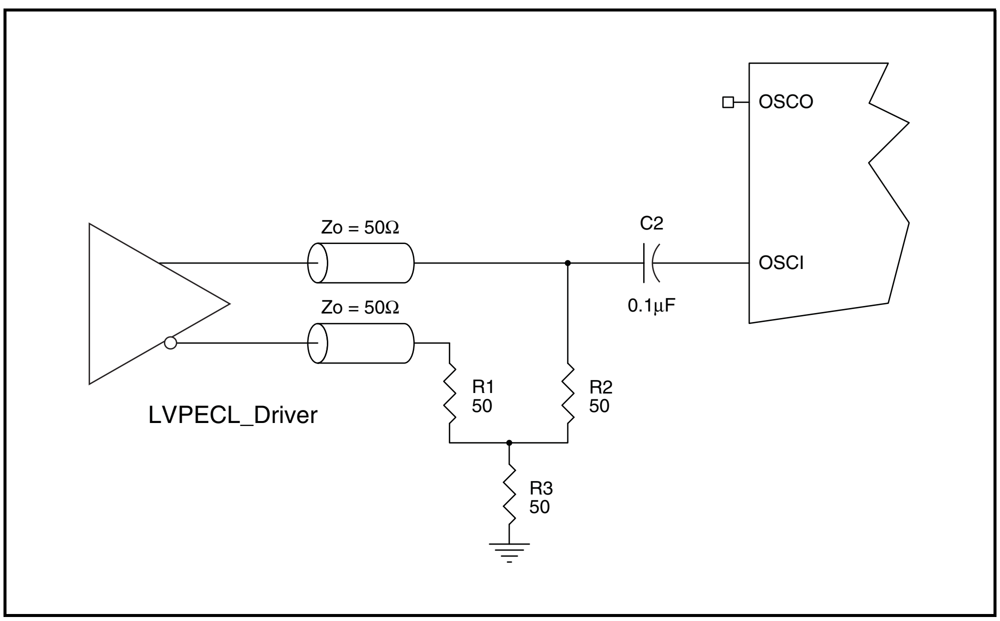


Figure 7B. General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 8 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

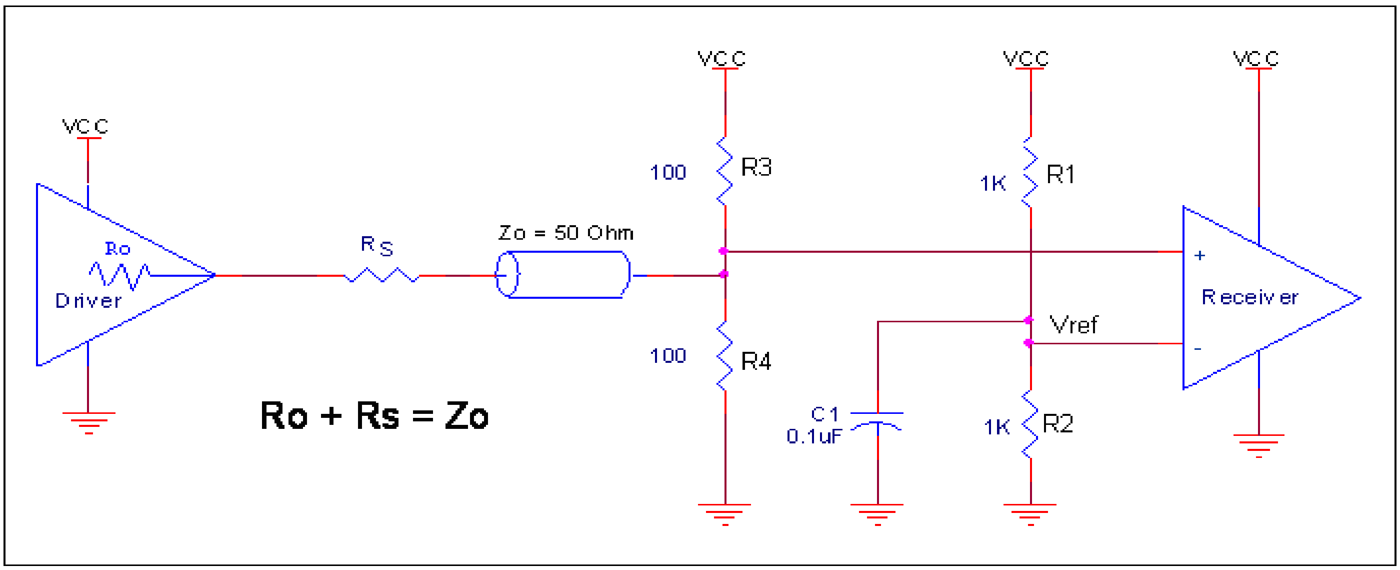


Figure 8. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 9A to Figure 9E show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 9A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

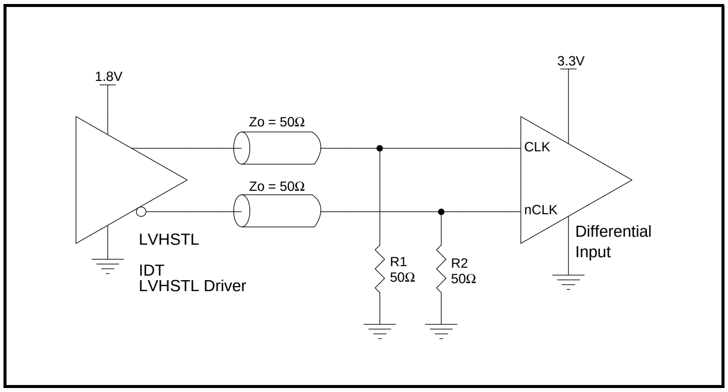


Figure 9A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

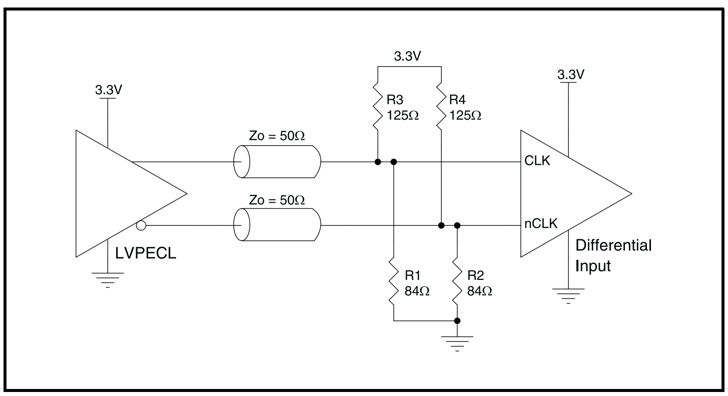


Figure 9B. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

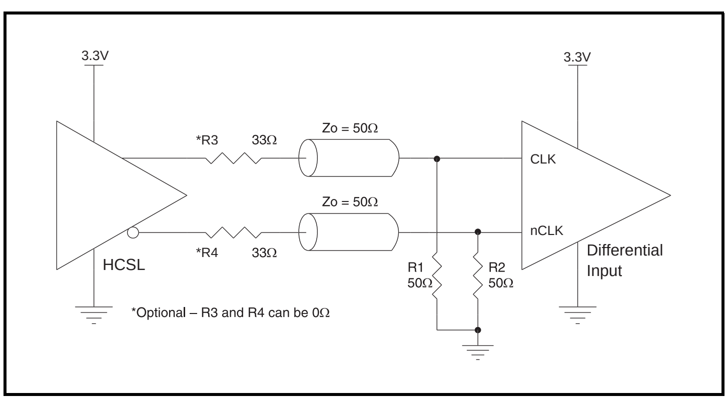


Figure 9C. CLKx/nCLKx Input Driven by a 3.3V HCSL Driver

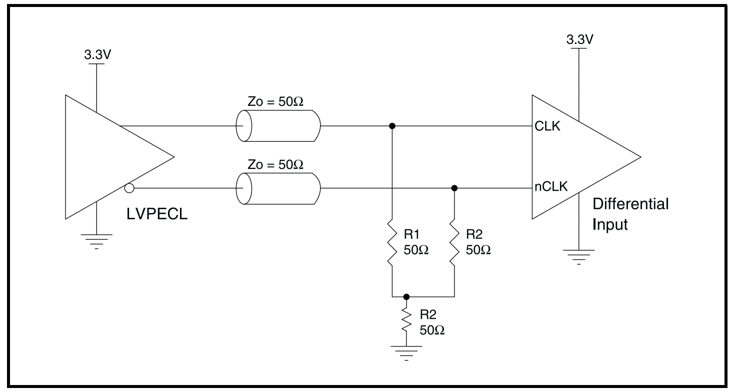


Figure 9D. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

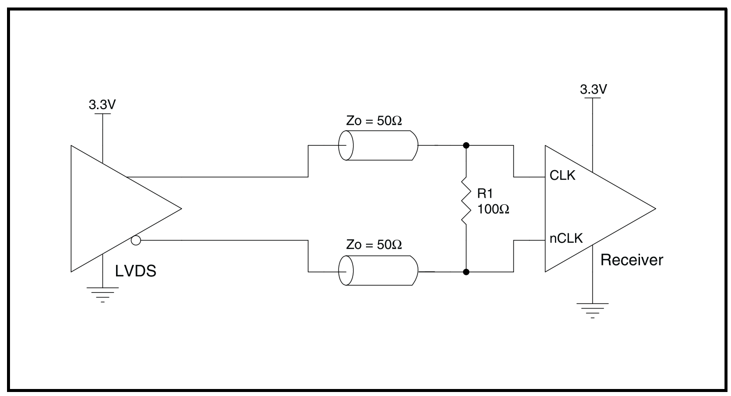


Figure 9E. CLKx/nCLKx Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 10A* to *Figure 10E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 10A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

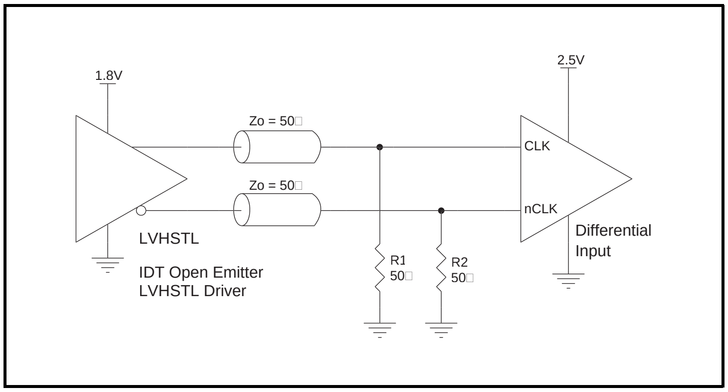


Figure 10A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

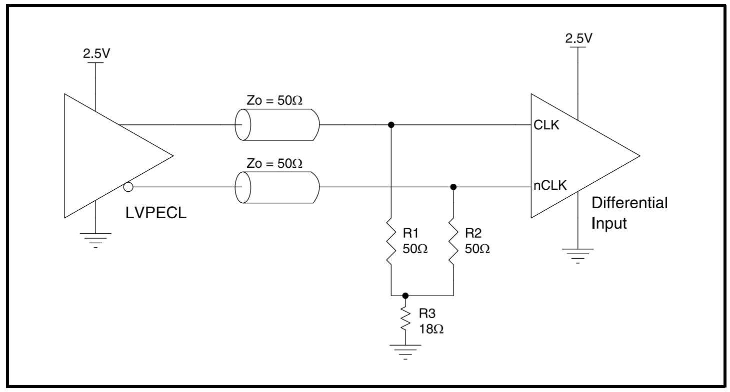


Figure 10D. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

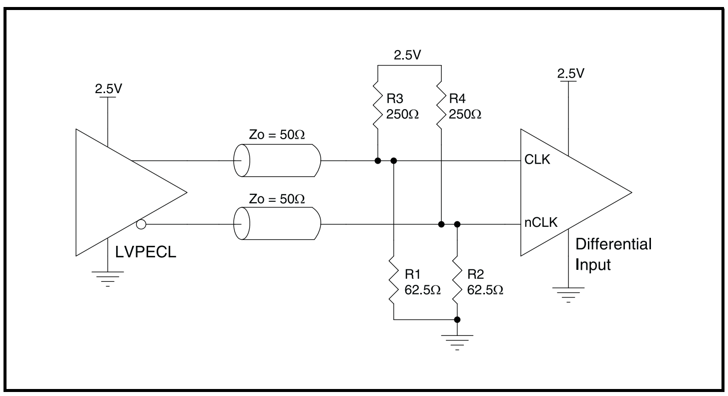


Figure 10B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

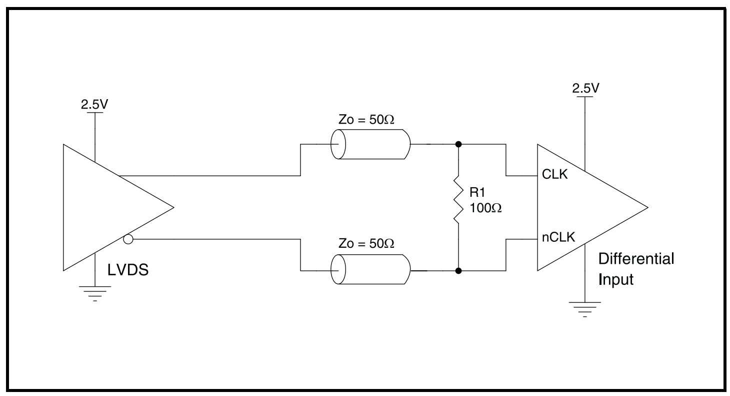


Figure 10E. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

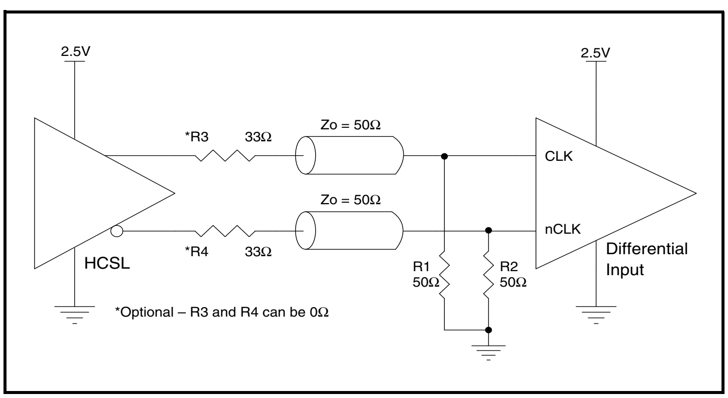


Figure 10C. CLKx/nCLKx Input Driven by a 2.5V HCSL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 11A* can be used with either type of output structure. *Figure 11B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

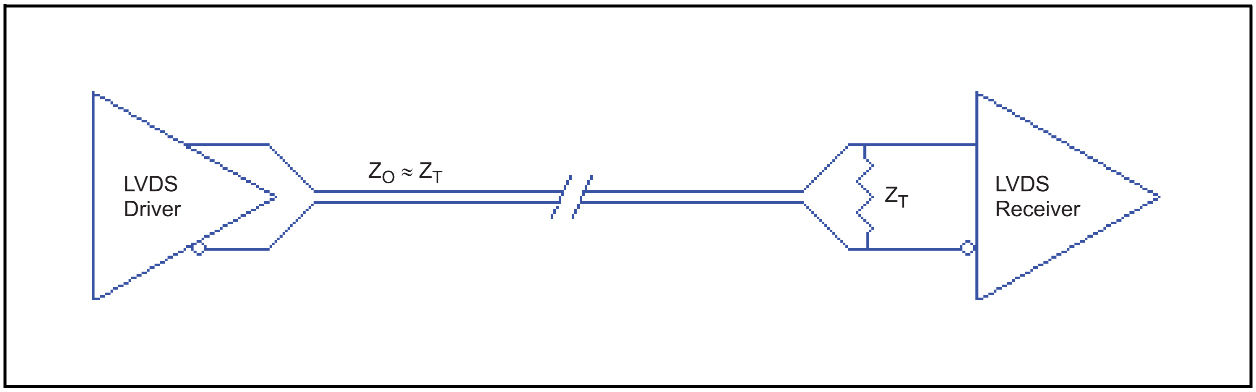


Figure 11A. Standard LVDS Termination

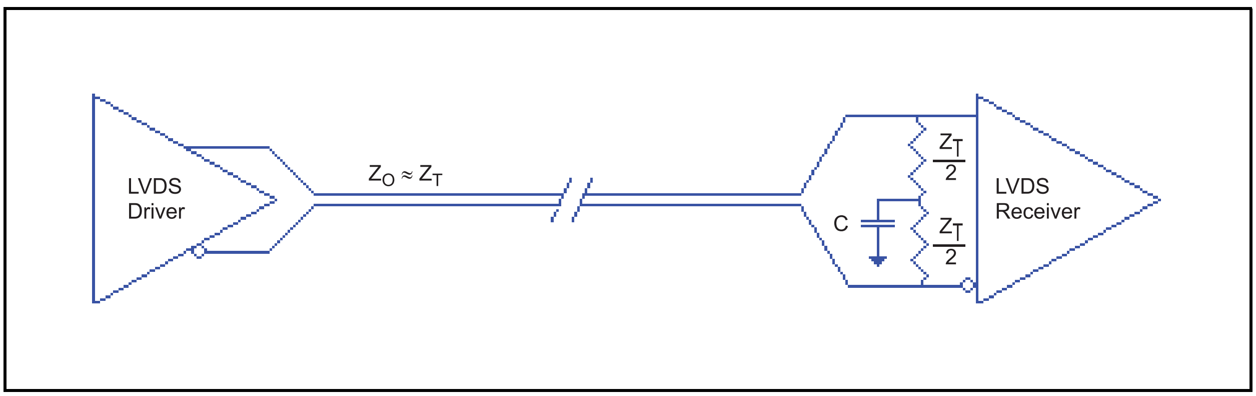


Figure 11B. Optional LVDS Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 12A and Figure 12B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

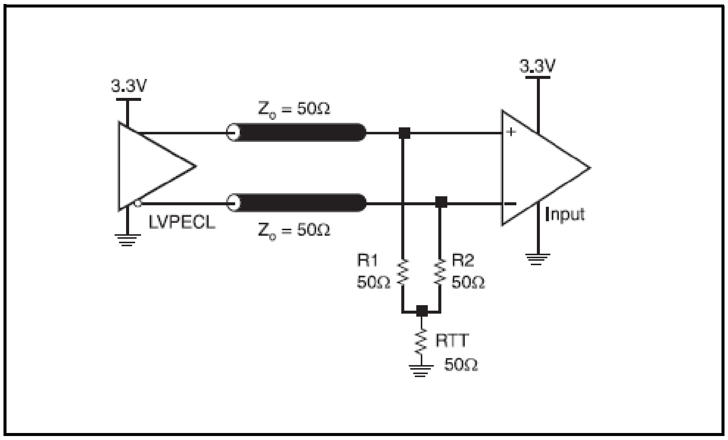


Figure 12A. 3.3V LVPECL Output Termination

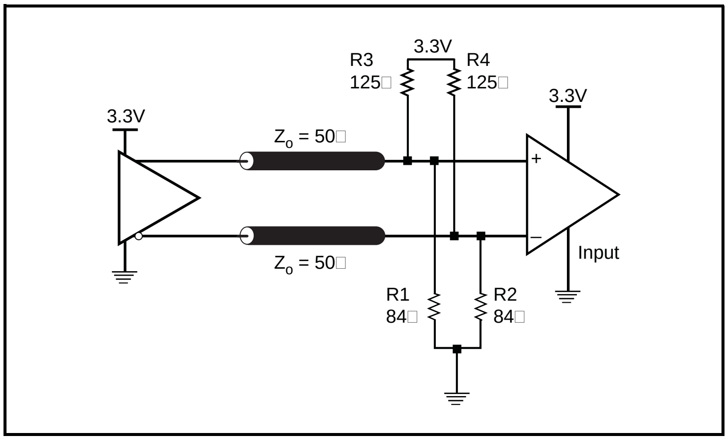


Figure 12B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 13A and *Figure 13C* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in *Figure 13C* can be eliminated and the termination is shown in *Figure 13B*.

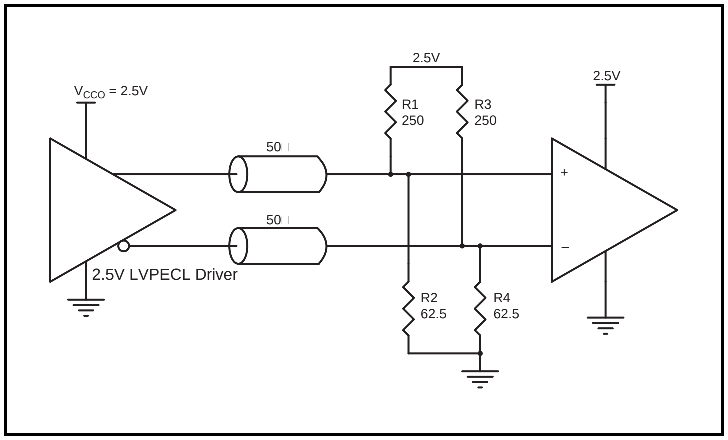


Figure 13A. 2.5V LVPECL Driver Termination Example

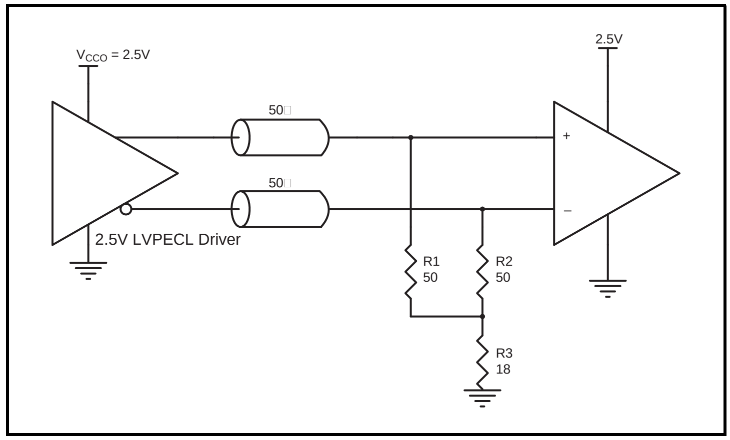


Figure 13C. 2.5V LVPECL Driver Termination Example

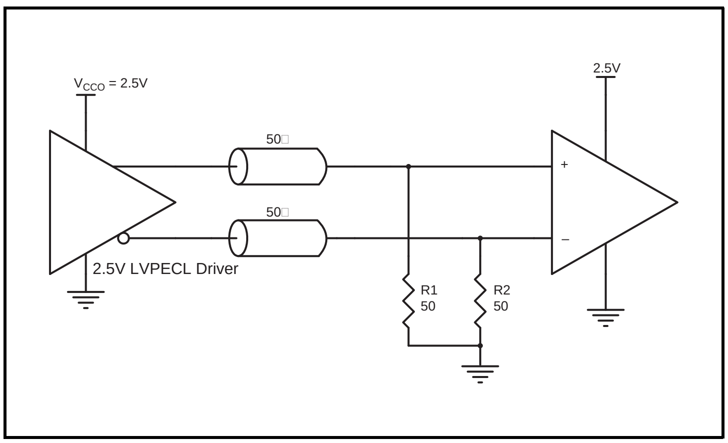


Figure 13B. 2.5V LVPECL Driver Termination Example

HCSL Recommended Termination

Figure 14A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

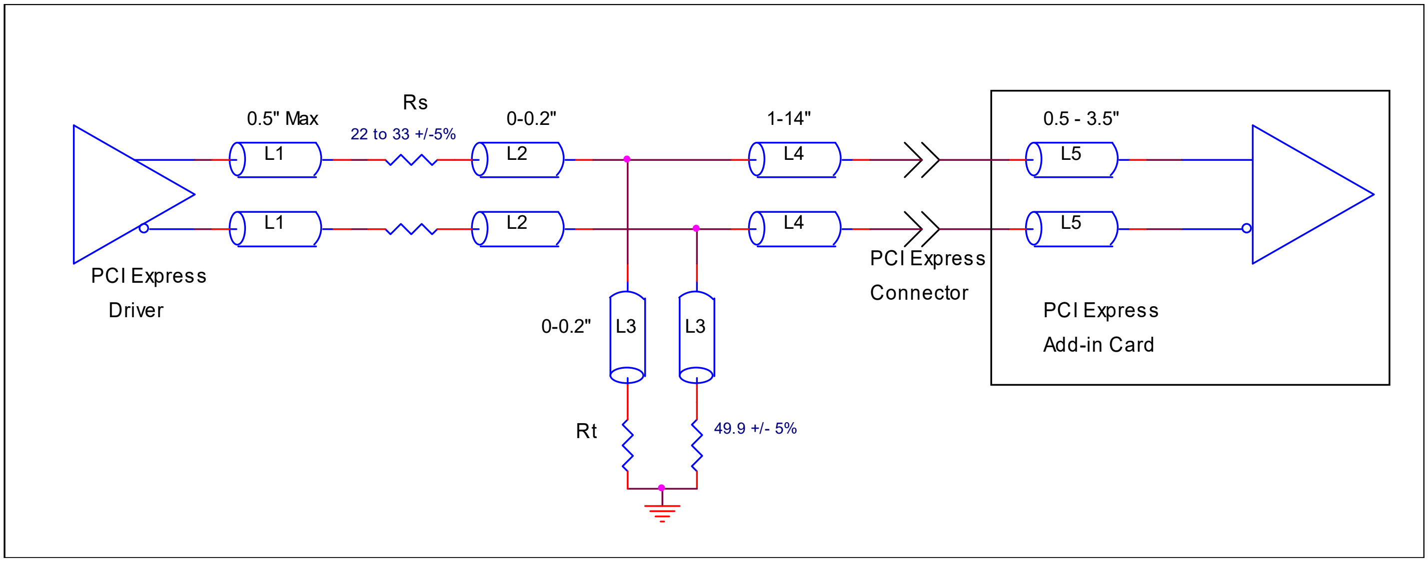


Figure 14A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 14A is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

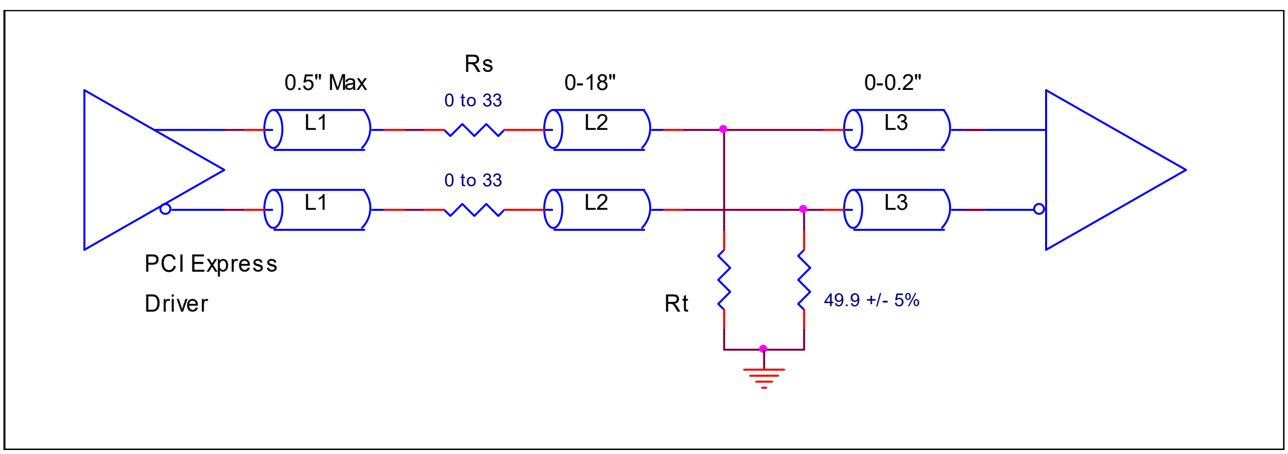


Figure 14B. Recommended Termination (where a point-to-point connection can be used)

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 15*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

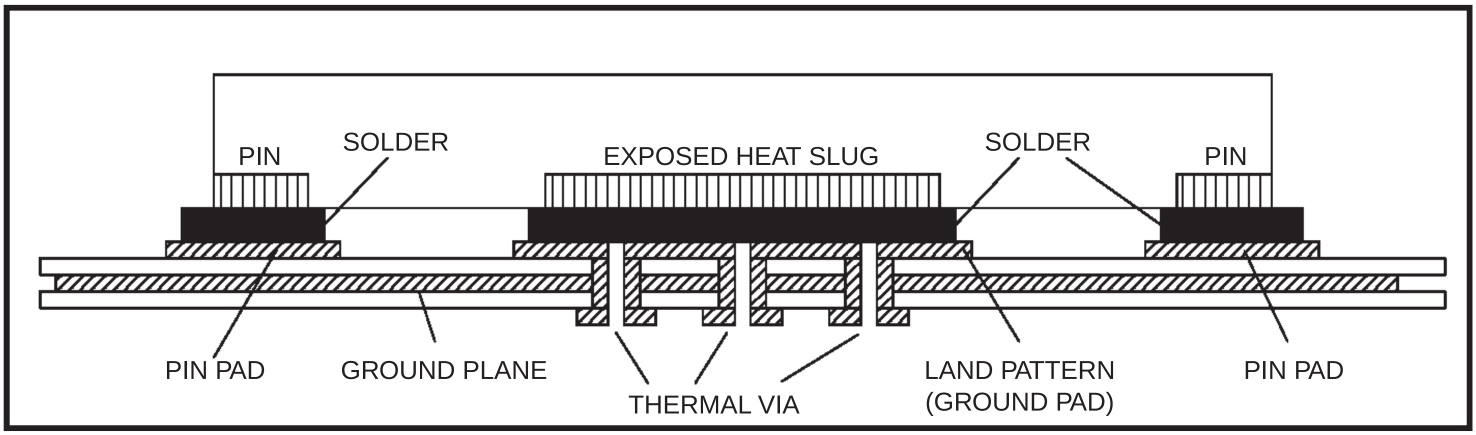


Figure 15. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic and Layout Information

Schematics for the 8T49N242 can be found on IDT.com. Please search for the 8T49N242 and click on the link for *evaluation board.* The evaluation board user guide includes schematic and layout information.

Crystal Recommendation

This device was validated using FOX 277LF series through-hole crystals including Part # 277LF-40-18 (40MHz). If a surface mount crystal is desired, we recommend IDT Part # 603-40-48 (40MHz) and FOX Part #603-40-48 (40MHz).

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

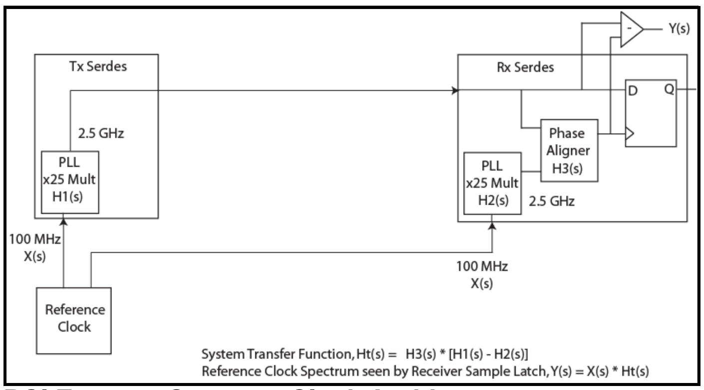
In the jitter analysis, the transmit (Tx) and receive (Rx) SerDes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

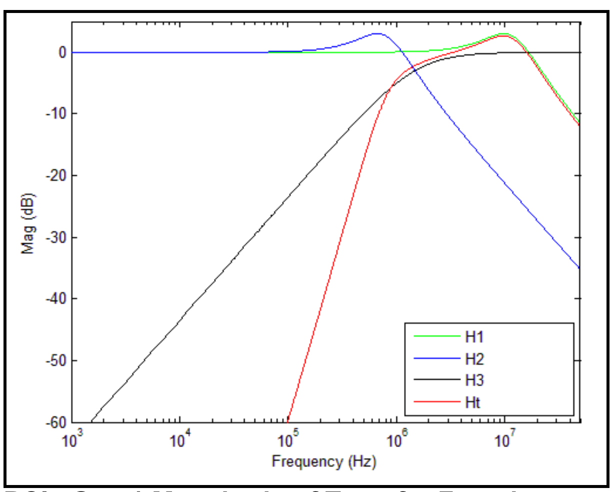
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



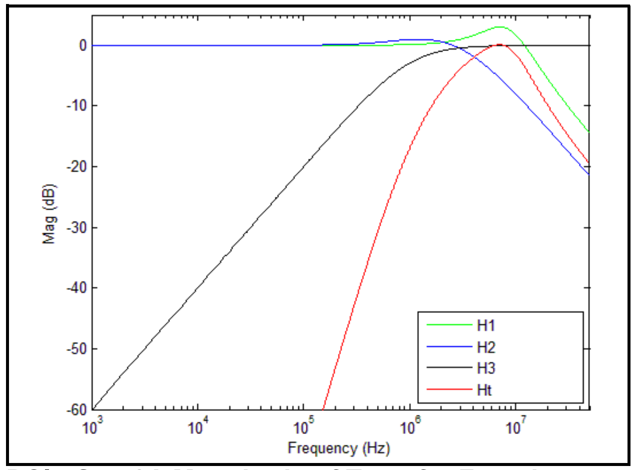
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

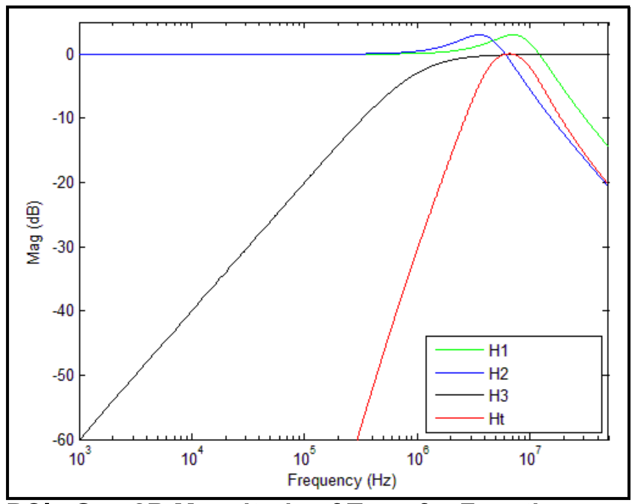


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

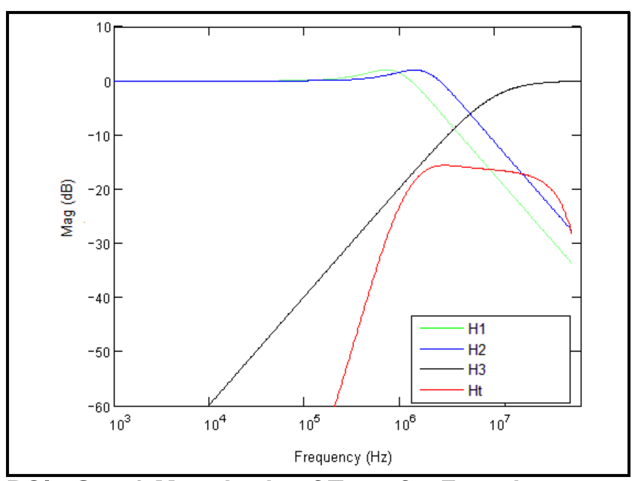


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Dissipation and Thermal Considerations

The 8T49N242 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as these features and functions are enabled.

The 8T49N242 is designed and characterized to operate within the ambient industrial temperature range of -40°C to 85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below are generated using maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8T49N242 has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). *Figure 16* below indicates the individual domains and the associated power pins.

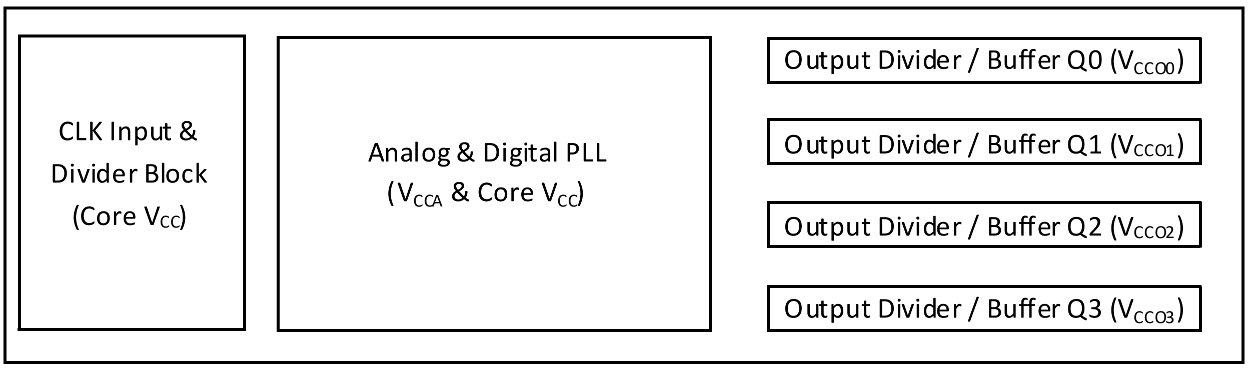


Figure 16. 8T49N242 Power Domains

Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core and analog voltage supplies from *Table 8A* and *Table 8B*.
2. Determine the nominal power consumption of each enabled output path which consists of:
   a. A base amount of power that is independent of operating frequency, as shown in Table 15A through Table 15I (depending on the chosen output protocol).
   b. A variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in Table 15A through Table 15I.
3. All of the above totals are summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heatsink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in *Table 14* below. Please contact IDT for assistance in calculating results under other scenarios.

Table 14. Thermal Resistance θ_{JA} for 40-Lead VFQFPN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.3°C/W	23.2°C/W	21.7°C/W

Current Consumption Data and Equations

Table 15A. 3.3V LVPECL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00682	33.3
Q1		
Q2		
Q3		

Table 15B. 3.3V HCSL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00675	33.2
Q1		
Q2		
Q3		

Table 15C. 3.3V LVDS Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00713	42.0
Q1		
Q2		
Q3		

Table 15G. 3.3V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	31.3
Q1	
Q2	
Q3	

Table 15D. 2.5V LVPECL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00476	28.1
Q1		
Q2		
Q3		

Table 15E. 2.5V HCSL Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00448	28.2
Q1		
Q2		
Q3		

Table 15F. 2.5V LVDS Output Calculation Table

Output	FQ_Factor (mA/MHz)	Base_Current (mA)
Q0	0.00496	36.3
Q1		
Q2		
Q3		

Table 15H. 2.5V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	26.2
Q1	
Q2	
Q3	

Table 15I. 1.8V LVCMOS Output Calculation Table

Output	Base_Current (mA)
Q0	24.2
Q1	
Q2	
Q3	

Applying the values to the following equation will yield output current by frequency:

Qx Current (mA) = FQ_Factor * Frequency (MHz) + Base_Current

where:

Qx Current is the specific output current according to output type and frequency

FQ_Factor is used for calculating current increase due to output frequency

Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pd_{total})$

where:

T_J is the junction temperature (°C)

T_A is the ambient temperature (°C)

θ_{JA} is the thermal resistance value from Table 14, dependent on ambient airflow (°C/W)

Pd_{total} is the total power dissipation of the 8T49N242 under usage conditions, including power dissipated due to loading (W).

Note that the power dissipation per output pair due to loading is assumed to be 27.95mW for LVPECL outputs and 44.5mW for HCSL outputs. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using C_{PD} (found in Table 2) and output frequency:

$Pd_{OUT} = C_{PD} * F_{OUT} * V_{CCO}^2$

where:

Pd_{OUT} is the power dissipation of the output (W)

C_{PD} is the power dissipation capacitance (pF)

F_{OUT} is the output frequency of the selected output (MHz)

V_{CCO} is the voltage supplied to the appropriate output (V)

Example Calculations

Example 1. Common Customer Configuration (3.3V Core Voltage)

Output	Output Type	Frequency (MHz)	V_{CCO}
Q0	LVPECL	125	3.3
Q1	LVPECL	100	3.3
Q2	LVPECL	50	3.3
Q3	LVPECL	25	3.3

- Core Supply Current + Control and Status Supply Current = I_{CC} + I_{CCCS} = **52mA (max)**
- Analog Supply Current, I_{CCA} = **119mA (max)**
- Output Supply Current:
  Q0 Current = 125 * 0.00682 + 33.3 = 34.15mA
  Q1 Current = 100 * 0.00682 + 33.3 = 33.98mA
  Q2 Current = 50 * 0.00682 + 33.3 = 33.64mA
  Q3 Current = 25 * 0.00682 + 33.3 = 33.47mA

- Total Output Supply Current = **135.24mA (max)**
- Total Device Current = 52mA + 119mA + 135.24mA = **306.24mA**
- Total Device Power = 3.465V * 306.24mA = **1061.12mW**
- Power dissipated through output loading:
  LVPECL = 27.95mW * 4 = **111.8mW**
  LVDS = already accounted for in device power
  HCSL = n/a
  LVCMOS = n/a
- Total Power = 1061.12mW + 111.8mW = **1172.92mW or 1.17W**

With an ambient temperature of 85°C and no airflow, the junction temperature is:

T_J = 85°C + 26.3°C/W * 1.17W = **115.8°C**

This is below the limit of 125°C.

Example 2. Common Customer Configuration (2.5V Core Voltage)

Output	Output Type	Frequency (MHz)	V_{CCO}
Q0	LVPECL	156.25	2.5
Q1	LVDS	125	2.5
Q2	HCSL	125	2.5
Q3	LVCMOS	25	2.5

- Core Supply Current + Control and Status Supply Current = I_{CC} + I_{CCCS} = **52mA (max)**
- Analog Supply Current, I_{CCA} = **116mA (max)**
- Output Supply Current:
  Q0 Current = 156.25 * 0.00476 + 28.1 = 28.84mA

  Q1 Current = 125 * 0.00496 + 36.3 = 36.92mA

  Q2 Current = 125 * 0.00448 + 28.2= 28.76mA

  Q3 Current = 26.2mA

- Total Output Supply Current = **120.72mA (max)**
- Total Device Current = 52mA + 116mA + 120.72mA = **288.72mA**
- Total Device Power = 2.625V * 288.72mA = **757.89mW**
- Power dissipated through output loading:
  LVPECL = 27.95mW * 1 = **27.95mW**

  LVDS = already accounted for in device power

  HCSL = 45.5mW * 1 = **44.5mW**

  LVCMOS = 10.5pF * 25MHz * $(2.625V)^2$ * 1 output pair = **1.81mW**
- Total Power = 757.89mW + 27.95mW + 44.5mW + 1.81mW = **832.15mW or 0.832W**

With an ambient temperature of 85°C and no airflow, the junction temperature is:

T_J = 85°C + 26.3°C/W * 0.832W = **106.9°C**

This is below the limit of 125°C.

Example 3. Common Customer Configuration (2.5V Core Voltage)

Output	Output Type	Frequency (MHz)	V_{CCO}
Q0	LVPECL	250	2.5
Q1	LVCMOS	100	1.8
Q2	LVCMOS	50	1.8
Q3	LVCMOS	25	1.8

- Core Supply Current + Control and Status Supply Current = I_{CC} + I_{CCCS} = **52mA (max)**
- Analog Supply Current, I_{CCA} = **116mA (max)**
- Output Supply Current:
  Q0 Current = 250 * 0.00476 + 28.1 = 29.29mA

  Q1 Current = 24.2mA

  Q2 Current = 24.2mA

  Q3 Current = 24.2mA
- Total Output Supply Current = **29.29mA** (V_{CCO} = 2.5V), **72.6mA** (V_{CCO} = 1.8V)
- Total Device Current:
  2.5V: 52mA + 116mA + 29.29mA = **197.29mA**
  1.8V: 72.6mA
- Total Device Power = 2.625V * 197.29mA + 1.89V * 72.6mA = **655.1mW**
- Power dissipated through output loading:
  LVPECL = 27.95mW * 1 = **27.95mW**

  LVDS = already accounted for in device power

  HCSL = n/a

  LVCMOS = 6.87mW
  11pF * 100MHz * $(1.89V)^2$ * 1 output pair = **3.93mW**
  11pF * 50MHz * $(1.89V)^2$ * 1 output pair = **1.96mW**
  11pF * 25MHz * $(1.89V)^2$ * 1 output pair = **0.98mW**
- Total Power = 655.1mW + 27.95mW + 6.87mW = **689.92mW or 0.69W**

With an ambient temperature of 85°C and no airflow, the junction temperature is:

T_J = 85°C + 26.3°C/W * 0.69W = **103.1°C**

This is below the limit of 125°C.

Reliability Information

Table 16. θ_{JA} vs. Air Flow Table for a 40 Lead VFQFPN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.3°C/W	23.2°C/W	21.7°C/W

NOTE: Assumes 5x5 grid of thermal vias under ePAD area for thermal conduction.

Transistor Count

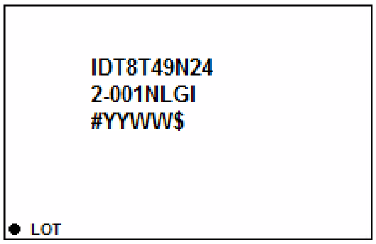
The transistor count for 8T49N242 is: 438,370

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/40-vfqfpn-package-outline-drawing-60-x-60-x-09-mm-05mm-pitch-465-x-465-mm-epad-nlnlg40p2

Marking Diagram



1. Line 1 and Line 2 indicate the part number. "001" will vary due to configuration.
2. "Line 3 indicates the following:
   - #" denotes sequential lot number.
   - "YYWW" is the last two digits of the year and week that the part was assembled.
   - "$" denotes the mark code.

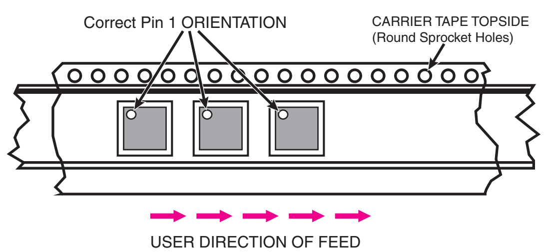
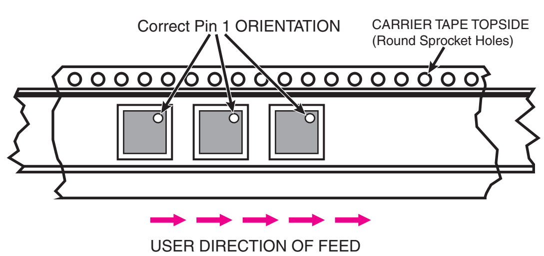
Ordering Information

Table 17. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N242-dddNLGI	IDT8T49N242-dddNLGI	40 Lead VFQFN, Lead-Free	Tray	-40°C to +85°C
8T49N242-dddNLGI8	IDT8T49N242-dddNLGI	40 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to +85°C
8T49N242-dddNLGI#	IDT8T49N242-dddNLGI	40 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to +85°C

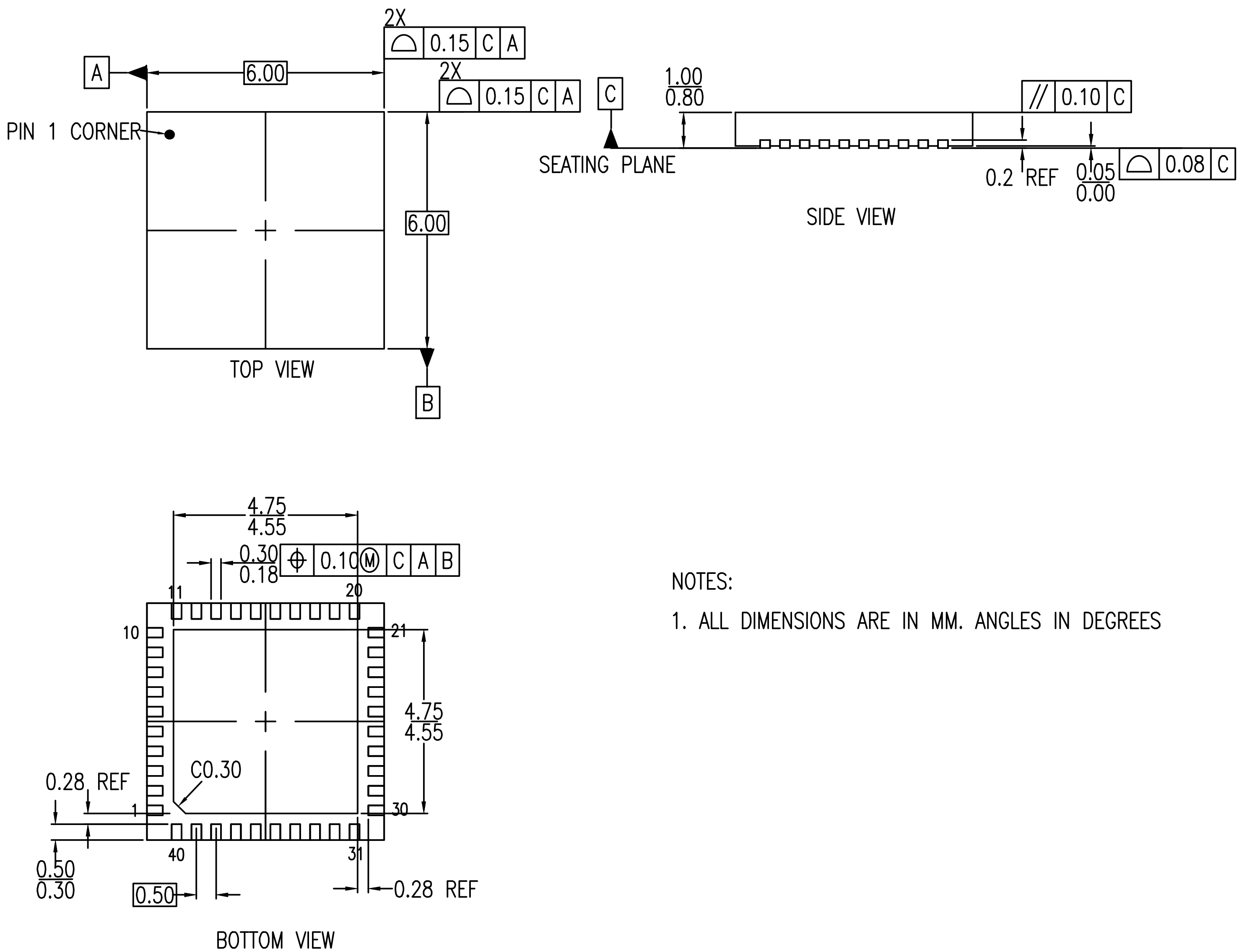
NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

Table 18. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
NLGI8	Quadrant 1 (EIA-481-C)	
NLGI#	Quadrant 2 (EIA-481-D)	

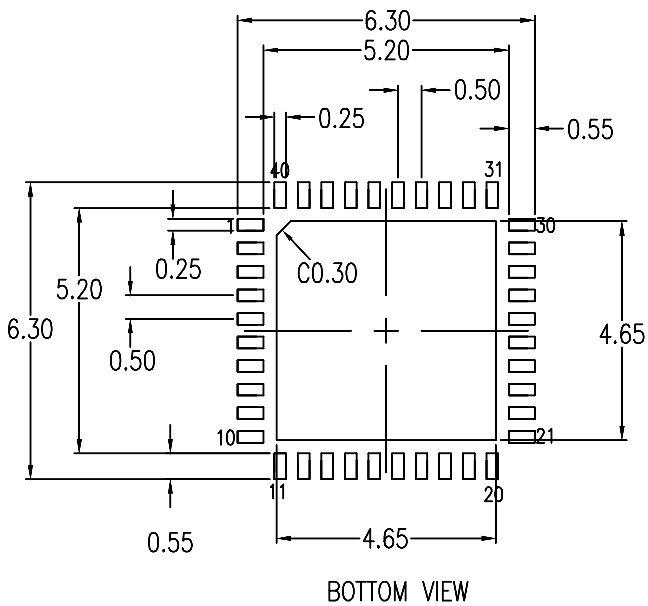
Revision History

Date	Description of Change
January 16, 2019	• Corrected the I^2C read sequence diagrams in Figure 5 and Figure 6 to match I^2C specification and device actual performance. Note: Only the drawings were incorrect – the part's behavior did not change and continues to meet the I^2C specification. • Added a Marking Diagram
July 30, 2018	Per PCN# N1807-01, effective date August 19, 2018 Updated the package outline drawings; however, no technical changes
January 31, 2018	Updated I2C Mode Operation to indicate support for v2.1 of the I2C specification Changed all package references to QFN or VFQFN to VFQFPN Updated the package outline drawings; however, no technical changes
October 10, 2017	Fixed some minor typographical errors. No technical changes.
August 3, 2017	Added C_{XTAL} symbol. Updated the package outline drawings – no technical differences.
October 31, 2016	Crystal Recommendation - deleted IDT crystal reference.
September 9, 2016	Register Blocks Table, changed 0202 - 020B row. Corrected register location in paragraph from 0x0219 to 0x020C. Analog PLL Control Register Descriptions Table, changed VCOMAN[2:0] row.
February 26, 2016	Features section - added additional information on use of external oscillator. Pin Description Table - updated pins 33, 34, 37, 38. Principles of Operation - Output Phase Control on Switchover - added sentence to second and third paragraphs. GPIO Configuration Table - added Note 1. Power Supply Table - Updated table notes. Power Supply Table - Updated table notes. Maximum Output Supply Current Table - updated table notes.
August 7, 2015	Miscellaneous content enhancement in: Table 6, row 0213 - 03FF (from 0213 - 3FF), Table 7Q, row 0212 (from 212); Table 13B, Test Conditions, corrected 25MHz to 40MHz; Table 16, updated note.
July 21, 2015	Device Start-up and Reset Behavior - added sentence to second paragraph.



NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC
   REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Jan 22, 2018	Rev 02	Change QFN to VFQFPN
June 1, 2016	Rev 01	Add Chamfer on Epad

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