Programmable FemtoClock® NG LVPECL/LVDS Dual 4-Output Fractional Clock Generator

IDT8T49N524I

DATA SHEET

General Description

The IDT8T49N524I is an eight output programmable any-rate dual clock generator with selectable LVDS or LVPECL outputs. Both clock generators use Fractional Output Dividers to be able to generate output frequencies that are independent of each other and independent of the input frequency. Output frequencies for both clock generators are generated from a single crystal or reference clock.

Clock Generator A supports three different factory-programmed default frequencies that can be selected from using only the FSEL control pins. Alternatively any desired output frequency can be programmed over the I^2C serial port. The chosen output frequency is then driven out the QA0 to QA3 outputs.

Clock Generator B supports a single factory-programmed default frequency. It can also be programmed for any output frequency via the serial port. The output frequency is driven out the QB0 to QB3 outputs.

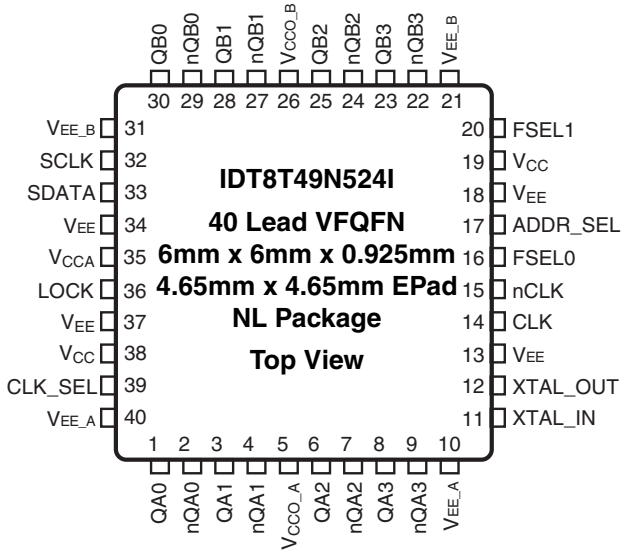
Some examples of frequency configurations that can be achieved are shown in Table 5A. Please consult IDT for programming software that can be used to determine the required settings for any desired configuration.

Excellent phase noise performance is achieved with IDT's fourth Generation FemtoClock® NG PLL technology, which delivers sub-0.5ps RMS phase jitter in the integer divide mode.

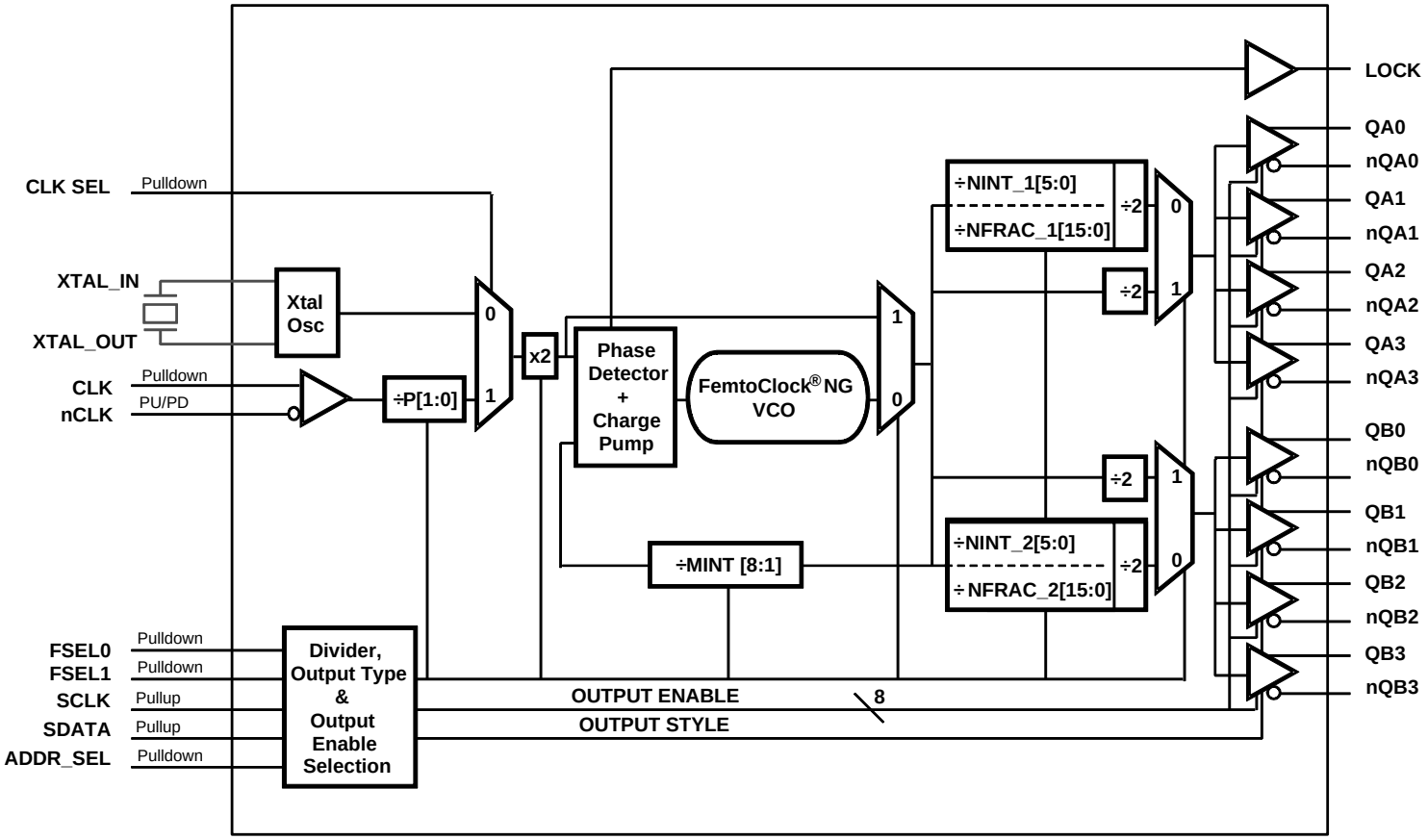
Features

- Fourth Generation FemtoClock® NG PLL technology
- Eight outputs selectable as LVPECL or LVDS
- Input selectable: fundamental mode crystal or clock reference
- Supports fundamental mode crystals from 10MHz - 40MHz
- CLK, nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- Input frequencies from 5MHz up to 800MHz
- Two independent output frequencies can be generated
- Output frequencies independent of each other and of input
- Output frequencies from 15.234MHz - 645MHz, and 975MHz - 1290MHz, (See Table 5D for details)
- RMS phase jitter at 125MHz (12kHz - 20MHz): 0.282ps (typical)
- RMS phase jitter at 156.25MHz (12kHz - 20MHz): 0.278ps (typical)
- Full 2.5V or 3.3V power supply
- I^2C programming interface
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging
- V_{CC} / V_{CCA} / V_{CCO}
  3.3V / 3.3V / 3.3V
  3.3V / 3.3V / 2.5V (LVPECL only)
  2.5V / 2.5V / 2.5V

Pin Assignment



Block Diagram



Pin Description & Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Clock generator A differential output pair. LVPECL or LVDS interface levels.
3, 4	QA1, nQA1	Output		Clock generator A differential output pair. LVPECL or LVDS interface levels.
5	V_{CCO_A}	Power		Clock generator A output supply pin.
6, 7	QA2, nQA2	Output		Clock generator A differential output pair. LVPECL or LVDS interface levels.
8, 9	QA3, nQA3	Output		Clock generator A differential output pair. LVPECL or LVDS interface levels.
10, 13, 18, 21, 31, 34, 37, 40	V_{EE}	Power		Negative supply pins.
11, 12	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
14	CLK	Input	Pulldown	Non-inverting differential clock input.
15	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
16, 20	FSEL0, FSEL1	Input	Pulldown	Frequency select pins. See Table 4A for frequency selection. LVCMOS/LVTTL interface levels.
17	ADDR_SEL	Input	Pulldown	I^2C Address select pin. LVCMOS/LVTTL interface levels.
19, 38	V_{CC}	Power		Core supply pins.
22, 23	nQB3, QB3	Output		Clock generator B differential output pair. LVPECL or LVDS interface levels.
24, 25	nQB2, QB2	Output		Clock generator B differential output pair. LVPECL or LVDS interface levels.
26	V_{CCO_B}	Power		Clock generator B output supply pin.
27, 28	nQB1, QB1	Output		Clock generator B differential output pair. LVPECL or LVDS interface levels.
29, 30	nQB0, QB0	Output		Clock generator B differential output pair. LVPECL or LVDS interface levels.
32	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.
33	SDATA	Input/Output	Pullup	I^2C Data Input. Input: LVCMOS/LVTTL interface levels. Output: Open Drain.
35	V_{CCA}	Power		Analog supply pin.
36	LOCK	Output		PLL Lock Indicator.
39	CLK_SEL	Input	Pulldown	Input source control pin. LVCMOS/LVTTL interface levels. 0 = Crystal is input source (default) 1 = CLK, nCLK input reference clock is input source

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Register Map

Table 3. I²C Register Map

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	MINT0[7]	MINT0[6]	MINT0[5]	MINT0[4]	MINT0[3]	MINT0[2]	MINT0[1]	MINT0[0]
1	00001	MINT1[7]	MINT1[6]	MINT1[5]	MINT1[4]	MINT1[3]	MINT1[2]	MINT1[1]	MINT1[0]
2	00010	MINT2[7]	MINT2[6]	MINT2[5]	MINT2[4]	MINT2[3]	MINT2[2]	MINT2[1]	MINT2[0]
3	00011	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
4	00100	unused	unused	NINTB[5]	NINTB[4]	NINTB[3]	NINTB[2]	NINTB[1]	NINTB[0]
5	00101	unused	unused	unused	unused	unused	unused	DIVB_BYPASS	DIVB_INT
6	00110	NFRACB[7]	NFRACB[6]	NFRACB[5]	NFRACB[4]	NFRACB[3]	NFRACB[2]	NFRACB[1]	NFRACB[0]
7	00111	NFRACB[15]	NFRACB[14]	NFRACB[13]	NFRACB[12]	NFRACB[11]	NFRACB[10]	NFRACB[9]	NFRACB[8]
8	01000	NINTA_0[5]	NINTA_0[4]	NINTA_0[3]	NINTA_0[2]	NINTA_0[1]	NINTA_0[0]	CP0[1]	CP0[0]
9	01001	NINTA_1[5]	NINTA_1[4]	NINTA_1[3]	NINTA_1[2]	NINTA_1[1]	NINTA_1[0]	CP1[1]	CP1[0]
10	01010	NINTA_2[5]	NINTA_2[4]	NINTA_2[3]	NINTA_2[2]	NINTA_2[1]	NINTA_2[0]	CP2[1]	CP2[0]
11	01011	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
12	01100	OE_QB3	OE_QB2	OE_QB1	OE_QB0	OE_QA3	OE_QA2	OE_QA1	OE_QA0
13	01101	unused	unused	unused	unused	LVDS_SEL	PLL_BYPASS	P[1]	P[0]
14	01110	1	1	DOUBLER_ ENABLE	unused	unused	unused	DIVA_BYPASS	DIVA_INT
15	01111	unused	unused	1	1	1	1	1	1
16	10000	NFRACA_0[15]	NFRACA_0[14]	NFRACA_0[13]	NFRACA_0[12]	NFRACA_0[11]	NFRACA_0[10]	NFRACA_0[9]	NFRACA_0[8]
17	10001	NFRACA_1[15]	NFRACA_1[14]	NFRACA_1[13]	NFRACA_1[12]	NFRACA_1[11]	NFRACA_1[10]	NFRACA_1[9]	NFRACA_1[8]
18	10010	NFRACA_2[15]	NFRACA_2[14]	NFRACA_2[13]	NFRACA_2[12]	NFRACA_2[11]	NFRACA_2[10]	NFRACA_2[9]	NFRACA_2[8]
19	10011	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
20	10100	NFRACA_0[7]	NFRACA_0[6]	NFRACA_0[5]	NFRACA_0[4]	NFRACA_0[3]	NFRACA_0[2]	NFRACA_0[1]	NFRACA_0[0]
21	10101	NFRACA_1[7]	NFRACA_1[6]	NFRACA_1[5]	NFRACA_1[4]	NFRACA_1[3]	NFRACA_1[2]	NFRACA_1[1]	NFRACA_1[0]
22	10110	NFRACA_2[7]	NFRACA_2[6]	NFRACA_2[5]	NFRACA_2[4]	NFRACA_2[3]	NFRACA_2[2]	NFRACA_2[1]	NFRACA_2[0]
23	10111	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Function Tables

Table 4A. Frequency Select Table

FSEL1	FSEL0	Pre-scaler Ratio	Feedback Divider Ratio	QAn Operation		QBn Operation	
0 (default)	0 (default)	P	MINT0	NINTA_0	NFRACA_0	NINTB	NFRACB
0	1	P	MINT1	NINTA_1	NFRACA_1	NINTB	NFRACB
1	0	P	MINT2	NINTA_2	NFRACA_2	NINTB	NFRACB
1	1	Reserved					

Table 4B. I^2C Register Function Descriptions

Bits	Name	Function
MINTn[7:0]	Integer Feedback Divider Register n (n = 0...2)	Sets the integer feedback divider value. See Table 5B for the feedback divider coding.
P[1:0]	Input Divider Register	Sets the PLL input divider. The divider value has the range of 1, 2, 4 and 8. See Table 5C for the divider coding.
NINTA_n[5:0]	Output Divider A - Integer Portion n (n = 0...2)	Sets the integer portion of the output divider A. See Table 5D for the output divider coding.
NFRACA_n[15:0]	Output Divider A - Fractional Portion (n = 0...2)	Sets the fractional portion of the output divider A. See Table 5D for the output divider coding.
NINTB[5:0]	Output Divider B - Integer Portion	Sets the integer portion of the output divider B. See Table 5D for the output divider coding.
NFRACB[15:0]	Output Divider B - Fractional Portion	Sets the fractional portion of the output divider B. See Table 5D for the output divider coding.
CPn[1:0]	PLL Bandwidth n (n = 0...2)	Sets the FemtoClock® NG PLL Charge Pump current to support the selected operating frequency. See Table 5E.
OE_Qxx	Output Enable	Sets the desired output to Active or High impedance. 0 = Output is high-impedance (default) 1 = Output is active.
LVDS_SEL	Output Style	Selects differential output style 0 = LVPECL (default) 1 = LVDS
PLL_BYPASS	PLL Bypass	Bypasses PLL. Input to phase detector is routed through output dividers A and B to the output fanout buffers. Dividers should be programmed for integer divide operation (DIVA_INT = DIVB_INT = 0) for proper operation.
DOUBLER_ ENABLE	Input Doubler	Enables the input frequency doubler. 0 = Input frequency presented directly to PLL 1 = Input frequency doubled before PLL (default)
DIVA_BYPASS	Bypass Output Divider A	Bypasses output divider A. QAn output frequency is VCO/2.
DIVB_BYPASS	Bypass Output Divider B	Bypasses output divider B. QBn output frequency is VCO/2.
DIVA_INT	Divider A Integer Mode	Disables fractional portion of divider A. Setting this bit will provide better phase noise performance in cases where the fractional portion is 0.
DIVB_INT	Divider B Integer Mode	Disables fractional portion of divider B. Setting this bit will provide better phase noise performance in cases where the fractional portion is 0.

Frequency Configuration

The IDT8T49N524I is capable of being loaded with up to three different frequency configurations. Use of the FSEL[1:0] inputs allows a user to select from any of those three configurations at any time. The three frequency configurations may be pre-loaded at the factory or can be setup at any time over the I^2C serial port. Table 5A shows a number of example configurations.

It is recommended to use the IDT8T49N524I Configuration SW to generate the desired configurations for the device.

Table 5A. Frequency Configuration Examples

Output Frequencies (MHz)	Input or Crystal Frequency (MHz)	Input Divider P	Effective Feedback Divider Ratio M	VCO Frequency (MHz) f_{VCO}	Effective Output Divider Ratio N
62.5	25	1	100	2500	40
78.125	25	1	100	2500	32
100	25	1	96	2400	24
106.25	25	1	102	2550	24
125	25	1	100	2500	20
133.333	25	1	96	2400	18
150	25	1	96	2400	16
156.25	25	1	100	2500	16
166.666	25	1	80	2000	12
187.5	25	1	90	2250	12
200	25	1	96	2400	12
212.5	25	1	102	2550	12
250	25	1	100	2500	10
300	25	1	96	2400	8
312.5	25	1	100	2500	8
375	25	1	90	2250	6
400	25	1	96	2400	6
625	25	1	100	2500	4
1250	25	1	100	2500	2
30.72	25	1	88	2200	71.6145833333
61.44	25	1	88	2200	35.8072916667
76.8	25	1	88	2200	28.6458333333
122.88	25	1	88	2200	17.9153094463
148.5	25	1	88	2200	14.8148148148
153.6	25	1	88	2200	14.3229166667
155.52	25	1	88	2200	14.1460905350
159.375	25	1	88	2200	13.8039215686
160	25	1	88	2200	13.75
161.1328125	25	1	88	2200	13.6533333333
164.355	25	1	88	2200	13.3856590916
166.6285	25	1	88	2200	13.2030234924
184.32	25	1	88	2200	11.9357638889
311.04	25	1	88	2200	7.0730452675

Table 5B. Feedback Divider MINTn Coding

Register Bit	
MINTn[7:0]	Feedback Divide Ratio M
000000xx	Do Not Use
0000100	8
0000101	10
0000110	12
0000111	14
00001000 thru 11111111	16 thru 510

Table 5C. Input Pre-scaler (P) Coding

Register Bit		
P1	P0	Input Pre-scaler Divide Ratio P
0	0	1
0	1	2
1	0	4
1	1	8

Table 5D. Output Divider NINTx and NFRACx Coding

Frequency Divider N	Output Frequency		Register Bit
	f_{MIN} (MHz)	f_{MAX} (MHz)	NINTx[5:0]
Do Not Use			00000x
2	975	1290	xxxxxx (NOTE 2)
4	487.5	645	000010
6	325	430	000011
8 – 9.99999999 (NOTE 1)	195	322.5	000100
N – N +1.99999999	1950/ (N + 1.99999999)	2580 / N	...
126 - 127.99999999	15.234	20.476	111111

NOTE: When operating in Integer-mode, set NFRACx = 0, DIVA_INT = 1, and NINTx to desired output frequency configurations.
NOTE 1: When operating in fractional-mode, output frequency is limited to 322.5MHz. NFRACx must be set to 0 if NINTx = 000010 or 000011.
NOTE 2: The output divider is bypassed to generate frequencies in this range on the output. Set DIVx_INT and DIVx_BYPASS bits for the desired output divider (A or B) for a ÷2 operation on that output bank.

Table 5E. Charge Pump CPn[1:0] Settings

Register Bit		Feedback Divider (M) Value Range	
CPn[1]	CPn[0]	Minimum	Maximum
0	0	16	48
0	1	49	100
1	0	101	192
1	1	193	510

NOTE: FemtoClock® NG PLL stability is only guaranteed over the feedback divider ranges listed in Table 5B.

The IDT8T49N524I supports a variety of options such as different output styles, number of programmed default frequencies, output enable and operating temperature range. The device options and default frequencies must be specified at the time of order and are programmed by IDT prior to shipment. The document, *Programmable FemtoClock® NG Product Ordering Guide* specifies the available order codes.

Other order codes with respective programmed frequencies are available from IDT upon request. After power-up changes to the output frequencies, and state of outputs, active or high impedance, are controlled by FSEL[1:0] or the I^2C interface.

Serial Interface Configuration Description

The IDT8T49N524I has an I^2C-compatible configuration interface to access any of the internal registers (Table 3) for frequency and PLL parameter programming. The IDT8T49N524I acts as a slave device on the I^2C bus and has the address 0b110111x, where x is set by the value on ADDR_SEL input. (See Tables 6A & 6B). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 3) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Table 6C, 6D). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate the I^2C read or write transfer after accessing byte #23 by sending a stop command.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50KΩ typical.

Table 6A. I^2C Device Slave Address ADDR_SEL = 0 (default)

1	1	0	1	1	1	0	R/W

Table 6B. I^2C Device Slave Address ADDR_SEL = 1

1	1	0	1	1	1	1	R/W

Table 6C. Block Write Operation

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte P	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 6D. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address byte P	ACK	Repeated START	Slave address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltages, V_{CC}, V_{CCA}, V_{CCO_A}, V_{CCO_B}	3.6V
Inputs, V_I XTAL_IN Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Outputs, I_O (LVCMOS) Continuous Current (LOCK) Continuous Current (SDATA) Surge Current (all)	 12mA 10mA 22mA
Package Thermal Impedance, θ_{JA}	32.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 7A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			264	300	mA
I_{CCA}	Analog Supply Current			15	18	mA

Table 7B. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 2.5V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.17	2.5	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			256	290	mA
I_{CCA}	Analog Supply Current			14	17	mA

Table 7C. LVPECL Power Supply DC Characteristics,
V_{CC} = 3.3V±5%, V_{CCO_A} = V_{CCO_B} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			264	300	mA
I_{CCA}	Analog Supply Current			15	18	mA

Table 7D. LVDS Power Supply DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			188	212	mA
I_{CCA}	Analog Supply Current			15	18	mA
I_{CCO_A} + I_{CCO_B}	Output Supply Current			148	167	mA

Table 7E. LVDS Power Supply DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.17	2.5	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current			177	200	mA
I_{CCA}	Analog Supply Current			14	17	mA
I_{CCO_A} + I_{CCO_B}	Output Supply Current			147	166	mA

Table 7F. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	SCLK, SDATA	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SCLK, SDATA	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 7G. Differential DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage: NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, NOTE 2			V_{EE} + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less then -0.3V.
NOTE 2: Common mode input voltage is at the crosspoint.

Table 7H. LVPECL DC Characteristics, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_X} – 1.1		V_{CCO_X} – 0.75	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_X} – 2.0		V_{CCO_X} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE: V_{CCO_X} denotes V_{CCO_A} and V_{CCO_B}.
NOTE 1: Outputs terminated with 50Ω to V_{CCO_X} – 2V.

Table 7I. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO\_X} - 1.2$		$V_{CCO\_X} - 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO\_X} - 2.0$		$V_{CCO\_X} - 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.5		1.0	V

NOTE: V_{CCO_X} denotes V_{CCO_A} and V_{CCO_B}
NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_X} - 2V$.

Table 7J. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO\_A} = V_{CCO\_B} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO\_X} - 1.2$		$V_{CCO\_X} - 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO\_X} - 2.0$		$V_{CCO\_X} - 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.5		1.0	V

NOTE: V_{CCO_X} denotes V_{CCO_A} and V_{CCO_B}
NOTE 1: Outputs termination with 50Ω to $V_{CCO\_X} - 2V$.

Table 7K. LVDS DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Output Low Voltage;		1.15		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 7L. LVDS DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Output Low Voltage;		1.15		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 8. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Load Capacitance (CL)		12		18	pF

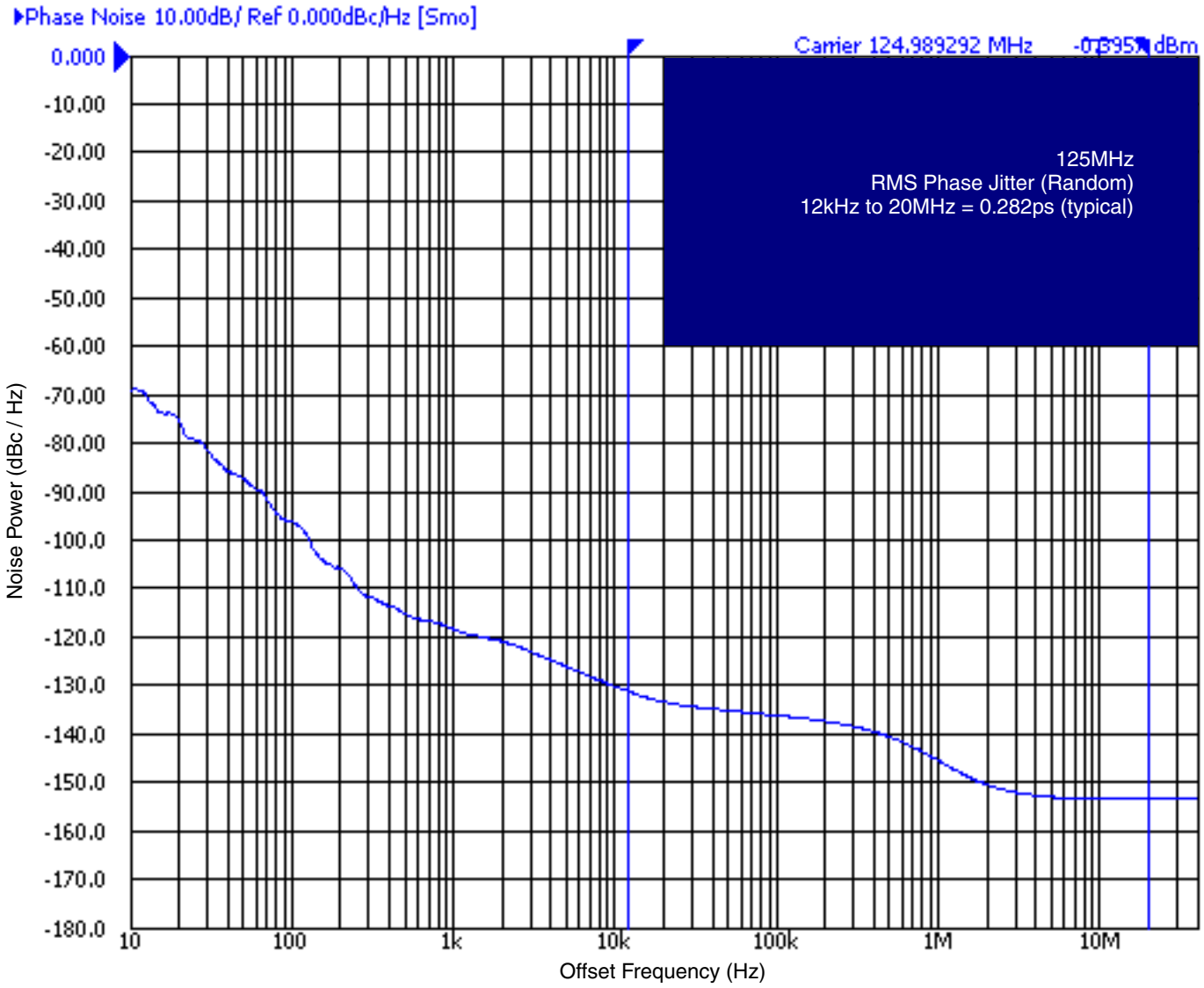
AC Electrical Characteristics

Table 9. AC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ $V_{EE} = 0V$, $T_A = -40°C$ to $85°$

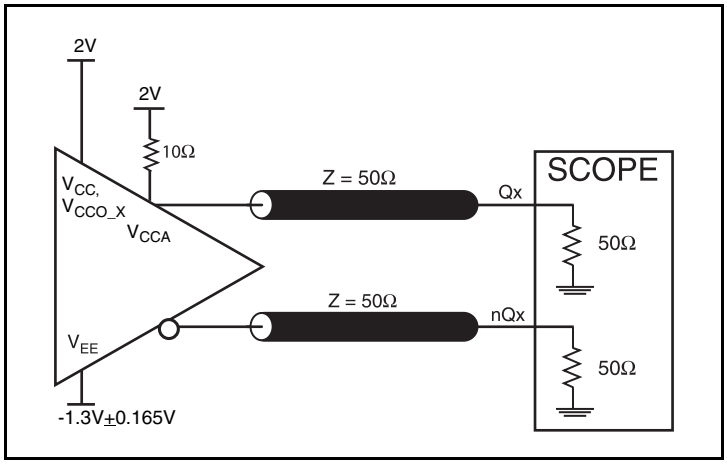
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{DIFF_IN}	Differential Input Frequency			5		800	MHz
f_{PFD}	Phase / Frequency Detector Frequency			5		100	MHz
f_{VCO}	VCO Frequency			1950		2580	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1		100MHz, Integration Range: 12kHz – 20MHz		0.303	0.405	ps
			125MHz, Integration Range: 12kHz – 20MHz		0.282	0.383	ps
			156.25MHz, Integration Range: 12kHz – 20MHz		0.278	0.371	ps
			212.5MHz, Integration Range: 12kHz – 20MHz		0.341	0.734	ps
tsk(b)	Bank Skew; NOTE 2, 3	LVPECL Outputs	LVDS_SEL = 0			40	ps
		LVDS Outputs	LVDS_SEL = 1				
t_{LOCK}	PLL Lock Time; NOTE 4					25	ms
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% - 80%, LVDS_SEL = 0	100		400	ps
		LVDS Outputs	20% - 80%, LVDS_SEL = 1	100		400	ps
odc	Output Duty Cycle	LVPECL	$N \leq 3$	45		55	%
		LVDS					
		LVPECL	$N > 3$	40		60	%
		LVDS					
t_S	Setup Time	SDATA to SCLK		5			ns
t_H	Hold Time	SDATA from SCLK		5			ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All Integer mode characterizations done using 25MHz, 12pf resonant Crystal.
NOTE: Output dividers using even integer divide ratios.
NOTE 1: Please refer to Phase Noise Plots.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Refer to f_{LOCK} in Parameter Measurement Information.

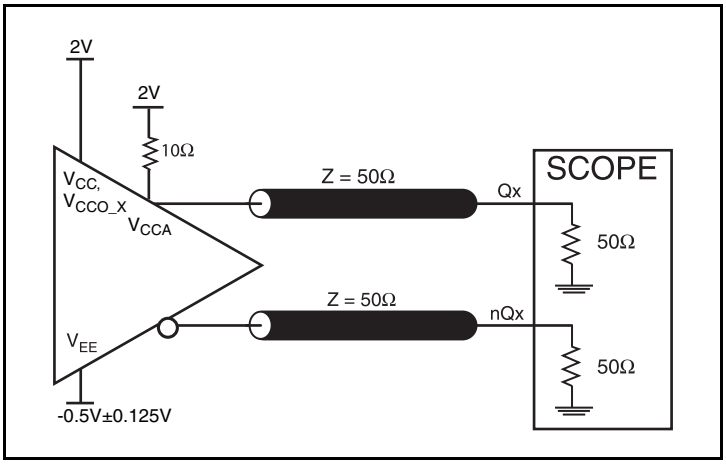
Typical Phase Noise at 125MHz



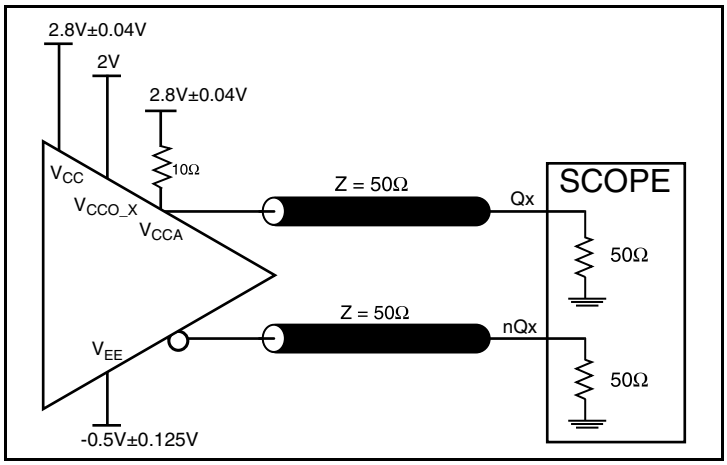
Parameter Measurement Information



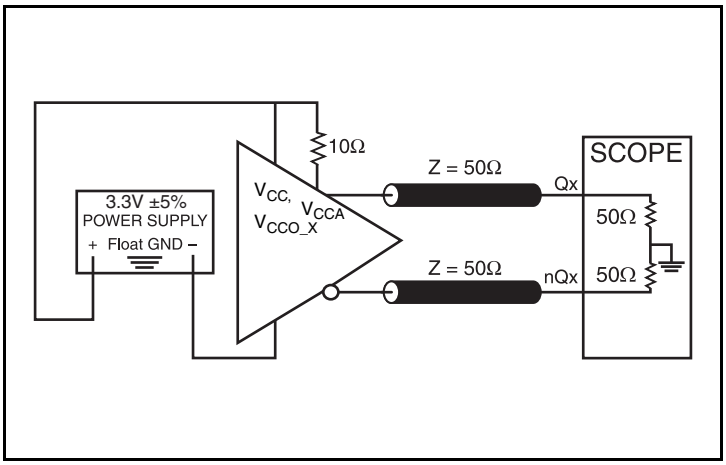
3.3V Core/3.3V LVPECL Output Load Test Circuit



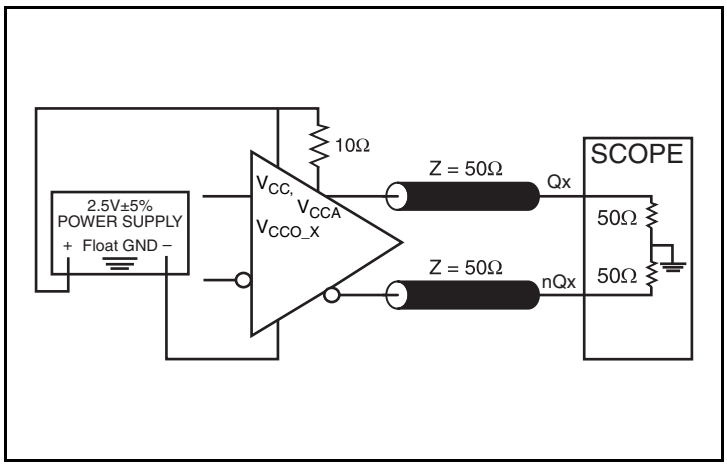
2.5V Core/2.5V LVPECL Output Load Test Circuit



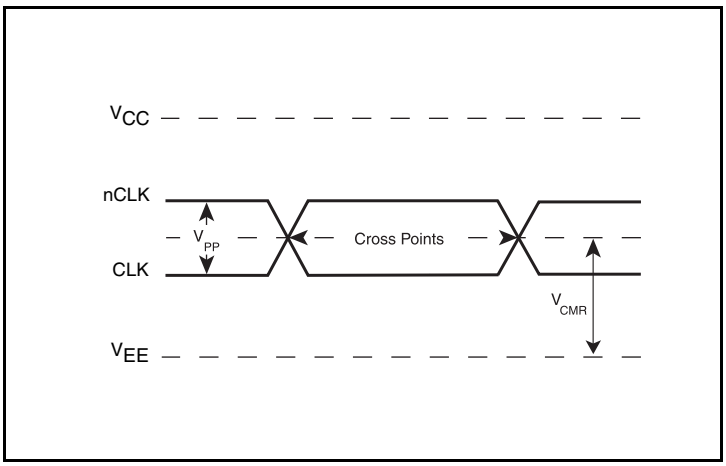
3.3V Core/2.5V LVPECL Output Load Test Circuit



3.3V Core/3.3V LVDS Output Load Test Circuit

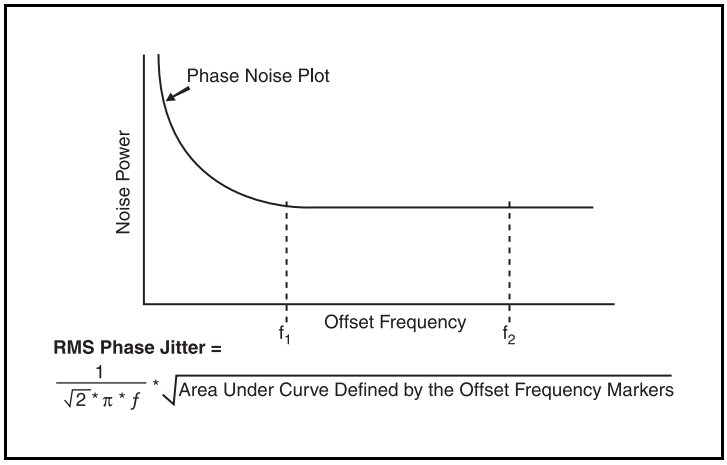


2.5V Core/2.5V LVDS Output Load Test Circuit

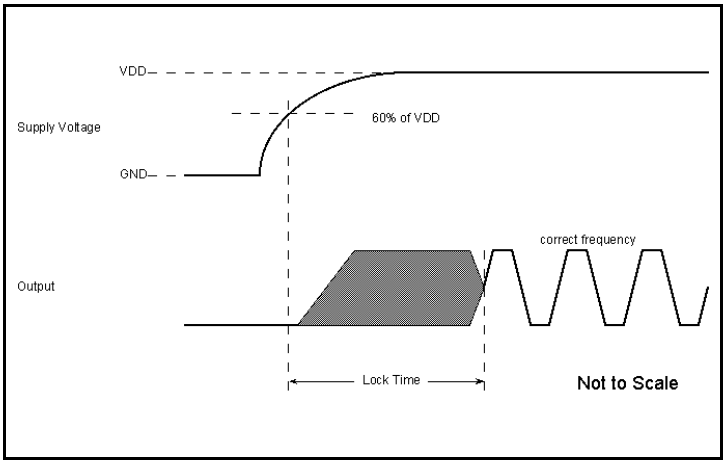


Differential Input Levels

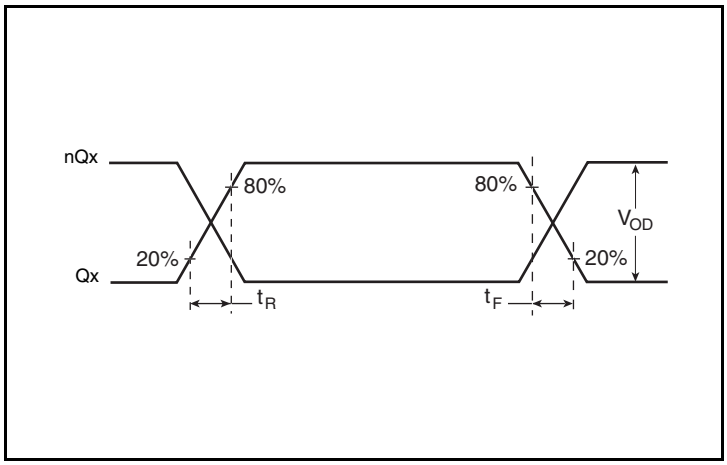
Parameter Measurement Information, continued



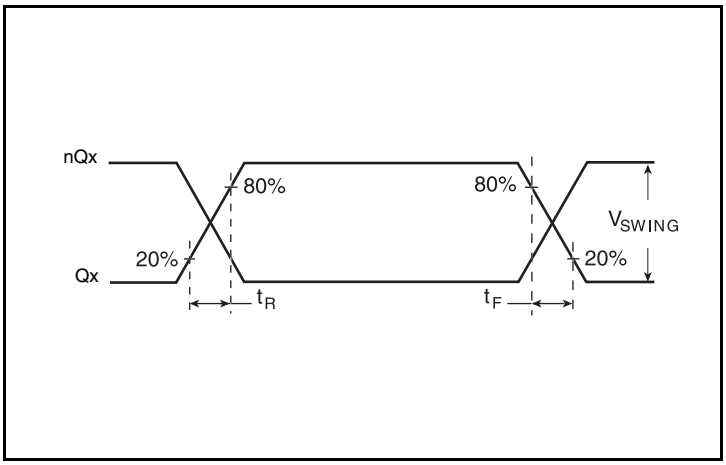
RMS Phase Jitter



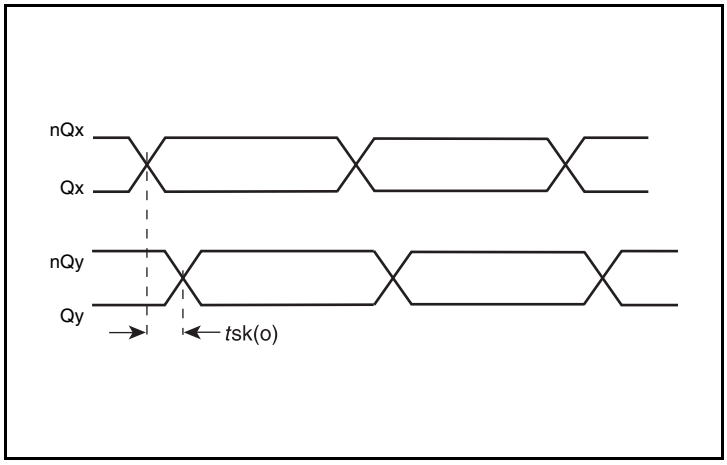
PLL Lock Time



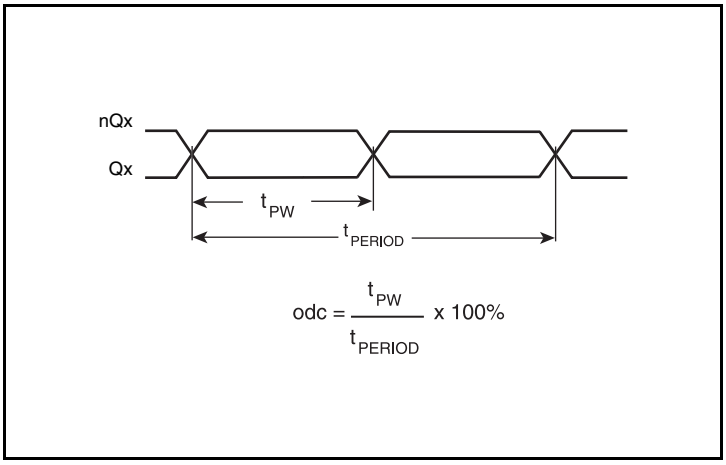
LVDS Output Rise/Fall Time



LVPECL Output Rise/Fall Time

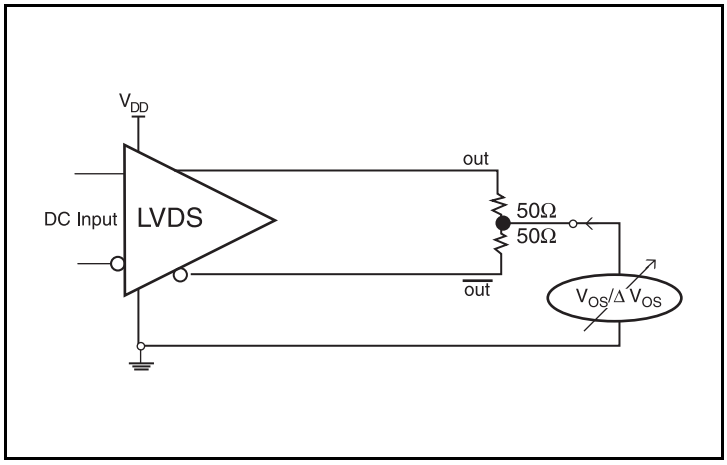


Output Skew

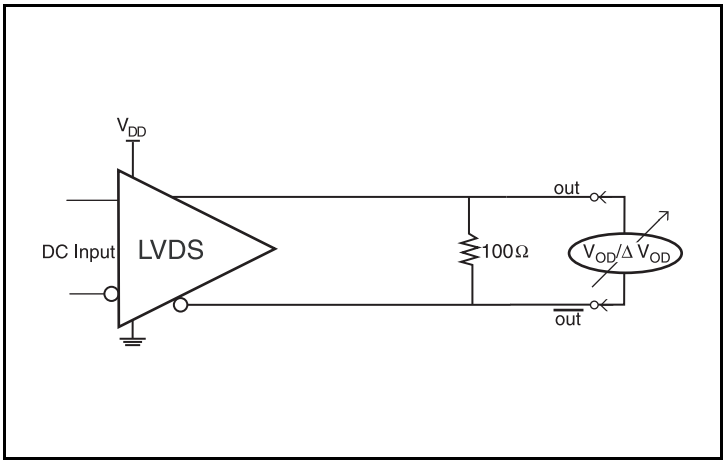


Differential Output Duty Cycle/Output Pulse Width/Period

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground. It is recommended that CLK, nCLK be left unconnected in frequency synthesizer mode.

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

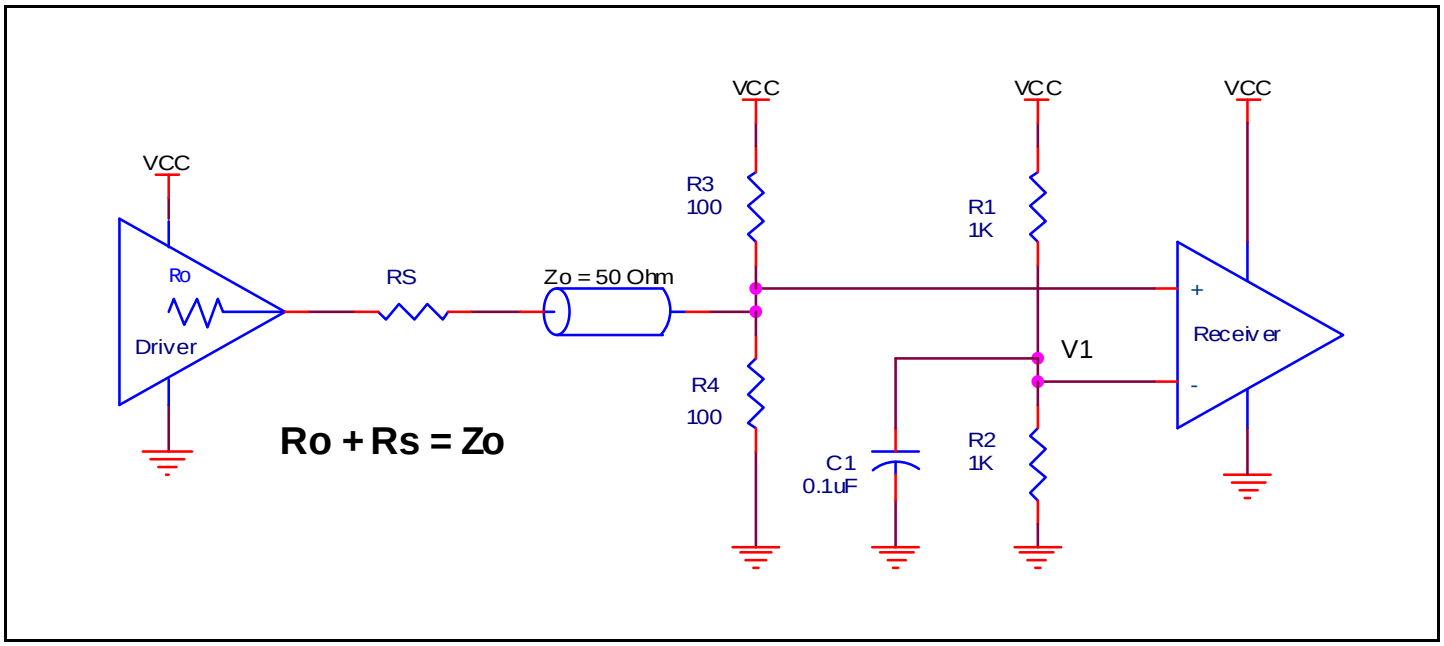


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

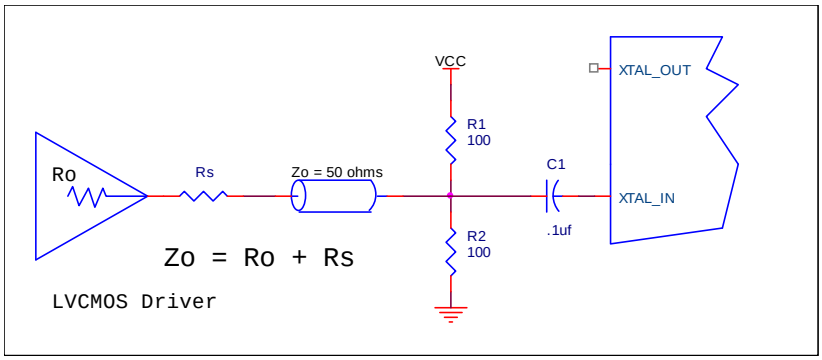


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

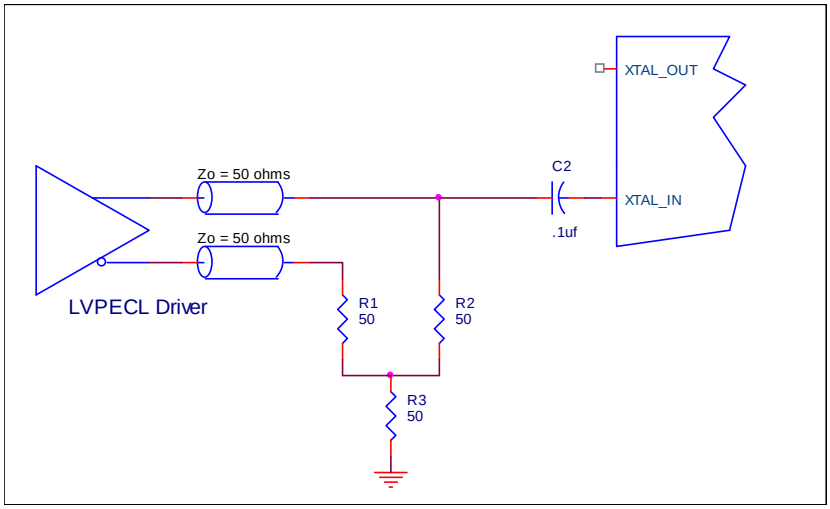


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

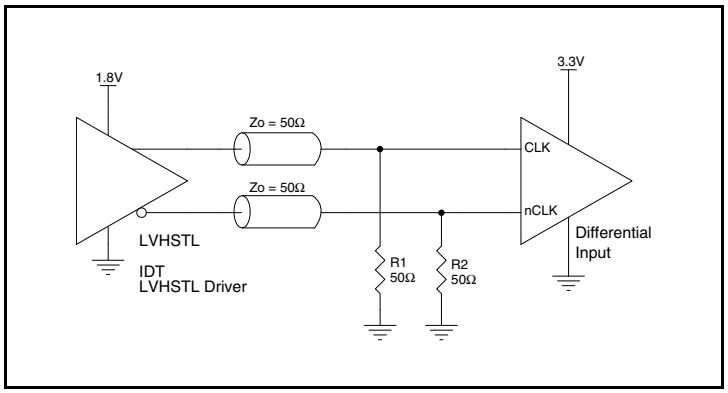


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

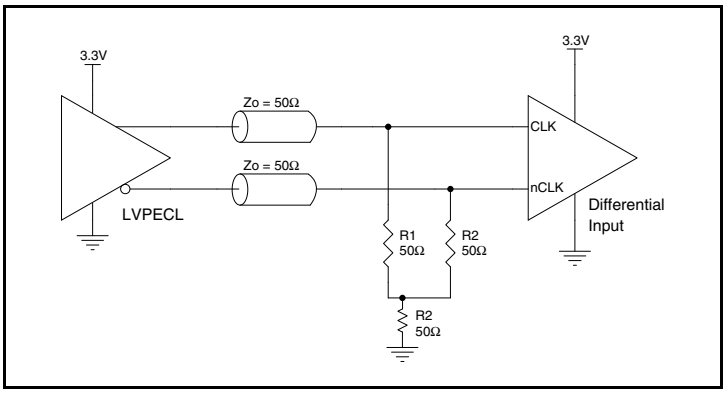


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

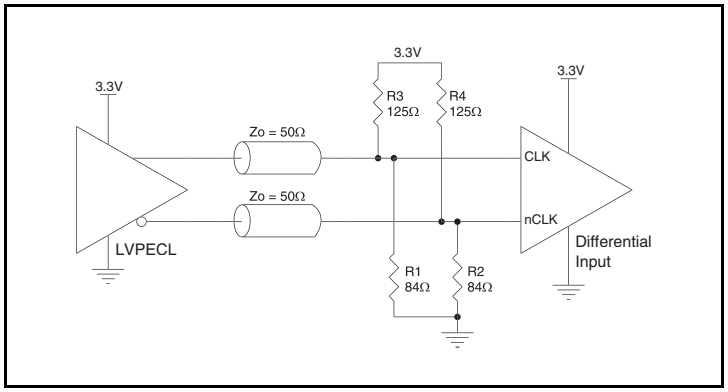


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

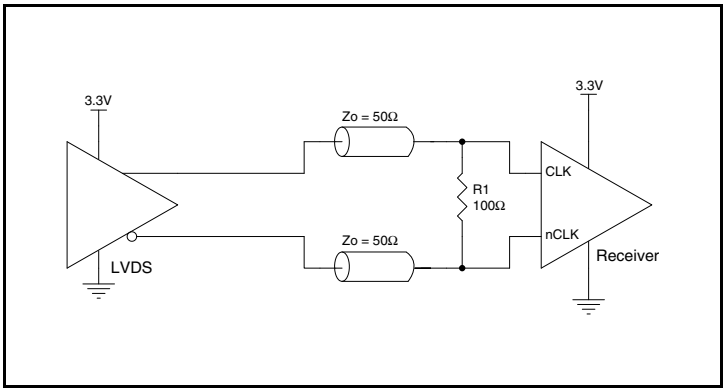


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

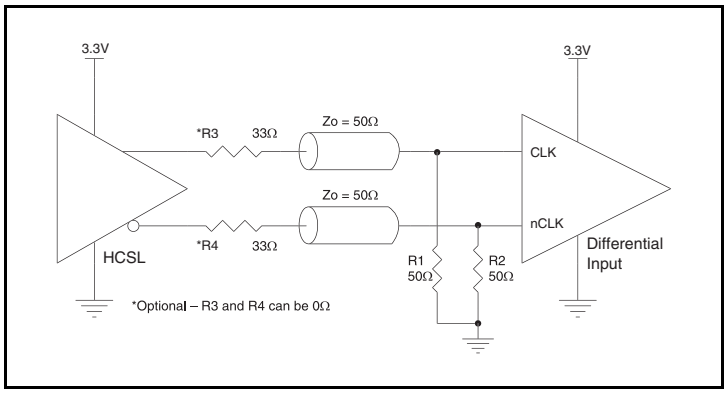


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

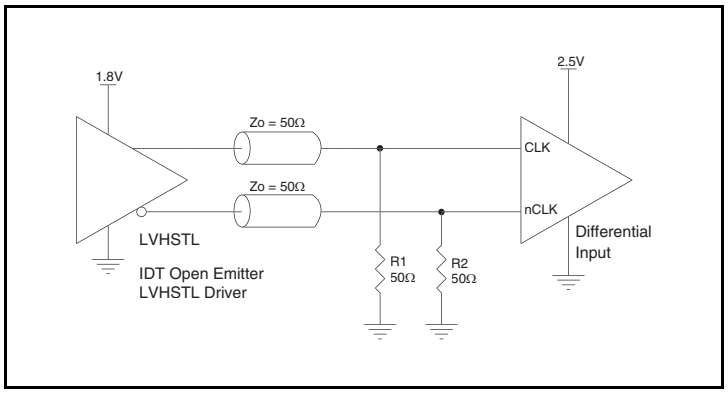


Figure 4A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

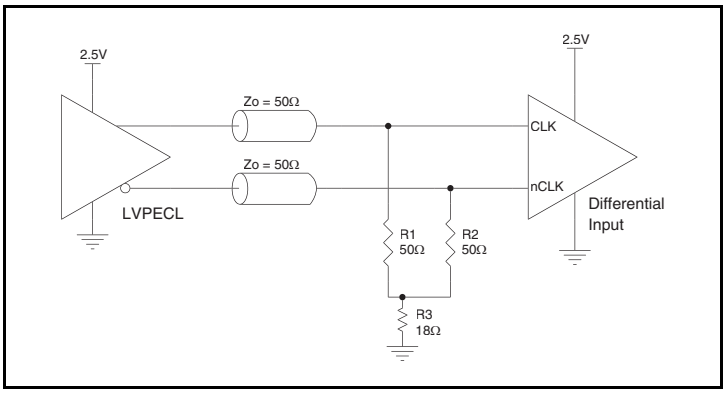


Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

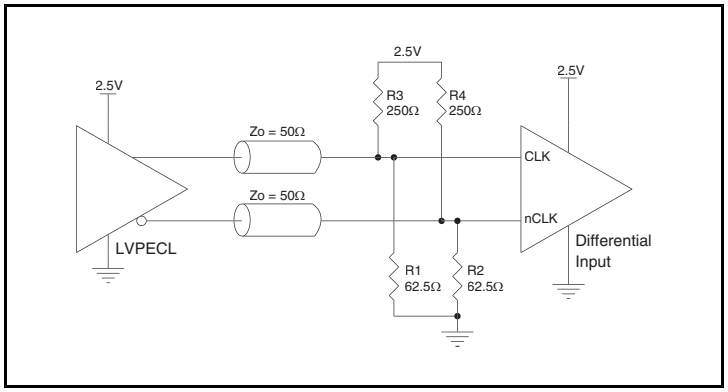


Figure 4C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

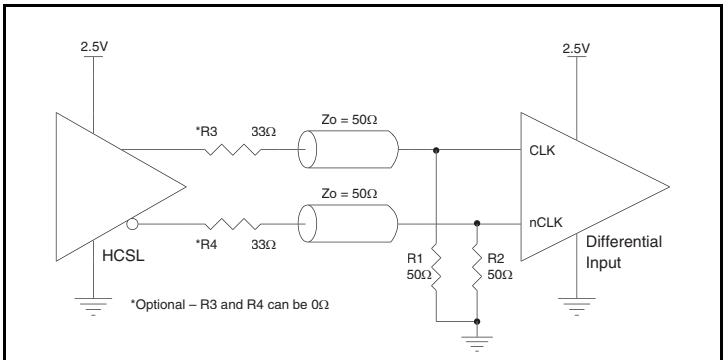


Figure 4D. CLK/nCLK Input Driven by a 2.5V HCSL Driver

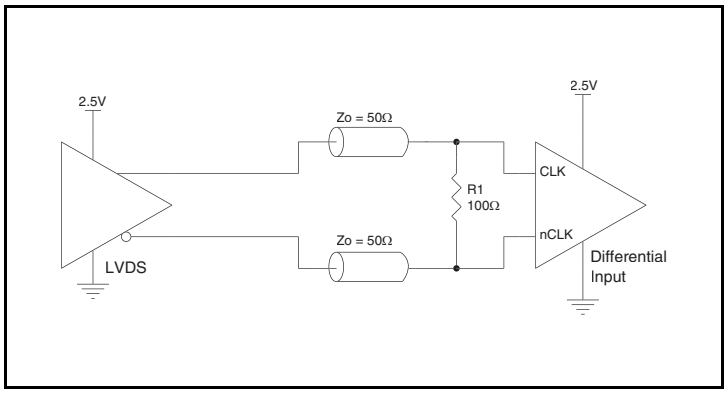


Figure 4E. CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

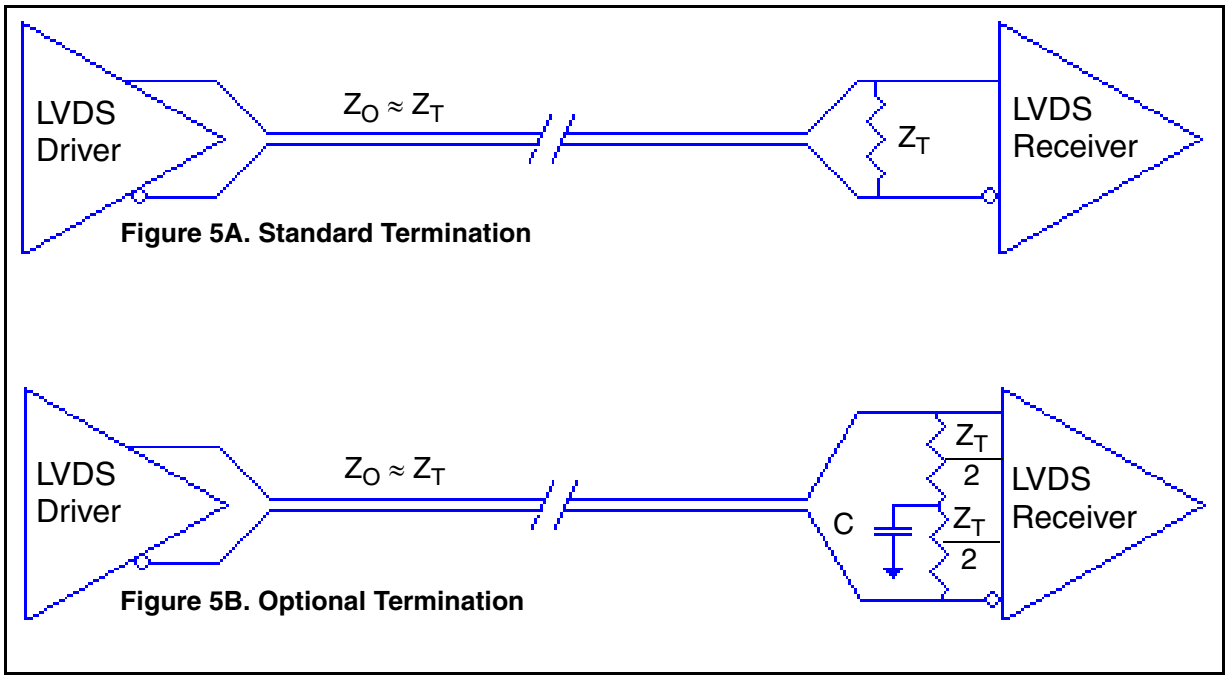


Figure 5A. Standard Termination

Figure 5B. Optional Termination

LVDS Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

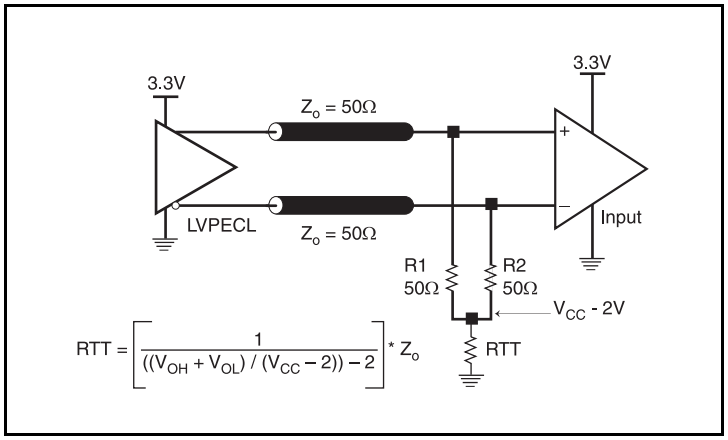


Figure 6A. 3.3V LVPECL Output Termination

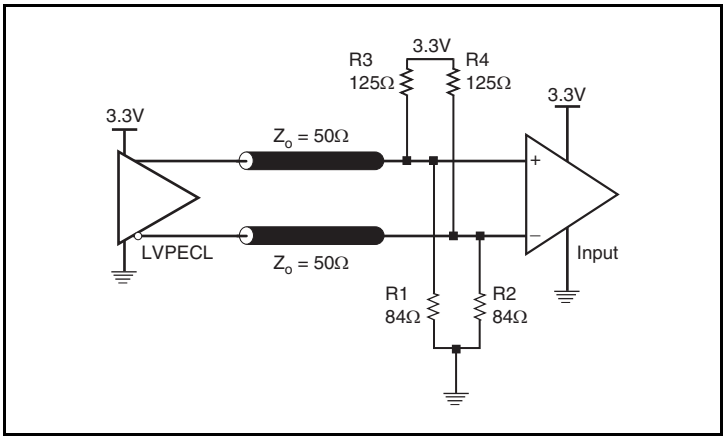


Figure 6B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 7A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

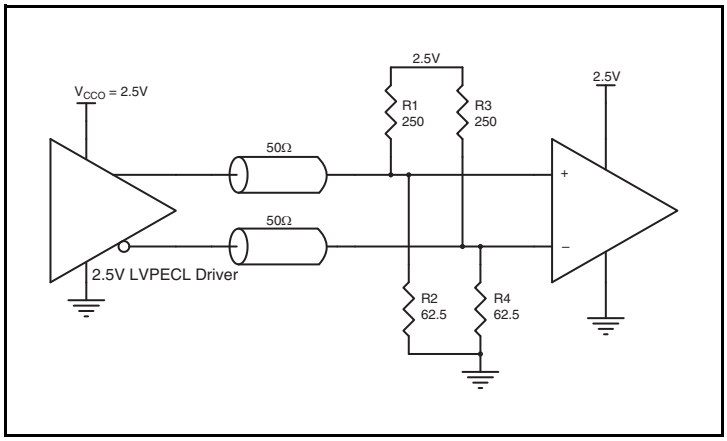


Figure 7A. 2.5V LVPECL Driver Termination Example

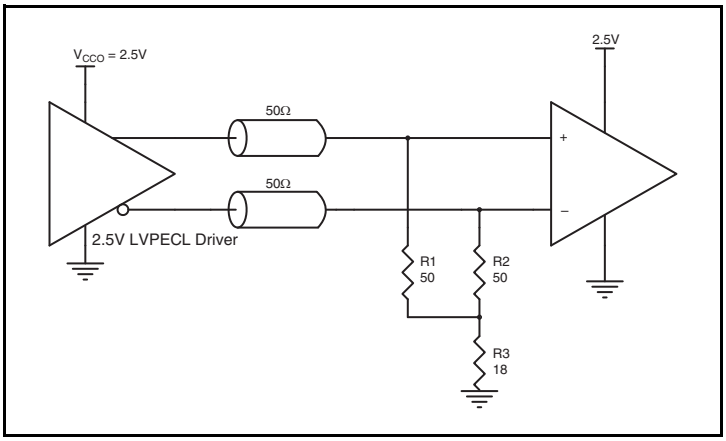


Figure 7B. 2.5V LVPECL Driver Termination Example

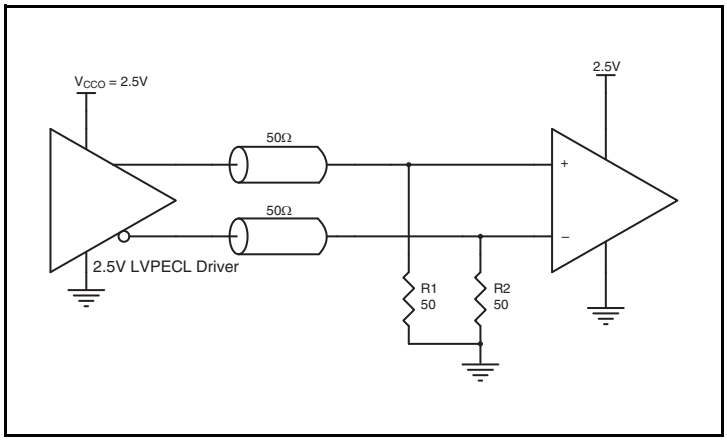


Figure 7C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

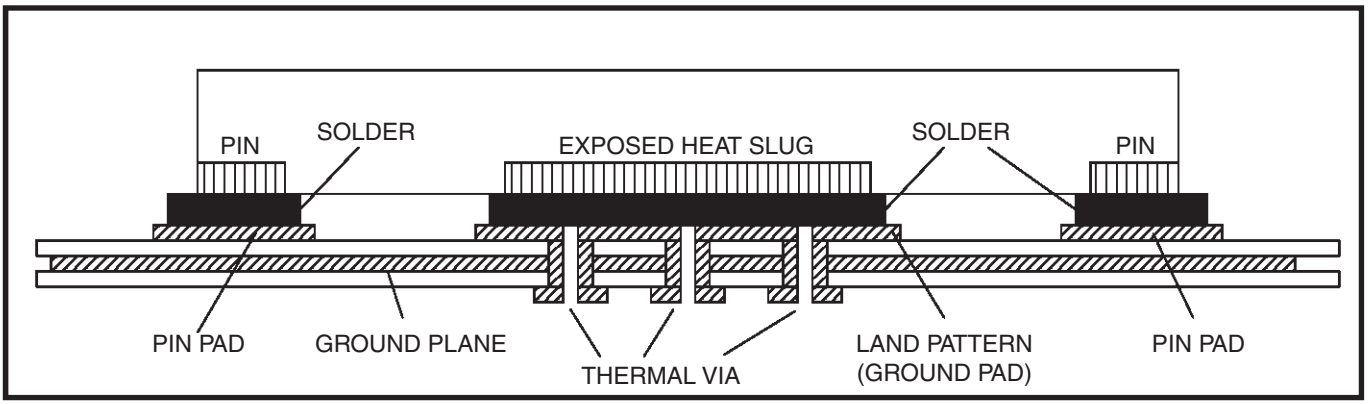


Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 9 (next page) shows an example IDT8T49N524I application schematic that focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. In this example, the input reference is LVDS and the outputs have all been configured for LVPECL.

In this example a 12pF parallel resonant Fox FX325BS 25MHz crystal is used with load caps C1 = C2 = 10pF. The load caps are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N524I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter and the resistor of the V_{DDA} power filters should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

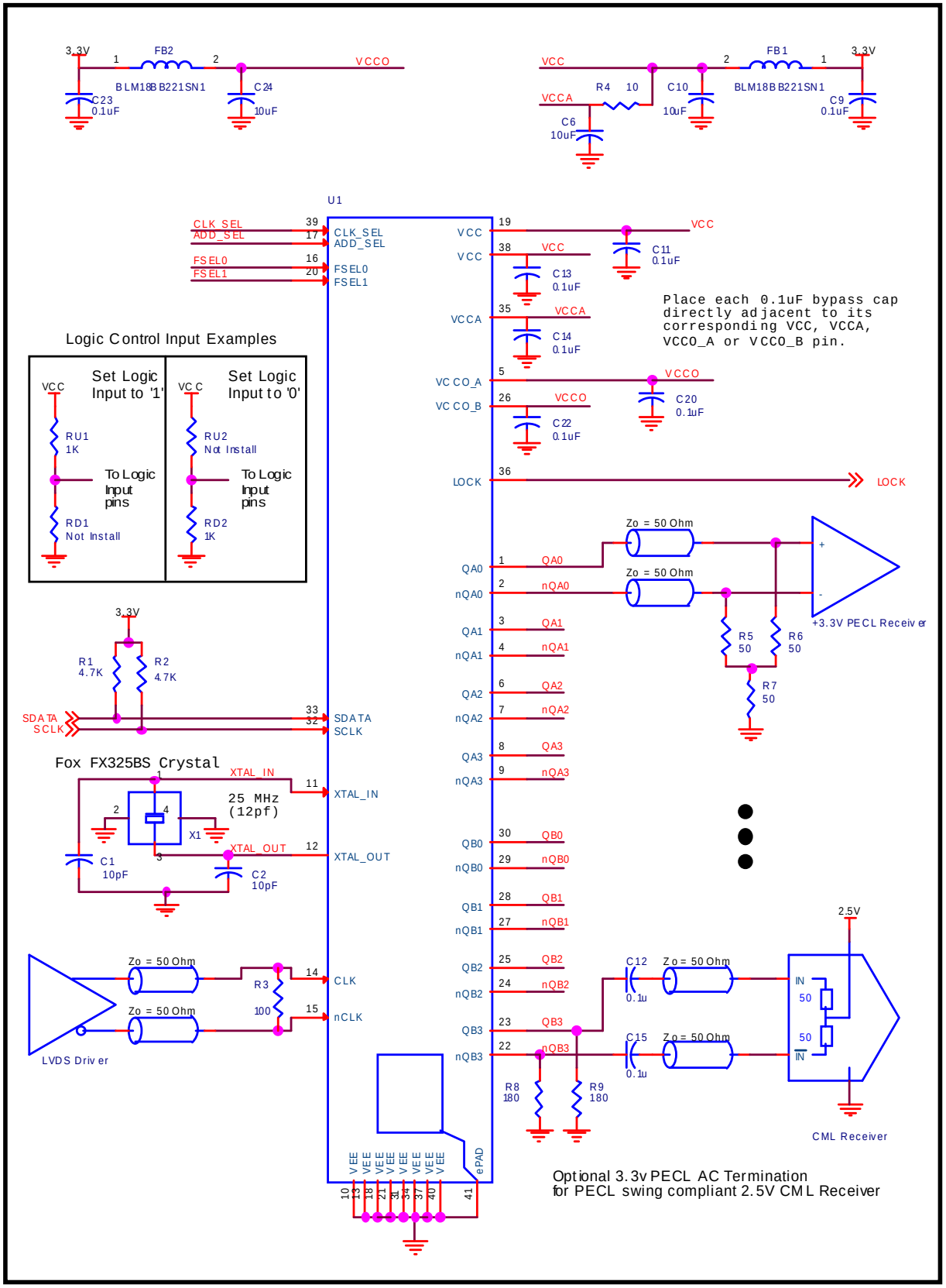


Figure 9. IDT8T49N524I Application Schematic

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N524I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N524I is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 300mA = **1039.5mW**
- Power (outputs)$_{MAX}$ = **31.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 31.6mW = **252.8mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 1039.5mW + 252.8mW = **1292.3mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 27.9°C/W per Table 10 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.292W * 27.9°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 10. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 10.*

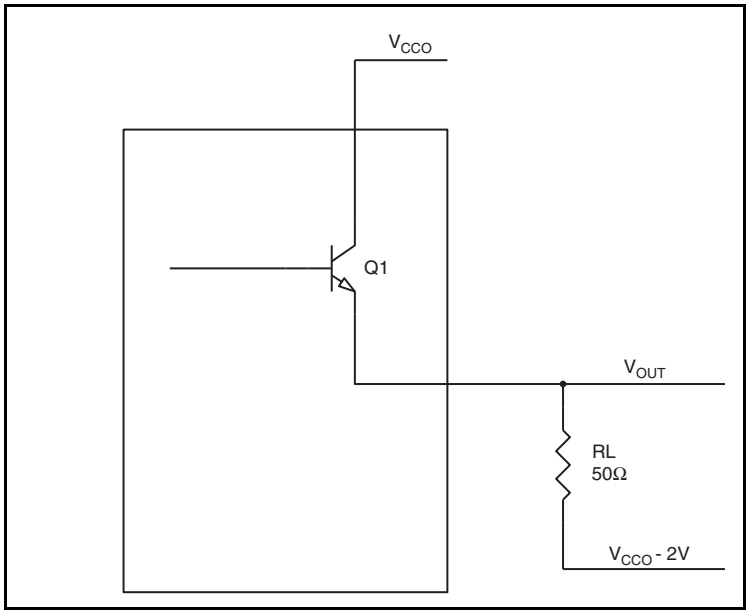


Figure 10. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.75V**
  ($V_{CCO\_MAX} - V_{OH\_MAX}$) = **0.75V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.6V**
  ($V_{CCO\_MAX} - V_{OL\_MAX}$) = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.75V)/50Ω] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.6V)/50Ω] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.6mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N524I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N524I is the sum of the core power plus the analog power plus the power dissipated due to the load. The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{CC_MAX} * (I_{CC_MAX} + I_{CCA_MAX}) = 3.465V * (212mA + 18mA) = **796.95mW**
- Power (outputs)$_{MAX}$ = V_{CCO_MAX} * I_{CCO_MAX} = 3.465V * 167mA = **578.66mW**

Total Power$_{\_MAX}$ = 796.95mW + 578.66mW = **1375.61mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 27.9°C/W per Table 11 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.376W * 27.9°C/W = 123.40°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 11. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

Reliability Information

Table 12. θ_{JA} vs. Air Flow Table for a 40 Lead VFQFN

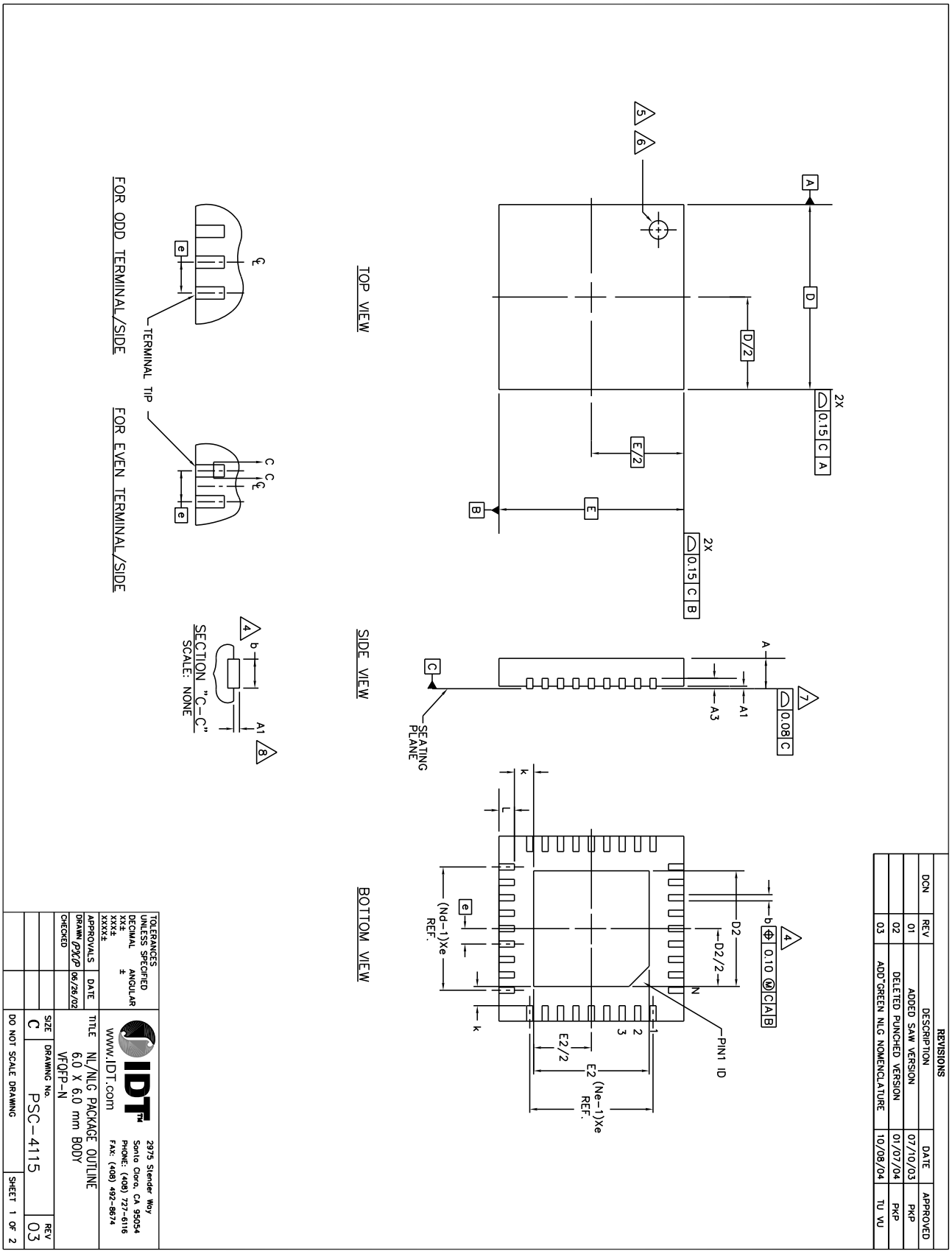
θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB; NOTE 1	27.9°C/W	21.6°C/W	19.1°C/W
Multi-Layer PCB, JEDEC Standard	NOTE 2	25.7°C/W	23.4°C/W

NOTE 1: θ_{JA} simulation is performed with 4-layers, 8in. x 8in. PCB.
NOTE 2: JEDEC Standard requires air flow.

Transistor Count

The transistor count for IDT8T49N524I is: 35,322

40 Lead VFQFN Package Outline and Package Dimensions



40 Lead VFQFN Package Outline and Package Dimensions, continued

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD"GREEN" NLG NOMENCLTURE	10/08/04	TU VU

SYMBOL	JEDEC VARIATION VJJC-3			NOTE	SYMBOL	JEDEC VARIATION VJJD-5			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e		0.65 BSC			e		0.50 BSC		
N		28		2	N		40		3
Nd		7		2	Nd		10		3
Ne		7		2	Ne		10		3
b	0.25	0.30	0.35	4	b	0.18	0.25	0.30	4
D2		–		10	D2		–		10
E2		–		10	E2		–		10

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
k	0.20	–	–	
L	0.35	0.40	0.45	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-220, VARIATION VJJC-3 & VJJD-5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.
    40 Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN PKP	06/26/02
CHECKED	

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TITLE NL/NLG PACKAGE OUTLINE
6.0 X 6.0 mm BODY
VFQFP-N

SIZE	DRAWING No.	REV
C	PSC-4115	03

DO NOT SCALE DRAWING | SHEET 2 OF 2

Ordering Information

Table 13. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N524-dddNLGI	IDT8T49N524-dddNLGI	“Lead-Free” 40 Lead VFQFN	Tray	-40°C to 85°C
8T49N524-dddNLGI8	IDT8T49N524-dddNLGI	“Lead-Free” 40 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: For the specific -ddd order codes, refer to *Programmable FemtoClock® NG Product Ordering Guide* document.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			In footer, corrected year of date from 2012 to 2013.	4/2/2013
A	T5D T9	1 12 18 32 33	Features: Changed 'Output frequencies from 15.5MHz - 650MHz, and 975MHz - 1300MHz' to 'Output frequencies from 15.234MHz - 645MHz, and 975MHz - 1290MHz, (See Table 5D for details)' Changed f_{MAX} column: 1300 to 1290; 650 to 645; 433.33333 to 430; 2600 to 2580; 20.635 to 20.476; NOTE 1: 325MHz to 322.5MHz. f_{VCO}: 1910MHz Min to 1950MHz Min; 2500MHz Max to 2580MHz Max 2nd paragraph: 18pF to 12pF Updated Applications schematic to include Fox crystal	7/10/2013
A	T13	8, 35 40	Changed name of the *IDT8T49N00xI Programmable FemtoClock® NG Product Ordering Information* document to *Programmable FemtoClock® Ordering Product Information* Deleted quantity from Tape & Reel, Deleted Lead Free note.	8/21/2013
A	T13	1 8 35	Changed title to Programmable FemtoClock® NG LVPECL/LVDS Dual 4-Output Fractional Clock Generator. Changed text from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.* Changed Note from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.*	9/26/13
A		2	Block diagram - corrected FSELx pin names.	1/23/14

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(Rev.1.0 Mar 2020)

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