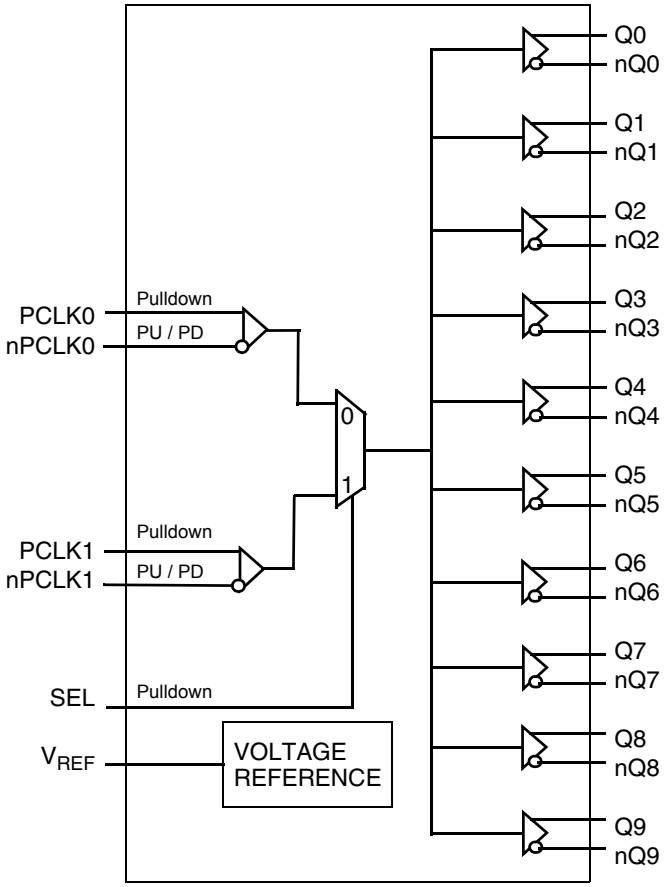
General Description

The IDT8T53S111I is a high-performance differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The IDT8T53S111I is characterized to operate from a 3.3V and 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the IDT8T53S111I ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and ten low skew outputs are available. The integrated V_{REF} voltage generator enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

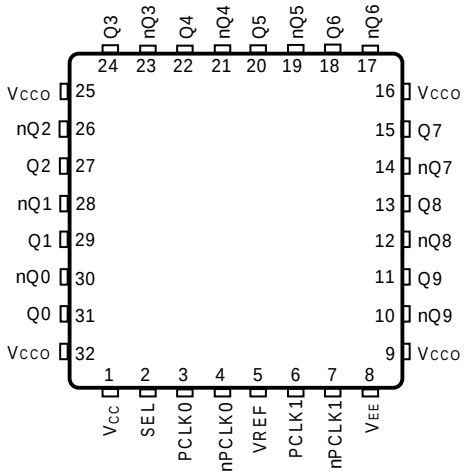
Features

- Ten low skew, low additive jitter LVPECL outputs
- Two selectable, differential LVPECL clock inputs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL and CML
- Maximum input clock frequency: 2.5GHz
- LVCMOS interface levels for the control input (input select)
- Output skew: 15ps (typical)
- Propagation delay: 250ps (typical)
- Additive phase jitter, RMS; f_{REF} = 156.25MHz (12kHz - 20MHz): 30fs (typical)
- Full 3.3V and 2.5V supply voltage
- Maximum device current consumption (I_{EE}): 126mA
- Lead-free (RoHS 6) 32-Lead VFQFN package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



IDT8T53S111I

32-lead VFQFN

5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm E-Pad

NL Package, Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Power supply pin.
2	SEL	Input	Pulldown	Reference select control. See Table 3 for function. LVCMOS/LVTTL interface levels.
3	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
4	nPCLK0	Input	Pulldown/ Pullup	Inverting differential LVPECL clock input.
5	V_{REF}	Output		Bias voltage generator for the nPCLK[0:1] inputs in single-ended input signal applications.
6	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
7	nPCLK1	Input	Pulldown/ Pullup	Inverting differential LVPECL clock input.
8	V_{EE}	Power		Negative power supply pin.
9, 16, 25, 32	V_{CCO}	Power		Output power supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3A. SEL Input Selection Function Table

Input	Operation
SEL	
0 (default)	PCLK0, nPCLK0 is the selected differential clock input.
1	PCLK1, nPCLK1 is the selected differential clock input.

NOTE: SEL is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
I_{REF}	±2mA
Package Thermal Impedance, θ_{JA}	48.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			95	126	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			90	119	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = V_{CCO} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nPCLK0, nPCLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{REF}	Reference Voltage for Input Bias		$I_{REF} = 2mA$	$V_{CC} – 1.6$		$V_{CC} – 1.1$	V
V_{OH}	Output High Voltage; NOTE 1			$V_{CCO} – 1.6$		$V_{CCO} – 0.6$	V
V_{OL}	Output Low Voltage; NOTE 1			$V_{CCO} – 2.0$		$V_{CCO} – 1.3$	V

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.

Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	$V_{CC} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-10			µA
		nPCLK0, nPCLK1	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{REF}	Reference Voltage for Input Bias		$I_{REF} = 2mA$	$V_{CC} – 1.6$		$V_{CC} – 1.1$	V
V_{OH}	Output High Voltage; NOTE 1			$V_{CCO} – 1.4$		$V_{CCO} – 0.8$	V
V_{OL}	Output Low Voltage; NOTE 1			$V_{CCO} – 2.0$		$V_{CCO} – 1.4$	V

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.

AC Electrical Characteristics

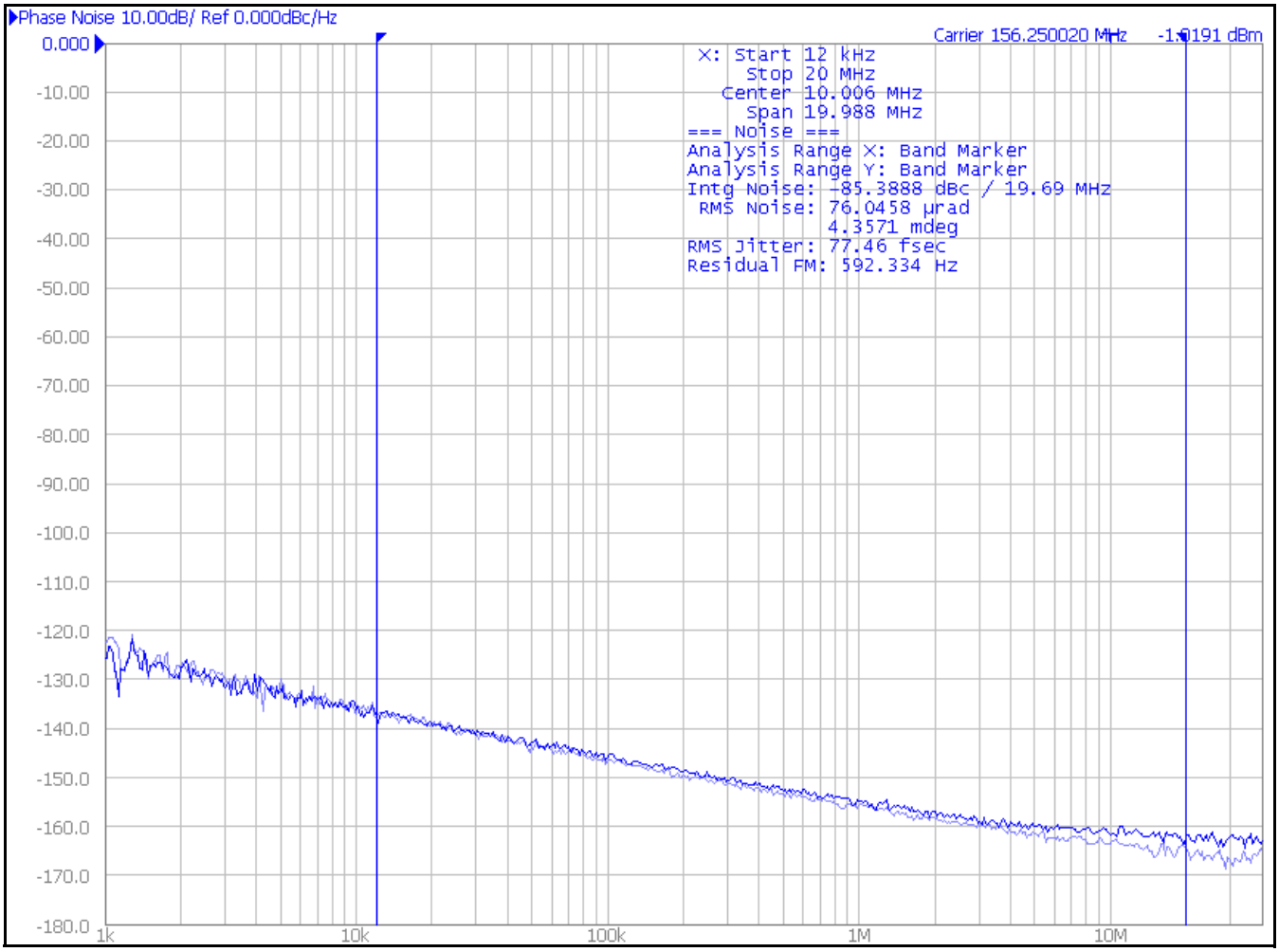
Table 5. AC Electrical Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		PCLK[0:1], nPCLK[0:1] to any Q[0:9], nQ[0:9] for V_{PP} = 0.1V or 0.3V	196	250	300	ps
*t*sk(o)	Output Skew; NOTE 2, 3				15	50	ps
*t*sk(i)	Input Skew; NOTE 3				5	25	ps
*t*sk(p)	Pulse Skew		f_{REF} = 50MHz		14	38	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				17	115	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 156.52MHz Integration Range: 12kHz – 20MHz		30	120	fs
t_R / t_F	Output Rise/ Fall Time		20% to 80%	50	90	160	ps
$MUX_{ISOLATION}$	MUX Isolation; NOTE 5		f_{REF} = 100MHz		-75		dB
V_{PP}	Input Peak-to-Peak Voltage; NOTE 5		f ≤ 1.5GHz	0.1		1.5	V
			f > 1.5GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage; NOTE 6, 7			1.0		V_{CCO} – 0.3	V
$V_{O(PP)}$	Output Voltage Swing, Peak-to-Peak		$f_{REF} \leq$ 2GHz	0.5	0.65	0.8	V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak-to-Peak		$f_{REF} \leq$ 2GHz	1.0	1.3	1.6	V

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, temperature, frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
NOTE 5: Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*
NOTE 6: V_{IL} should not be less than -0.3V.
NOTE 7: Common mode input voltage is defined as the crosspoint.

Additive Phase Jitter

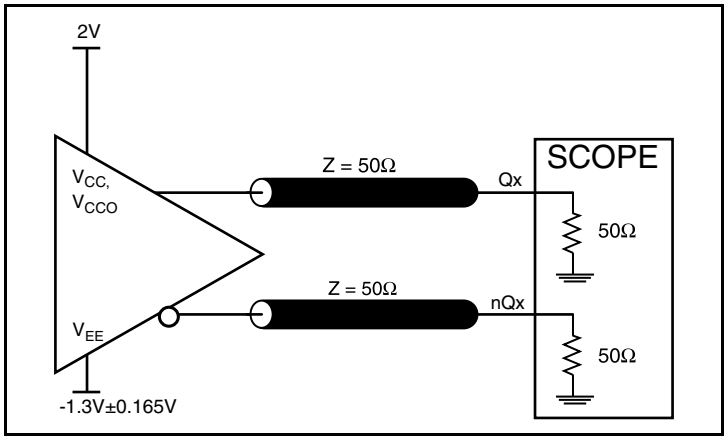
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



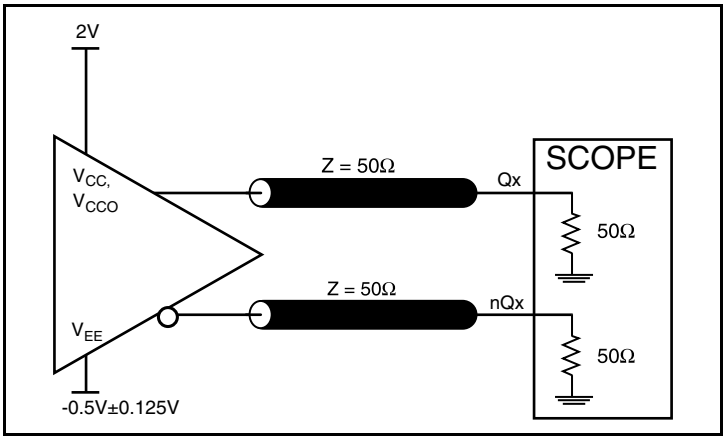
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using an Agilent - 5052 with a Wenzel 156.25MHz signal generator as the input source of the DUT.

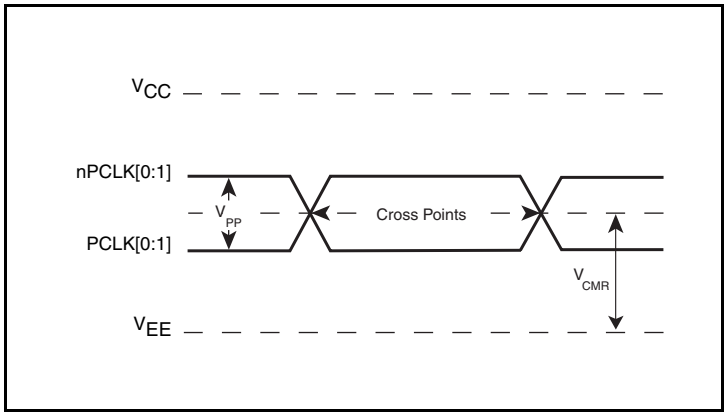
Parameter Measurement Information



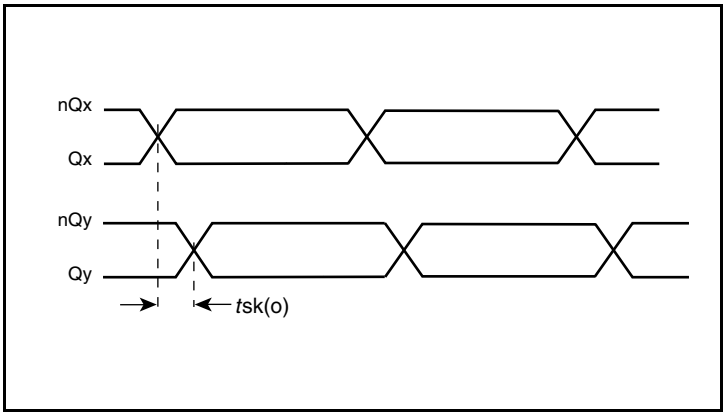
3.3V LVPECL Output Load AC Test Circuit



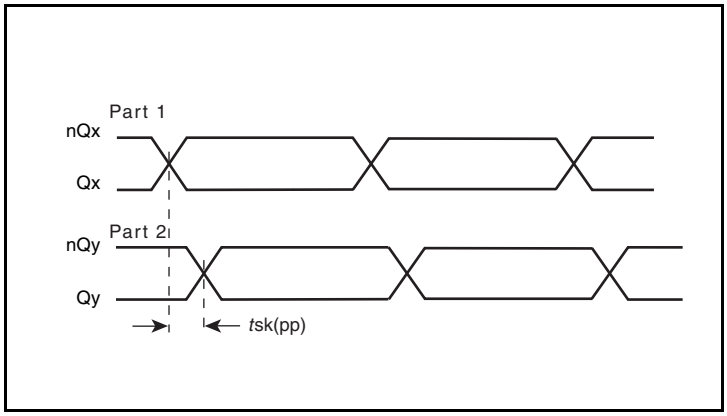
2.5V LVPECL Output Load AC Test Circuit



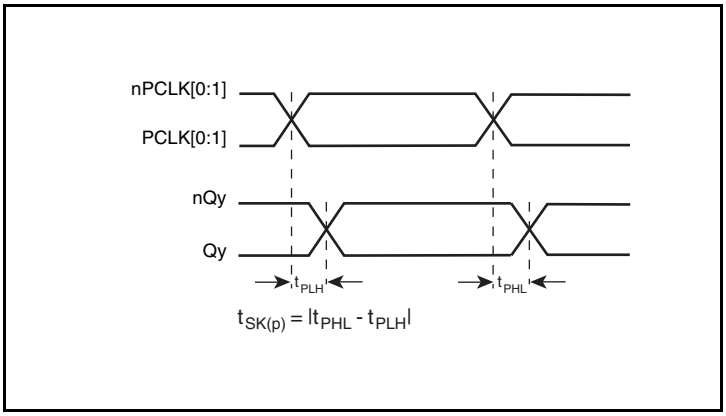
Differential Input Level



Output Skew

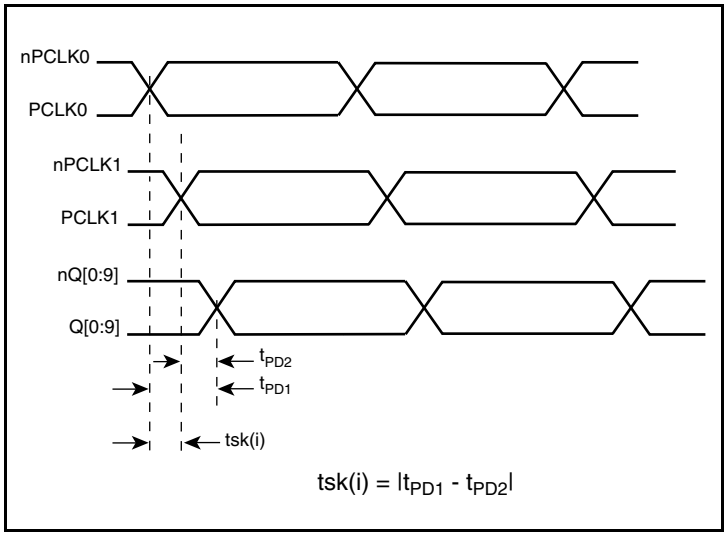


Part-to-Part Skew

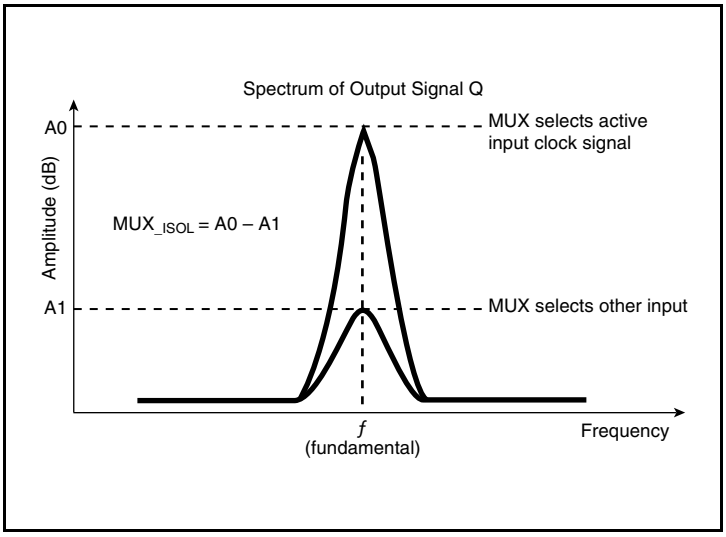


Pulse Skew

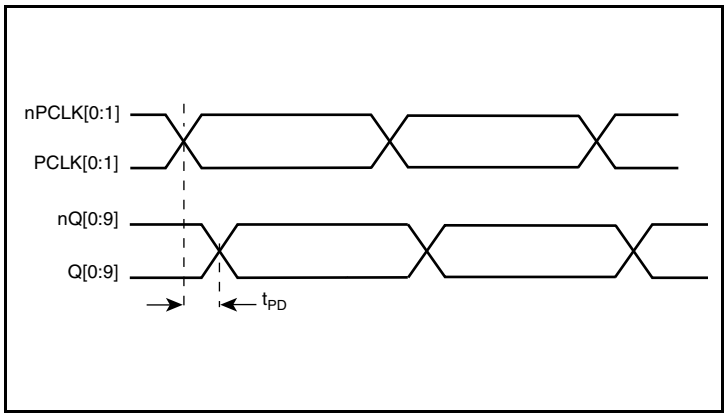
Parameter Measurement Information, continued



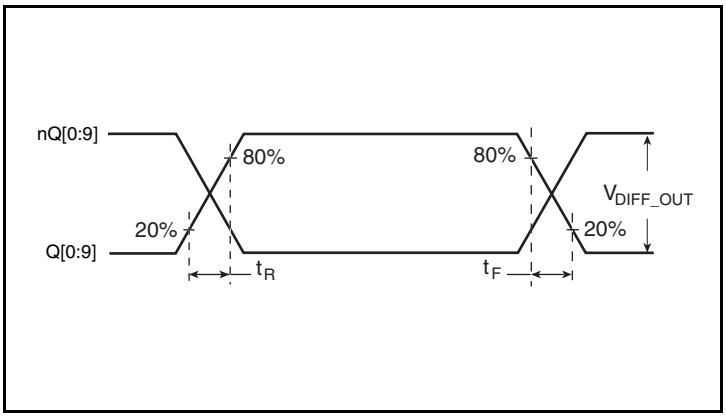
Input Skew



MUX Isolation



Propagation Delay



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

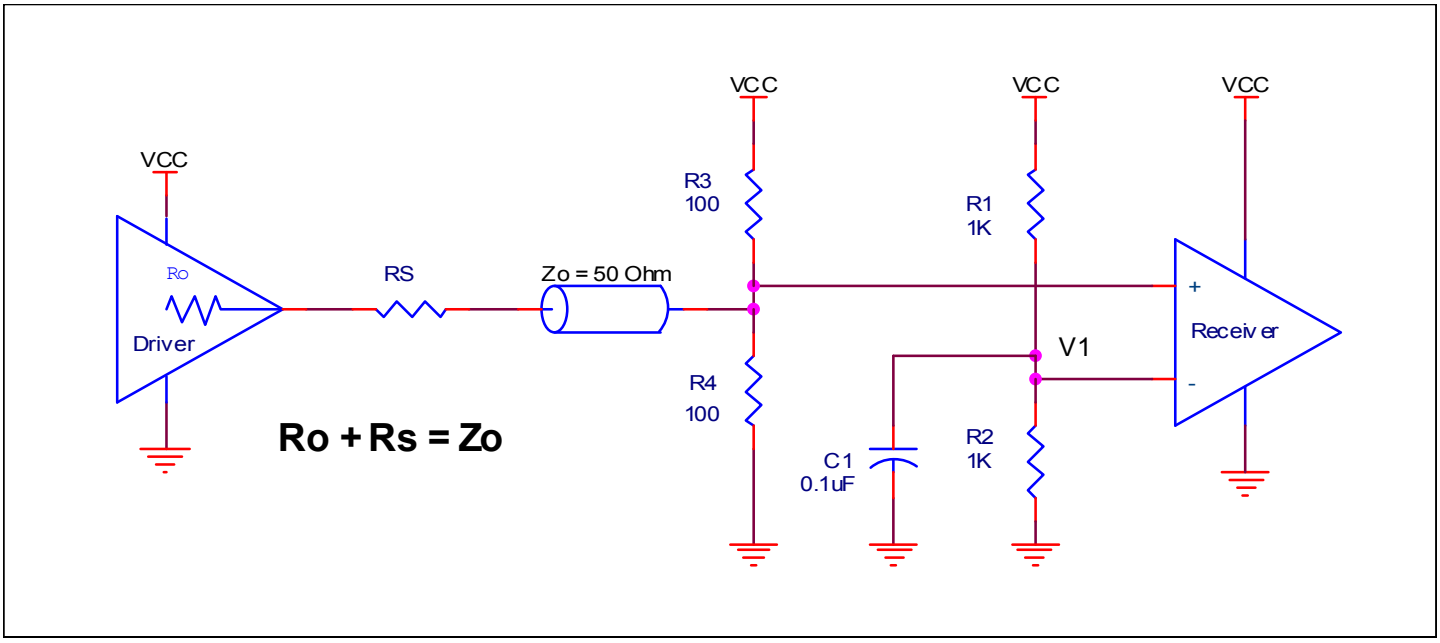


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

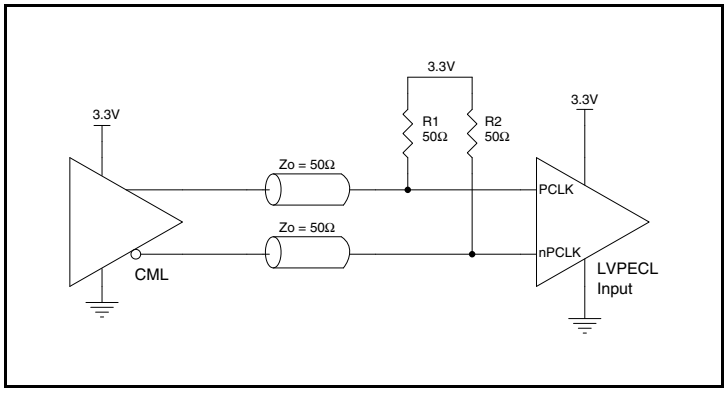


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

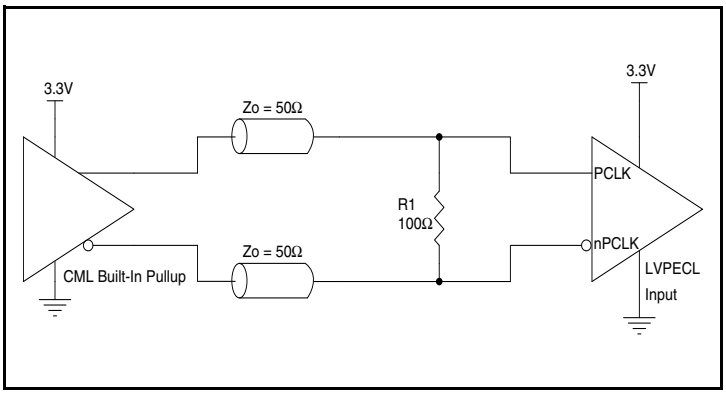


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

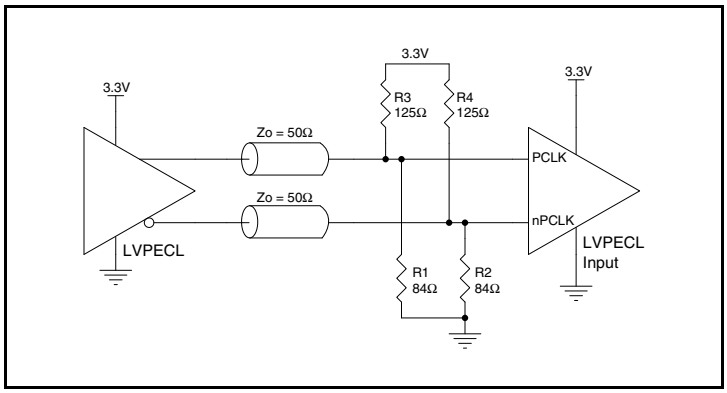


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

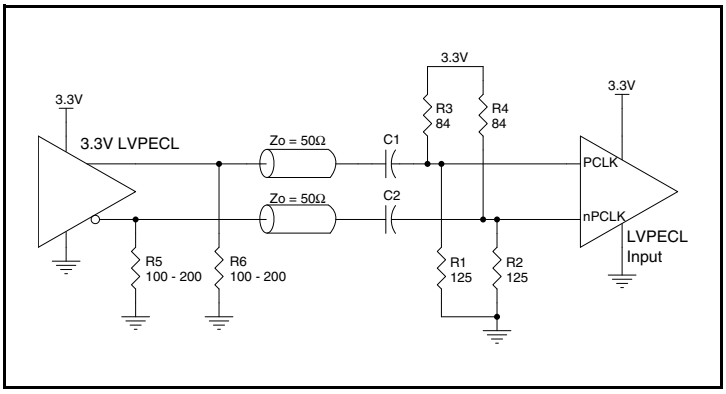


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

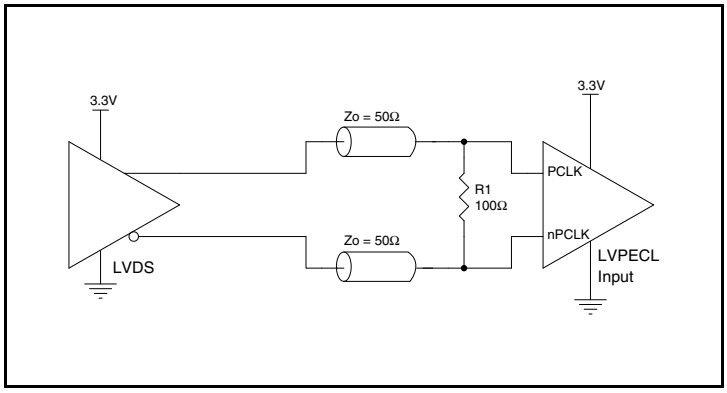


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

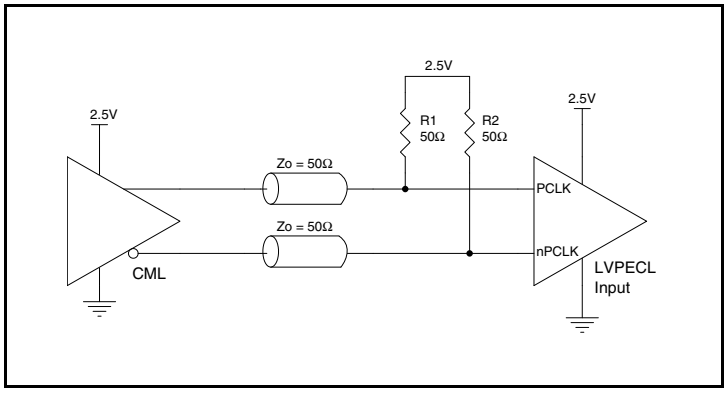


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

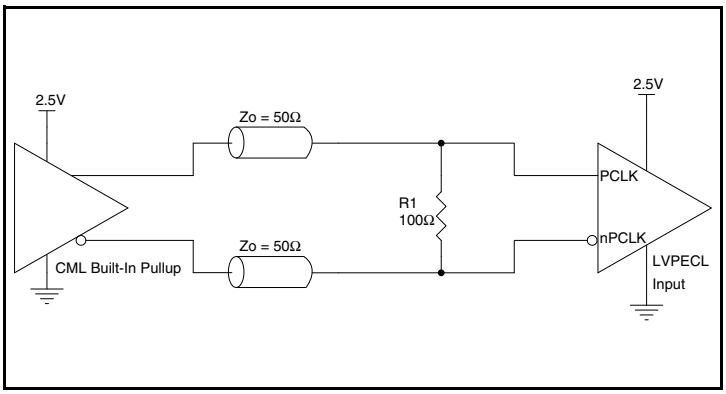


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

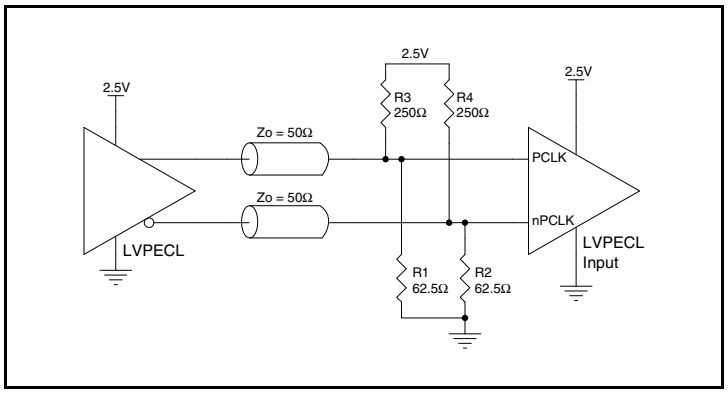


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

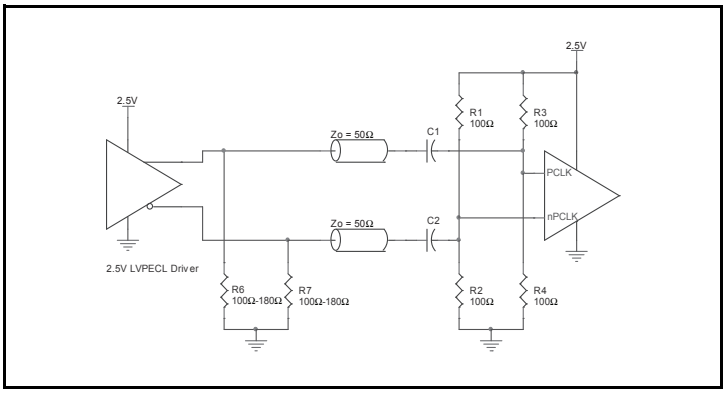


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

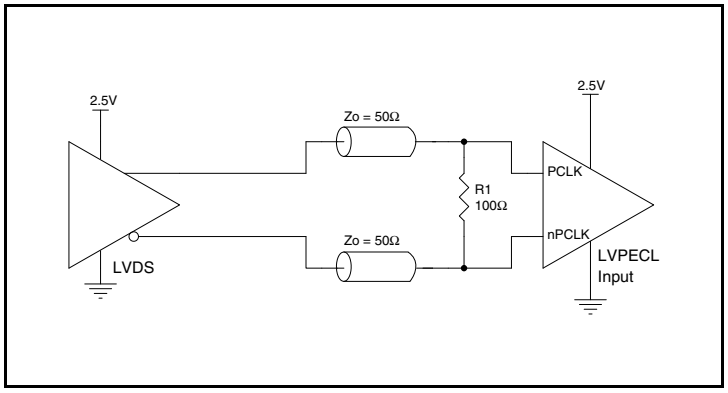


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

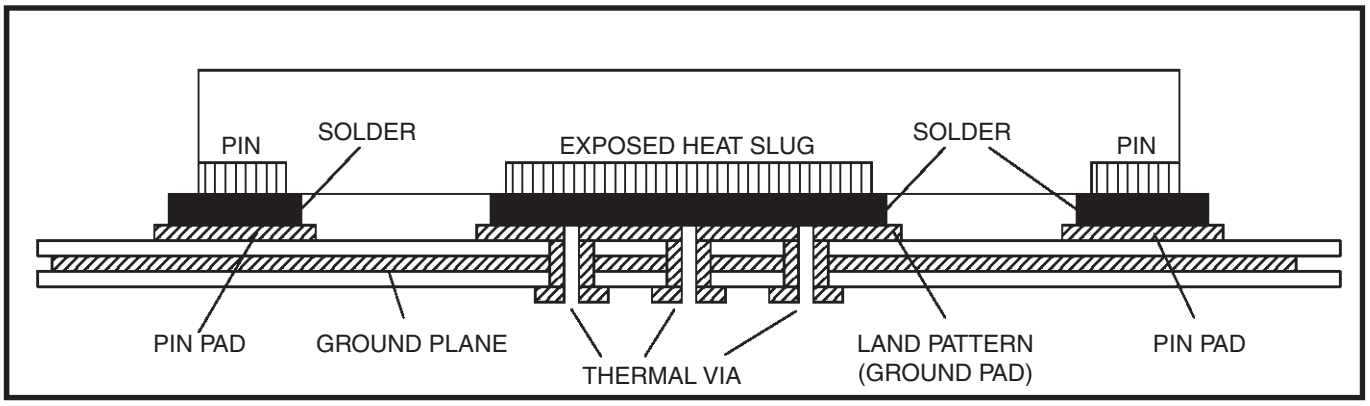


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T53S111I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T53S111I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 126mA = **436.59mW**
- Power $(outputs)_{MAX}$ = **35mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 35mW = **350mW**

Total Power$_{MAX}$ (3.465V, with all outputs switching) = 436.59W + 350mW = **786.59W**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 48.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.787W * 48.9°C/W = 123.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42.0°C/W	39.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 5.*

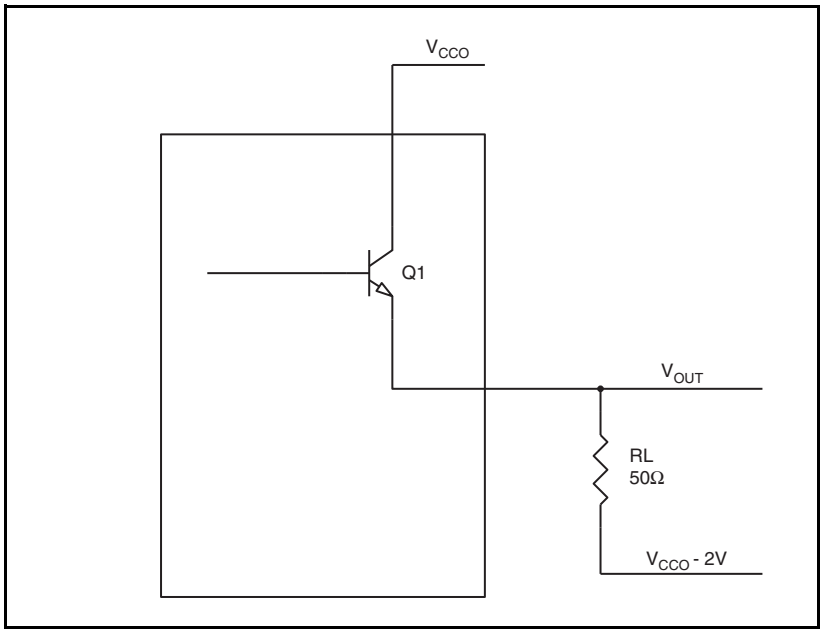


Figure 5. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.6V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.6V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.3V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.3V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.6V)/50\Omega] * 0.6V =$ **16.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.3V)/50\Omega] * 1.3V =$ **18.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **35mW**

Reliability Information

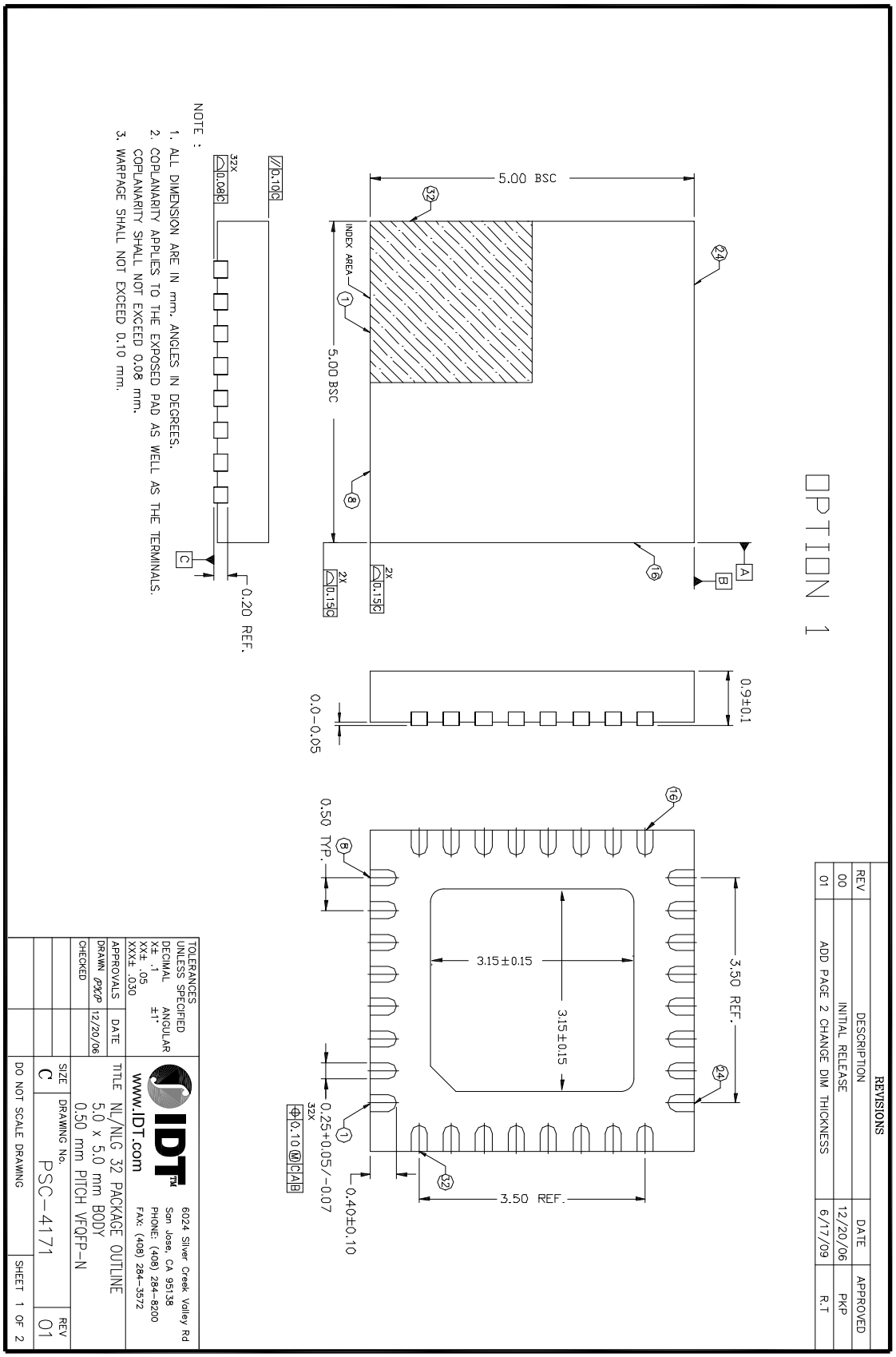
Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} at Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42.0°C/W	39.4°C/W

Transistor Count

The transistor count for the IDT8T53S111I is: 342

32 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T53S111NLGI	IDT8T53S111NLGI	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8T53S111NLGI8	IDT8T53S111NLGI	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with a “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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