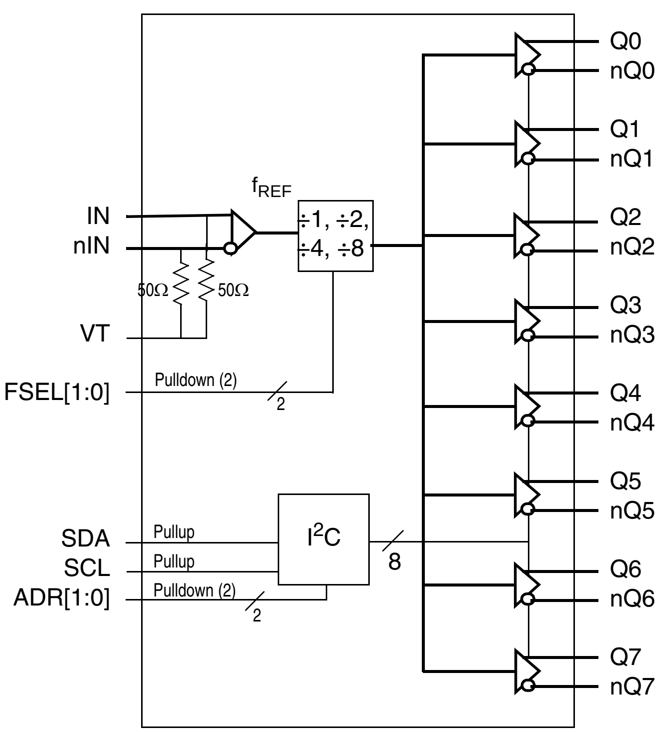
General Description

The 8T73S208 is a high-performance differential LVPECL clock divider and fanout buffer. The device is designed for the frequency division and signal fanout of high-frequency, low phase-noise clocks. The 8T73S208 is characterized to operate from a 2.5V and 3.3V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8T73S208 ideal for those clock distribution applications demanding well-defined performance and repeatability. The integrated input termination resistors make interfacing to the reference source easy and reduce passive component count. Each output can be individually enabled or disabled in the high-impedance state controlled by a I^2C register. On power-up, all outputs are enabled.

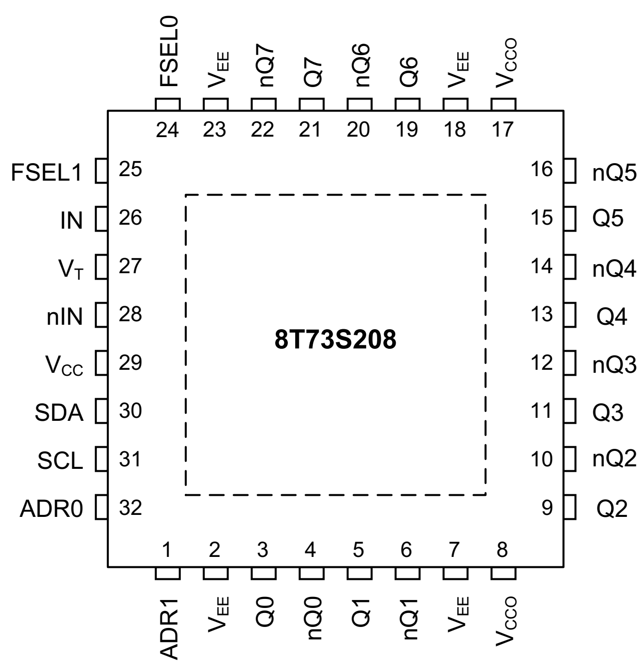
Features

- One differential input reference clock
- Differential pair can accept the following differential input levels: LVDS, LVPECL, CML
- Integrated input termination resistors
- Eight LVPECL outputs
- Selectable clock frequency division of ÷1, ÷2, ÷4 and ÷8
- Maximum input clock frequency: 1000MHz
- LVCMOS interface levels for the control inputs
- Individual output enable/disabled by I^2C interface
- Output skew: 15ps (typical)
- Output rise/fall times: 350ps (maximum)
- Low additive phase jitter, RMS: 0.182ps (typical)
- Full 2.5V and 3.3V supply voltages
- Lead-free (RoHS 6) 32-Lead VFQFN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



32-pin, 5mm x 5mm VFQFN

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 32	ADR1, ADR0	Input	Pulldown	I^2C Address inputs. LVCMOS/LVTTL interface levels.
2, 7, 18, 23	V_{EE}	Power		Negative supply pins.
3, 4	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
5, 6	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
8, 17	V_{CCO}	Power		Output supply pins.
9, 10	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
11, 12	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.
13, 14	Q4, nQ4	Output		Differential output pair 4. LVPECL interface levels.
15, 16	Q5, nQ5	Output		Differential output pair 5. LVPECL interface levels.
19, 20	Q6, nQ6	Output		Differential output pair 6. LVPECL interface levels.
21, 22	Q7, nQ7	Output		Differential output pair 7. LVPECL interface levels.
24, 25	FSEL0, FSEL1	Input	Pulldown	Frequency divider select controls. See Table 3A for function. LVCMOS/LVTTL interface levels.
26	IN	Input		Non-inverting differential clock input. RT = 50Ω termination to $V_{T.}$
27	V_T	Termination Input		Input for termination. Both IN and nIN inputs are internally terminated 50Ω to this pin. See input termination information in the applications section.
28	nIN	Input		Inverting differential clock input. RT = 50Ω termination to $V_{T.}$
29	V_{CC}	Power		Power supply pin.
30	SDA	I/O	Pullup	I^2C Data Input/Output. Input: LVCMOS/LVTTL interface levels. Output: open drain.
31	SCL	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Input Frequency Divider Operation

The FSEL1 and FSEL0 control pins configure the input frequency divider. In the default state (FSEL[1:0] are set to logic 0:0 or left open) the output frequency is equal to the input frequency (divide-by-1). The other FSEL[1:0] settings configure the input divider to divide-by-2, 4 or 8, respectively.

Table 3A. FSEL[1:0] Input Selection Function Table

Input		
FSEL1	FSEL0	Operation
0 (default)	0 (default)	$f_{Q[7:0]} = f_{REF} \div 1$
0	1	$f_{Q[7:0]} = f_{REF} \div 2$
1	0	$f_{Q[7:0]} = f_{REF} \div 4$
1	1	$f_{Q[7:0]} = f_{REF} \div 8$

NOTE: FSEL1, FSEL0 are asynchronous controls

Output Enable Operation

The output enable/disable state of each individual differential output Qx, nQx can be set by the content of the I^2C register (see Table 3C). A logic zero to an I^2C bit in register 0 enables the corresponding differential output, while a logic one disables the differential output (see Table 3B). After each power cycle, the device resets all I^2C bits (Dn) to its default state (logic 0) and all Qx, nQx outputs are enabled. After the first valid I^2C write, the output enable state is controlled by the I^2C register. Setting and changing the output enable state through the I^2C interface is asynchronous to the input reference clock.

The device supports the enable/disable of individual outputs. During an active operation of the device, enabling individual previously disabled outputs may degrade signal integrity of already enabled active outputs during the enabling transition. Disabling multiple outputs is supported without signal integrity constraints.

Table 3B. Individual Output Enable Control

Bit	
Dn	Operation
0 (default)	Output Qx, nQx is enabled.
1	Output Qx, nQx is disabled in high-impedance state.

Table 3C. Individual output enable control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Output	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Default	0	0	0	0	0	0	0	0

I^2C Interface Protocol

The IDT8T73S208I uses an I^2C slave interface for writing and reading the device configuration to and from the on-chip configuration registers. This device uses the standard I^2C write format for a write transaction, and a standard I^2C read format for a read transaction. Figure 1 defines the I^2C elements of the standard I^2C transaction. These elements consist of a start bit, data bytes, an acknowledge or Not-Acknowledge bit and the stop bit. These elements are arranged to make up the complete I^2C transactions as shown in Figure 2 and Figure 3. Figure 2 is a write transaction while Figure 3 is read transaction. The 7-bit I^2C slave address of the 8T73S208 is a combination of a 4-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0] (binary 11010, ADR1, ADR0). Bit 0 of slave address is used by the bus controller to select either the read or write mode. The hardware pins ADR1 and ADR0 and should be individually set by the user to avoid address conflicts of multiple 8T73S208 devices on the same bus.

Table 3D. I^2C Slave Address

7	6	5	4	3	2	1	0
1	1	0	1	0	ADR1	ADR0	R/W

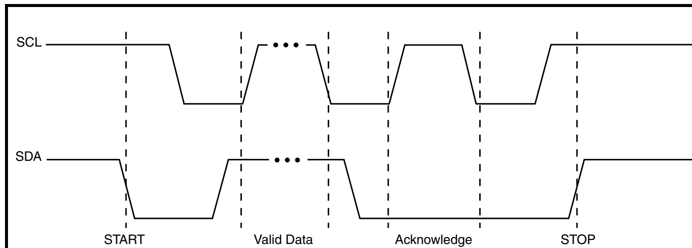


Figure 1: Standard I^2C Transaction

START (S) – defined as high-to-low transition on SDA while holding SCL HIGH.

DATA – between START and STOP cycles, SDA is synchronous with SCL. Data may change only when SCL is LOW and must be stable when SCL is HIGH.

ACKNOWLEDGE (A) – SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

STOP (S) – defined as low-to-high transition on SDA while holding SCL HIGH

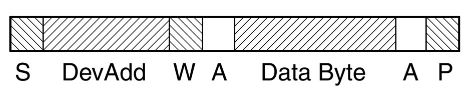


Figure 2: Write Transaction

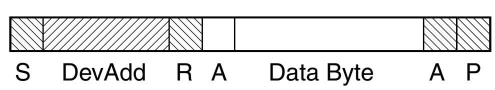


Figure 3: Read Transaction

S –	Start or Repeated Start
W –	R/~W is set for Write
R –	R/~W is set for Read
A –	Ack
DevAdd –	7 bit Device Address
P –	Stop

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Input Termination Current, I_{VT}	±35mA
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
Maximum Junction Temperature, TJ_{MAX}	125°C
ESD - Human Body Model[1]	2000V
ESD - Charged Device Model[1]	500V

NOTE 1. According to JEDEC/JS-001-2012-KJESD22- 22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO}$ = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
V_{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5V	2.625	V
V_{CCO}	Output Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current				95	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{CC} = V_{CCO}$ = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	$V_{CC} = V_{IN}$ = 2.625 or 3.465V			150	µA
		SCL, SDA	$V_{CC} = V_{IN}$ = 2.625 or 3.465V			10	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	V_{CC} = 2.625 or 3.465V, V_{IN} = 0V	-10			µA
		SCL, SDA	V_{CC} = 2.625 or 3.465V, V_{IN} = 0V	-150			µA

Table 4C. DC Characteristics, $V_{CC} = V_{CCO}$ = 2.5V ± 5% or 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IN}	Input Voltage Swing[1]			0.15			V
V_{IH}	Input High Voltage	IN, nIN	VIN<=1V	1.2		V_{CC}	V
V_{IH}	Input High Voltage	IN, nIN	VIN>1V	1.4		V_{CC}	V
V_{IL}	Input Low Voltage	IN, nIN		0		V_{IH} – 0.15	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
R_{IN}	Input Resistance	IN, nIN	IN to VT	40	50	60	Ω
R_{IN_DIFF}	Differential Input Resistance	IN, nIN	IN to nIN, VT = open	80	100	120	Ω

NOTE 1. Refer to Parameter Measurement Information, Input Voltage Swing diagram.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[1]		V_{CCO} – 1.102	V_{CCO} – 0.95	V_{CCO} – 0.775	V
V_{OL}	Output Low Voltage[1]		V_{CCO} – 1.802	V_{CCO} – 1.6	V_{CCO} – 1.367	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.60	0.65	1.00	V

NOTE 1. Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO}$ = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[1]		V_{CCO} – 1.125	V_{CCO} – 0.95	V_{CCO} – 0.767	V
V_{OL}	Output Low Voltage[1]		V_{CCO} – 1.799	V_{CCO} – 1.6	V_{CCO} – 1.359	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.60	0.65	1.00	V

NOTE 1. Outputs terminated with 50Ω to V_{CCO} – 2V.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol[1]	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	IN, nIN			1000	MHz
f_{OUT}	Output Frequency	FSEL[1:0] = 00			1000	MHz
		FSEL[1:0] = 01			500	MHz
		FSEL[1:0] = 10			250	MHz
		FSEL[1:0] = 11			125	MHz
f_{SCL}	I^2C Clock Frequency				400	kHz
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, measured with FSEL[1:0] = 00	f_{REF} = 100MHz, Integration Range: 12kHz – 20MHz		0.293	0.338	ps
		f_{REF} = 125MHz, Integration Range: 12kHz – 20MHz		0.219	0.245	ps
		f_{REF} =156.25MHz, Integration Range: 12kHz – 20MHz		0.182	0.207	ps
t_{PD}	Propagation Delay[2] — IN, nIN to Qx, nQx	FSEL[1:0] = 00		550	750	ps
		FSEL[1:0] = 01		675	870	ps
		FSEL[1:0] = 10		815	1052	ps
		FSEL[1:0] = 11		930	1230	ps
$t$sk(o)	Output Skew[3,4]			15	60	ps
$t$sk(p)	Pulse Skew			10	50	ps
$t$sk(pp)	Part-to-Part Skew[3,5,6]				500	ps
odc	Output Duty Cycle[7]	Any Frequency		50		%
		at f_{REF} = 100MHz	48	50	52	%
		at f_{REF} = 125MHz	48	50	52	%
		at f_{REF} = 156.25MHz	48	50	52	%
t_{PDZ}	Output Enable and Disable Time[8]	Output Enable/Disable State from/to Active/Inactive		1		µs
t_R / t_F	Output Rise/ Fall Time	20% to 80%		140	205	ps
		10% to 90%		180	350	ps

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Measured from the differential input crossing point to the differential output cross point.

NOTE 3. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.

NOTE 4. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

NOTE 6. Part-to-part skew specification does not guarantee divider synchronization between devices.

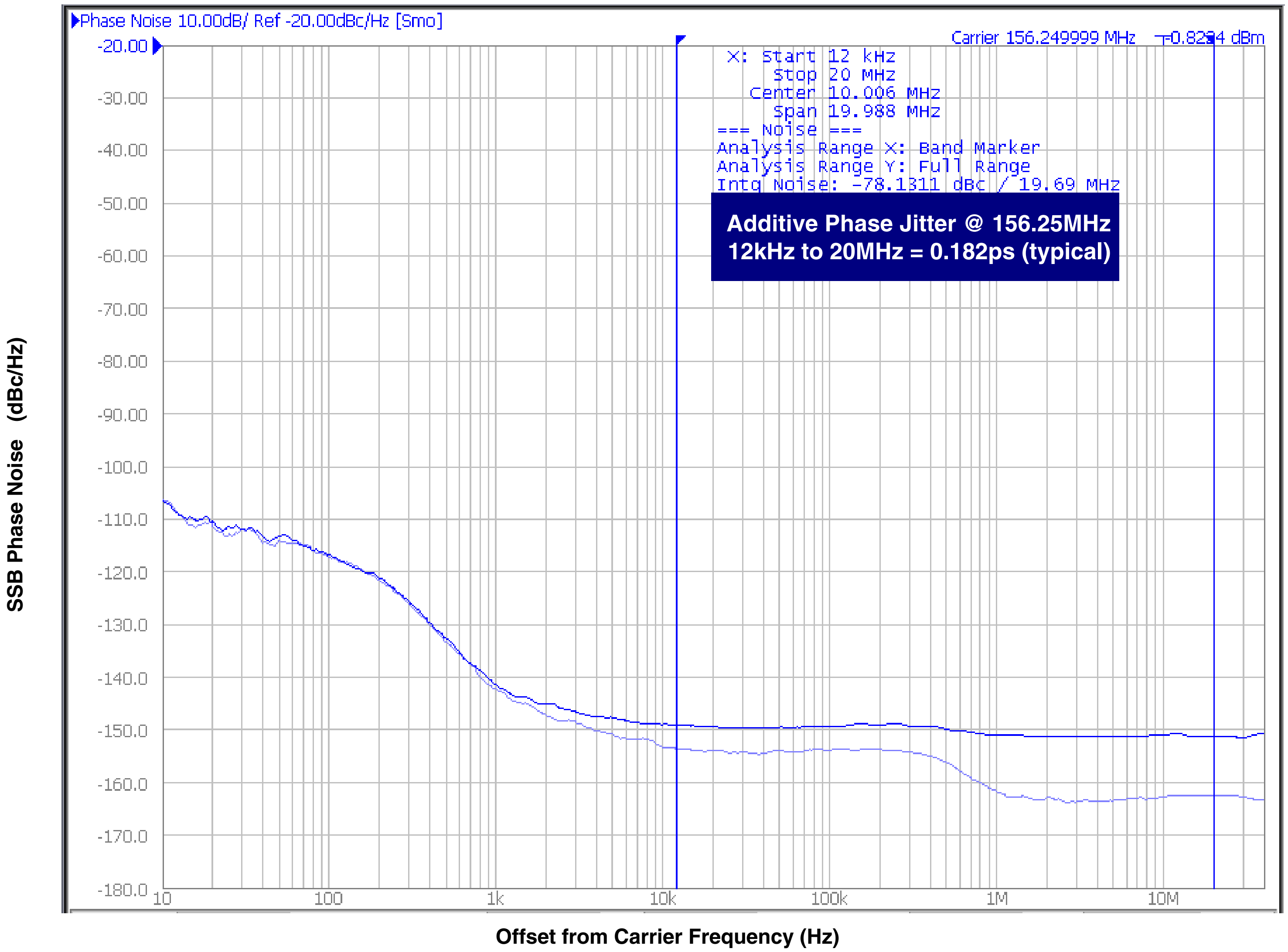
NOTE 7. If FSEL[1:0] = 00 (divide-by-one), the output duty cycle will depend on the input duty cycle.

NOTE 8. Measured from SDA rising edge of I^2C stop command.

Additive Phase Jitter

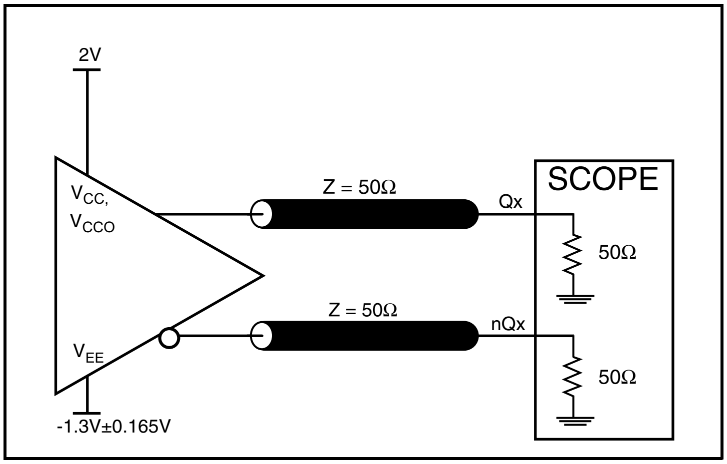
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Typical Phase Jitter at 156.25MHz

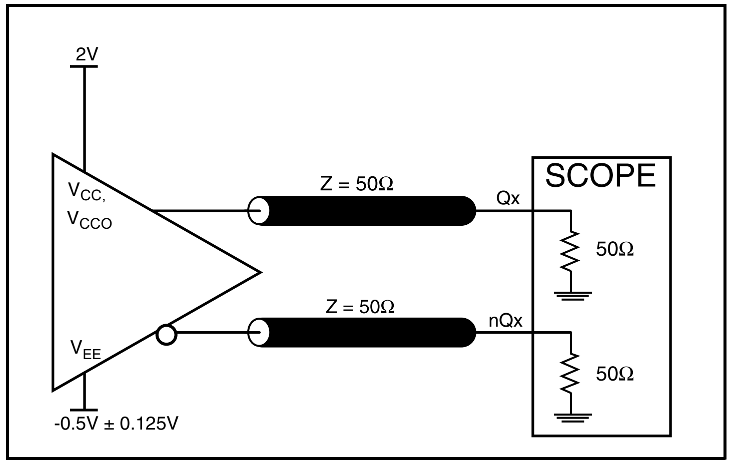


The input source is 156.25MHz Wenzel Oscillator.

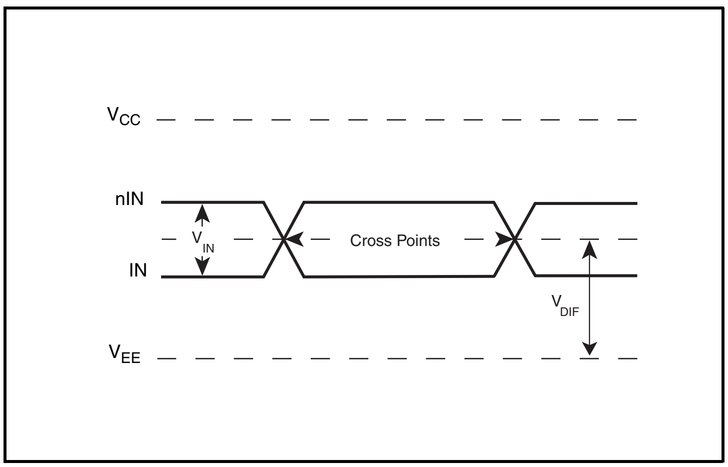
Parameter Measurement Information



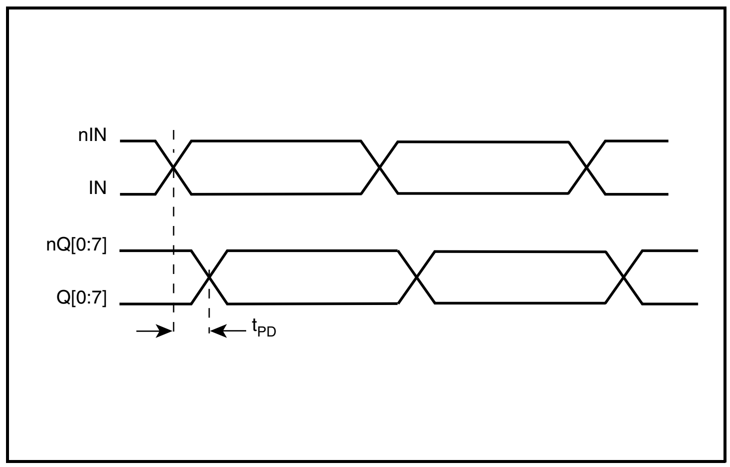
3.3 Core/3.3V LVPECL Output Load AC Test Circuit



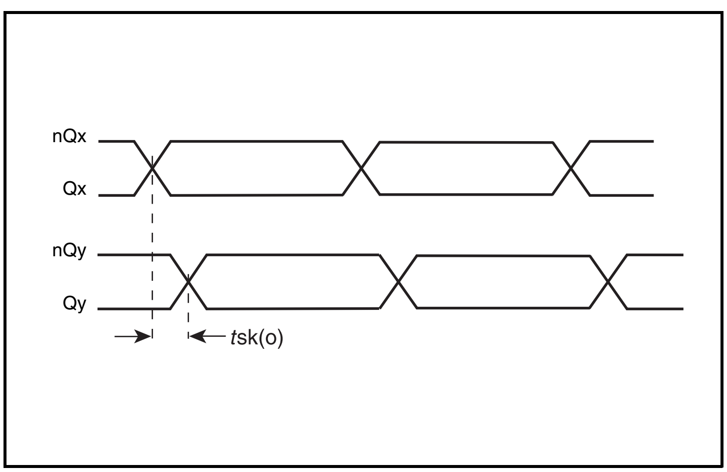
2.5V Core/2.5V LVPECL Output Load AC Test Circuit



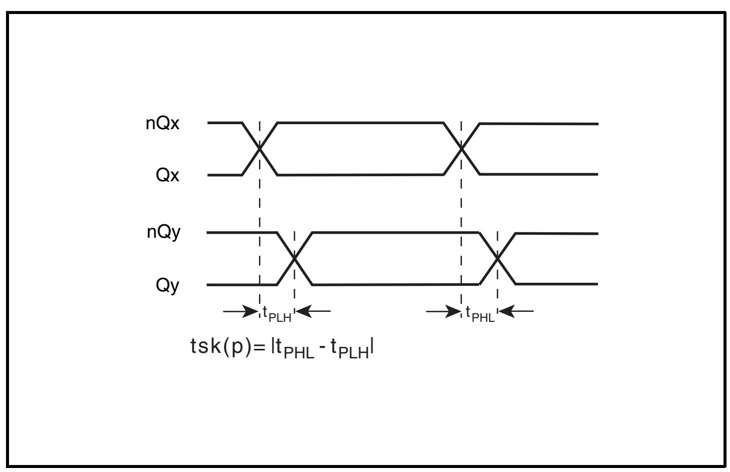
Differential Input Level



Propagation Delay

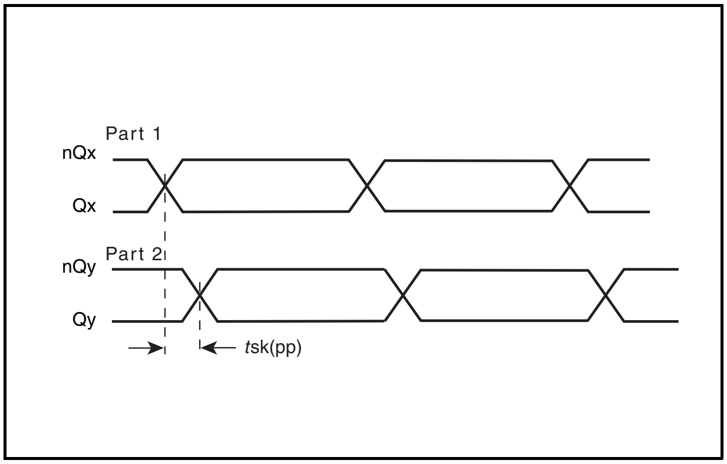


Output Skew

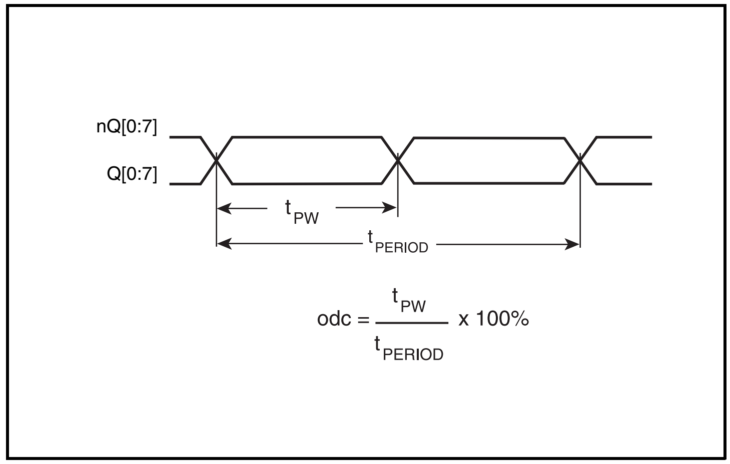


Pulse Skew

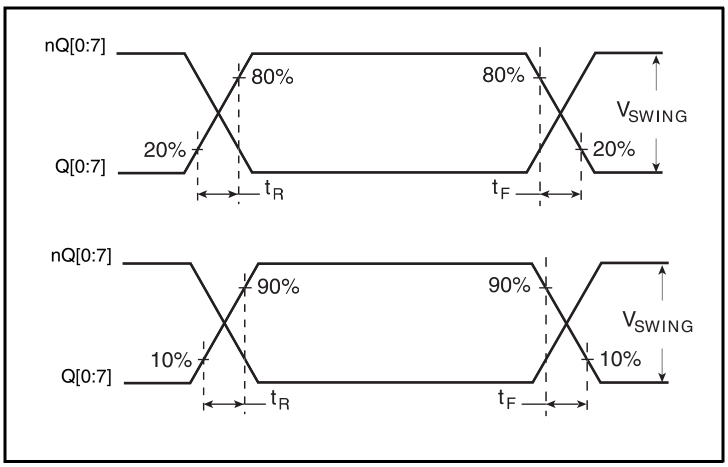
Parameter Measurement Information, continued



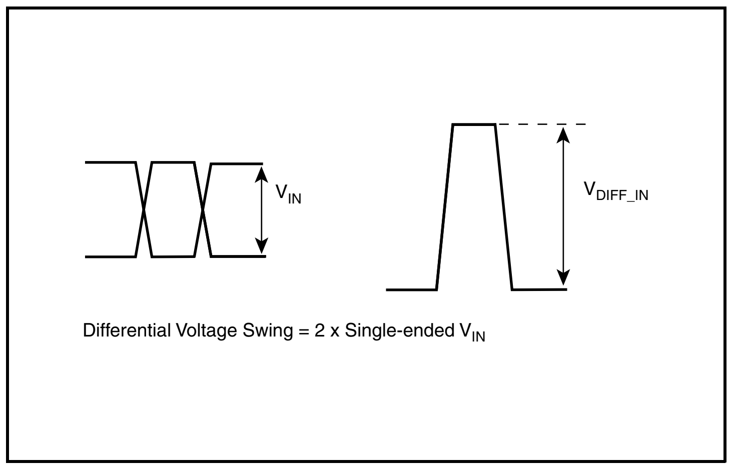
Part-to-Part Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Single-Ended & Differential Input, Output Voltage Swing

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 4A to 4D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

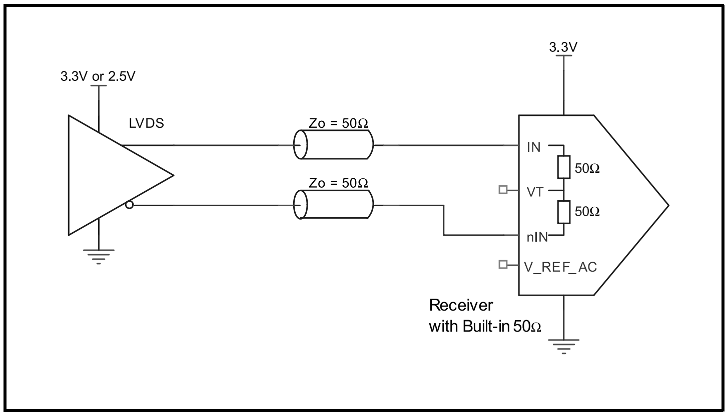


Figure 4A. N/nIN Input with Built-In 50Ω Driven by an LVDS Driver

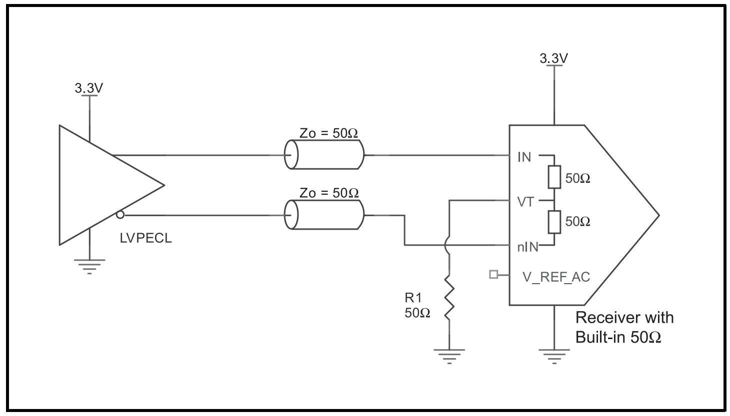


Figure 4B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

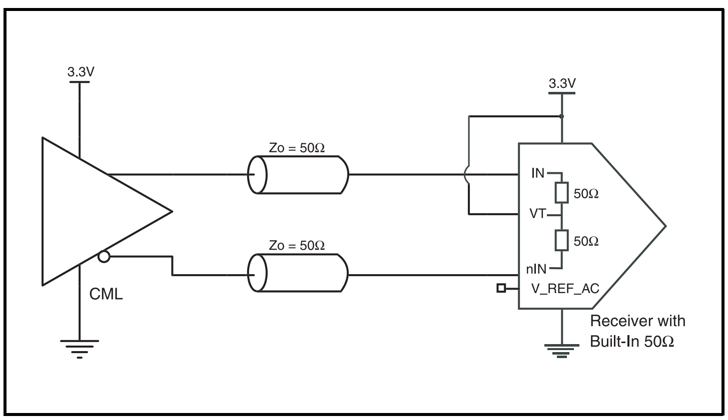


Figure 4C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

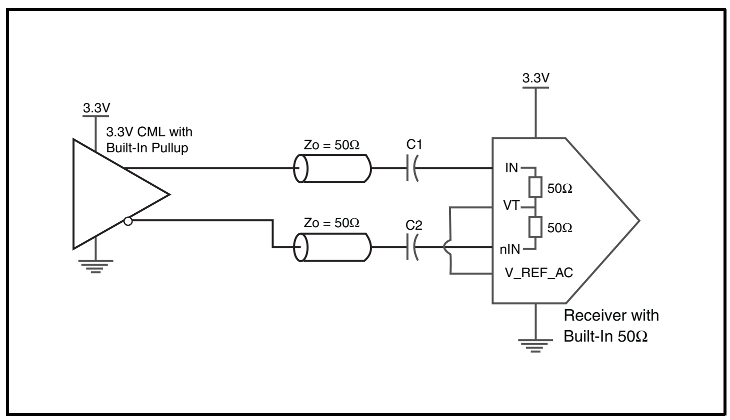


Figure 4D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 5A to 5D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

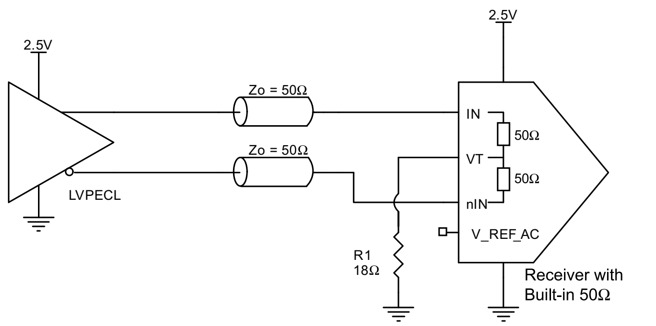


Figure 5A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

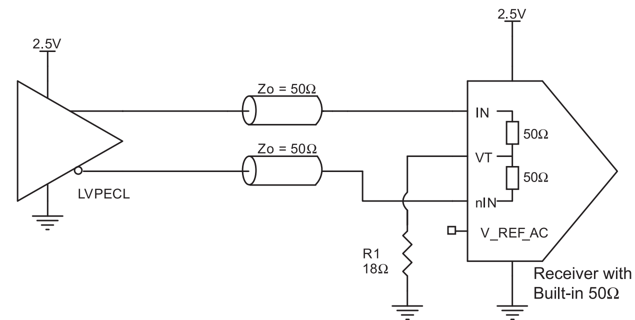


Figure 5B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

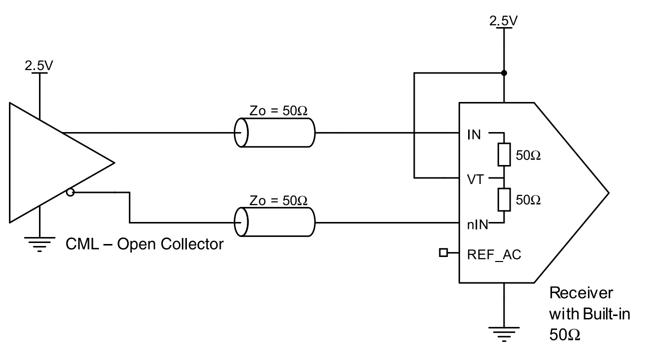


Figure 5C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

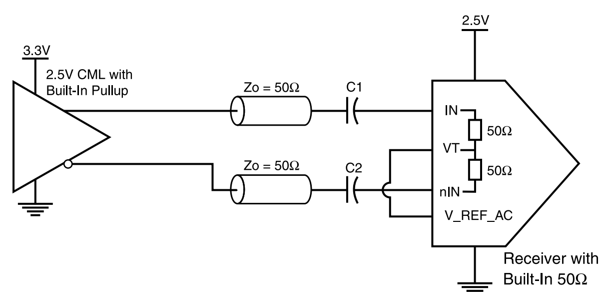


Figure 5D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

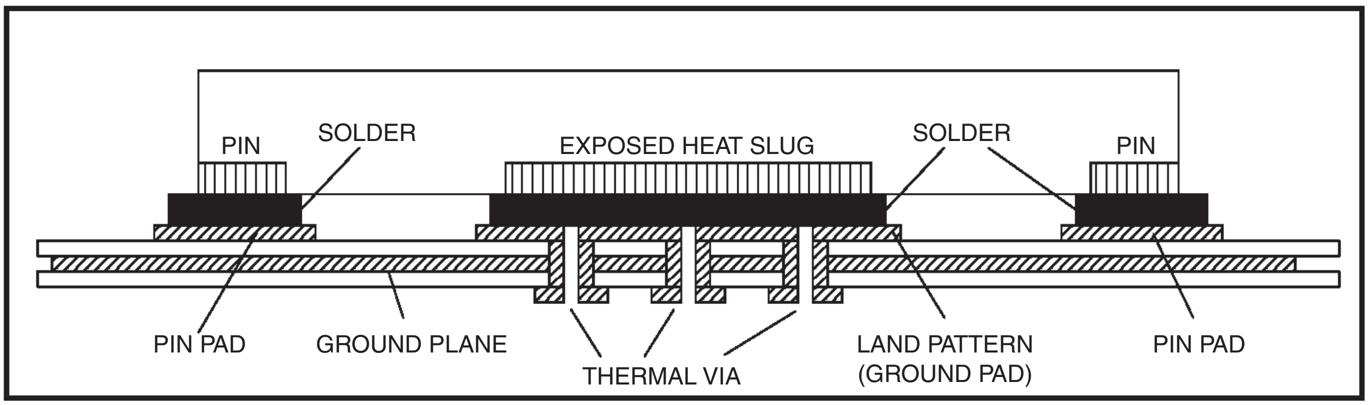


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

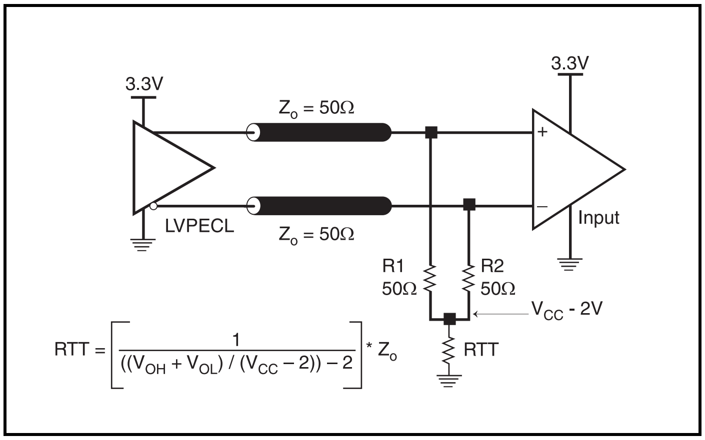


Figure 7A. 3.3V LVPECL Output Termination

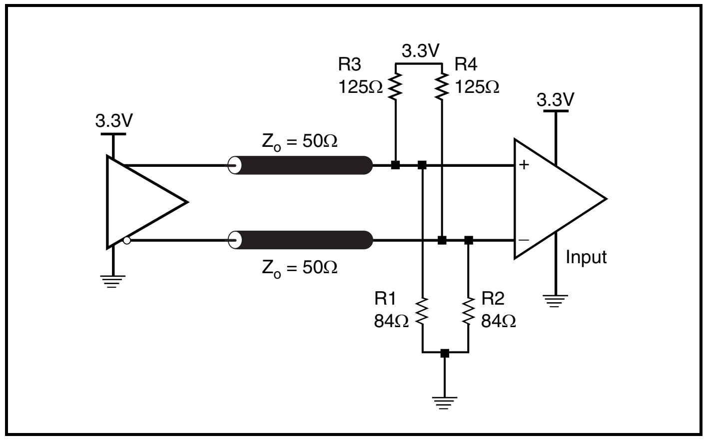


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 8B can be eliminated and the termination is shown in *Figure 8C.*

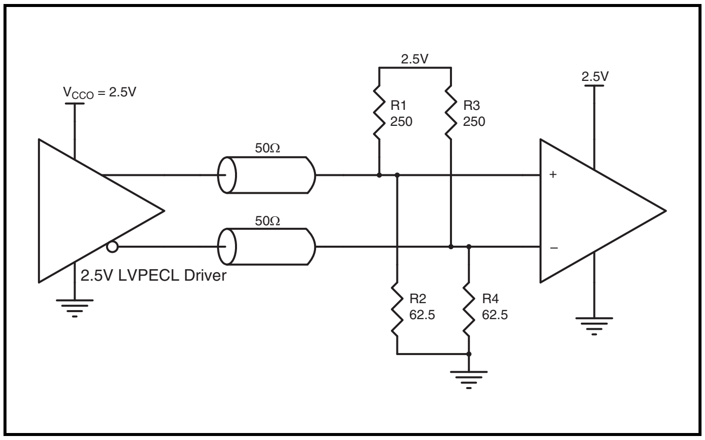


Figure 8A. 2.5V LVPECL Driver Termination Example

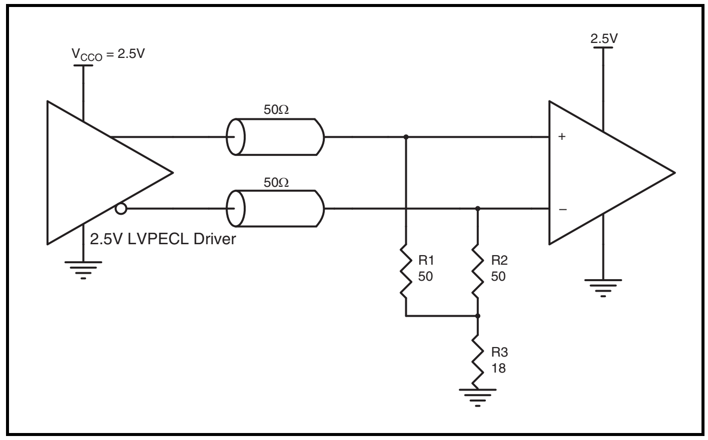


Figure 8B. 2.5V LVPECL Driver Termination Example

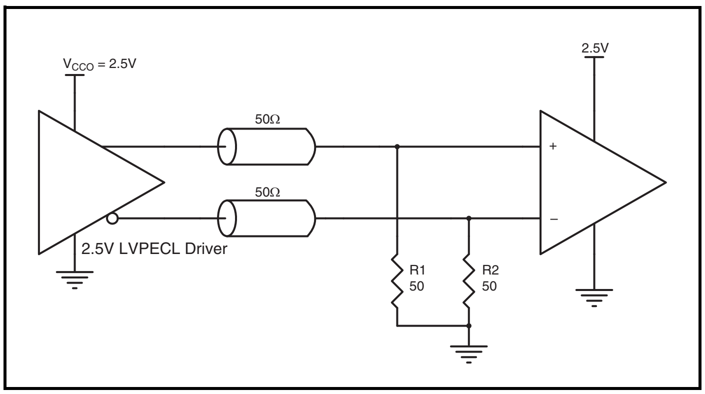


Figure 8C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T73S208.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T73S208 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 95mA = **329.175mW**
- Power $(outputs)_{MAX}$ = **36.3mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 36.3mW = **290.4mW**
- Power Dissipation for internal termination R_T
  (Assuming V_{IN} = 0.15V and V_{CMR} = 3.225V ⇒ V_{IH} = 3.3V and V_{IL} = 3.15V; and external 50Ω is connected from V_T pin to V_{EE}.)
  Power $(R_T)_{MAX}$ = **46.5mW**

Total Power$_{\_MAX}$ = (3.465V, with all outputs switching) = 329.175mW + 290.4mW + 46.5mW = **666.08mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.666W * 42.7°C/W = 113.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 9.*

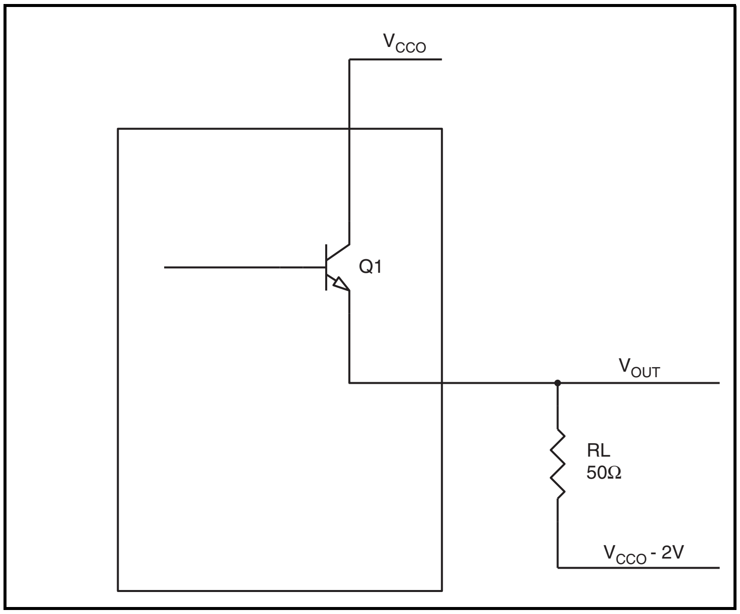


Figure 9. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.775V}$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) = \mathbf{0.82V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.367V}$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) = \mathbf{1.58V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.775V)/50\Omega] * 0.775V =$ **18.99mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.367V)/50\Omega] * 1.367V =$ **17.31mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **36.3mW**

Reliability Information

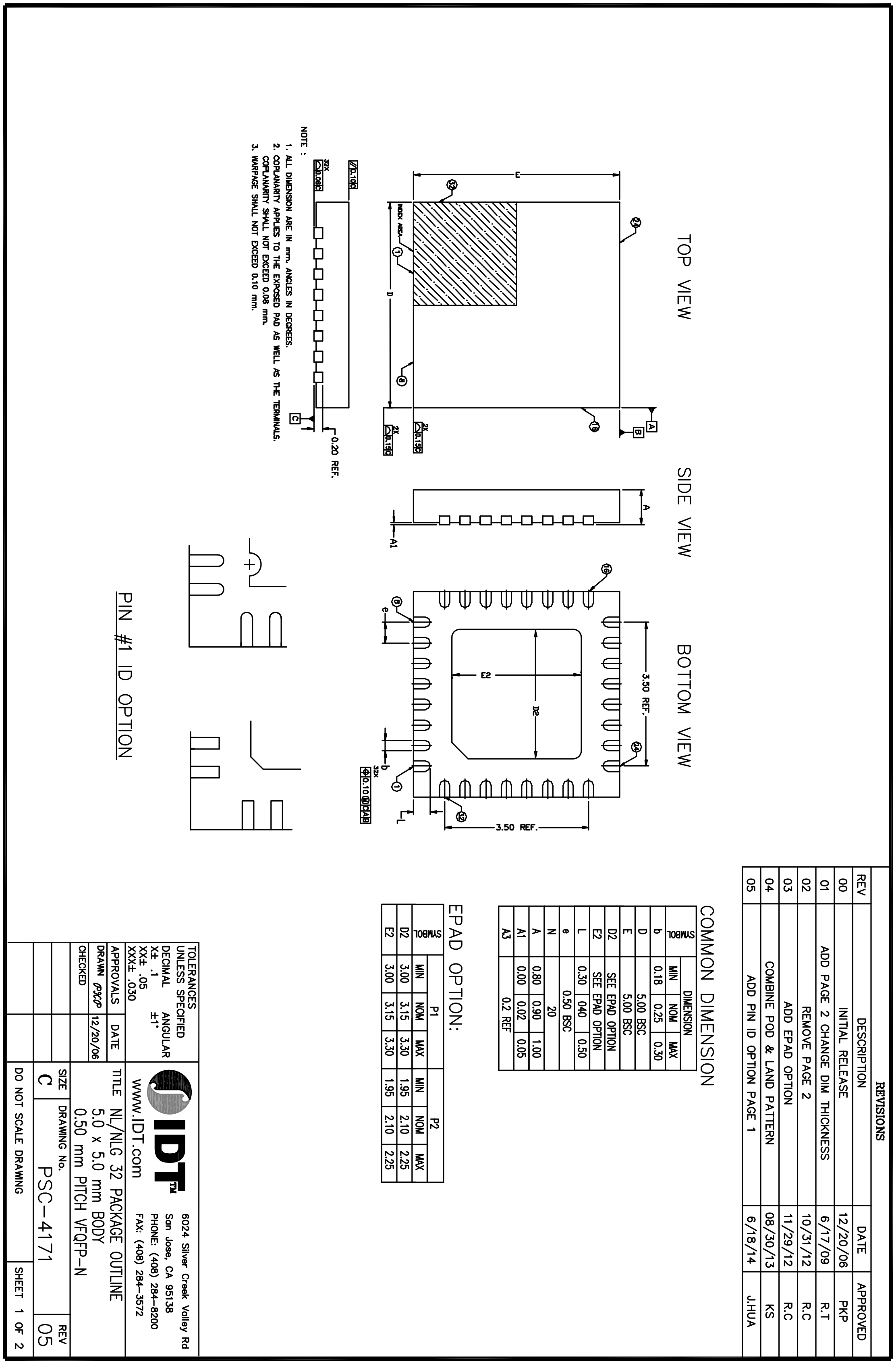
Table 7. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

The transistor count for 8T73S208 is: 4833

32 Lead VFQFN Package Outline and Package Dimensions



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	12/20/06	PKP
01	ADD PAGE 2 CHANGE DIM THICKNESS	6/17/09	R.T
02	REMOVE PAGE 2	10/31/12	R.C
03	ADD EPAD OPTION	11/29/12	R.C
04	COMBINE POD & LAND PATTERN	08/30/13	KS
05	ADD PIN ID OPTION PAGE 1	6/18/14	J.HUA

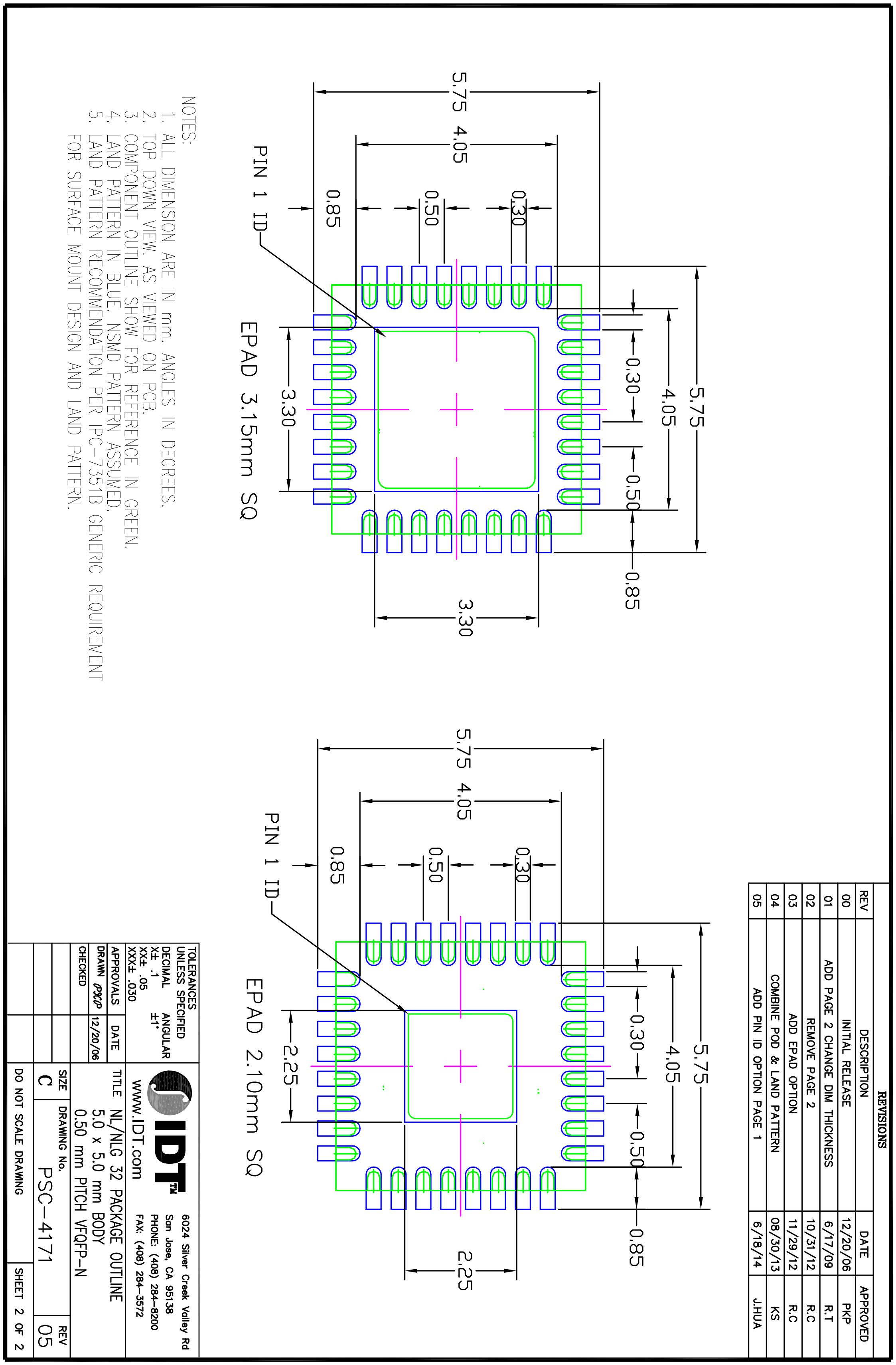
COMMON DIMENSION

SYMBOL	DIMENSION MIN	NOM	MAX
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2		SEE EPAD OPTION	
E2		SEE EPAD OPTION	
L	0.30	040	0.50
e		0.50 BSC	
N		20	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	

EPAD OPTION:

SYMBOL	P1 MIN	P1 NOM	P1 MAX	P2 MIN	P2 NOM	P2 MAX
D2	3.00	3.15	3.30	1.95	2.10	2.25
E2	3.00	3.15	3.30	1.95	2.10	2.25

32 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T73S208BNLGI	IDT8T73S208BNLGI	32 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8T73S208BNLGI8	IDT8T73S208BNLGI	32 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Added 'G' in the part number in footer.	4/8/2013
A		12-13	Re-rendered to make the fonts legible.	4/22/13
B		4 6 17 20 - 21	Absolute Maximum Ratings Table - added Input Termination Current row. Corrected NOTE 1. Changed Additive Phase Jitter plot. Power Considerations section - updated Power Dissipation section. Updated Package Outline and Dimensions section to Rev 5. Updated Header/Footer through-out the datasheet. Deleted "IDT" prefix and "I" suffix of the part number through-out the datasheet.	1/13/15
C		3	Section , "Output Enable Operation" - added last paragraph.	6/3/16
D	T8	3 20	Section , "Output Enable Operation" - updated last paragraph. Updated datasheet header/footer. Section , "Table 8. Ordering Information" - deleted table note.	6/15/16

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