

General Description

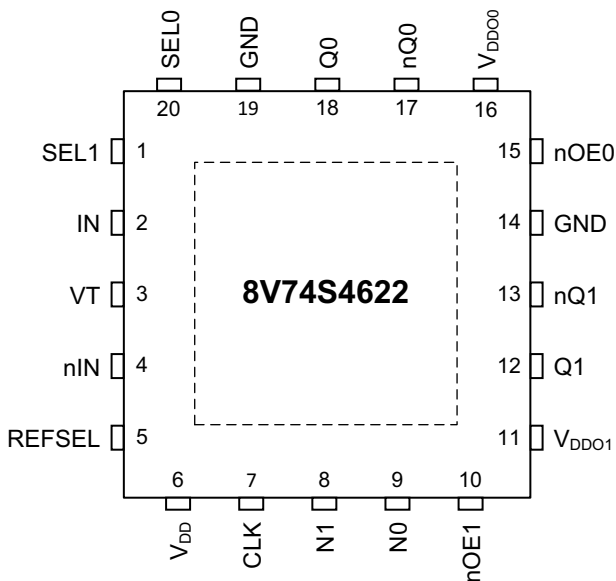
The 8V74S4622 is a versatile Clock Fanout Buffer/Frequency Divider. The device supports the selection, division and distribution of high-frequency clock signals with very low additive phase noise. The 8V74S4622 uses SiGe technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection and internal isolation.

Two selectable inputs are supported for differential and single ended clocks. Each of the two outputs can select a copy or a frequency-divided input signal. The available frequency divisions are divide-by-2, 4, 5 and 8. Both outputs support LVDS interfaces. For each of the two outputs, a synchronous output enabled control is implemented for stopping the output clock synchronously to the input clock signal. All device configurations are through a logic pin interface. The device is packaged in a lead-free (RoHS 6) 20-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

Features

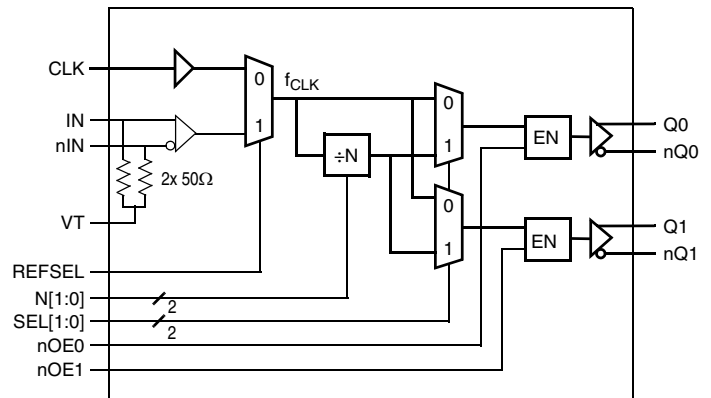
- Clock signal selection, frequency-division and distribution
- Two outputs individually select:
 - The input signal $\div 2$, $\div 4$, $\div 5$ and $\div 8$ or
 - The input signal without frequency division (input signal is passed through)
- Two inputs to support single-ended and differential operation
- Differential input supports LVDS and LVPECL signals
- Single-ended input supports LVCMOS signals
- Two differential LVDS outputs
- Maximum Input Frequency (differential input clock): 2000MHz
- Maximum Output Frequency: 2000MHz
- Output skew: 22ps (maximum)
- Additive phase noise RMS, 125MHz, SELn = 0, 12kHz - 20MHz integration range: 180fs (maximum)
- LVDS output rise/fall time: 260ps (maximum)
- 3.3V core and output supply voltages
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) 4x4 mm² 20-lead VFQFN packaging

Pin Assignment



20-pin, 4mm x 4mm VFQFN Package

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions¹

Number	Name	Type		Description
1	SEL1	Input	Pulldown	Function select control input. LVCMOS 3.3V interface. See Table 3B for function.
2	IN	Input		Differential clock signal non-inverting differential input. Internal termination 50Ω.
3	VT			Differential clock input termination pin for built-in 50Ω termination interface. See the application information for terminating LVDS and LVPECL input signals.
4	nIN	Input		Differential clock signal inverting differential input. Internal termination 50Ω.
5	REFSEL	Input	Pulldown	Input select control input. LVCMOS 3.3V interface. See Table 3A for function.
6	V _{DD}	Power		Positive supply voltage (3.3V).
7	CLK	Input	Pulldown	Single-ended LVCMOS 3.3V clock signal input.
8	N1	Input	Pullup	Frequency divider control input. LVCMOS 3.3V interface. See Table 3C for function.
9	N0	Input	Pulldown	
10	nOE1	Input	Pullup	Output Q1 enable control input. LVCMOS 3.3V interface. See Table 3D for function.
11	V _{DDO1}	Power		Positive supply voltage (3.3V) for the Q1 output.
12	Q1	Output		Differential clock output 1. LVDS interface signals.
13	nQ1	Output		
14	GND	Power		Ground supply voltage (0V). Connect to board GND.
15	nOE0	Input	Pullup	Output Q0 enable control input. LVCMOS 3.3V interface. See Table 3D for function.
16	V _{DDO0}	Power		Positive supply voltage (3.3V) for the Q0 output.
17	nQ0	Output		Differential clock output 0. LVDS interface signals.
18	Q0	Output		
19	GND	Power		Ground supply voltage (0V). Connect to board GND.
20	SEL0	Input	Pulldown	Function select control input. LVCMOS 3.3V interface. See Table 3B for function.
—	GND	Power		Exposed package ground supply voltage (GND). Connect to board GND.

NOTE: 1. *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			2		pF
R _{PULLUP}	Input Pullup Resistor			50		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			50		kΩ

Logic Truth Tables

Table 3A. Input Signal Source Select¹

REFSEL	Input Selection
0 (default)	LVC MOS input (CLK)
1	Differential input (IN, nIN)

NOTE: 1. Asynchronous control

Table 3B. Function Select¹

SEL0	SEL1	Q0	Q1
0 (default)	0 (default)	f_{CLK}	f_{CLK}
0	1	f_{CLK}	$f_{CLK} \div N$
1	0	$f_{CLK} \div N$	f_{CLK}
1	1	$f_{CLK} \div N$	$f_{CLK} \div N$

NOTE: 1. Asynchronous control. f_{CLK} is the selected input clock signal, N is the selected clock frequency divider.

Table 3C. Frequency Divider N Select¹

N1	N0	N Divider
0	0	$\div 2$
0	1	$\div 4$
1 (default)	0 (default)	$\div 5$
1	1	$\div 8$

NOTE: 1. Asynchronous control.

Table 3D. Output Q0 and Q1 Enable^{1 2}

nOE0, nOE1	Q0, Q1 State
0	Enabled
1 (default)	Disabled (output in logic low state)

NOTE: 1. Individual setting for each output Q0, Q1.

NOTE: 2. Synchronous to the clock signal to prevent runt pulses.
See [Figure 1](#)

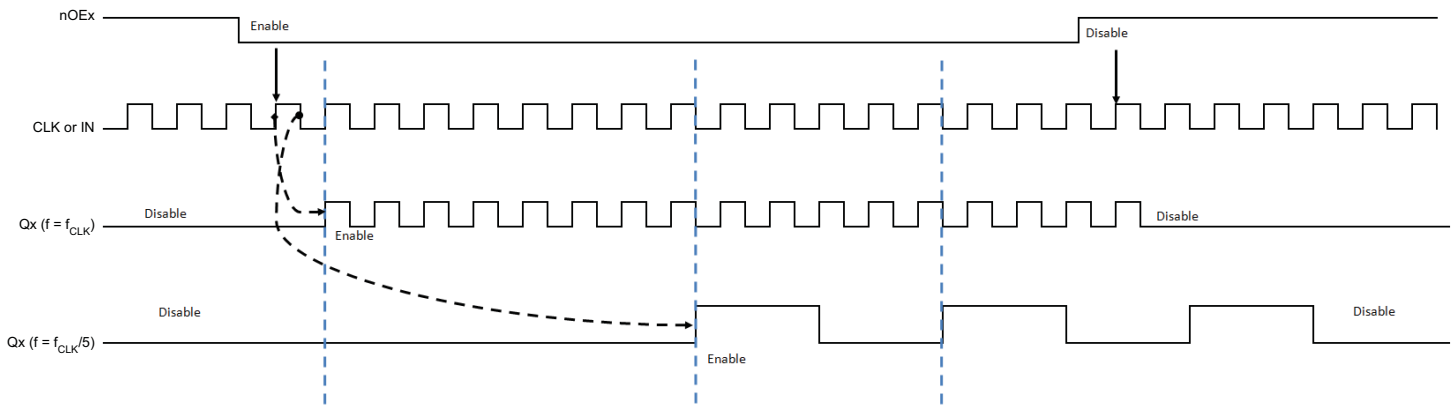


Figure 1. Synchronous Output Enable Timing Diagram

Table 3E. Synchronous Output Enable Timing

Divider	Max. Output Enable/Disable Delay (IN/ nIN or CLK to any Output), Measured in Number of Input Clock Pulses
pass-through	1
$\div 2$	4
$\div 4$	7
$\div 5$	9
$\div 8$	16

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVDS) Continuous Current Surge Current	10mA 15mA
Input Current I_{IN} , nIN	$\pm 50mA$
V_T Current (I_{VT})	$\pm 100mA$
Maximum Junction Temperature	125°C
Storage Temperature	-65°C to 125°C
ESD - Human Body Model ¹	2000V
ESD - Charged Device Model ¹	500V

NOTE: 1. According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Core Power Output Supply Current	All Outputs Terminated with 100Ω Between Qx and nQx		37	43	mA
I_{DDO}	Output Power Supply Current	All Outputs Terminated with 100Ω Between Qx and nQx		73	83	mA

Table 5B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	CLK, REFSEL, N0, SEL0, SEL1	$V_{DD} = V_{IN} = 3.465V$		150	μA
		N1, nOE0, nOE1	$V_{DD} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	CLK, REFSEL, N0, SEL0, SEL1	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		μA
		N1, nOE0, nOE1	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		μA

Table 5C. Differential Input DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance IN, nIN	IN to VT, nIN to VT		50		Ω
V_{CMR}	Common mode input voltage. ^{1, 2}		1		$V_{DD} - V_{PP}/2$	V
V_{PP}	Input Voltage Swing ²		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing IN, nIN		0.30			V
I_{IN}	Input Current IN, nIN				30	mA

NOTE: 1. V_{CMR} is defined as the signal crosspoint.

NOTE: 2. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{DD} .

Table 5D. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		460	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1		1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ ¹

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units	
f_{IN}	Input Frequency	IN, nIN		0		2000	MHz	
		CLK		0		250	MHz	
f_{OUT}	Output Frequency		SELn = 0	0		2000	MHz	
			SEL1 = 1, SEL0 = 1	0		$f_{IN} \div N$	MHz	
t_{PD}	Propagation Delay ^{2, 3}		SELn = 0 (pass-through)	300		550	ps	
			SEL1 = 1 and SEL0 = 1	N Divider = $\div 2, \div 4, \div 8$	450		760	ps
				N Divider = $\div 5$	550		900	ps
$t_{sk(o)}$	Output Skew ^{4, 5}					22	ps	
t_R / t_F	Output Rise/Fall Time	Q0, Q1	20% to 80%		145	260	ps	
	Output Isolation	Q0 to Q1 and Q1 to Q0	$f_{OUT} = 125MHz$ and $25MHz$		78		dBc	
	Input Mux Isolation		$f_{OUT} = 125MHz$		64		dBc	
$f_{jit(\emptyset)}$	RMS Additive Phase Jitter (Random)	Q0, Q1	$f_{OUT} = 125MHz$, Integration Range: 12kHz - 20MHz, SELn = 0		114	180	fs	
odc	Output Duty Cycle	Q0, Q1	50% Input Duty Cycle	45		55	%	

NOTE: 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

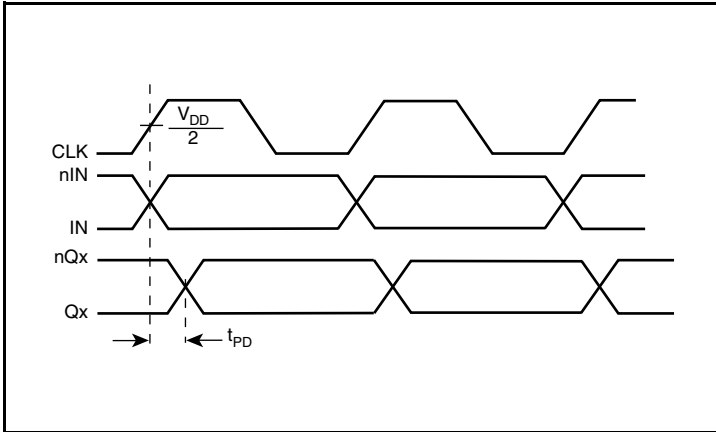
NOTE: 2. Measured from $V_{DD}/2$ of the input to the differential output crosspoint.

NOTE: 3. Measured from the differential input crossing point to the differential output crosspoint.

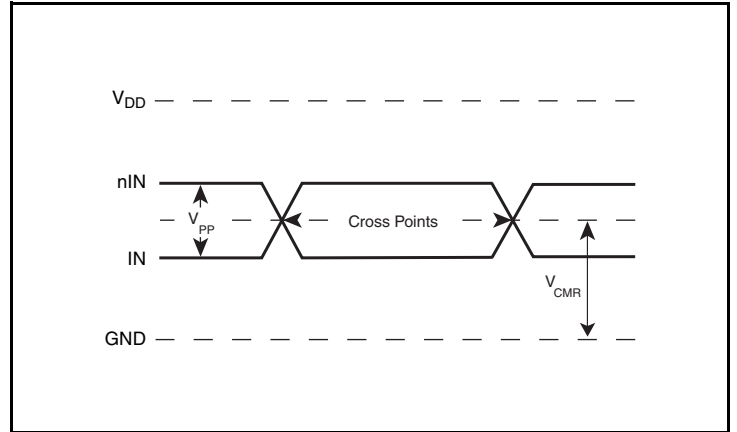
NOTE: 4. This parameter is defined in accordance with JEDEC standard 65.

NOTE: 5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

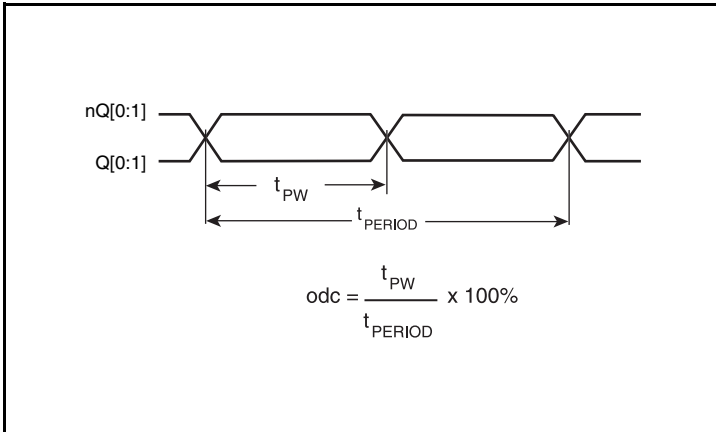
Parameter Measurement Information



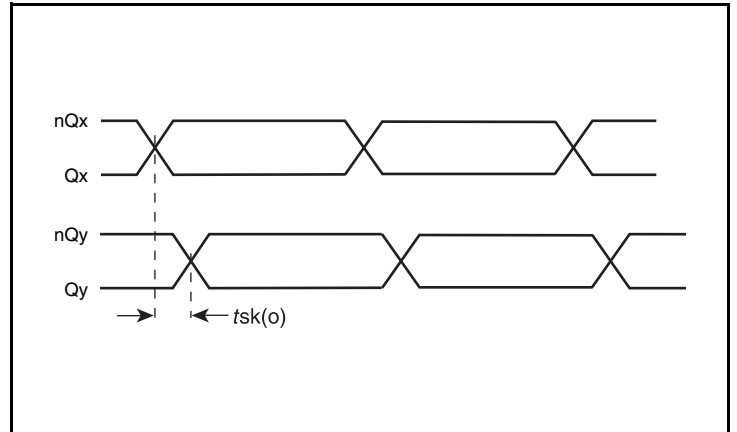
Propagation Delay



Differential Input Level

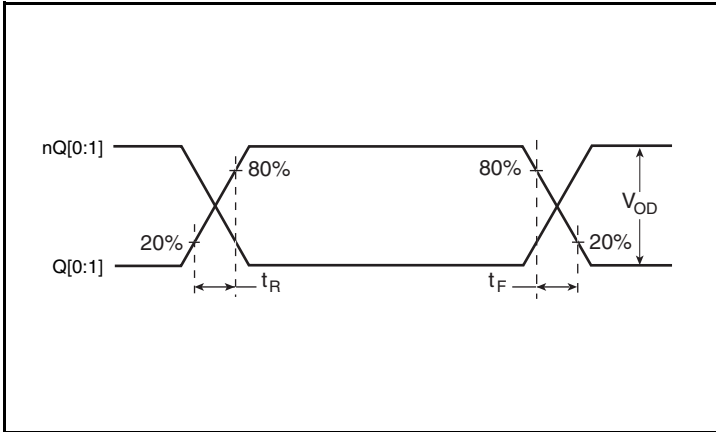


Output Duty Cycle/Pulse Width/Period

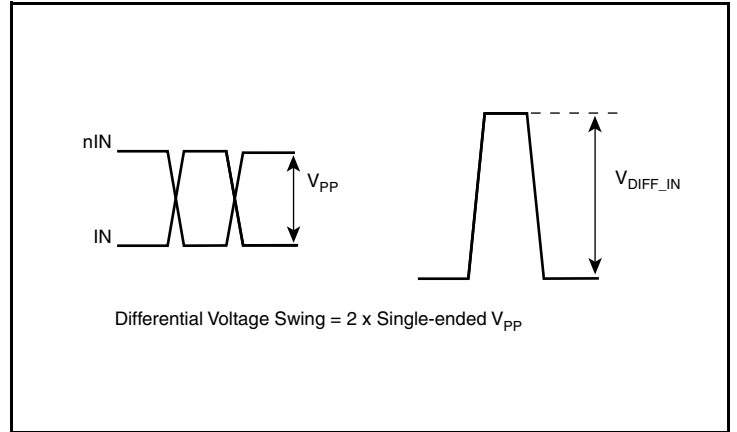


Output Skew

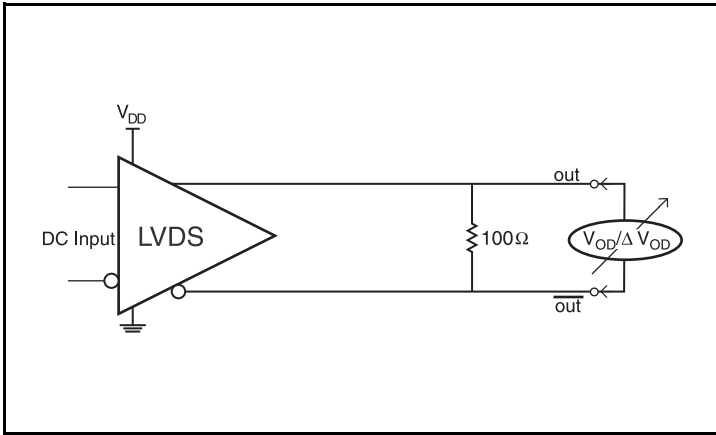
Parameter Measurement Information



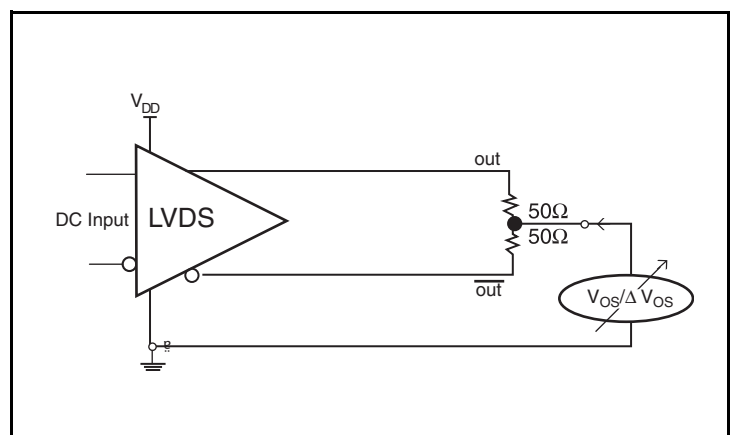
Output Rise/Fall Time



Differential Input Voltage Swing



Differential Output Voltage Setup



Offset Voltage

Applications Information

Differential Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A* to *Figure 2B* to show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces

suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

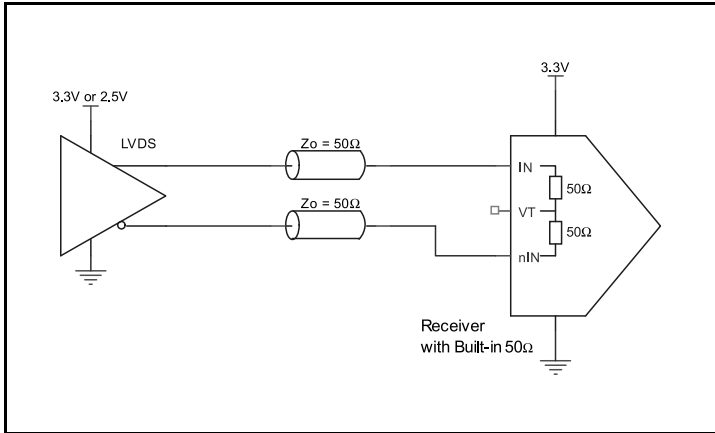


Figure 2A. IN/nIN Input with Built-In 50Ω driven by an LVDS Driver

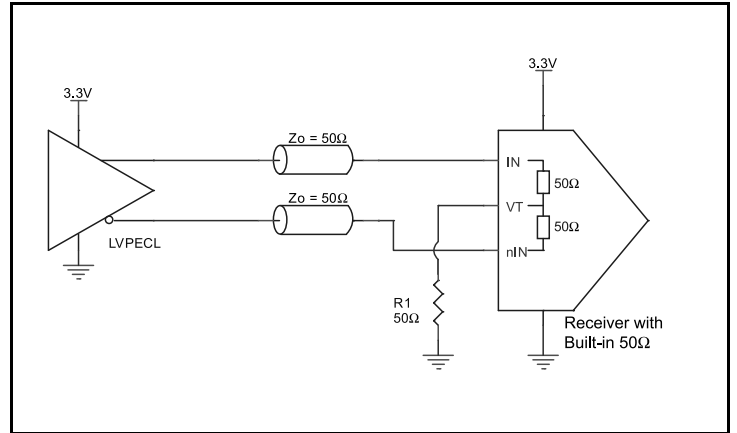


Figure 2B. IN/nIN Input with Built-In 50Ω driven by an LVPECL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

IN/nIN Inputs

For applications not requiring the use of a differential input, a 1kΩ resistor should tie IN to ground and a 1kΩ resistor should tie nIN to V_{CC} .

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.

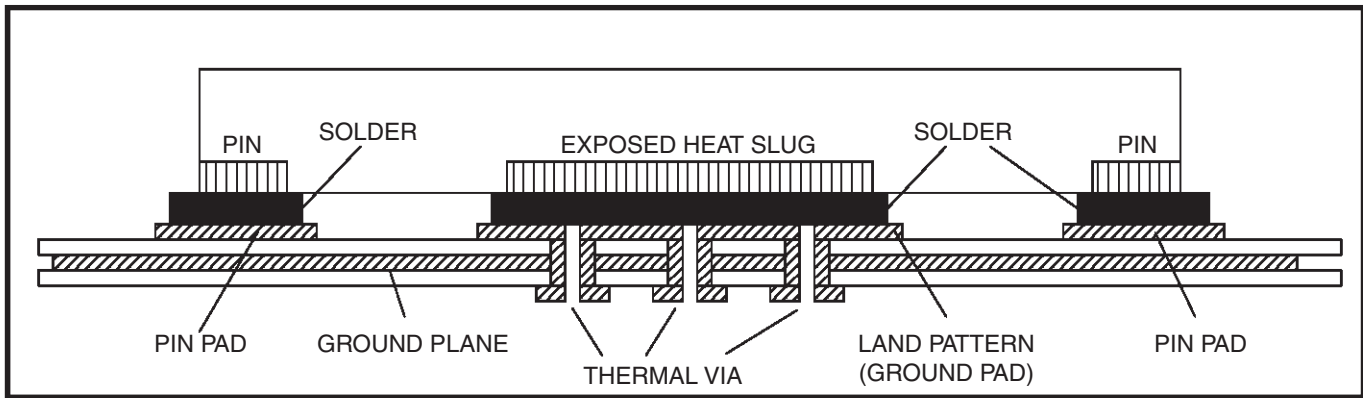


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in [Figure 4A](#) can be used with either

type of output structure. [Figure 4B](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

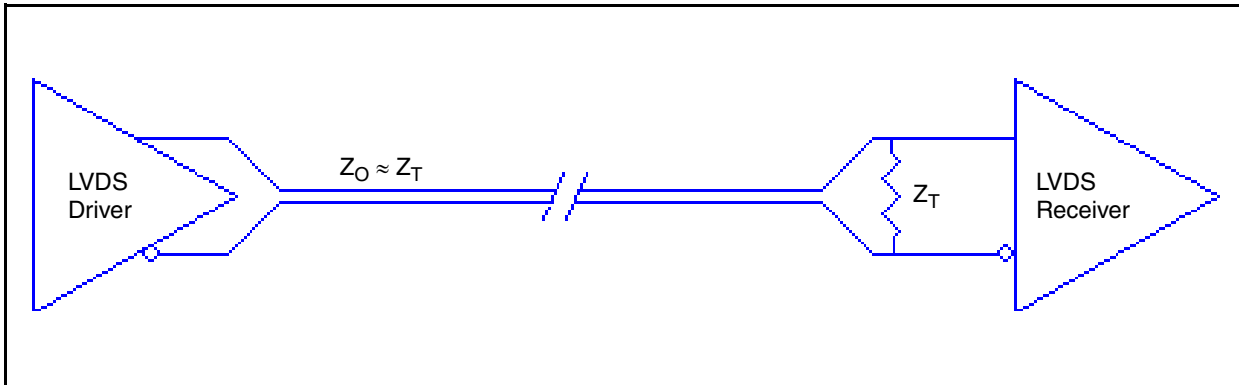


Figure 4A. Standard LVDS Termination

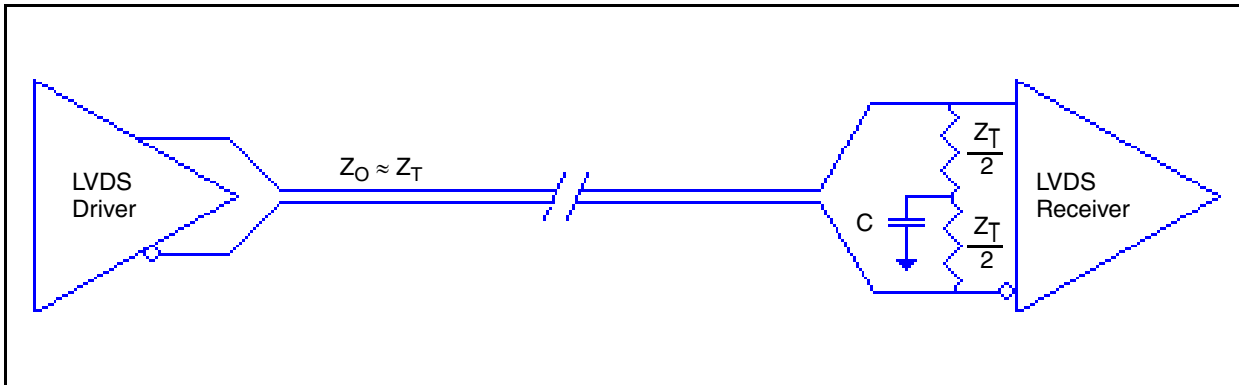


Figure 4B. Optional LVDS Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 8V74S4622. Equations and example calculations are also provided.

The following calculation is for maximum current at 85°C.

1. Power Dissipation.

The total power dissipation for the 8V74S4622 is the sum of the core power plus the power dissipated due to the load. The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 40.3mA = 139.6mW$
- Power (outputs)_{MAX} = $V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 78mA = 270.3mW$

Total Power_{MAX} = 139.6mW + 270.3mW = 409.9mW

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 62.2°C/W per [Table 7](#) below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85°C + 0.41W * 62.2°C/W = 110.5°C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20-Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

Reliability Information

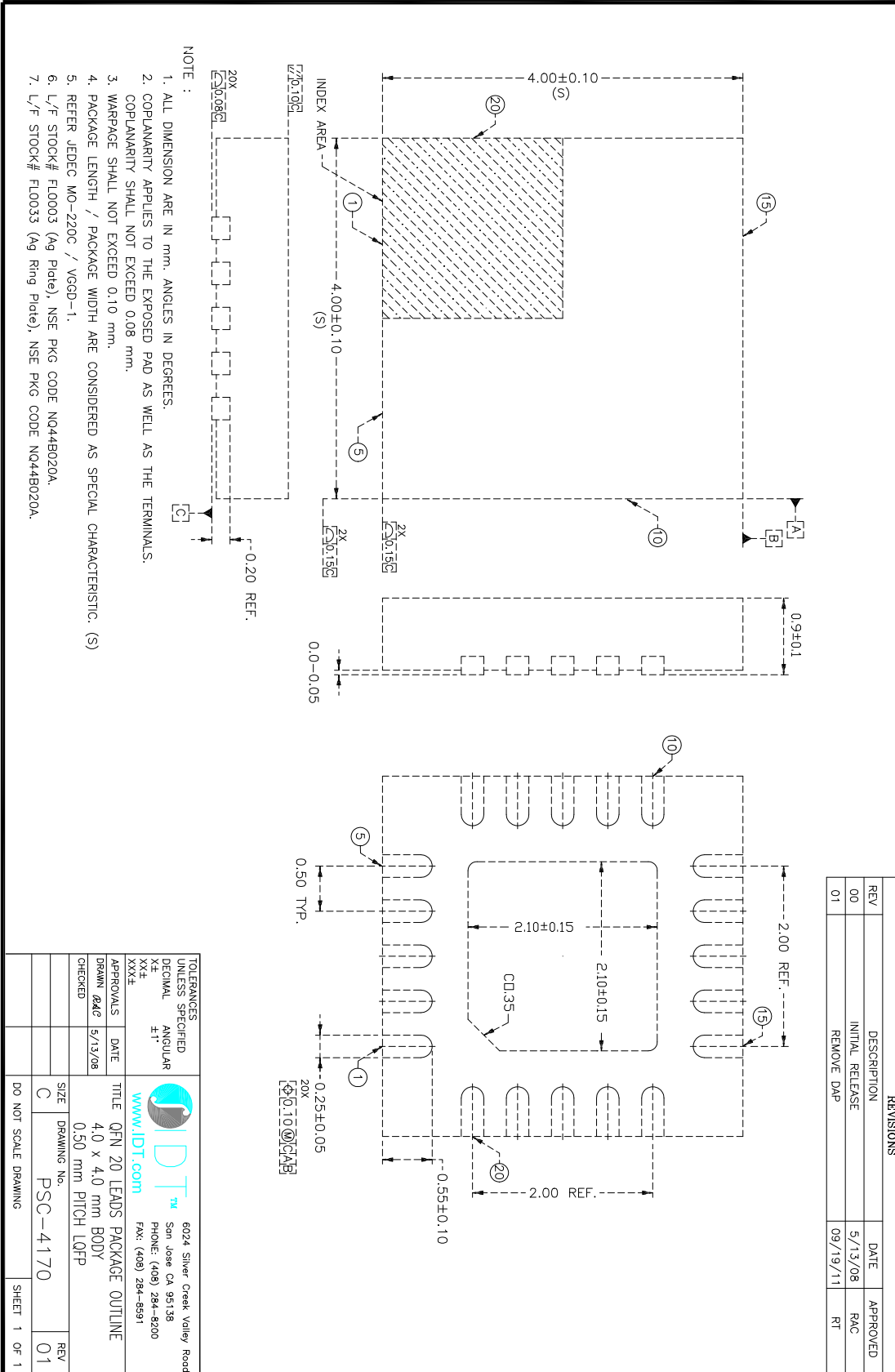
Table 8. θ_{JA} vs. Air Flow Table for a 20-lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

Transistor Count

The transistor count for 8V74S4622 is: 1723

20-Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V74S4622NLGI	8V74S4622NLGI	20-lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8V74S4622NLGI8	8V74S4622NLGI	20-lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C
8V74S4622NLGI/W	8V74S4622NLGI	20-lead VFQFN, Lead-Free	Tape & Reel, Pin 1 Orientation EIA-481-D	-40°C to 85°C

Table 10. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

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[PI6C10806BLEX](#) [ZL40226LDG1](#) [ZL40219LDG1](#) [8T73S208B-01NLGI](#) [SY75578LMG](#) [PI49FCT32805QEX](#) [PL133-27GC-R](#)
[MC10LVEP11DG](#) [MC10EP11DTG](#) [MC100LVEP11DG](#) [MC100E111FNG](#) [MC100EP11DTG](#) [NB6N11SMNG](#) [NB7L14MMNG](#)
[NB6L11MMNG](#) [NB6L14MMNR2G](#) [NB6L611MNG](#) [PL123-02NGI-R](#) [NB3N111KMNR4G](#) [ADCLK944BCPZ-R7](#) [ZL40217LDG1](#)
[NB7LQ572MNG](#) [HMC940LC4BTR](#) [ADCLK946BCPZ-REEL7](#) [ADCLK946BCPZ](#) [ADCLK846BCPZ-REEL7](#) [ADCLK854BCPZ-REEL7](#)
[ADCLK905BCPZ-R2](#)