Low EMI, Spread Modulating, Clock Generator

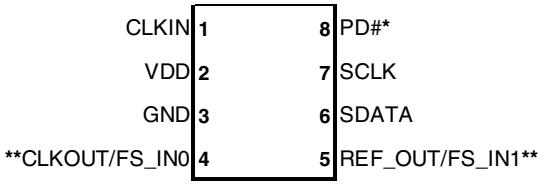
Features:

- ICS91718 is a Spread Spectrum Clock targeted for Mobile PC and LCD panel applications. Generates an EMI optimized clock signal (EMI peak reduction of 7-14 dB on 3rd-19th harmonics) through use of Spread Spectrum techniques.
- ICS91718 operates with input frequencies at 14.318 - 80 MHz.
- Spread modulation frequency range is 20kHz to 40kHz.
- Spread percentage/type programming through I^2C.

Specifications:

- Supply Voltages: V_{DD} = 3.3V ±0.3V
- Cyc to Cyc jitter: <150ps
- Output duty cycle 45/55%
- Guarantees +85°C operational condition
- 8-pin SOIC (150 mil) package

Pin Configuration



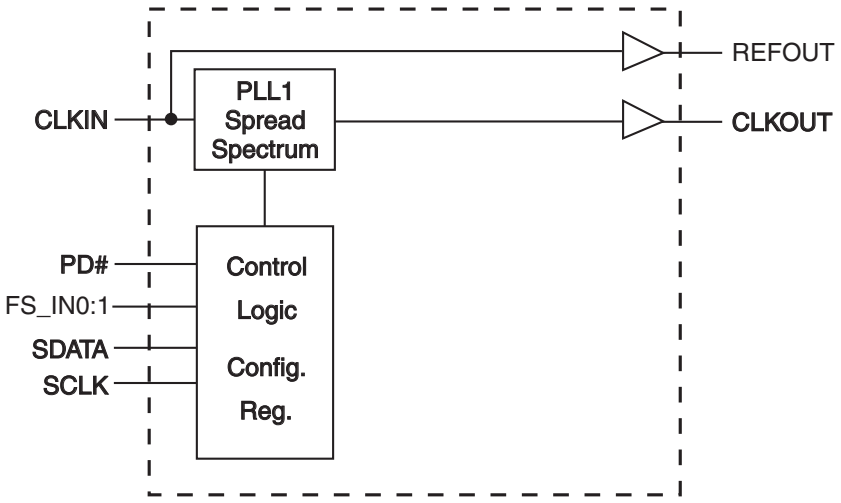
8-pin SOIC & TSSOP

Notes:
* Internal pull-up resistor
** Internal pull-down resistor

Input Select Functionality

FS_IN1	FS_IN0	MHz	SPREAD %
0	0	14.318 in 48.00 out	-1.0% down sprd
0	1	14.318 in 66.66 out	-1.0% down sprd
1	0	48.00 in/out 66.66 in/out	-1.0% down sprd
1	1	48.00 in/out 66.66 in/out	+/-1.0% center sprd

Block Diagram



Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	CLKIN	INPUT	Input clock
2	VDD	POWER	Power supply, nominal 3.3V
3	GND	POWER	Ground pin.
4	**CLKOUT/FS_IN0	I/O	CLKOUT modulated clock output FS_IN0 latched input, selects modulation percentage/type
5	REF_OUT/FS_IN1**	I/O	REF_OUT, unmodulated reference clock output FS_IN1 latched input, selects modulation percentage/type
6	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
7	SCLK	INPUT	Clock pin of I2C circuitry 5V tolerant
8	PD#*	INPUT	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Table 1: Frequency Configuration Table (See I2C Byte 0)

	FS4	FS3	FS2	FS1	FS0	Sprd Type	Sprd %
14in/48out	0	0	0	0	0	DOWN SPREAD (-)	0.80
	0	0	0	0	1		1.00
	0	0	0	1	0		1.25
	0	0	0	1	1		1.50
	0	0	1	0	0		1.75
	0	0	1	0	1		2.00
	0	0	1	1	0		2.50
	0	0	1	1	1	CENTER SPREAD (+/-)	0.60
	0	1	0	0	0		1.00
	0	1	0	0	1		1.25
	0	1	0	1	0		1.50
	0	1	0	1	1		2.00
14in/66out	0	1	1	0	0	DOWN SPREAD (-)	1.25
	0	1	1	0	1		1.00
	0	1	1	1	0		1.50
	0	1	1	1	1		2.00
48in/48out 66in/66out	1	0	0	0	0	DOWN SPREAD (-)	0.80
	1	0	0	0	1		1.00
	1	0	0	1	0		1.25
	1	0	0	1	1		1.50
	1	0	1	0	0		1.75
	1	0	1	0	1		2.00
	1	0	1	1	0		2.50
	1	0	1	1	1		3.00
	1	1	0	0	0	CENTER SPREAD (+/-)	0.30
	1	1	0	0	1		0.40
	1	1	0	1	0		0.50
	1	1	0	1	1		0.60
	1	1	1	0	0		0.80
	1	1	1	0	1		1.00
	1	1	1	1	0		1.25
	1	1	1	1	1		1.50

For 14.318 in 48.008 out default is…00001
For 14.318 in 66.66 out default is..01101
For 48/48 and 66/66 default is….10001

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D4(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D5(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

0500D—07/15/04

BYTE	Affected Pin			TYPE	Bit Control		
0	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	-	N/A	FS0	RW	See ROM TABLE		1
Bit 6	-	N/A	FS1	RW			0
Bit 5		N/A	FS2	RW			0
Bit 4		N/A	FS3	RW			0
Bit 3		N/A	FS4	RW			0
Bit 2		N/A	PD# Tri_Sate	RW	Hi-Z	LOW	1
Bit 1		N/A	Spread Enable	RW	OFF	ON	1
Bit 0		HW/SW Control	Spread Spectrum Control FS 2:4 Hard/Software Select	RW	HW	SW	0

BYTE	Affected Pin			TYPE	Bit Control		
1	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	5	REF_OUT	REF_OUT ENABLE	RW	Disable	Enable	1
Bit 6	5	REF_OUT	Slew Rate REF-OUT	RW	Nominal	Fast	1
Bit 5		FS_IN1 Readback	FS_IN1 Readback	RW	-	-	1
Bit 4		FS_IN0 Readback	FS_IN0 Readback	RW	-	-	1
Bit 3	4	CLK_OUT	Slew Rate CLK-OUT	RW	Nominal	Fast	1
Bit 2	4	CLK_OUT	CLK_OUT_Enable	RW	Disable	Enable	1
Bit 1		Reserved	Reserved	R	-	-	1
Bit 0		Reserved	Reserved	R	-	-	1

BYTE	Affected Pin			TYPE	Bit Control		
2	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	x	-	RESERVED	-	-	-	1
Bit 6	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 4	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 3	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	x	RESERVED	RESERVED	RW	Disable	Enable	1

BYTE	Affected Pin			TYPE	Bit Control		
3	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 6	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	X	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 4	X	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 3	x	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

BYTE	Affected Pin			TYPE	Bit Control		
4	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 6	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 4	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 3	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

BYTE	Affected Pin			TYPE	Bit Control		
5	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	-	-	-	1
Bit 6	X	RESERVED	RESERVED	-	-	-	1
Bit 5	X	RESERVED	RESERVED	-	-	-	1
Bit 4	X	RESERVED	RESERVED	-	-	-	1
Bit 3	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

BYTE	Affected Pin			TYPE	Bit Control		
6	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

BYTE	Affected Pin			TYPE	Bit Control		
7	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	DEVICE ID7	(Reserved)	R	-	-	0
Bit 6	X	DEVICE ID6	(Reserved)	R	-	-	0
Bit 5	X	DEVICE ID5	(Reserved)	R	-	-	0
Bit 4	X	DEVICE ID4	(Reserved)	R	-	-	0
Bit 3	X	DEVICE ID3	(Reserved)	R	-	-	0
Bit 2	X	DEVICE ID2	(Reserved)	R	-	-	0
Bit 1	X	DEVICE ID1	(Reserved)	R	-	-	0
Bit 0	X	DEVICE ID0	(Reserved)	R	-	-	1

BYTE	Affected Pin			TYPE	Bit Control		
8	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	Byte Count7	(Reserved)	R	-	-	0
Bit 6	X	Byte Count6	(Reserved)	R	-	-	0
Bit 5	X	Byte Count5	(Reserved)	R	-	-	0
Bit 4	X	Byte Count4	(Reserved)	R	-	-	0
Bit 3	X	Byte Count3	(Reserved)	R	-	-	0
Bit 2	X	Byte Count2	(Reserved)	R	-	-	1
Bit 1	X	Byte Count1	(Reserved)	R	-	-	1
Bit 0	X	Byte Count0	(Reserved)	R	-	-	1

Absolute Maximum Ratings

Supply Voltage . . . . . 3.7 V
Voltage on any pin with respect to GND . . . -0.5 to +3.7 V
Storage Temperature . . . . . –55°C to +125°C
Operating Temperature . . . . . 0°C to +85°C
Power Dissipation . . . . . 0.5 W

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	⍙A
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			⍙A
Supply Current	I_{DD}	f_{IN} = 14.318MHz		27	35	mA
		f_{IN} = 66.66MHz		42	50	mA
Powerdown Current	$I_{DD3.3PD}$			3	5	mA
Pin Inductance	L_{pin}				7	nH
Pin Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency		1	3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

AC Electrical Characteristics

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V ±0.3V

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
F_{IN}	Input Frequency	Input Clock	14.318		80	MHz
f_{OUT}	Output Frequency	Spread Off	14.318		80	MHz
t_R	Output Rise Time	15 pF load, 0.8V - 2.4V	0.5		1	ns
t_F	Output Fall Time	15 pF load, 2.4 - 0.8V	0.5		1	ns
I_{OD}	Output Duty Cycle	15 pf load	45		55	%
t_{ID}	Input Duty Cycle		45		55	%
t_{JCYC}	Jitter, Cycle-to-Cycle				250	ps

0500D—07/15/04

Electrical Characteristics - CLOCK_OUT

T_A = 0 - 85°C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			(
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	t_{r3}	V_{OL} = 0.41V, V_{OH} = 0.86V	0.5		1	ns
Fall Time	t_{f3}	V_{OH} = 0.86V V_{OL} = 0.41V	0.5		1	ns
Duty Cycle	d_{t3}	V_T = 50%	45	51	55	%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%			250	ps

[1]Guaranteed by design, not 100% tested in production.

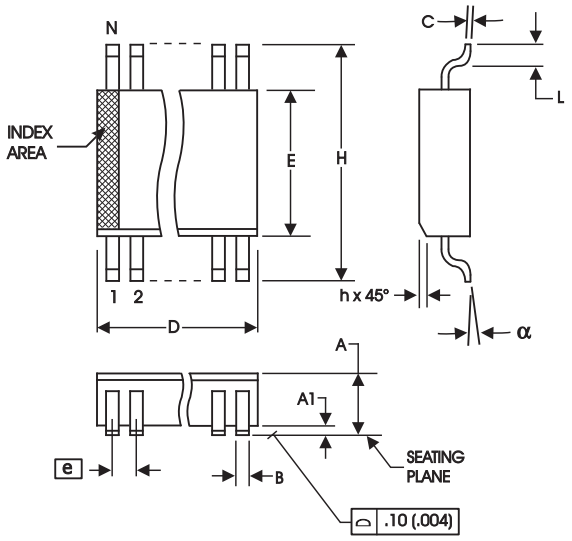
[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - REF

T_A = 0 - 85°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	20		60	∠
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Accumulated Jitter	$t_{jlongterm}$	V_T = 1.5 V 10us.			2	ns
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.



150mil Body, .50mil pitch

150 mil (Narrow Body) SOIC

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

Reference Doc.: JEDEC Publication 95, MS-012
10-0030

Ordering Information

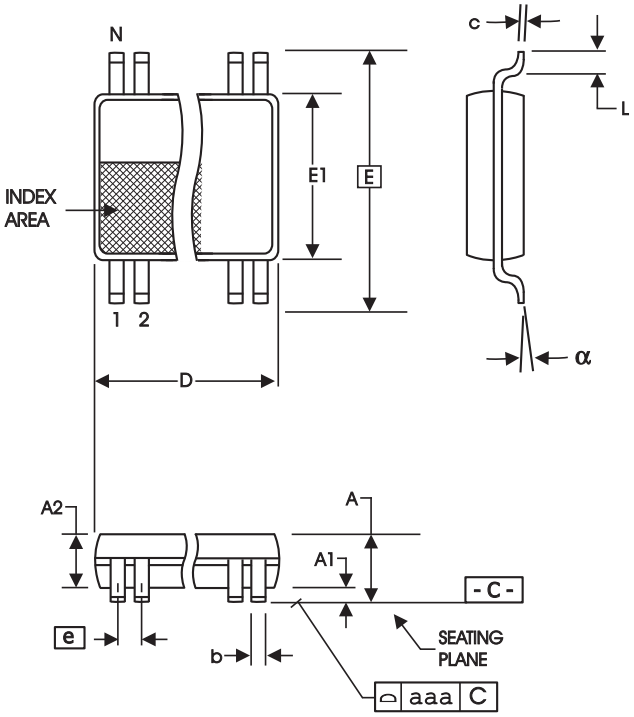
ICS91718yMLF-T

Example:

ICS XXXX y M LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  M = SOIC
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0500D—07/15/04



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	2.90	3.10	.114	.122

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

ICS91718yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0500D—07/15/04

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