

PCIE GEN 2/3 & QPI CLOCK FOR ROMLEY-BASED SERVERS

932SQ420D

General Description

The 932SQ420D is a main clock synthesizer for Romley-generation Intel based server platforms. The 932SQ420D is driven with a 25 MHz crystal for maximum performance. It generates CPU outputs of 100 or 133.33 MHz.

Recommended Application

CK420BQ

Output Features

- 4 HCSL CPU outputs
- 4 HCSL Non-Spread SAS/SRC outputs
- 3 HCSL SRC outputs
- 1 HCSL DOT96 output
- 1 3.3V 48M output
- 5 3.3V PCI outputs
- 1-3.3V REF output

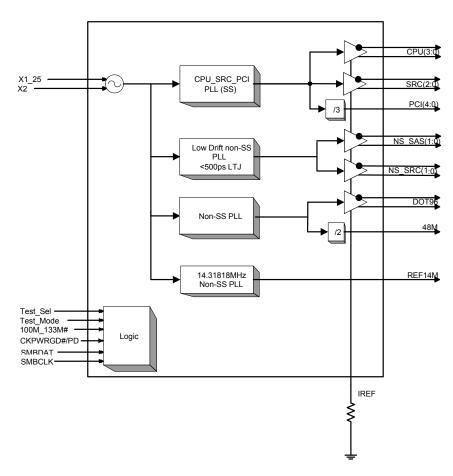
Features/Benefits

- 0.5% down spread capable on CPU/SRC/PCI outputs/Lower EMI
- 64-pin TSSOP and MLF packages/Space Savings

Key Specifications

- Cycle to cycle jitter: CPU/SRC/NS_SRC/NS_SAS < 50ps.
- Phase jitter: PCle Gen2 < 3ps rms, Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms
- Phase jitter: NS-SAS < 0.4ps rms using raw phase data
- Phase jitter: NS-SAS < 1.3ps rms using Clk Jit Tool 1.6.3

Block Diagram



Pin Configuration - 64TSSOP

SMBCLK GND14 AVDD14	2		63	SMBDAT VDDCPU CPU3T
VDD14	-			CPU3C
VREF14 3x/TEST SEL				CPU2T
GND14				CPU2C
GNDXTAL	-			GNDCPU
X1_25				VDDCPU
X2 25				CPU1T
VDDXTAL	10		55	CPU1C
GNDPCI	11		54	CPU0T
VDDPCI	12		53	CPU0C
PCI4_2x	13		52	GNDNS
PCI3_2x	14	0	51	AVDD_NS_SAS
PCI2_2x	15	5	50	NS_SAS1T
PCI1_2x	16	932SQ420	49	NS_SAS1C
PCI0_2x	17	S	48	NS_SAS0T
GNDPCI	-	32		NS_SAS0C
VDDPCI		6		GNDNS
VDD48	20		45	VDDNS
^48M_2x/100M_133M#	21		44	NS_SRC1T
GND48	22		43	NS_SRC1C
GND96	23			NS_SRC0T
DOT96T				NS_SRC0C
DOT96C				IREF
AVDD96				GNDSRC
TEST_MODE				AVDD_SRC
CKPWRGD#/PD				VDDSRC
VDDSRC				SRC2T
SRC0T				SRC2C
SRC0C				SRC1T
GNDSRC	32		33	SRC1C
		64-TSSOP		

Note: Pins with ^ prefix have internal 120K pullup Pins with v prefix have internal 120K pulldown

Spread Spectrum Control

SS_Enable	CPU, SRC &
(B1 b0)	PCI
0	OFF
1	ON

Power Group Pin Numbers

MLI	F	TSS	SOP	Description	
VDD	GND	VDD	GND	Description	
57	56	3	2	14MHz PLL Analog	
58	60	4	6	REF14M Output and Logic	
64	61	10	7	25MHz XTAL	
2,9	1,8	12, 19	11, 18	PCI Outputs and Logic	
10	12	20	22	48MHz Output and Logic	
16	13	26	23	96MHz PLL Analog, Output and Logic	
19, 27	22	29, 37	32	SRC Outputs and Logic	
28	29	38	39	SRC PLL Analog	
35	36	45	46	Non-Spreading Differential Outputs & Logic	
41	42	51	52	NS-SAS/SRC PLL Analog	
47, 53	48	57,63	58	CPU Outputs and Logic	

932SQ420 Power Down Functionality

CKPWRGD#/PD	Differential Outputs	Single-ended Outputs	Single ended Outputs w/Latch	
1	HI-Z ¹	Low	Low ²	
0		Running		

- 1. Hi-Z on the differential outputs will result in both True and Complement being low due to the termination network
- 2. These outputs are Hi-Z after VDD is applied and before the first assertion of CKPWRGD#.

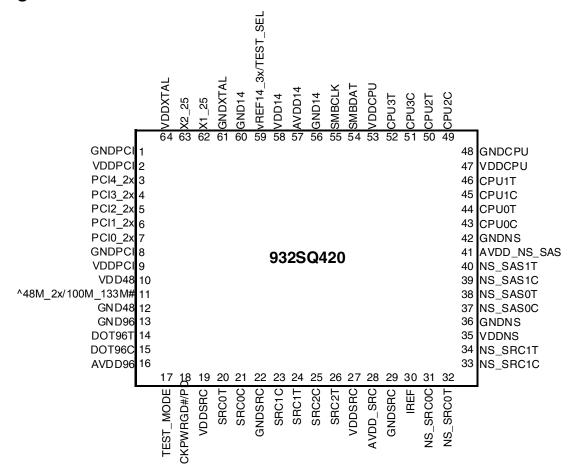
Pin Descriptions - 64 TSSOP

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PIN #	PIN NAME	TYPE	
1	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
2	GND14		Ground pin for 14MHz output and logic.
3	AVDD14		Analog power pin for 14MHz PLL
4	VDD14	PWR	Power pin for 14MHz output and logic
_	ADEE14 OW/TEST SEL	1/0	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode.
5	vREF14_3x/TEST_SEL	1/0	Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
6	GND14	PWR	Ground pin for 14MHz output and logic.
7	GNDXTAL		Ground pin for Crystal Oscillator.
8	X1_25		Crystal input, Nominally 25.00MHz.
9	X2 25		Crystal output, Nominally 25.00 MHz.
10	VDDXTAL		3.3V power for the crystal oscillator.
11	GNDPCI		Ground pin for PCI outputs and logic.
12	VDDPCI		3.3V power for the PCI outputs and logic
13	PCI4_2x		3.3V PCI clock output
14	PCI3 2x		3.3V PCI clock output
15	PCI2_2x		3.3V PCI clock output
16	PCI1_2x		3.3V PCI clock output
_			
17	PCI0_2x		3.3V PCI clock output
18	GNDPCI		Ground pin for PCI outputs and logic.
19	VDDPCI		3.3V power for the PCI outputs and logic
20	VDD48	PWR	3.3V power for the 48MHz output and logic
			3.3V 48MHz output/ 3.3V tolerant CPU frequency select latched input pin. See ViIFS and VihFS values for
21	^48M_2x/100M_133M#	I/O	thresholds. This pin has a weak (~120Kom) internal pull up.
			1 = 100MHz, 0 = 133MHz operating frequency
22	GN D48		Ground pin for 48MHz output and logic.
23	GN D96	PWR	Ground pin for DOT96 output and logic.
24	DOT96T	OUT	True clock of differential 96MHz output. These are current mode outputs. These are current mode outputs
24	DO 1961	001	and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
0.5	DOTOGO	OUT	Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm
25	DOT96C	001	series resistors and 49.9 ohm shunt resistors are required for termination.
26	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
07	TEST MODE		TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to
27	TEST_MODE	IN	Test Clarification Table.
			CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an
28	CKPWRGD#/PD	IN	asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs
			are stopped.
29	VDDSRC	PWR	3.3V power for the SRC outputs and logic
	12233		
30	SRC0T	OUT	True clock of differential SRC output. These are current mode outputs. These are current mode outputs and
50	3.1001	~ .	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
 			Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm
31	SRC0C	OUT	
32	GNDSRC	DWD	series resistors and 49.9 ohm shunt resistors are required for termination. Ground pin for SRC outputs and logic.
32	GNUONU		Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm
33	SRC1C	OUT	
			series resistors and 49.9 ohm shunt resistors are required for termination.
			True clock of differential SRC output. These are current mode outputs. These are current mode outputs and
34	SRC1T	OUT	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
			· ·
35	SRC2C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm
	0.1020	00.	series resistors and 49.9 ohm shunt resistors are required for termination.
			True clock of differential SRC output. These are current mode outputs. These are current mode outputs and
36	SRC2T	OUT	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
			· ·
37	VDDSRC	PWR	3.3V power for the SRC outputs and logic
38	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
39	GNDSRC		Ground pin for SRC outputs and logic.
			This pin establishes the reference current for the differential current-mode output pairs. This pin requires a
40	IREF	OUT	fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard
			value.
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Pin Descriptions - 64 TSSOP(cont.)

NS_SRCOC		•		
NS_SRCIC OUT Complementary clock of differential onn-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VDDNS PWR 3.3V power for the Non-Spreading GRC output. These are current mode outputs and external 30 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VDDNS PWR 3.3V power for the Non-Spreading GRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VDDNS PWR Ground pin for non-spreading differential outputs and logic. OUT Complementary clock of differential on-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VS_SASOT OUT True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VS_SAS1T OUT True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VS_SAS1T OUT True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VS_CANDNS PWR Ground pin for non-spreading SAS/SRC PLL analog circuits. CPU0C OUT True clock of differential clouptuts and device termination. VPWR Ground pin for non-spreading differential outputs and device termination. VPWR Ground pin for non-spreading differential outputs and device termination. VPWR Ground pin for Pun spreading SAS/SRC PLL analog circuits. CPU1C OUT True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. VPWR Ground pin for CPU outputs and logic. CPU2C OU	41	NS_SRC0C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
NS_SECT OUT 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.	42	NS_SRC0T	OUT	,
NS_SRUT WODNS PWR 3.3V power for the Non-Spreading differential outputs outputs and logic GNDNS PWR Ground pin for non-spreading differential outputs outputs and logic NS_SASOC OUT Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. OUT Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. CPU0T OUT True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. CPU2T OUT True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. CPU2T OUT	43	NS_SRC1C	OUT	
AVECUATE	44	NS_SRC1T	ОПТ	
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CPU3T OUT True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. PWR 3.3V power for the CPU outputs and logic	52 53 54 55 56 57 58 59	GNDNS CPU0C CPU0T CPU1C CPU1T VDDCPU GNDCPU CPU2C	PWR OUT OUT OUT PWR PWR OUT	Ground pin for non-spreading differential outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 3.3V power for the CPU outputs and logic Ground pin for CPU outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
63 VDDCPU PWR 3.3V power for the CPU outputs and logic	52 53 54 55 56 57 58 59 60	GNDNS CPU0C CPU0T CPU1C CPU1T VDDCPU GNDCPU CPU2C CPU2T	PWR OUT OUT OUT PWR PWR OUT OUT	Ground pin for non-spreading differential outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 3.3V power for the CPU outputs and logic. Ground pin for CPU outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
	52 53 54 55 56 57 58 59 60	GNDNS CPU0C CPU0T CPU1C CPU1T VDDCPU GNDCPU CPU2C CPU2T CPU3C	PWR OUT OUT OUT PWR PWR OUT OUT OUT	Ground pin for non-spreading differential outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 3.3V power for the CPU outputs and logic. Ground pin for CPU outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors are required for termination.
	52 53 54 55 56 57 58 59 60 61	GNDNS CPU0C CPU0T CPU1C CPU1T VDDCPU GNDCPU CPU2C CPU2T CPU3C CPU3T	PWR OUT OUT OUT PWR PWR OUT OUT OUT OUT	Ground pin for non-spreading differential outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 3.3V power for the CPU outputs and logic. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.

Pin Configuration - 64 MLF



Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldowm

Pin Descriptions - 64 MLF

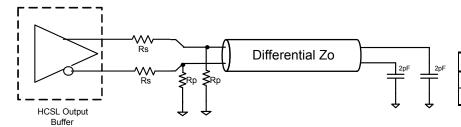
1 GNDPCI PWR Ground pin for PCI outputs and logic. 2 VDDPCI PWR 3.3V power for the PCI outputs and logic. 3 PCI4_2X OUT 3.3V PCI clock output 4 PCI3_2X OUT 3.3V PCI clock output 5 PCI2_2X OUT 3.3V PCI clock output 6 PCI1_2X OUT 3.3V PCI clock output 7 PCI0_2X OUT 3.3V PCI clock output 8 GNDPCI PWR Ground pin for PCI outputs and logic. 9 VDDPCI PWR Ground pin for PCI outputs and logic. 10 VDDP4 PWR 3.3V power for the PCI outputs and logic. 11 *48M_2X/100M_133M# PWR Ground pin for PCI outputs and logic. 12 GND48 PWR Ground pin for 48MHz output and logic. 13 GND96 PWR Ground pin for 48MHz output and logic. 14 DOT96T OUT Ground pin for 48MHz output and logic. 15 DOT96C OUT Ground pin for 48MHz output and logic. 16 AVDD96 PWR Ground pin for DOT96 output and logic. 17 Tue clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 16 AVDD96 PWR 3.3V power for the 48/96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 17 TEST_MODE NWR 3.3V power for the 48/96MHz putput. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 18 CKPWRGD#/PD NWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic. 20 SRC0T OUT True clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors are required for termination. 21 SRC0C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors are required for termination. 22 GNDSRC PWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic. 23 SRC1C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors are required for termination. 24 SRC1C OUT Ground PWR 3.9 power for the 88/96 output and logic. 35 COUTPIEMENT SWR 35 PWR 35	PIN #	PIN NAME	TYPE	DESCRIPTION
2 VDDPCI PWR 13.3 V power for the PCI outputs and logic 3 PCId 2x OUT 3.3 V PCI dock output 4 PCIG 2x OUT 3.3 V PCI dock output 5 PCIG 2x OUT 3.3 V PCI dock output 6 PCII 2x OUT 3.3 V PCI dock output 7 PCIG 2x OUT 3.3 V PCI dock output 8 GNDPCI PWR IG mound pin for PCI outputs and logic 9 VDDPCI PWR IG mound pin for PCI outputs and logic 10 VDD48 PWR IS 33V power for the 48MHz output and logic 11 ^448M_2x/100M_133MWF I/O (15 PWR IS 34V power for the 74MHz output and logic 13 GND96 PWR IS 33V power for the 48MHz output and logic 14 ODT96T OUT Intercholds. This pin has a weak (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon PWR IS OUT 1-1 COMPAN (-120Kom) internal pull up. 1-1 colon of differential SPC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shurt resistors are required for termination. 1-1 COMPAN (-120Kom) internal pu				
PCI3 2x				
4 PCI3 2x OUT 33 VP CI clock output 5 PCI2 2x OUT 33 VP CI clock output 6 PCI1 2x OUT 33 VP CI clock output 7 PCI0 2x OUT 33 VP CI clock output 8 GNDPCI PWR Ground pin for PCI outputs and logic 9 VDDPCI PWR 33 VP ower for the PCI outputs and logic 10 VDD48 PWR 33 VP ower for the PCI outputs and logic 11 A4M_2x100M_133M# PCI 33MHz output 33 VI obterant CPU frequency select latched input pin. See VIFS and VihFS values for thresholds. This pin has a weak (~120Kcm) internal pull up. 11 A4M_2x100M_133M# PWR Ground pin for PCID outputs and logic 12 GND48 PWR Ground pin for 48MHz output and logic. 13 VAND96 PWR Ground pin for 48MHz output and logic. 14 DOT96T OUT True clock of differential 98MHz output and logic. 15 DOT96C OUT Complementary clock of differential 98MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49 9 ohm shurt resistors are required for termination. 16 AVDD96 PWR 33 VP ower for the 4898MHz PLL and the 98MHz output and logic. 17 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 18 CKPWRGD#/PD IN SAMP OUTPUT AND SEE A REAL PROPERTIES AND SEE A REAL PROPE				· · ·
5 PCIZ 2X OUT 3.3 VPCI clock output 6 PCID 2X OUT 3.3 VPCI clock output 7 PCID 2X OUT 3.3 VPCI clock output 8 RONDPCI PWB Ground pin for PCI outputs and logic. 9 VDDPCI PWB Ground pin for PCI outputs and logic. 10 VDD48 PWB 3.3 VPC pweer for the 48MHz output and logic. 11 48M_2x/100M_133Mf PWB 3.3 VPC pweer for the 48MHz output and logic. 12 ROND48 PWB 3.3 VPC pweer for the 48MHz output and logic. 13 ROND48 PWB 3.3 VPC pweer for the 48MHz output and logic. 14 DOT96T PWB 1.5 SW pweer for the 48MHz output and logic. 15 ROND48 PWB 6 ROUND pin for 48MHz output and logic. 16 ROND48 PWB 6 ROUND pin for 48MHz output and logic. 17 ROND48 PWB 6 ROUND pin for 48MHz output and logic. 18 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 19 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 19 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 10 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 10 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 10 ROND96 PWB 6 ROUND pin for 48MHz output and logic. 11 ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of romination. 12 ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of romination. 13 ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of romination. 14 ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of ROND96 PWB 3.3 VPC pweer for the 489MHz PLL and the 98MHz output and logic of ROND96 PWB 3.3 VPC pweer for the 58C output sand logic of ROND96 PWB 3.3 VPC pweer for the 58C output sand logic of ROND96 PWB 3.3 VPC pweer for the 58C output sand logic of ROND96 PWB 3.3 VPC pweer for the 58C output sand logic. 18 ROCC OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 o				·
6 PCIL 2x OUT 33 VP CI clock output 7 PCIO 2x OUT 33 VP CI clock output 8 GNDPCI PWB Ground pin for PCI outputs and logic 9 VDDPCI PWB 33 Vp ower for the PCI outputs and logic 10 VDD48 PWB 33 Vp ower for the PCI outputs and logic 11 \(^{48M}_{-2}Z/100M_{-133MW}\) 11 \(^{48M}_{-2}Z/100M_{-133MW}\) 12 \(^{48M}_{-2}Z/100M_{-133MW}\) 12 \(^{48M}_{-2}Z/100M_{-133MW}\) 13 \(^{48M}_{-2}Z/100M_{-133MW}\) 14 \(^{48M}_{-2}Z/100M_{-133MW}\) 15 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 17 \(^{48M}_{-2}Z/100M_{-133WW}\) 18 \(^{48M}_{-2}Z/100M_{-133WW}\) 19 \(^{48M}_{-2}Z/100M_{-133WW}\) 19 \(^{48M}_{-2}Z/100M_{-133WW}\) 19 \(^{48M}_{-2}Z/100M_{-133WW}\) 10 \(^{48M}_{-2}Z/100M_{-133WW}\) 11 \(^{48M}_{-2}Z/100M_{-133WW}\) 12 \(^{48M}_{-2}Z/100M_{-133WW}\) 12 \(^{48M}_{-2}Z/100M_{-133WW}\) 13 \(^{48M}_{-2}Z/100M_{-133WW}\) 14 \(^{48M}_{-2}Z/100M_{-133WW}\) 15 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 16 \(^{48M}_{-2}Z/100M_{-133WW}\) 17 \(^{48M}_{-2}Z/10M_{-133WW}\) 18 \(^{48M}_{-2}Z/10M_{-133WW}\) 18 \(^{48M}_{-2}Z/10M_{-133WW}\) 19 \(^{48M}_{-2}Z/10M_{-133WW}\) 19 \(^{48M}_{-2}Z/10M_{-133WW}\) 19 \(^{48M}_{-2}Z/10M_{-133WW}\) 10 \(^{48M}_{-2}Z/10M_{-133WW}\) 10 \(^{48M}_{-2}Z/10M_{-133WW}\) 10 \(^{48M}_{-2}Z/10M_{-133WW}\) 10 \(^{48M}_{-2}Z/10M_{-133WW}\) 11 \(^{48M}_{-2}Z/10M_{-133WW}\) 12 \(^{48M}_{-2}Z/10M_{-133WW}\) 13 \(^{48M}_{-2}Z/10M_{-133WW}\) 14 \(^{48M}_{-2}Z/10M_{-133WW}\) 15 \(^{48M}_{-2}Z/10M_{-133WW}\) 16 \(^{48M}_{-2}Z/10M_{-133WW}\) 16 \(^{48M}_{-2}Z/10M_{-133WW}\) 17 \(^{48M}_{-2}Z/10M_{-133WW}\) 18 \(^{48M}_{-2}Z/10M_{-133WW}\) 18 \(^{48M}_{-2}Z/10M_{-133WW}\) 18 \(^{48M}_{-2}Z/10M_{-133WW}\) 1		_		
7 PCIO.2x OUT 33V PCI dock output 8 RONDPCI PWR Ground pin for PCI outputs and logic. 9 VDDPCI PWR Ground pin for PCI outputs and logic. 10 VDDPCI PWR 33V power for the ARMHZ output and logic. 11 *48M_2x/100M_133M# Up				
8 (ANDPCI PWR 3.3V power for the PCI outputs and logic PWR 3.3V power for the PCI outputs and logic PWR 3.3V power for the PCI output and logic 3.3V power for the PCI output and logic 3.3V power for the PCI output and logic 3.3V power for the 48MHz output 3.3V power for the 48MPX output 3.3V power for the 58KC output 3.3V power		_		
9 VDDPCI PWR 3.3V power for the PCI outputs and logic	7			
NDD48	8			
33.7 48MHz output 3.3V blerant CPU frequency select latched input pin. See VIFS and VihFS values for I/O Meshodos. This pin has a weak (1-120Kom) internal pull up. 12 GND48 PWR Ground pin for 48MHz output and logic. 13 GND96 PWR Ground pin for 48MHz output and logic. 14 DOT96T OUT True clock of differential 95MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 4.99 ohm shunt resistors are required for termination. 15 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 4.99 ohm shunt resistors are required for termination. 16 AVDD96 PVR 3.3V power for the 4896MHz PLL and the 96MHz output and logic. 17 TEST_MODE IN TEST_MODE IN TEST_MODE is a real time input to select between 14½ and REF/N divider mode while in test mode. Refer to Test Clarification Table. 18 CKPWRGD#/PD IN Say power for the 4896MHz PLL and the 96MHz output and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are stopped. 20 SRC0T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. 21 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. 22 GNDSRC PWR Ground pin for SRC outputs and logic. 23 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. 24 SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. 25 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 3	9	VDDPCI		
ASM_2x/100M_133M# I/O	10	VDD48	PWR	
1				3.3V 48MHz output/ 3.3V tolerant CPU frequency select latched input pin. See VilFS and VihFS values for
AND AND PWR Ground pin for 48MHz output and logic.	11	^48M_2x/100M_133M#	I/O	thresholds. This pin has a weak (~120Kom) internal pull up.
AND AND PWR Ground pin for 48MHz output and logic.				1 = 100MHz, 0 = 133MHz operating frequency
AND	12	GND48	PWR	
True clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. TEST_MODE Note: Test_Mo	13			
DOT96C				
DOT96C	14	DOT96T	OUT	· · · · · · · · · · · · · · · · · · ·
AVDD96				
AVDD96	15	DOT96C	OUT	i i i i i i i i i i i i i i i i i i i
IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. CKPWRGD#/PD IN an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are stopped. PWR 3.3V power for the SRC outputs and logic True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential SRC output. These are current mode outputs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.	16	AVDDOG	DWD	
18 CKPWRGD#/PD 18 CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL: are stopped. 19 VDDSRC 20 SRCOT 20 True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 21 SRCOC 22 GNDSRC 23 SRC1C 24 SRC1C 25 SRC1C 26 OUT 27 Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 24 SRC1T 25 SRC2C 26 OUT 27 Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm serie resistors and 49.9 ohm shunt resistors are required for termination. 26 SRC2C 27 COUT 28 SRC2C 39 COUT 30 True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27 VDDSRC 48 AVDD SRC 49 VR 3.3V power for the SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 38 AVDD SRC 59 VR Ground pin for SRC outputs and logic. 39 IREF 40 OUT 40 Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 30 IREF 50 COUT 50 COMPLEMENT AND	10	AADD90	FVVN	
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External 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27	-00	CDCOT	OUT	True clock of differential SRC output. These are current mode outputs. These are current mode outputs and
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AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits PWR Ground pin for SRC outputs and logic. This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs and externa 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. OUT True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and externa 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. NS_SRC1C OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs and externa 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SRC output. These are current mode outputs and externa 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SRC output. These are current mode outputs and externa 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SRC output. These are current mode outputs. These are current	27	VDDSRC	PWR	
GNDSRC PWR Ground pin for SRC outputs and logic. This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs and externation. NS_SRCOT OUT True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and externation and eventual standard value. OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and externation and eventual standard value. OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs and externation and eventual standard value. OUT Complementary clock of differential non-spreading SRC output. These are current mode outputs and externation. True clock of differential non-spreading SRC output. These are current mode outputs and externation. True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs. These are current mode outputs and externation.	28	AVDD SRC		
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32 NS_SRC01 33 NS_SRC1C OUT mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SRC output. These are current mode outputs. These are current				SO OHIT SELECTESISIONS AND 49.9 OHIT STUTIL RESISIONS ARE REQUIRED TO LEMBER 1011.
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33 NS_SRC1C OUI 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential non-spreading SRC output. These are current mode outputs. These are current	-			
True clock of differential non-spreading SRC output. These are current mode outputs. These are current	33	NS SRC1C	OUT	, , , , , , , , , , , , , , , , , , ,
34 INS SECTION 1 OUT 1				33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
34 INS SECTION 1 OUT 1				True clock of differential non-spreading SRC output. These are current mode outputs. These are current
mode supule and strend of shirt sorted to store and 40.0 shirt share required for termination	34	NS_SRC1T	OUT	i i i i i i i i i i i i i i i i i i i
				Store and Store

Pin Descriptions - 64 MLF (cont).

35	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
36	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
37	NS_SAS0C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external
37	N3_3A30C	001	33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
38	NS_SAS0T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
39	NS_SAS1C	OUT	Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
40	NS_SAS1T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
41	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
	GNDNS		Ground pin for non-spreading differential outputs and logic.
	CPU0C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
44	СРU0Т	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
45	CPU1C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
46	CPU1T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
47	VDDCPU	PWR	3.3V power for the CPU outputs and logic
48	GNDCPU	PWR	Ground pin for CPU outputs and logic.
49	CPU2C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series
	01 020	001	resistors and 49.9 ohm shunt resistors are required for termination.
50	CPU2T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
51	CPU3C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
52	СРИЗТ	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
53	VDDCPU	PWR	3.3V power for the CPU outputs and logic
	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
	GND14		Ground pin for 14MHz output and logic.
	AVDD14		Analog power pin for 14MHz PLL
58	VDD14	PWR	Power pin for 14MHz output and logic
59	vREF14_3x/TEST_SEL	I/O	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
60	GND14		Ground pin for 14MHz output and logic.
61	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
	X1_25		Crystal input, Nominally 25.00MHz.
	X2_25		Crystal output, Nominally 25.00MHz.
64	VDDXTAL	PWR	3.3V power for the crystal oscillator.

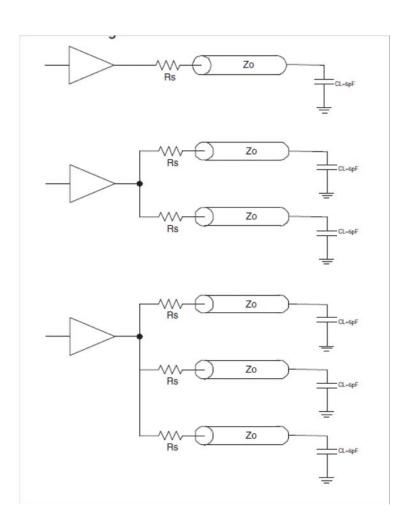
Test Loads and Recommended Terminations

932SQ420 Differential Test Loads



Differential Output Termination Table

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.3 or 43.2



Single-ended Output Termination Table

		Rs Value (for each load			
Output	Loads	ads $Zo = 50\Omega$ $Zo = 60\Omega$			
PCI/USB	1	36 43			
PCI/USB	2	22 33			
REF	1	39	47		
REF	2	27 36			
REF	3	10 20			

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	٧	1,2
Input Low Voltage	V_{IL}		GND-0.5			٧	1
Input High Voltage	V_{IH}	Except for SMBus interface			V _{DD} +0.5V	٧	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	٧	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Case Temperature	Тс				110	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

DC Electrical Characteristics - Differential Current Mode Outputs

 $T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1	2.4	4	V/ns	1, 2, 3
Slew rate matching	∆dV/dt	Slew rate matching, Scope averaging on		9	20	%	1, 2, 4
Rise/Fall Time Matching	∆Trf	Rise/fall matching, Scope averaging off			125	ps	1, 8, 9
Voltage High	VHigh	Statistical measurement on single-ended signal using	660	772	850	mV	1
Voltage Low	VLow	oscilloscope math function. (Scope averaging on)	-150	9	150] ""	1
Max Voltage	Vmax	Measurement on single ended		810	1150	mV	1, 7
Min Voltage	Vmin	signal using absolute value.	-300	-17		IIIV	1, 7
Vswing	Vswing	Scope averaging off	300	1446		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	351	550	mV	1, 5
Crossing Voltage (var)	∆-Vcross	Scope averaging off		24	140	mV	1, 6

¹Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O =50Ω (100Ω differential impedance).

² Operation under these conditions is neither implied nor guaranteed.

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

⁷ Includes overshoot and undershoot.

⁸ Measured from single-ended waveform

⁹ Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics - Input/Supply/Common Parameters

 $TA = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T _{COM}	Commmercial range	0		70	ů	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri- level inputs	2		V _{DD} + 0.3	٧	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri- level inputs	GND - 0.3		0.8	٧	1
	I _{IN}	Single-ended inputs, $V_{IN} = GND$, $V_{IN} = VDD$	-5		5	uA	1
Input Current	I _{INP}	Single-ended inputs. V _{IN} = 0 V; Inputs with internal pullup resistors V _{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Low Threshold Input- High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V _{DD} + 0.3	V	1
Low Threshold Input- Low Voltage	V_{IL_FS}	3.3 V +/-5%	V _{SS} - 0.3		0.35	V	1
Input Frequency	Fi			25.00		MHz	2
Pin Inductance	L_pin				7	nΗ	1
	C_{IN}	Logic Inputs			5	pF	1
Capacitance	C _{out}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	рF	1
Clk Stabilization	T_{STAB}	From V _{DD} Power-Up and after input clock stabilization or deassertion of PD# to 1st clock			1.8	ms	1,2
SS Modulation Frequency	f _{M OD IN}	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz	1
Tdrive_PD#	t _{DRVPD}	Differential output enable after PD# de-assertion		200.000	300	us	1,3
Tfall	t _F	Fall time of control inputs			5	ns	1,2
Trise	t _R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	٧	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V _{DDSMB}	٧	1
SMBus Output Low Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	٧	1
SMBus Sink Current	I _{PULLUP}	@ V _{OL}	4			mΑ	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t _{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t _{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f _{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1

¹Guaranteed by design and characterization, not 100% tested in production.

 $^{^2 \}text{Control}$ input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

AC Electrical Characteristics - Differential Current Mode Outputs

 $TA = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t _{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1
Skew, Output to Output	t _{sk3 SRC}	Across all SRC outputs, $V_T = 50\%$		13.5	50	ps	1
Skew, Output to Output	t _{sk3CPU}	Across all CPU outputs, $V_T = 50\%$		43	50	ps	1
Jitter, Cycle to cycle	t.	CPU, SRC, NS_SAS outputs		35	50	ps	1,3
ortier, Cycle to cycle	ι _{jcyc-cyc}	DOT96 output		75	250	ps	1,3

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Phase Jitter Parameters

 $T_A = 0 - 70$ °C; Supply Voltage $V_{DD/}V_{DDA} = 3.3 \text{ V +/-5}\%$,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
	t _{jphPCleG1}	PCIe Gen 1		28	86	ps (p-p)	1,2,3,6
		PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	3	ps (rms)	1,2,6
	t _{jphPCleG2}	PCle Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.7	3.1	ps (rms)	1,2,6
	^t jphPCleG3	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.4	1	ps (rms)	1,2,4,6
Phase Jitter	t _{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.5	ps (rms)	1,5,7
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.13	0.3	ps (rms)	1,5,7
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.11	0.2	ps (rms)	1,5,7
	t _{jphSAS12G}	SAS12G (Filtered REFCLK Jitter 20KHz to 20MHz.)		0.34	0.4	ps (rms)	1,8,9
	t _{jphSAS12G}	SAS 12G		0.70	1.3	ps (rms)	1,5,8

¹ Guaranteed by design and characterization, not 100% tested in production.

 $^{^{2}}I_{BEF} = V_{DD}/(3xR_{B})$. For $R_{B} = 475\Omega$ (1%), $I_{BEF} = 2.32$ mA. $I_{OH} = 6$ x I_{BEF} and $V_{OH} = 0.7$ V @ $Z_{O} = 50\Omega$.

³ Measured from differential waveform

² See http://www.pcisig.com for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

⁶ Applied to SRC outputs

⁷ Applies to CPU outputs

⁸ Applies to NS_SAS, NS_SRC outputs, Spread Off

⁹ Intel calculation from raw phase noise data

Electrical Characteristics - PCI

 $T_A = 0 - 70$ °C; Supply Voltage $V_{DD}/V_{DDA} = 3.3 \text{ V +/-5}\%$,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}^*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4			V	1
Output Low Voltage	V_{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	1	MIN $@V_{OH} = 1.0 \text{ V}$	-33			mΑ	1
Output High Current	I _{ОН}	MAX $@V_{OH} = 3.135 \text{ V}$			-33	mΑ	1
Output Low Current	1	MIN $@V_{OL} = 1.95 \text{ V}$	30			mΑ	1
Output Low Guiteint	I _{OL}	MAX @ $V_{OL} = 0.4 V$			38	mA	1
Clock High Time	T _{HIGH}	1.5V	12			ns	1
Clock Low Time	T_LOW	1.5V	12			ns	1
Edge Rate	t _{sle wr/f}	Rising/Falling edge rate	1	1.8	4	V/ns	1,2
Duty Cycle	d _{t1}	V _T = 1.5 V	45	50.5	55	%	1
Group Skew	t _{skew}	$V_{T} = 1.5 V$		294	500	ps	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	$V_{T} = 1.5 V$		108	500	ps	1

See "Single-ended Test Loads Page" for termination circuits

Electrical Characteristics - 48MHz

 $T_A = 0 - 70^{\circ}C$; Supply Voltage $V_{DD}/V_{DDA} = 3.3 \text{ V +/-5\%}$,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	$V_O = V_{DD}^*(0.5)$	20		60	Ω	1
Output High Voltage	V _{OH}	$I_{OH} = -1 \text{ mA}$	2.4			V	1
Output Low Voltage	V_{OL}	$I_{OL} = 1 \text{ mA}$			0.55	V	1
Output High Current	ı	MIN $@V_{OH} = 1.0 \text{ V}$	-29			mA	1
Output High Curient	Іон	MAX $@V_{OH} = 3.135 \text{ V}$			-33	mA	1
Output Low Current	1	MIN $@V_{OL} = 1.95 \text{ V}$	29			mA	1
Output Low Current	I _{OL}	MAX @ $V_{OL} = 0.4 V$			27	mA	1
Clock High Time	T _{HIGH}	1.5V	8.094		10.036	ns	1
Clock Low Time	T_LOW	1.5V	7.694		9.836	ns	1
Edge Rate	t _{slewr/f_USB}	Rising/Falling edge rate	1	1.5	2	V/ns	1,2
Duty Cycle	d _{t1}	$V_{T} = 1.5 V$	45	51	55	%	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	$V_{T} = 1.5 \text{ V}$		109	350	ps	1

See "Single-ended Test Loads Page" for termination circuits

Electrical Characteristics - Current Consumption

 $TA = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I _{DD3.3OP}	All outputs active @100MHz, C _L = Full load;		380	400	mA	1
Powerdown Current	I _{DD3.3PDZ}	All differential pairs tri-stated		16	20	mA	1

Guaranteed by design and characterization, not 100% tested in production.

¹Guaranteed by design and characterization, not 100% tested in production.

 $^{^{2}\,\}mbox{Measured}$ between 0.8V and 2.0V

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Electrical Characteristics - REF

 $T_A = 0 - 70$ °C; Supply Voltage $V_{DD}/V_{DDA} = 3.3 \text{ V } +/-5\%$,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R_{DSP}	$V_O = V_{DD}^*(0.5)$	12		55	Ω	1
Output High Voltage	V _{OH}	$I_{OH} = -1 \text{ mA}$	2.4			V	1
Output Low Voltage	V_{OL}	$I_{OL} = 1 \text{ mA}$			0.55	V	1
Output High Current	ı	MIN $@V_{OH} = 1.0 \text{ V}$	-33			mA	1
Output High Current	I _{ОН}	MAX $@V_{OH} = 3.135 \text{ V}$			-33	mA	1
Output Low Current	_	MIN $@V_{OL} = 1.95 \text{ V}$	30			mA	1
Output Low Guiterit	I _{OL}	MAX @ $V_{OL} = 0.4 V$			38	mA	1
Clock High Time	T_{HIGH}	1.5V	27.5			ns	1
Clock Low Time	T_LOW	1.5V	27.5			ns	1
Edge Rate	t _{sle wr/f}	Rising/Falling edge rate	1	1.9	4	V/ns	1,2
Duty Cycle	d _{t1}	V _T = 1.5 V	45	50.5	55	%	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	V _T = 1.5 V		75	1000	ps	1

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Clock AC Tolerances

	CPU	SRC, NS_SAS, NS_SRC	PCI	DOT96	48MHz	REF	
PPM tolerance	100	100	100	100	100	100	ppm
Cycle to Cycle Jitter	50	50	500	250	350	1000	ps
Spread	-0.50%	-0.50%	-0.50%	0	0.00%	0.00%	%

Clock Periods – Outputs with Spread Spectrum Disabled

				М	easurement Wi	ndow				
	Center	1 Clock	1 us	0.1s	0.1s	0.1s	1us	1 Clock	1	
SSC ON	Freq. MHz	-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max	Units	Notes
OBLI	100.00000	9.94900		9.99900	10.00000	10.00100	HUX	10.05100	ns	1,2
CPU	133.33333	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2
SRC, NS_SAS, NS_SRC	100.00000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1.0
PCI	33.33333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2 1,2
DOT96	96.00000	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2
48MHz	48.00000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
REF	14.31818	69.78429		69.83429	69.84128	69.84826		69.89826	ns	1,2

Clock Periods – Outputs with Spread Spectrum Enabled

				М	easurement Wi	ndow				
	Center	1 Clock	1 us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC ON	Freq. MHz	-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max	Units	Notes
CPU	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2
CPU	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2
PCI	33.25	29.49718	29.99718	30.07218	30.07519	30.07820	30.15320	30.65320	ns	1,2
SRC	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2

 $^{^1\}text{Guaranteed}$ by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information

How to Write

- · Controller (host) sends a start bit
- · Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

	Index Block Write Operation										
Controll	er (Host)		IDT (Slave/Receiver)								
Т	starT bit										
Slave A	Address										
WR	WRite										
			ACK								
Beginning	Byte = N										
			ACK								
Data Byte	Count = X										
			ACK								
Beginnin	g Byte N										
			ACK								
0		×									
0		X Byte	0								
0		ė	0								
			0								
Byte N	+ X - 1										
			ACK								
Р	stoP bit										

SMBus write address = D2 hex

SMBus read address = D3 hex

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if X_(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- · Controller (host) will send a stop bit

	Index Block F	Read O	peration
Cor	ntroller (Host)		IDT (Slave/Receiver)
Т	starT bit		
SI	ave Address		
WR	WRite		
			ACK
Begi	nning Byte = N		
			ACK
RT	Repeat starT		
SI	ave Address		
RD	ReaD		
			ACK
			Data Byte Count=X
	ACK		
			Beginning Byte N
	ACK		
		<u>e</u>	0
	0	X Byte	0
	0		0
	0		
			Byte N + X - 1
N	Not acknowledge		
Р	stoP bit		

SMB us Table: Output Enable Register

Byte	0 Pin#	Name	Control Function		0	1	Default
Bit 7	24/25 DOT96 Enable		Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 6	50/49 NS_SAS1 Enable		Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 5	48/47	NS_SAS0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 4	44/43	NS_SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	42/41	NS_SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	36/35	SRC2 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	34/33	SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	30/31	SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1

SMBus Table: Output Enable Register

Byte	e 1 Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	REF14_3x Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6		RESERVED					
Bit 5	RESERVED						
Bit 4	62/61	CPU3	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	60/59	CPU2	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	56/55	CPU1	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	54/53	CPU0	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	CPU/SRC/ PCI	Spread Spectrum Enable	Spread Off/On	RW	Spread Off	Spread On	0

SMBus Table: Output Enable Register

Byte	2 Pin #	Name	Control Function	Type	0	1	Default	
Bit 7		RESERVED						
Bit 6			RESERVED				0	
Bit 5	13	PCI4 Enable	Output Enable	RW	Disable-Low	Enable	1	
Bit 4	14	PCI3 Enable	Output Enable	RW	Disable-Low	Enable	1	
Bit 3	15	PCI2 Enable	Output Enable	RW	Disable-Low	Enable	1	
Bit 2	16	PCI1 Enable	Output Enable	RW	Disable-Low	Enable	1	
Bit 1	17	PCI0 Enable	Output Enable	RW	Disable-Low	Enable	1	
Bit 0	21	48MHz Enable	Output Enable	RW	Disable-Low	Enable	1	

SMB us Table: Reserved

Byte	93 Pin #	Name	Control Function	Type	0	1	Default			
Bit 7			RESERVED				0			
Bit 6			RESERVED				0			
Bit 5			RESERVED				0			
Bit 4			RESERVED				0			
Bit 3			RESERVED				0			
Bit 2			RESERVED				0			
Bit 1			RESERVED				0			
Bit 0			RESERVED							

SMBus Table: Reserved

Byte	yte 4 Pin #		Name	Control Function	Type	0	1	Default
Bit 7				RESERVED				0
Bit 6				RESERVED				0
Bit 5				RESERVED				0
Bit 4				RESERVED				0
Bit 3				RESERVED				0
Bit 2				RESERVED				0
Bit 1				RESERVED				0
Bit 0				RESERVED				0

SMB us Table: Reserved

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	it 7 RESERVED						0
Bit 6			RESERVED				0
Bit 5			RESERVED				0
Bit 4	-	FS4	Freq. Sel 4	RW		0	
Bit 3		FS3	Freq. Sel 3	RW	Soo NS S/	AS/NS SRC	1
Bit 2	-	FS2	Freq. Sel 2	RW	_	1	
Bit 1	-	FS1	Freq. Sel 1	RW	Frequency Table.		1
Bit 0	-	FS0	Freq. Sel 0	RW			1

SMB us Table: Test Mode and CPU/SRC/PCI Frequency Select Register

Byte	e 6 Pin #	Name	Control Function	Type	0	1	Default
Bit 7	1	Test Mode	Test Mode Type	RW	Hi-Z	REF/N	0
Bit 6	-	Test Select	Select Test Mode	RW	Disable	Enable	0
Bit 5	-		RESERVED				0
Bit 4	-	100M_133M# (See note)	Frequency Select	R	133MHz	100MHz	Latch
Bit 3	-	FS3	Freq. Sel 3	RW			1
Bit 2	-	FS2	Freq. Sel 2	RW	See CPU/SRC/	PCI Frequency	0
Bit 1	-	FS1	FS1 Freq. Sel 1 RW Select Table		Table	0	
Bit 0	- FS0		Freq. Sel 0	RW			0

Note: Internal Pull up on $100M_133M\#$ pin will result in default CPU frequency of 100~MHz.

SMBus Table: Vendor & Revision ID Register

Byte	7 Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3		R	0011 for D rev		0
Bit 6	-	RID2	REVISION ID	R			0
Bit 5	-	RID1	REVISION ID	R			1
Bit 4	-	RID0		R			1
Bit 3	-	VID3		R			0
Bit 2	-	VID2	VENDOR ID	R	0001 for	JCC/IDT	0
Bit 1	-	VID1	VENDORID	R	0001 for ICS/IDT		0
Bit 0	-	VID0		R			1

SMBus Table: Byte Count Register

Byte	8 Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7		RW		0	
Bit 6	-	BC6		RW	Writing to this register will configure how many bytes will be read back, default is A		0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4	Byte Count	RW			0
Bit 3	-	BC3	Programming b (7:0)	RW		•	1
Bit 2		BC2		RW	bytes. (0 to 9		0
Bit 1	-	BC1]	RW			1
Bit 0	-	BC0		RW			0

SMB us Table: Device ID Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DID7		R	-	-	0
Bit 6		DID6	1	R	-	-	0
Bit 5		DID5		R	-	-	0
Bit 4		DID4	Device ID	R	-	-	1
Bit 3		DID3	(17 hex)	R	-	-	0
Bit 2		DID2		R	-	-	1
Bit 1		DID1		R	-	-	1
Bit 0		DID0		R	-	-	1

CPU/SRC/PCI Frequency Selection Table

Line	Byte 1, Bit 0 Spread Enable	Byte6 Bit3 FS3	Byte6 Bit2 FS2	Byte6 Bit1 FS1	Byte6 Bit0 FS0	CPU Speed for 100MHz	CPU Speed for 133MHz	SRC (MHz)	PCI (MHz)	Spread %
0	0	0	0	0	0	89.97	119.97	89.97	29.99	
1	0	0	0	0	1	91.28	121.70	91.28	30.43	
2	0	0	0	1	0	92.58	123.44	92.58	30.86	
3	0	0	0	1	1	93.75	125.00	93.75	31.25	
4	0	0	1	0	0	95.05	126.73	95.05	31.68	
5	0	0	1	0	1	96.22	128.30	96.22	32.07	
6	0	0	1	1	0	97.53	130.03	97.53	32.51	
7	0	0	1	1	1	98.83	131.77	98.83	32.94	0%
8	0	1	0	0	0	100.00	133.33	100.00	33.33	U /o
9	0	1	0	0	1	101.30	135.07	101.30	33.77	
10	0	1	0	1	0	102.47	136.63	102.47	34.16	
11	0	1	0	1	1	103.78	138.37	103.78	34.59	
12	0	1	1	0	0	105.08	140.10	105.08	35.03	
13	0	1	1	0	1	106.25	141.67	106.25	35.42	
14	0	1	1	1	0	107.55	143.40	107.55	35.85	
15	0	1	1	1	1	110.03	146.70	110.03	36.68	
16	1	0	0	0	0	89.97	119.97	89.97	29.99	
17	1	0	0	0	1	91.28	121.70	91.28	30.43	
18	1	0	0	1	0	92.58	123.44	92.58	30.86	
19	1	0	0	1	1	93.75	125.00	93.75	31.25	
20	1	0	1	0	0	95.05	126.73	95.05	31.68	
21	1	0	1	0	1	96.22	128.30	96.22	32.07	
22	1	0	1	1	0	97.53	130.03	97.53	32.51	
23	1	0	1	1	1	98.83	131.77	98.83	32.94	-0.5%
24	1	1	0	0	0	100.00	133.33	100.00	33.33	-0.5 /6
25	1	1	0	0	1	101.30	135.07	101.30	33.77	
26	1	1	0	1	0	102.47	136.63	102.47	34.16	
27	1	1	0	1	1	103.78	138.37	103.78	34.59	
28	1	1	1	0	0	105.08	140.10	105.08	35.03	
29	1	1	1	0	1	106.25	141.67	106.25	35.42	
30	1	1	1	1	0	107.55	143.40	107.55	35.85	
31	1	1	1	1	1	110.03	146.70	110.03	36.68	

NS_SAS Margining Table

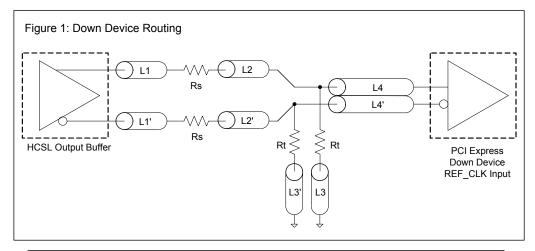
	Byte5	Byte5	Byte5	Byte5	Byte5	
	Bit4	Bit3	Bit2	Bit1	Bit0	NS_xxx
Line	FS4	FS3	FS2	FS1	FS0	(MHz)
0	0	0	0	0	0	58.33
1	0	0	0	0	1	61.11
2	0	0	0	1	0	63.89
3	0	0	0	1	1	66.67
4	0	0	1	0	0	69.44
5	0	0	1	0	1	72.22
6	0	0	1	1	0	75.00
7	0	0	1	1	1	77.78
8	0	1	0	0	0	80.56
9	0	1	0	0	1	83.33
10	0	1	0	1	0	86.11
11	0	1	0	1	1	88.89
12	0	1	1	0	0	91.67
13	0	1	1	0	1	94.44
14	0	1	1	1	0	97.22
15	0	1	1	1	1	100.00
16	1	0	0	0	0	102.78
17	1	0	0	0	1	105.56
18	1	0	0	1	0	108.33
19	1	0	0	1	1	111.11
20	1	0	1	0	0	113.89
21	1	0	1	0	1	116.67
22	1	0	1	1	0	119.44
23	1	0	1	1	1	122.22
24	1	1	0	0	0	125.00
25	1	1	0	0	1	127.78
26	1	1	0	1	0	130.56
27	1	1	0	1	1	133.33
28	1	1	1	0	0	136.11
29	1	1	1	0	1	138.89
30	1	1	1	1	0	141.67
31	1	1	1	1	1	144.44

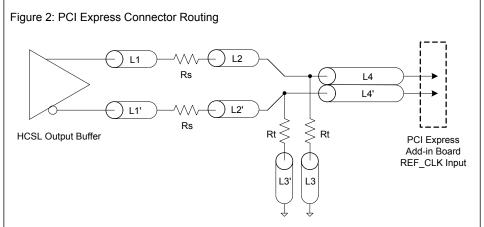
NOTE: Operation at other than the default entry is not guaranteed. These values are for margining purposes only.

DIF Reference Clock					
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure		
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1		
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1		
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1		
Rs	33	ohm	1		
Rt	49.9	ohm	1		

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

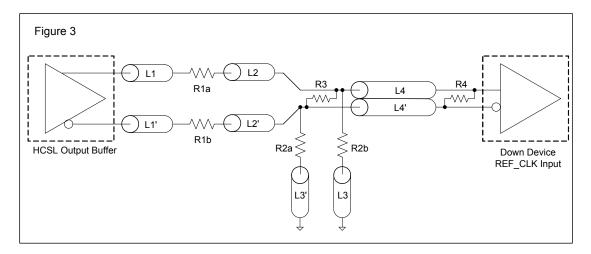
Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2



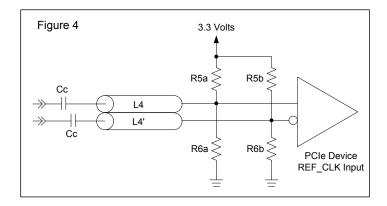


	Alternative Termination for LVDS and other Common Differential Signals (figure 3)						
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1 R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)				
Component	Value	Note		
R5a, R5b	8.2K 5%			
R6a, R6b	1K 5%			
Сс	0.1 μF			
Vcm	0.350 volts			



Test Clarification Table

Comments	emments HW		SW		
	TEST_SEL HW PIN	TEST_MODE HW PIN	TEST ENTRY BIT B6b6	REF/N or HI-Z B6b7	OUTPUT
	0	X	0	Χ	NORMAL
Power-up w/ TEST_SEL = 1 (>2.0V) to enter test mode.	1	0	Χ	0	HI-Z
Cycle power to disable test mode.	1	0	X	1	REF/N
	1	1	X	0	REF/N
	1	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up,	0	Χ	1	0	HI-Z
test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N. TEST_Mode pin is not used. Cycle power to disable test mode.	0	x	1	1	REF/N

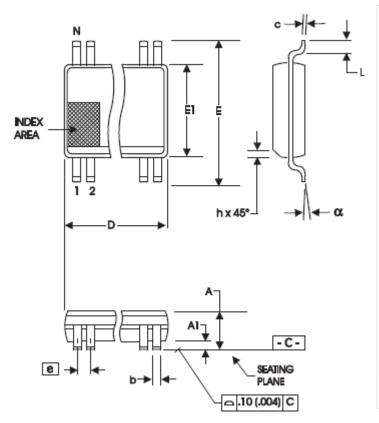
B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B6b7: 1= REF/N, Default = 0 (HI-Z)

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Thermal Resistance Junction to	$\theta_{\sf JA}$	Still air		68.2		°C/W
Ambient	$\theta_{\sf JA}$	1 m/s air flow		63.3		°C/W
	$\theta_{\sf JA}$	2 m/s air flow		59.6		°C/W
Thermal Resistance Junction to Case	θJC			32.5		°C/W
Thermal Resistance Junction to Board	θ_{JB}			51.5		°C/W

Package Outline and Package Dimensions (64-pin TSSOP)



	6.10 mm. Bo (240 mil)	dy, 0.50 mm. (20 mil)	Pitch TSSOP	
OVADOL	In Milli		25-25-25-25-25-25-25-25-25-25-25-25-25-2	nches
SYMBOL	COMMON D	IMENSIONS	COMMON L	IMENSIONS
	MIN	MAX	MIN	MAX
Α	-	1.20		.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
С	0.09	0.20	.0035	.008
D	SEE VAR	NATIONS	SEE VARIATIONS	
E	8.10 B	BASIC	0.319	BASIC
E1	6.00	6.20	.236	.244
е	0.50 B	BASIC	0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VAR	RIATIONS
α	0°	8°	0°	8°
aaa	-	0.10		.004

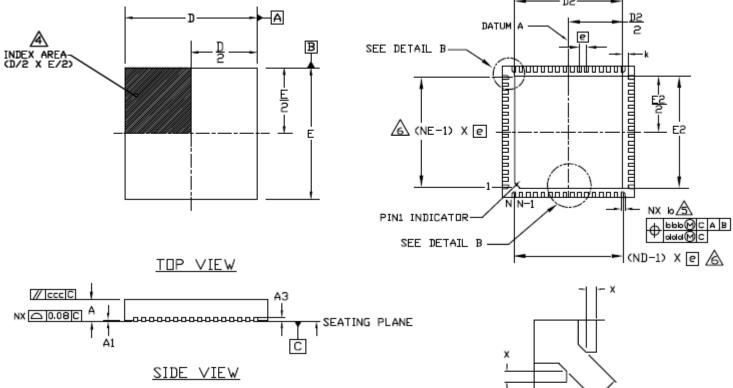
VARIATIONS

N	Dn	nm.	D (inch)		
N	MIN	MAX	MIN	MAX	
64	16.90	17.10	.665	.673	

Reference Doc.: JEDEC Publication 95, MO-153

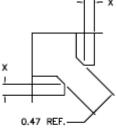
10-0039

Package Outline and Package Dimensions (64-pin MLF)

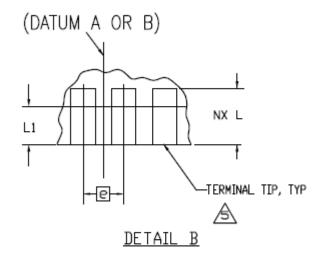


NOTES:

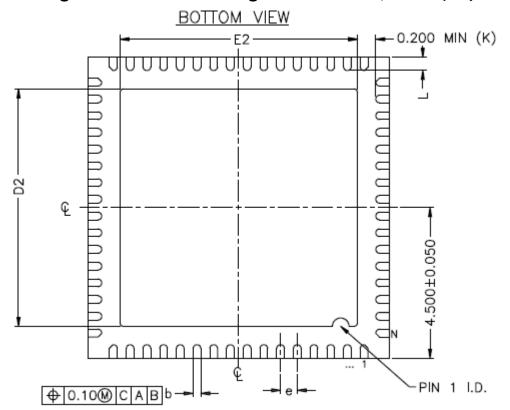
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- 4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- ⚠ DIMENSION 5 APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- AND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- 7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- 8 CORNER LEAD CHAMFERS ARE APPLIED TO MAINTAIN MINIMUM CORNER LEAD SPACING (8 PLACES).



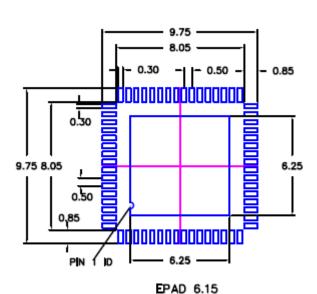
DETAIL B CORNER LEAD CHAMFER DETAILS Æ



Package Outline and Package Dimensions, cont. (64-pin MLF)



DIMENSIONS					
PACKAGE	ACKAGE 64L 9.0×9.0 - 0.50				
REF.	MIN.	NDM.	MAX.		
Α	0.80	0.90	1.00		
b	0.18	0.25	0,30		
D		9.00 BSC			
D2	6.0	6.15	6.25		
E		9.00 BSC			
E2	6.0	6.15	6.25		
6		0.50 BSC.			
L	0.30	0.40	0.50		
N		64			
ND		16			
NE		16			
k	0.20				



SYMB0	COMMO	M + Z			
L	MIN.	N□M.	MAX.	E	
A1	0	0.02	0.05		
АЗ	-	0.20 REF.	-		
×	b/2	-	-		
TOLERANCES OF FORM AND POSIT				ION	
bbb		0.10			
ccc	0.10				
dold	0.05				

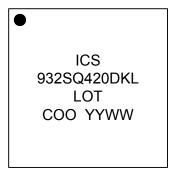
NOTES:

- 1, ALL DIMENSION ARE IN mm, ANGLES IN DEGREES,
- 2, TOP DOWN VIEW, AS VIEWED ON PCB,
- 3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
- 4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

Marking Diagram (TSSOP)



Marking Diagram (MLF)



Notes:

- 1. 'LOT' denotes lot number.
- 2. 'YYWW' is the date code.
- 3. 'COO' denotes country of origin.
- 4. 'L' or 'LF' denotes RoHS compliant package.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
932SQ420DGLF	Tubes	64-pin TSSOP	0 to +70° C
932SQ420DGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C
932SQ420DKLF	Tray	64-pin MLF	0 to +70° C
932SQ420DKLFT	Tape and Reel	64-pin MLF	0 to +70° C

[&]quot;LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"D" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Who	Description	Page #
Α	9/20/2010	RDW	Minor typo corrections	Various
В	3/1/2011	RDW	Added rise/fall variation to DC Electrical Characteristics Table	9
С	3/9/2011	RDW	Corrected Line 0 of NS_SAS Margining Table.	19
D	4/28/2011	RDW	Corrected MLF packaging pin description. Pin 37 was missing.	7
			Updated Power Down Functionality table to clarify functionality of single-	
E	7/26/2011	RDW	ended outputs in power down.	2
			Added "Case Temperature" spec to Abs Max ratings	
F	9/20/2011	RDW	2. Added Thermal Characteristics	Various
			1. Updated Phase Jitter Table to correct typo in "Conditions" column for	11, 23,
G	12/8/2011	RDW	SAS.	24
			2. Mark Spec Added.	2-7
Ιн	4/18/2012	BDW	Updated Rp values on Output Terminations Table from 43.2 ohms to	8
	- /,10/2012	11000	42.2 or 43.2 ohms to be consistent with Intel.	J
J	1/7/2015	DC	Updated package drawing and dimensions from PUNCH to SAWN	Various
			version.	

SYNTHESIZERS

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