Description

The 9DBL0255/9DBL0455 are 2 and 4-output PCIe Clock fan-out buffers for PCIe Gen1-5 applications. Both parts have an open drain Loss of Signal (LOS) output to indicate the absence or presence of an input clock. The LOS circuit also implements Automatic Clock Parking (ACP) to cleanly park the outputs low/low when the input clock goes away. The devices implement several additional features to aid robust designs. Flexible Power Sequencing (FPS) ensures well-defined behavior under various power up scenarios, while Power Down Tolerant (PDT) ESD protection allows input pins to be driven before VDD is applied. The 9DBL0255/9DBL0455 are spread-spectrum compatible and provide direct connection to 85Ω transmission lines. They can also be used in 100Ω environments with simple external series resistors.

PCIe Architectures

- Common Clocked (CC)
- Independent Reference Clock (SRIS, SRnS)

Typical Applications

- PCIe clock distribution in:
  - PCIe Riser Cards
  - NVME eSSD and JBOD
  - High-Performance Computing and Accelerators

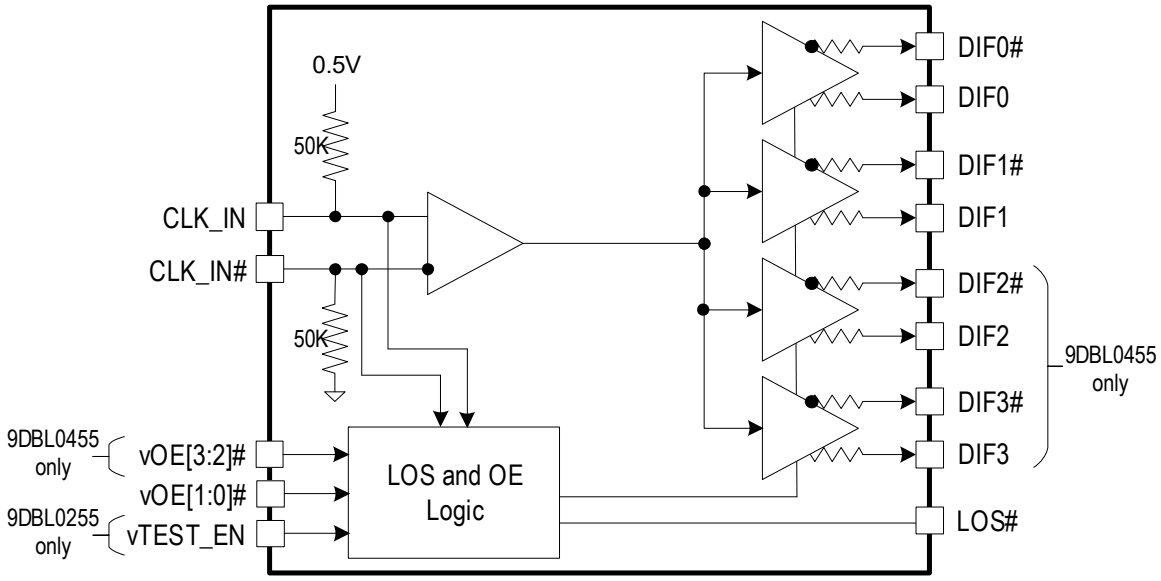
Features

- FPS: VDD may be applied with floating input clock, or input clock may be driven before VDD is applied
- ACP: Outputs automatically park low/low when LOS occurs and cleanly start when LOS is removed
- PDT: Input pins may be driven before VDD is applied and will not damage the device
- 2 or 4 Low-power HCSL (LP-HCSL) DIF pairs
- 85Ω loads require 0 termination resistors
- 100Ω loads require only 2 series resistors per output
- OE# pin for each output
- Spread-spectrum tolerant
- Industrial temperature range (-40°C to +85°C)
- Space saving 3 × 3 mm 16-VFQFPN (9DBL0255)
- Space saving 4 × 4 mm 20-VFQFPN (9DBL0455)
- Easy AC-coupling to other logic families. See application note AN-891.

Key Specifications

- Input-to-output delay < 3ns
- Output-to-output skew < 50ps
- Operating frequency up to 267MHz (9DBL0455)
- Additive phase jitter < 15fs RMS for PCIe Gen5
- Additive phase jitter 46fs RMS (typical) at 156.25MHz (12kHz–20MHz)

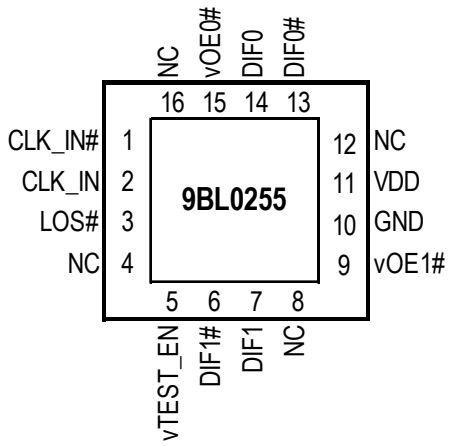
Block Diagram



Contents

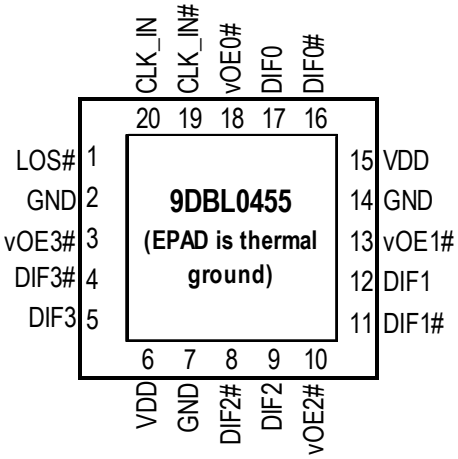
Pin Assignments

Figure 1. Pin Assignments for 3 x 3 mm 16-VFQFPN Package – Top View



16-VFQFPN, 3 × 3mm, 0.5mm pitch
^ prefix indicates internal 120kOhm pull-up resistor
v prefix indicates internal 120kOhm pull-down resistor

Figure 2. Pin Assignments for 4 x 4 mm 20-VFQFPN Package – Top View



20-VFQFPN, 4 x 4 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

9DBL0255 Pin Descriptions

Table 1. 9DBL0255 Pin Descriptions

Number	Name	Type	Description
1	CLK_IN#	Input	Complementary input for differential reference clock.
2	CLK_IN	Input	True input for differential reference clock.
3	LOS#	Open Drain Out	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
4	NC	—	No connection.
5	vTEST_EN	Input	Test Enable Pin for forcing the outputs during board test. It has an internal pull down. See the Test Mode (9DBL0255 only) table for additional details.
6	DIF1#	Output	Differential complementary clock output.
7	DIF1	Output	Differential true clock output.
8	NC	—	No connection.
9	vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
10	GND	GND	Ground pin.
11	VDD	Power	Power supply, nominally 3.3V.
12	NC	—	No connection.
13	DIF0#	Output	Differential complementary clock output.
14	DIF0	Output	Differential true clock output.
15	vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
16	NC	—	No connection.
17	EPAD	GND	Connect EPAD to ground.

9DBL0455 Pin Descriptions

Table 2. 9DBL0455 Pin Descriptions

Number	Name	Type	Description
1	LOS#	Open Drain Out	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
2	GND	GND	Ground pin.
3	vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
4	DIF3#	Output	Differential complementary clock output.
5	DIF3	Output	Differential true clock output.
6	VDD	Power	Power supply, nominally 3.3V.

Table 2. 9DBL0455 Pin Descriptions (Cont.)

Number	Name	Type	Description
7	GND	GND	Ground pin.
8	DIF2#	Output	Differential complementary clock output.
9	DIF2	Output	Differential true clock output.
10	vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
11	DIF1#	Output	Differential complementary clock output.
12	DIF1	Output	Differential true clock output.
13	vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
14	GND	GND	Ground pin.
15	VDD	Power	Power supply, nominally 3.3V.
16	DIF0#	Output	Differential complementary clock output.
17	DIF0	Output	Differential true clock output.
18	vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
19	CLK_IN#	Input	Complementary input for differential reference clock.
20	CLK_IN	Input	True input for differential reference clock.
21	EPAD	GND	Connect to Ground.

Power Management

Table 3. Power Management

CLK_IN	OEx# Pin	DIFx	DIFx#
Floating[a]	x	Low	Low
Stopped	x	Low	Low
Running	1	Low	Low
Running	0	Running	Running

[a] The CLK_IN has an internal network that biases the clock input to a differential '1' state.

Table 4. Test Mode (9DBL0255 only)

TEST_EN	OEx# Pin	DIFx	DIFx#
x	0	Normal Operation	
0	1	Low	Low
1	1	High	High

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DBL0255/9DBL0455 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDx}				3.9	V	1,2
Input Voltage	V_{IN}	Single-ended control inputs.	-0.5		3.9	V	1
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins.			3.9	V	1
Junction temperature	T_J		-65		150	°C	1
Storage temperature	T_S				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Thermal Characteristics

Table 6. Thermal Characteristics

Parameter	Symbol	Conditions	Package	Typical Value	Units	Notes
Thermal Resistance	θ_{JC}	Junction to case.	9DBL0255 NLG16P3	66	°C/W	1
	θ_{Jb}	Junction to base.		5.1	°C/W	1
	θ_{JA0}	Junction to air, still air.		63	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		56	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		51	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		49	°C/W	1
Thermal Resistance	θ_{JC}	Junction to case.	9DBL0455 NLG20P1	65.8	°C/W	1
	θ_{Jb}	Junction to base.		5.1	°C/W	1
	θ_{JA0}	Junction to air, still air.		63.2	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		55.9	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		51.4	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		49.2	°C/W	1

[1] EPAD soldered to board.

Electrical Characteristics

$T_A = T_{AMB}$, supply voltages per normal operation condition. See Test Loads for loading conditions.

Table 7. CLK_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage	V_{CROSS}	Crossover voltage.	150		900	mV	1
Input Swing	V_{SWING}	Differential value (±150mV single-ended).	300			mV	1
Input Slew Rate	dv/dt	Measured differentially.	0.6		8	V/ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 8. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DD}	Supply voltage.	3.135	3.3	3.465	V	
Pull-up Voltage	V_{DDPup}	Pull-up voltage for LOS# pin.			3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs.	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Output High Voltage	V_{OH}	LOS# output (1kΩ pull resistor, V_{DDPup} = 3.3V.	0.9 V_{DDPup}		V_{DDPup}	V	
Output Low Voltage	V_{OL}		-0.3		0.15 V_{DDPup}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-50		100	µA	
Input Frequency	F_{IN}	9DBL0255	10		220	MHz	
		9DBL0455	10		267		
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except CLK_IN.	1.5		5	pF	1
	C_{INCLK_IN}	CLK_IN differential clock inputs.	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	t_{STAB}	From V_{DD} valid, input clock stabilization and OE# pins low.		224	300	µs	1,2
LOS# De-assertion Time	$t_{LOS\#\_De\text{-}assert}$	Time for LOS# to de-assert after return of input clock.		224	300	µs	1
LOS# Assertion Time	$t_{LOS\#\_Assert}$	Time for LOS# to assert after loss of input clock.		73	100	ns	1

Table 8. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1		3	clocks	1,3
Tfall	t_F	Fall time of single-ended control inputs.			5	ns	2
Trise	t_R	Rise time of single-ended control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV, assuming input clock is running.

Table 9. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current (9DBL0255)	I_{DD}	220MHz, all outputs running.		26	36	mA	
		100MHz, all outputs running.		14	20	mA	
Operating Supply Current (9DBL0455)	I_{DD}	267MHz, all outputs running		48	65	mA	
		100MHz, all outputs running.		24	33	mA	
Powerdown Current	I_{DDRPD}	Input clock stopped.		1.7	2.5	mA	1

[1] Input clock stopped.

Table 10. Output Duty Cycle, Jitter, and Skew Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially, 100MHz.	0	0.4	0.7	%	1,3
Skew, Input to Output	t_{pd}	V_T = 50%, V_{SWING} > 600mV (±300mV single-ended).	1.5	2.2	3.0	ns	1,2,5
		V_T = 50%, 400mv ≤ V_{SWING} ≤ 600mV (±200mV to ±300 mV single-ended).	1.9	2.8	3.7	ns	1,2,6
		V_T = 50%, 300mv ≤ V_{SWING} < 400mV (±150mV to ±200 mV single-ended).	2.9	3.9	4.9	ns	1,2
Skew, Output to Output	t_{sk3}	V_T = 50%, 9DBL0255.		2	15	ps	2,4
		V_T = 50%, 9DBL0455.		14	25	ps	1,2,4

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

[4] All outputs equally loaded.

[5] The maximum absolute difference between minimum and maximum t_{pd} at any given V_{SWING} in this range is 1.15ns.

[6] The maximum absolute difference between minimum and maximum t_{pd} at any given V_{SWING} in this range is 1.4ns.

Table 11. LP-HCSL Outputs – 9DBL0255

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	3.0	3.4	3.9	1–5	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		5	11	20	%	1,4,7
Max Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	800	843	885	660–1150	mV	7,8
Min Voltage	Vmin		-104	-74	-47	-300–150		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	324	367	421	250–550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		21	71	140	mV	1,6,7

Table 12. LP-HCSL Outputs – 9DBL0455

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	3.8	4.4	5	1–5	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		7	15	20	%	1,4,7
Max Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	804	846	888	660–1150	mV	7,8
Min Voltage	Vmin		-154	-109	-62	-300–150		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	278	347	415	250–550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		18	25	140	mV	1,6,7

Notes for LP-HCSL Outputs tables:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Table 13. Additive Phase Jitter for Fanout Buffers[7]

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
Additive PCIe Phase Jitter (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s)		0.480	0.901	86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s)		0.011	0.017	3	ps (RMS)	1,2
		PCIe Gen2 Lo Band (5.0 GT/s)		0.045	0.075	3.1	ps (RMS)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s)		0.020	0.033	1	ps (RMS)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s)		0.020	0.033	0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s)		0.007	0.012	0.15	ps (RMS)	1,2,3,5
Additive PCIe Phase Jitter (SRIS Architecture)	$t_{jphPCIeG1-SRIS}$	PCIe Gen1 (2.5 GT/s)		0.063	0.103	N/A	ps (RMS)	1,2,6
	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (5.0 GT/s)		0.055	0.091		ps (RMS)	1,2,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (8.0 GT/s)		0.014	0.024		ps (RMS)	1,2,6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen4 (16.0 GT/s)		0.015	0.024		ps (RMS)	1,2,6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen5 (32.0 GT/s)		0.014	0.022		ps (RMS)	1,2,6
Additive Phase Jitter (12kHz–20MHz)	$t_{jphPCIe12k-20M}$	156.25MHz		46	54		fs (RMS)	

[1] The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The **total** REFCLK jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. If oscilloscope data is used, equipment noise is removed from all results.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the N/A in the “Limit” column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A “rule-of-thumb” SRIS limit would be either 0.5ps RMS/$\sqrt{2}$ = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/$\sqrt{2}$ = 0.5ps RMS if the clock chip is near the clock input.

[7] Additive jitter for RMS values is calculated by solving for “b” [$b = \sqrt{(c^2 - a^2)}$], where “a” is RMS input jitter and “c” is RMS output jitter.

Test Loads

Figure 3. LOS# Test Load

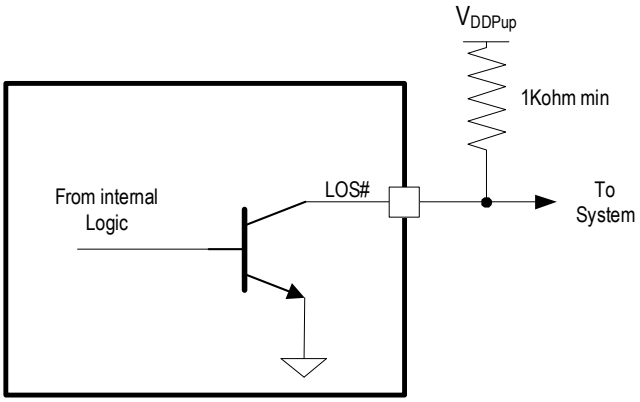


Figure 4. AC/DC Test Load

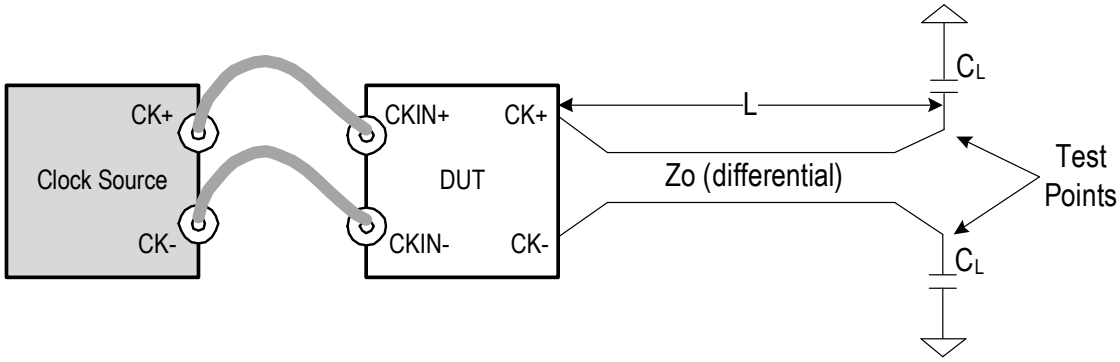


Figure 5. Jitter Measurement Circuit

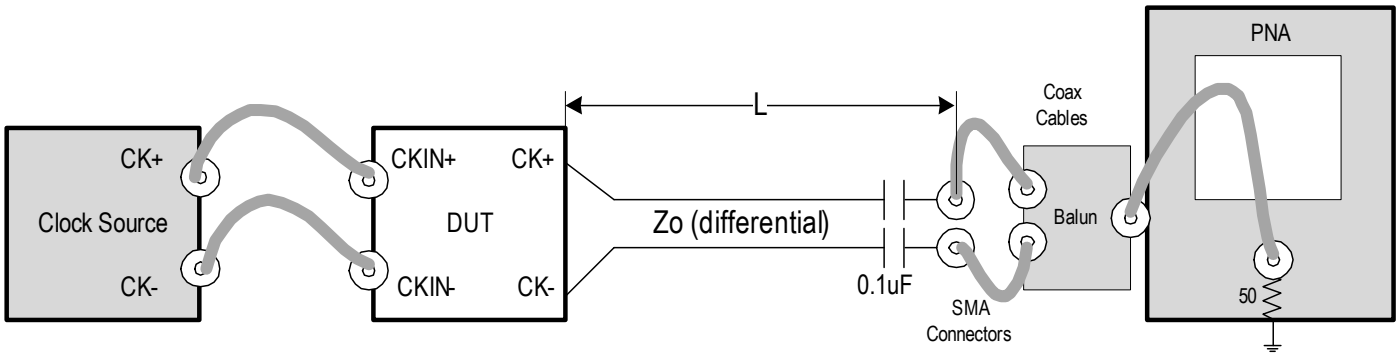


Table 14. Parameters for Output Test Loads

Clock Source	Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
SMA100B	Internal	85	5	2
SMA100B	7.5	100	5	2

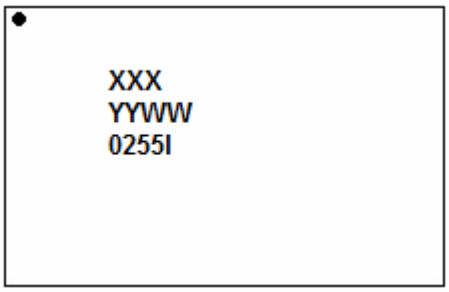
Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with Renesas' "Universal" Low-Power HCSL Outputs" for details.

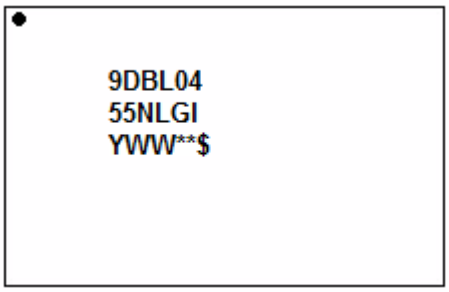
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagrams



- Line 1 indicates the last three characters of Asm lot number.
- Line 2 indicates the following:
  - "YY" is the last digits of the year; "WW" is the work week number when the part was assembled.
- Line 3 indicates the truncated part number.



- Lines 1 and 2 indicate the part number.
- Line 3 indicates the following:
  - "Y" is the last digit of the year; "WW" is the work week number when the part was assembled.
  - "**" denotes the lot sequence.
  - "$" denotes the mark code.

Ordering Information

Orderable Part Number	Carrier Type	Number of Outputs	Package	Temperature
9DBL0255NLGI	Tray	2	3 × 3mm, 16-VFQFPN	-40° to +85°C
9DBL0255NLGI8	Tape and Reel			
9DBL0455NLGI	Tray	4	4 × 4 mm, 20-VFQFPN	
9DBL0455NLGI8	Tape and Reel			

"G" denotes Pb-free, RoHS complaint configuration.

Revision History

Revision Date	Description of Change
March 17, 2021	▪ Updated front page description text and features bullets. ▪ Modified block diagram to indicate pin that are 9DBL0255 only and 9DBL0455 only. ▪ Updated Package Outline Drawings section and Ordering Information table. ▪ Reformatted to Renesas.
September 30, 2019	Merged 9DBL0255 and 9DBL0455 into one single document.
August 23, 2019	Initial release.

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