Description

The 9DBV05x1/9DBV07x1/9DBV09x1 fanout buffers are low-power, high-performance fanout buffers in Renesas' Full Featured PCIe family. The buffers have 5, 7 or 9 outputs with each output having an OE# to support the PCIe CLKREQ# function. The devices have 3 selectable SMBus addresses.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

Typical Applications

- Servers/High-performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

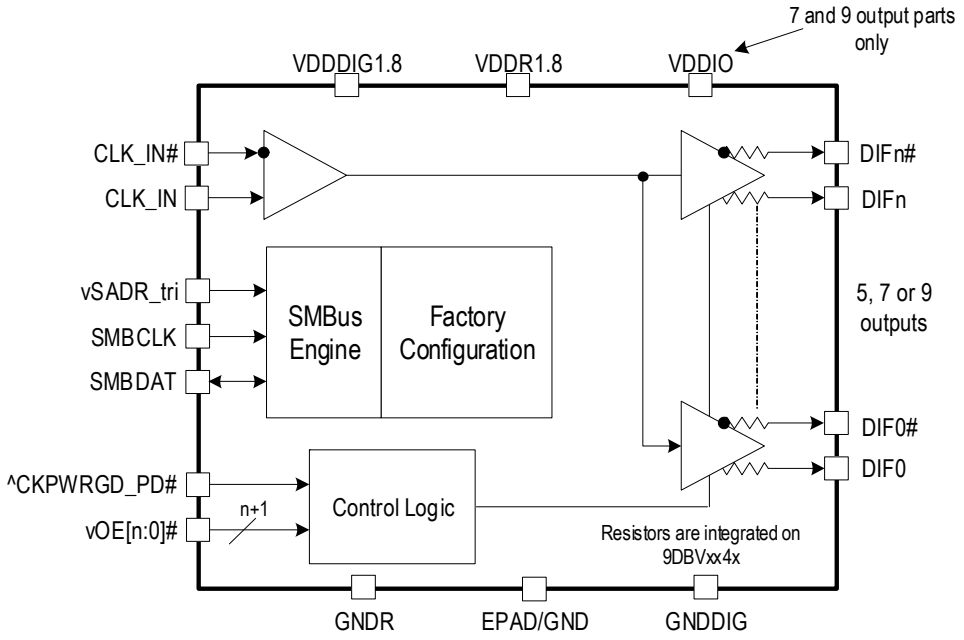
Key Specifications

- PCIe Gen5 CC additive phase jitter < 40fs RMS
- 12kHz–20MHz additive phase jitter = 165fs RMS at 156.25MHz (typical)
- Output-to-output skew < 50ps
- Power consumption as low as 41mW (typical)
- 1MHz to 200MHz operating frequency

Features

- 5–9 Low-Power HCSL (LP-HCSL) outputs
  - 100Ω outputs eliminate 4 resistors per output pair (9DBVxx41)
  - 33Ω outputs eliminate 2 resistors per output pair allowing use in both 85Ω and 100Ω systems (9DBVxx31)
- Easy AC-coupling to other logic families, see application note AN-891
- Spread spectrum compatible
- OE# pins support PCIe CLKREQ# function
- 3 selectable SMBus addresses
- 3.3V tolerant SMBus interface
- SMBus-selectable features allow optimization to customer requirements:
  - Individual slew rate control for each output
  - Differential output amplitude
  - Device contains default configuration; SMBus interface not required for device operation
- -40°C to +85°C operating temperature range
- Packages: See Ordering Information for more details

Block Diagram



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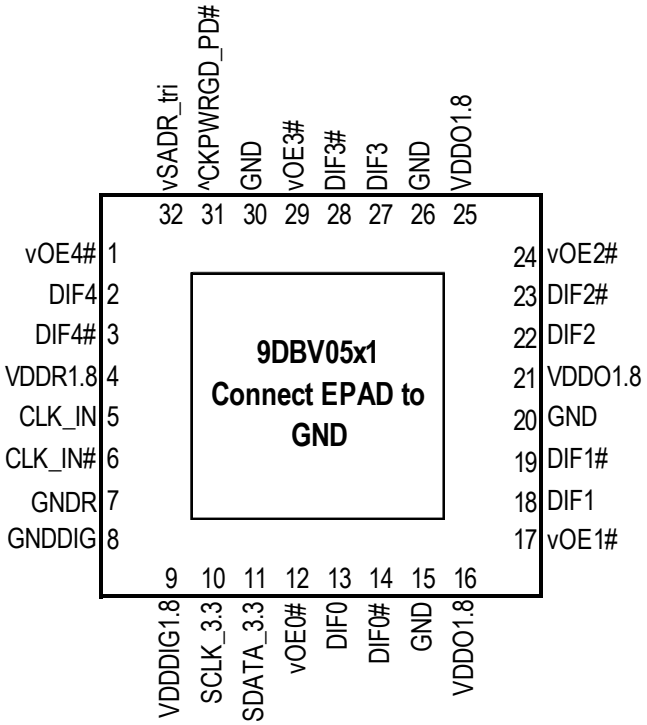
Pin Assignments

9DBV05x1 Pin Assignment

Figure 1. Pin Assignment for 5 × 5 mm 32-VFQFPN Package – Top View



32-VFQFPN, 5 x 5 mm, 0.5mm pitch

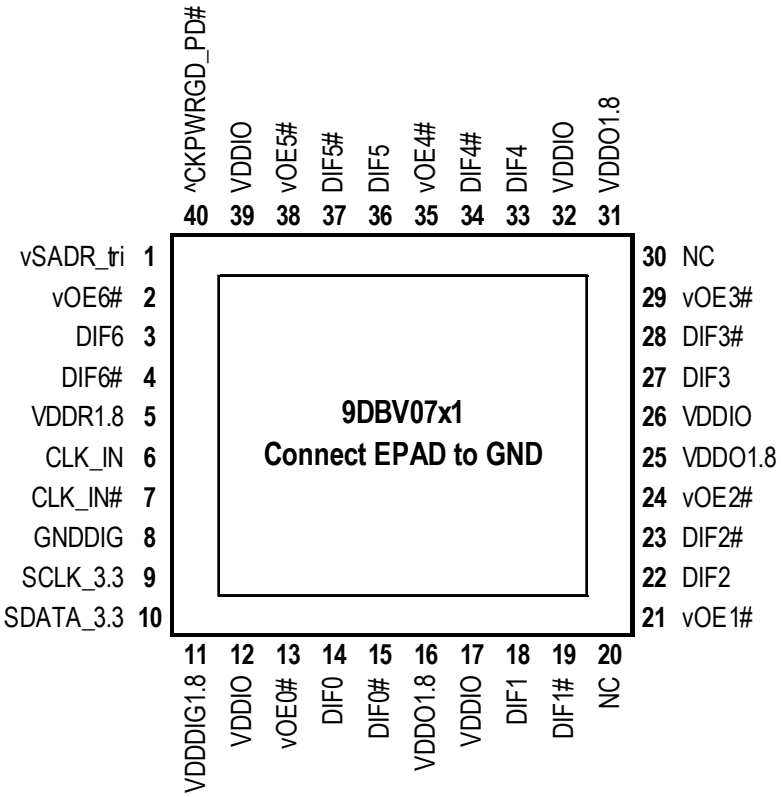
^ prefix indicates internal 120kOhm pull-up resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistor (biased to VDD/2)

v prefix indicates internal 120kOhm pull-down resistor

9DBV07x1 Pin Assignment

Figure 2. Pin Assignment for 5 × 5 mm 40-VFQFPN Package – Top View



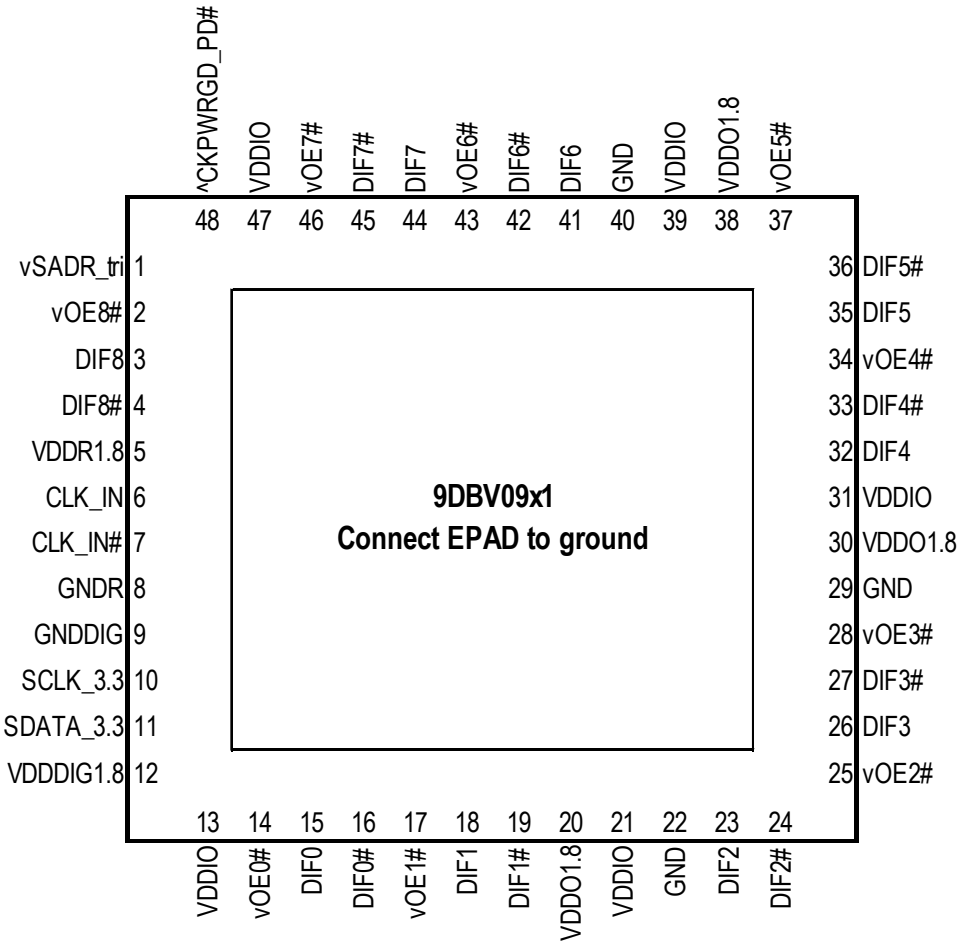
40-VFQFPN, 5 x 5 mm 0.4mm pitch

^ prefix indicates internal pull-up resistor

v prefix indicates internal pull-down resistor

9DBV09x1 Pin Assignment

Figure 3. Pin Assignment for 6 × 6 mm 48-VFQFPN Package – Top View



48-VFQFPN, 6 x 6 mm, 0.4mm pitch

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistor (biased to VDD/2)

Pin Descriptions

Table 1. Pin Descriptions

Name	Type	Description	9DBV09xx Pin No.	9DBV07xx Pin No.	9DBV05xx Pin No.
^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.	48	40	31
CLK_IN	Input	True input for differential reference clock.	6	6	5
CLK_IN#	Input	Complementary input for differential reference clock.	7	7	6
DIF0	Output	Differential true clock output.	15	14	13
DIF0#	Output	Differential complementary clock output.	16	15	14
DIF1	Output	Differential true clock output.	18	18	18
DIF1#	Output	Differential complementary clock output.	19	19	19
DIF2	Output	Differential true clock output.	23	22	22
DIF2#	Output	Differential complementary clock output.	24	23	23
DIF3	Output	Differential true clock output.	26	27	27
DIF3#	Output	Differential complementary clock output.	27	28	28
DIF4	Output	Differential true clock output.	32	33	2
DIF4#	Output	Differential complementary clock output.	33	34	3
DIF5	Output	Differential true clock output.	35	36	—
DIF5#	Output	Differential complementary clock output.	36	37	—
DIF6	Output	Differential true clock output.	41	3	—
DIF6#	Output	Differential complementary clock output.	42	4	—
DIF7	Output	Differential true clock output.	44	—	—
DIF7#	Output	Differential complementary clock output.	45	—	—
DIF8	Output	Differential true clock output.	3	—	—
DIF8#	Output	Differential complementary clock output.	4	—	—
EPAD	GND	Connect epad to ground.	49	41	33
GND	GND	Ground pin.	22, 29, 40	41	15, 20, 26, 30
GNDDIG	GND	Ground pin for digital circuitry.	9	41	8
GNDR	GND	Analog ground pin for the differential input (receiver).	8	41	7
NC	—	No connect.	—	20,30	—
SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.	10	30	10
SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.	11	9	11
VDDDIG1.8	Power	1.8V digital power (dirty power).	12	11	9
VDDIO	Power	Power supply for differential outputs.	13, 21, 31, 39, 47	12, 17, 26, 32, 39	—
VDDO1.8	Power	Power supply for outputs. Nominally 1.8V.	20, 30, 38	16, 25, 31	16, 21, 25

Table 1. Pin Descriptions (Cont.)

Name	Type	Description	9DBV09xx Pin No.	9DBV07xx Pin No.	9DBV05xx Pin No.
VDDR1.8	Power	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 1.8V.	5	5	4
vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	14	13	12
vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	17	21	17
vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	25	24	24
vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	28	29	29
vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	34	35	1
vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	37	38	—
vOE6#	Input	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	43	2	—
vOE7#	Input	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	46	—	—
vOE8#	Input	Active low input for enabling output 8. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	2	—	—
vSADR_tri	Latched In	Tri-level latch to select SMBus Address. It has an internal pull-down resistor. See SMBus Address Selection table.	1	1	32

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV05x1/9DBV07x1/9DBV09x1. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DD}x$	Applies to V_{DD}, V_{DDA} and V_{DDIO}.	-0.5		2.5	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD} + 0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins.			3.6	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

Thermal Characteristics

Table 3. Thermal Characteristics

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
9DBV09x1 Thermal Resistance	θ_{JC}	Junction to case.	NDG48	33	°C/W	1
	θ_{Jb}	Junction to base.		2	°C/W	1
	θ_{JA0}	Junction to air, still air.		37	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		30	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		27	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		26	°C/W	1
9DBV07x1 Thermal Resistance	θ_{JC}	Junction to case.	NDG40	42	°C/W	1
	θ_{Jb}	Junction to base.		2	°C/W	1
	θ_{JA0}	Junction to air, still air.		39	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		33	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		28	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		27	°C/W	1

Table 3. Thermal Characteristics (Cont.)

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
9DBV05x1 Thermal Resistance	θ_{JC}	Junction to case.	NLG32	42	°C/W	1
	θ_{Jb}	Junction to base.		2	°C/W	1
	θ_{JA0}	Junction to air, still air.		39	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		33	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		28	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		27	°C/W	1

[1] EPAD soldered to ground.

Electrical Characteristics

$T_A = T_{COM}$ or T_{IND}. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 4. Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Crossover voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	40		60	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 5. Input/Supply/Common Parameters–Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DD}x$	Supply voltage for core and analog.	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDIO}	Supply voltage for DIF outputs, if present.	0.9975	1.05 - 1.8	1.9	V	
Ambient Operating Temperature	T_{AMB}	Commercial range (T_{COM}).	0	25	70	°C	
		Industrial range (T_{IND}).	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix).	0.4 V_{DD}		0.6 V_{DD}	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus.	-0.3		0.25 V_{DD}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, $V_{IN} = V_{DD}$.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors.	-200		200	µA	

Table 5. Input/Supply/Common Parameters–Normal Operating Conditions (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Frequency	F_{IN}		1		200	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1, 6
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.			1	ms	1, 2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular modulation).	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable frequency for non-PCIe applications (Triangular modulation).	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# deassertion.			300	µs	1,3
Tfall	t_F	Fall time of single-ended control inputs.			5	ns	2
Trise	t_R	Rise time of single-ended control inputs.			5	ns	2
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V, see note 4 for VDDSMB < 3.3V.			0.8	V	4
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V, see note 5 for VDDSMB < 3.3V.	2.1		3.3	V	5
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		1.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency.			400	kHz	7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] For V_{DDSMB} < 3.3V, V_{ILSMB} < = 0.35V_{DDSMB}.

[5] For V_{DDSMB} < 3.3V, V_{ILSMB} < = 0.65V_{DDSMB}.

[6] DIF_IN input.

[7] The differential input clock must be running for the SMBus to be active.

Table 6. Current Consumption – 9DBV09x1

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDR}	V_{DDR} at 100MHz.		3	5	mA	
	I_{DDDIG}	V_{DDIG}, all outputs at 100MHz.		6	10	mA	
	I_{DDO}	$V_{DDO1.8}$ + V_{DDIO}, all outputs at 100MHz.		35	40	mA	
Power Down Current	I_{DDRPD}	V_{DDR}, CKPWRGD_PD# = 0.		0.4	1	mA	1
	$I_{DDDIGPD}$	V_{DDIG}, CKPWRGD_PD# = 0.		0.6	1	mA	1
	I_{DDOPD}	$V_{DDO1.8}$ + V_{DDIO}, CKPWRGD_PD# = 0.		0.002	0.1	mA	1

[1] Input clock stopped.

Table 7. Current Consumption – 9DBV07x1

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDR}	V_{DDR} at 100MHz.		3	5	mA	
	I_{DDDIG}	V_{DDIG}, all outputs at 100MHz.		5	8	mA	
	I_{DDO}	$V_{DDO1.8}$ + V_{DDIO}, all outputs at 100MHz.		26	32	mA	
Power Down Current	I_{DDRPD}	V_{DDR}, CKPWRGD_PD# = 0.		0.4	1	mA	1
	$I_{DDDIGPD}$	V_{DDIG}, CKPWRGD_PD# = 0.		0.5	1	mA	1
	I_{DDOPD}	$V_{DDO1.8}$ + V_{DDIO}, CKPWRGD_PD# = 0.		0.0005	0.10	mA	1

[1] Input clock stopped.

Table 8. Current Consumption – 9DBV05x1

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDR}	V_{DDR} at 100MHz.		2	3	mA	
	I_{DDDIG}	V_{DDIG}, all outputs at 100MHz.		0.2	0.5	mA	
	I_{DDO}	$V_{DDO1.8}$, all outputs at 100MHz.		23	27	mA	
Power Down Current	I_{DDRPD}	V_{DDR}, CKPWRGD_PD# = 0.		0.001	0.1	mA	1
	$I_{DDDIGPD}$	V_{DDIG}, CKPWRGD_PD# = 0.		0.2	0.3	mA	1
	I_{DDOPD}	$V_{DDO1.8}$, CKPWRGD_PD# = 0.		0.4	0.8	mA	1

[1] Input clock stopped.

Table 9. Output Duty Cycle, Jitter, Skew and PLL Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially at 100MHz.	-1	0	1	%	1,3
Skew, Input to Output	t_{pdBYP}	V_T = 50%.	1800	2421	3000	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%.		29	60	ps	1, 4
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	*Additive* jitter.		1.1	5	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock

[4] All outputs at default slew rate.

Table 10. LP-HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast slew rate setting.	1.6	2.9	4.3	1–4	V/ns	1,2,3
		Scope averaging on, slow slew rate setting.	1.2	2.0	3.3		V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		6	18	20	%	1,4,7
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	694	804	976.8	660–1150	mV	7,8
Minimum Voltage	Vmin		-108	-18		-300		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	303	405	507	250–550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		12	50	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 33Ω for Zo = 50Ω (100Ω differential trace impedance)

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings. 660mV V_{HIGH} is the minimum when V_{DDIO} is >= 1.05V ±5%. If V_{DDIO} is < 1.05V ±5%, the minimum V_{HIGH} will be V_{DDIO}min - 250mV. For example, for V_{DDIO} = 0.9V ±5%, V_{HIGH}min will be 860mV - 250mV = 610mV.

[8] Includes previously separate values of +300mV overshoot and -300mV of undershoot.

Table 11. Additive PCIe Phase Jitter for Fanout Buffer Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limits	Units	Notes
Additive PCIe Phase Jitter, Fanout Buffer Mode[7] (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s)		1.7	3.0	86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)		0.033	0.049	3	ps (RMS)	1,2
		PCIe Gen 2 Lo Band (5.0 GT/s)		0.122	0.199	3.1	ps (RMS)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s)		0.059	0.098	1	ps (RMS)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s)		0.059	0.098	0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s)		0.023	0.038	0.15	ps (RMS)	1,2,3,5
Additive PCIe Phase Jitter, Fanout Buffer Mode[7] (SRIS Architecture)	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1 (2.5 GT/s)		0.175	0.275	N/A	ps (RMS)	1,2,6
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (5.0 GT/s)		0.156	0.247		ps (RMS)	1,2,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (8.0 GT/s)		0.041	0.064		ps (RMS)	1,2,6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (16.0 GT/s)		0.043	0.066		ps (RMS)	1,2,6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen 5 (32.0 GT/s)		0.036	0.059		ps (RMS)	1,2,6

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. If oscilloscope data is used, equipment noise is removed from all results.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/$\sqrt{2}$ = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/$\sqrt{2}$ = 0.5ps RMS if the clock chip is near the clock input.

[7] Additive jitter for RMS values is calculated by solving for "b" where $b = \sqrt{(c^2 - a^2)}$ and "a" is rms input jitter and "c" is rms output jitter.

Table 12. Phase Jitter Parameters – 12kHz to 20MHz

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
12kHz–20MHz Additive Phase Jitter, Fanout Buffer Mode	$t_{jph12k-20MFOB}$	Fanout Buffer Mode, SSC OFF, 100MHz		156		N/A	fs (RMS)	1,2,3

[1] Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values, additive jitter is calculated by solving for "b" where $b = \sqrt{(c^2 - a^2)}$, "a" is rms input jitter and "c" is rms total jitter.

Power Management

Table 13. Power Management

CKPWRGD_PD#	CLK_IN	SMBus EN bit	OE[x]# Pin	DIF[x]
0	X	X	X	Low/Low
1	Running	0	X	Low/Low
1	Running	1	0	Low/Low
1	Running	1	1	Running

Test Loads

Figure 4. Test Load for AC/DC Measurements

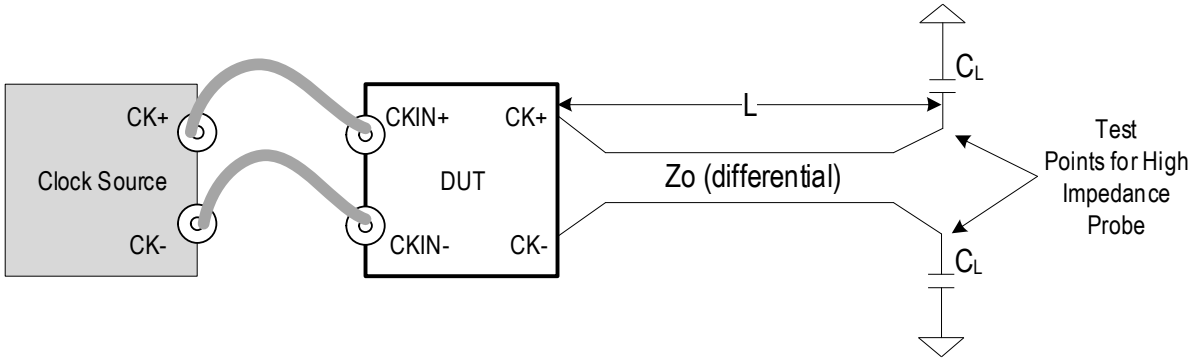


Table 14. Parameters for AC/DC Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Parameters Measured
SMA100B	9DBVxx3x	33 External	100	12.7	2	AC/DC parameters
SMA100B	9DBVxx3x	24 External	85	12.7	2	
SMA100B	9DBVxx4x	Internal	100	12.7	2	

Figure 5. Test Load for Phase Jitter Measurements using Phase Noise Analyzer

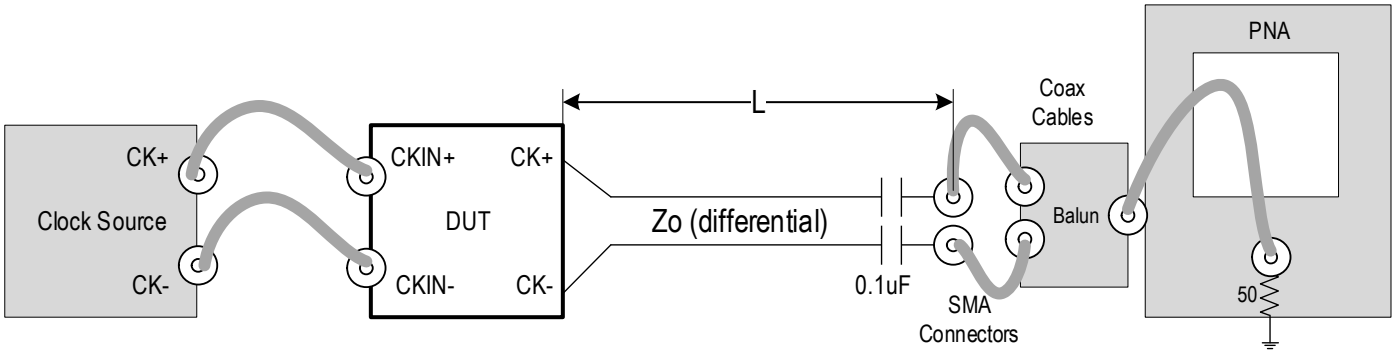


Table 15. Parameters for Phase Jitter Measurements using Phase Noise Analyzer

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Parameters Measured
SMA100B	9DBVxx3x	33 External	100	12.7	2	PCIe
SMA100B	9DBVxx3x	24 External	85	12.7	2	
SMA100B	9DBVxx4x	Internal	100	12.7	2	

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 16. SMBus Address Selection

	SADR	Address	+ Read/Write Bit
State of SADR_tri on first application of CKPWRGD_PD#	0	1101011	X
	M	1101100	X
	1	1101101	X

Table 17. Byte 0: Output Enable Register 1

Byte 0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output Enable							
Type	R/W							
0	Low/Low							
1	OE# Pin Control							
9DBV09xx Name	DIF7_en	DIF6_en	DIF5_en	DIF4_en	DIF3_en	DIF2_en	DIF1_en	DIF0_en
9DBV09xx Default	1	1	1	1	1	1	1	1
9DBV07xx Name	DIF5_en	DIF4_en	Reserved	DIF3_en	DIF2_en	DIF1_en	Reserved	DIF0_en
9DBV07xx Default	1	1	1	1	1	1	1	1
9DBV05xx Name	Reserved	DIF3_en	DIF2_en	Reserved	DIF1_en	Reserved	DIF0_en	Reserved
9DBV05xx Default	1	1	1	1	1	1	1	1

Table 18. Byte 1: Output and Amplitude Control Register

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved Default is 0	Reserved Default is 1	Output _enable	Reserved Default is 1	Reserved Default is 1	Reserved Default is 0	Controls Output Amplitude	
Type			RW				RW	RW
0			Low/Low				00 = 0.6V	01 = 0.7V
1			OE# Pin Control				10= 0.8V	11 = 0.9V
9DBV09xx Name			DIF8_en				Amplitude(1) Default is 1	Amplitude(0) Default is 0
9DBV09xx Default			1					
9DBV07xx Name			DIF6_en					
9DBV07xx Default			1					
9DBV05xx Name			DIF4_en					
9DBV05xx Default			1					

Table 19. Byte 2: Slew Rate Control Register

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Slew Rate Adjustment							
Type	RW							
0	Slow Setting							
1	Fast Setting							
9DBV09xx Name	Slewrate DIF7	Slewrate DIF6	Slewrate DIF5	Slewrate DIF4	Slewrate DIF3	Slewrate DIF2	Slewrate DIF1	Slewrate DIF0
9DBV09xx Default	1	1	1	1	1	1	1	1
9DBV07xx Name	Slewrate DIF5	Slewrate DIF4	Reserved	Slewrate DIF3	Slewrate DIF2	Slewrate DIF1	Reserved	Slewrate DIF0
9DBV07xx Default	1	1	1	1	1	1	1	1
9DBV05xx Name	Reserved	Slewrate DIF3	Slewrate DIF2	Reserved	Slewrate DIF1	Reserved	Slewrate DIF0	Reserved
9DBV05xx Default	1	1	1	1	1	1	1	1

Table 20. Byte 3: Slew Rate Control Register

Byte 3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved Default is 1	Reserved Default is 1	Reserved Default is 0	Reserved Default is 0	Reserved Default is 0	Reserved Default is 1	Reserved Default is 1	Slew Rate Adjustment
Type								RW
0								Slow Setting
1								Fast Setting
9DBV09xx Name								Slewrate DIF8
9DBV09xx Default								1
9DBV07xx Name								Slewrate DIF6
9DBV07xx Default								1
9DBV05xx Name								Slewrate DIF4
9DBV05xx Default								1

Byte 4: Reserved Register – default is 0hFF

Table 21. Byte 5: Revision and Vendor ID Register

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				Vendor ID			
Type	R	R	R	R	R	R	R	R
0	A rev = 0010				IDT/Renesas = 0001			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0
Default	0	0	0	0	0	0	0	1

Table 22. Byte 6: Device ID Register

Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Device Type		Device ID					
Type	R	R	R	R	R	R	R	R
0	00 = FG, 01 = ZDB 10 = Mux, 11 = Fanout Buffer		Device ID					
1								
Name	Device Type 1	Device Type 0	DevID 5	DevID 4	DevID 3	DevID 2	DevID 1	DevID 0
9DBV09xx	0hC9							
9DBV07xx	0hC7							
9DBV05xx	0hC5							

Table 23. Byte 7: Byte Count Register

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Writing to this register configures how many bytes will be read back on a block read.				
Type				RW	RW	RW	RW	RW
0				Default value is 0b01000				
1								
Name				BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	1	0	0	0

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

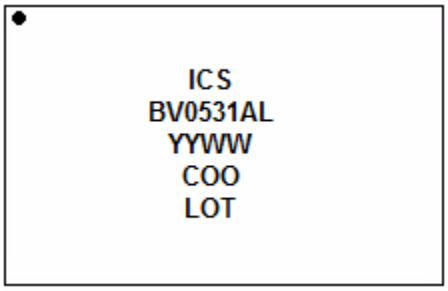
9DBV05x1:
www.idt.com/document/psc/32-vfqfpn-package-outline-drawing-50-x-50-x-090-mm-body-epad-315-x-315-mm-nlg32p1

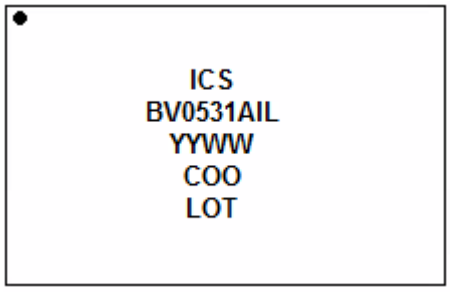
9DBV07x1:
www.idt.com/document/psc/ndndg40-package-outline-50-x-50-mm-bodyepad-350mm-sq-040-mm-pitch-qfn

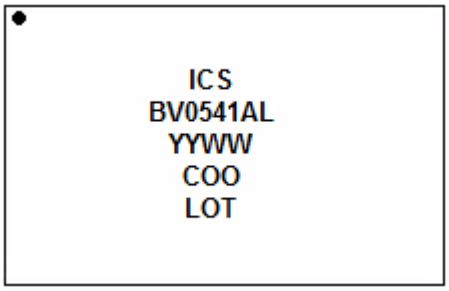
9DBV09x1:
www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-41-x-41-mm-040mm-pitch-ndg48p1

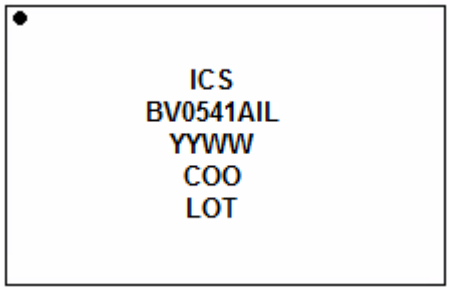
Marking Diagrams

9DBV05x1



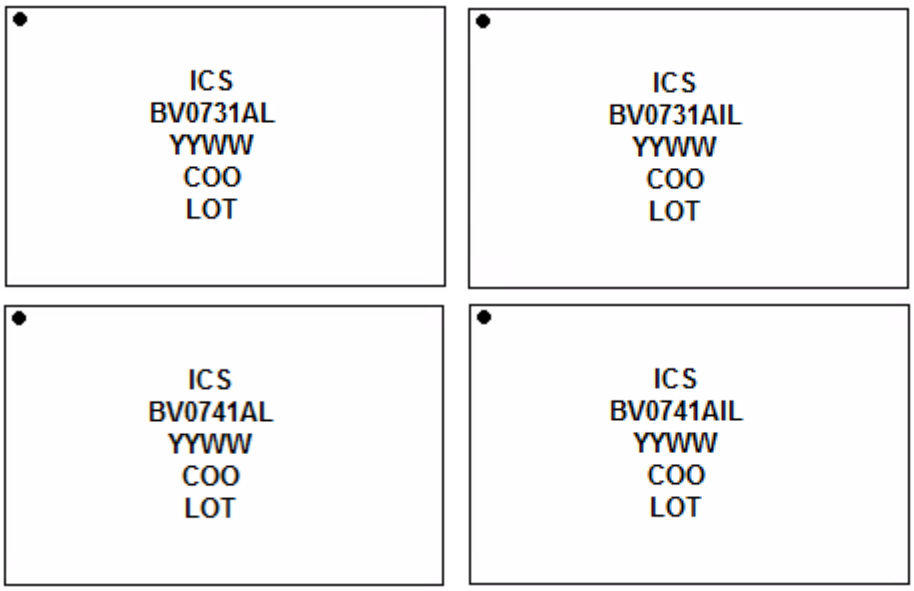






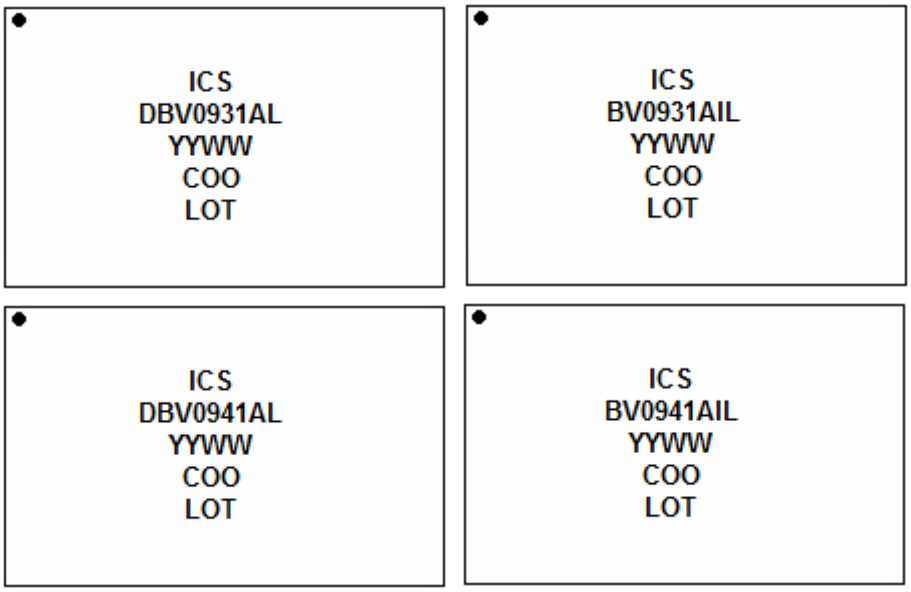
- Lines 1 and 2: truncated part number (“I” denotes industrial temperature range)
- Line 3: “YYWW” is the last two digits of the year and the work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” denotes the lot number.

9DBV07x1



- Lines 1 and 2: truncated part number ("I" denotes industrial temperature range)
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

9DBV09x1



- Lines 1 and 2: truncated part number ("I" denotes industrial temperature range)
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

Ordering Information

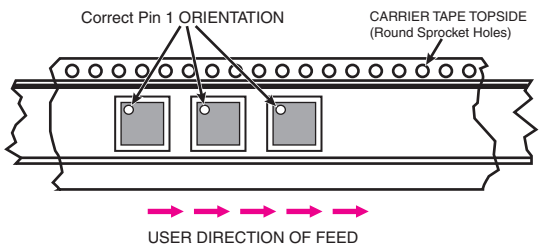
Table 24. Ordering Information

Number of Clock Outputs	Output Impedance	Orderable Part Number	Package	Temperature Range	Part Number Suffix and Shipping Method
5	33	9DBV0531AKILF	5 × 5 × 0.5 mm 32-VFQFPN	-40°C to +85°C	None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 25 for more details)
		9DBV0531AKILFT			
	100	9DBV0541AKILF			
		9DBV0541AKILFT			
7	33	9DBV0731AKILF	5 × 5 × 0.4 mm 40-VFQFPN		
		9DBV0731AKILFT			
	100	9DBV0741AKILF			
		9DBV0741AKILFT			
9	33	9DBV0931AKILF	6 × 6 × 0.4 mm 48-VFQFPN		
		9DBV0931AKILFT			
	100	9DBV0941AKILF			
		9DBV0941AKILFT			
5	33	9DBV0531AKLF	5 × 5 × 0.5 mm 32-VFQFPN	0°C to +70°C	None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 25 for more details)
		9DBV0531AKLFT			
	100	9DBV0541AKLF			
		9DBV0541AKLFT			
7	33	9DBV0731AKLF	5 × 5 × 0.4 mm 40-VFQFPN		
		9DBV0731AKLFT			
	100	9DBV0741AKLF			
		9DBV0741AKLFT			
9	33	9DBV0931AKLF	6 × 6 × 0.4 mm 48-VFQFPN		
		9DBV0931AKLFT			
	100	9DBV0941AKLF			
		9DBV0941AKLFT			

"A" is the device revision designator (will not correlate with the datasheet revision).

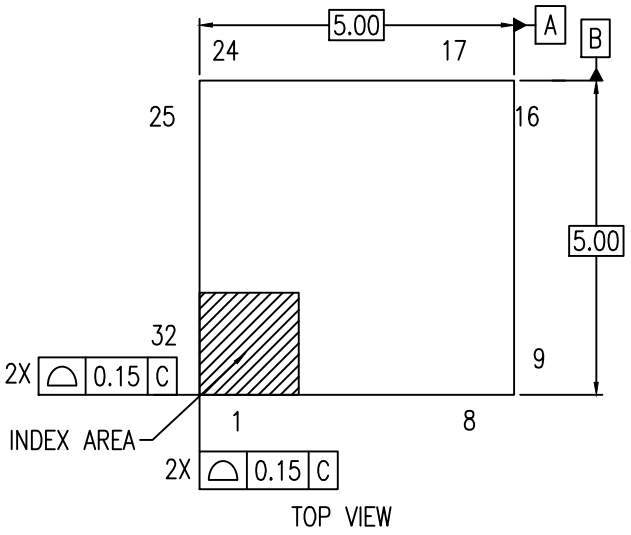
"LF" denotes Pb-free configuration, RoHS compliant; "T" denotes the orderable suffix for Tape and Reel.

Table 25. Pin 1 Orientation in Tape and Reel Packaging

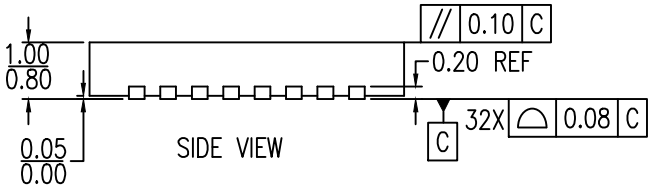
Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	

Revision History

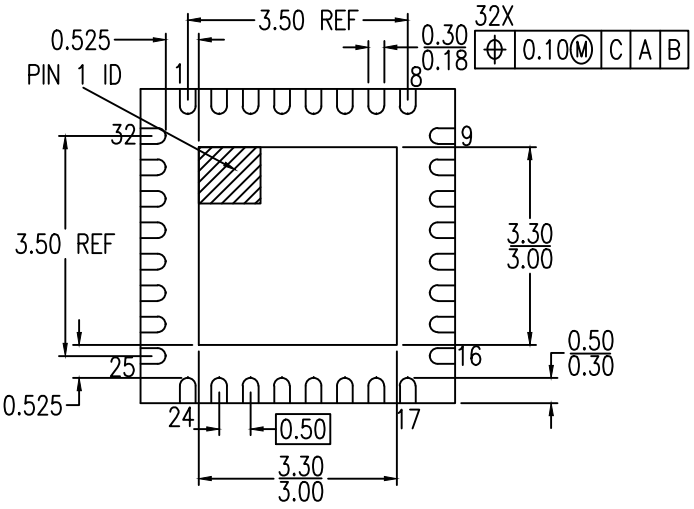
Revision Date	Description of Change
June 30, 2020	▪ Merged duplicate pin names in table 1 into single rows and combined pin numbers into a single row for the duplicate pin names. Rows merged were VDDIO, VDDO1.8, and GND. ▪ Removed duplicate table subtitle "T_A = T_{COM} or T_{IND}. Supply voltages per normal operation conditions; see Test Loads for loading conditions" from Tables 10, 11 and 12. This phrase is at the beginning of the Electrical Characteristics section and applies to all electrical tables. ▪ Corrected PCIe SRIS maximum values in Table 11. They were shifted down by one cell.
February 13, 2020	▪ Corrected 9DBV05xx pin number typos in pin description table. ▪ Rebranded datasheet.
October 22, 2019	Combined 9DBV0531_0541, 9DBV0731_741, and 9DBV0931_941 datasheets into one single document.
March 10, 2017	Last revision date of the 9DBV0531 datasheet.
May 30, 2017	Last revision date of the 9DBV0541 datasheet.
March 10, 2017	Last revision date of the 9DBV0731 datasheet.
March 10, 2017	Last revision date of the 9DBV0741 datasheet.
March 14, 2017	Last revision date of the 9DBV0931 datasheet.
March 14, 2017	Last revision date of the 9DBV0941 datasheet.



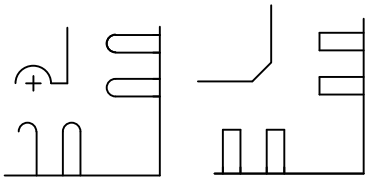
TOP VIEW



SIDE VIEW

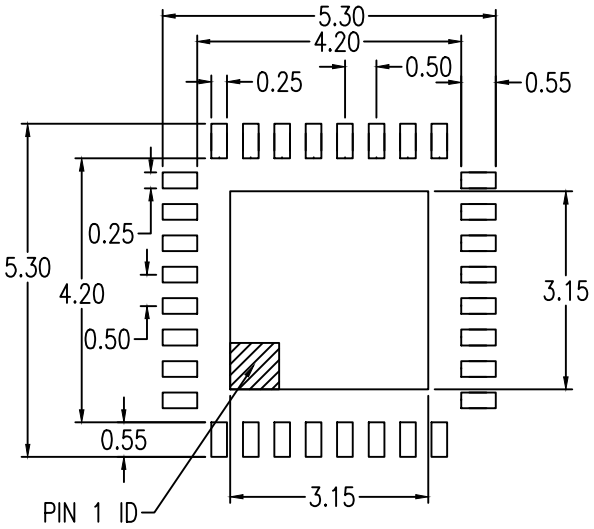


BOTTOM VIEW



PIN #1 ID OPTION

NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIE TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PIN LOCATION IS UNDENTIFIED BY EITHER CHAMFER OR NOTCH.

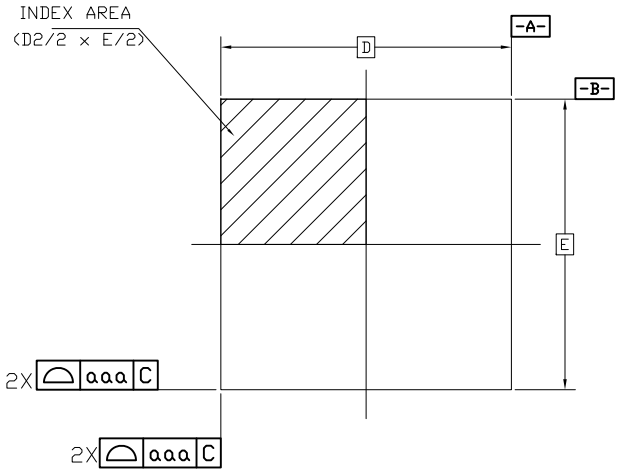


RECOMMENDED LAND PATTERN DIMENSION

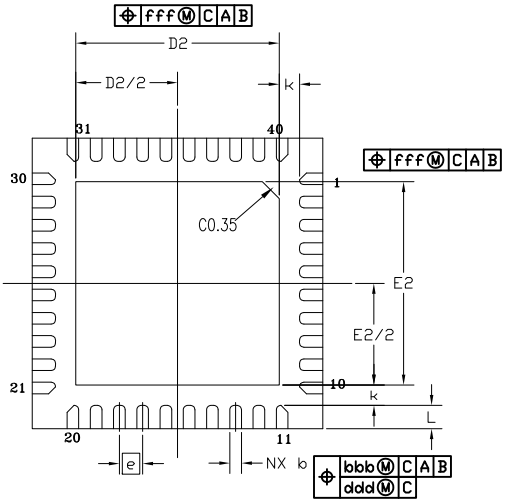
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
April 12, 2018	Rev 02	New Format
Feb 8, 2016	Rev 01	Added "k: Value

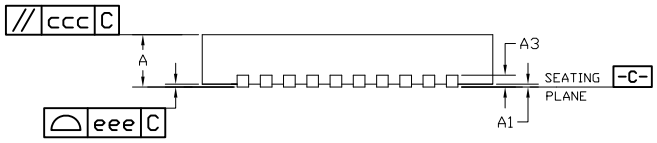
RE	
REV	DESCRI
00	INITIAL R



TOP VIEW



BOTTOM VIEW



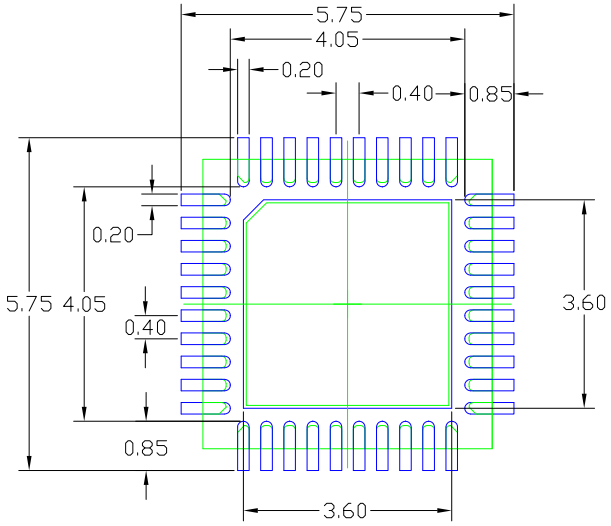
SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2 ALL DIMENSIONS ARE IN MILLIMETERS.
3. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

TOLERANCES UNLESS SPECIFIED DECIMAL X±.1 XX±.05 XXX± .030 ANGULAR ±1°		
APPROVALS	DATE	TITLE
DRAWN ma	05/31/10	
CHECKED		
		SIZE C
		DO NO

RE	
REV	DESCRI
00	INITIAL R



RECOMMENDED LAND PATTERN

NOTES:

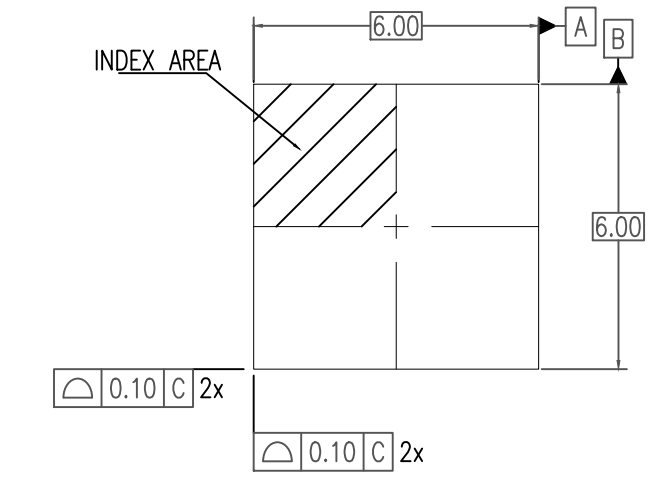
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL X±.1 XX±.05 XXX± .030 ANGULAR ±1°		
APPROVALS	DATE	TITLE
DRAWN mx	05/31/10	
CHECKED		
		SIZE C
		DO N

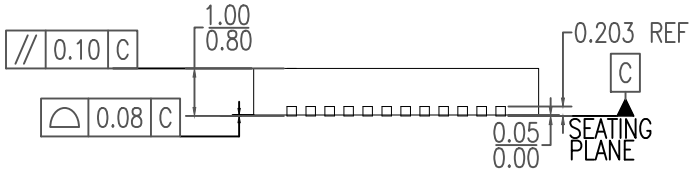
48-VFQFPN Package Outline Drawing

6.0 x 6.0 x 0.90 mm Body, Epad 4.1x 4.1 mm, 0.40mm Pitch

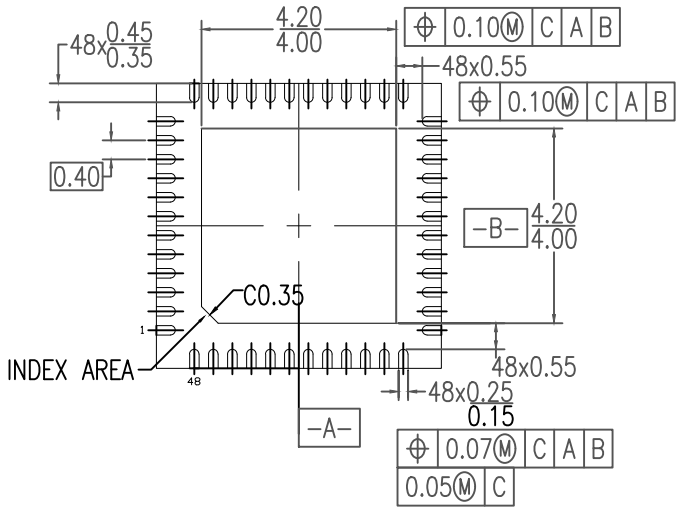
NDG48P1, PSC-4212-01, Rev 01, Page 1



TOP VIEW



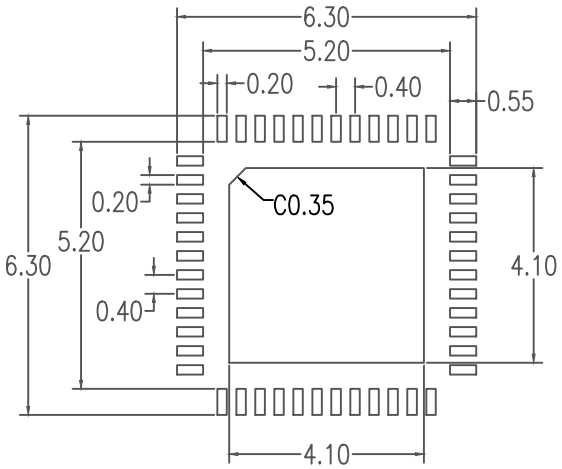
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Aug16, 2018	Rev 01	New Format Change QFN to VFQFPN, Recalculate Land Pattern
May 6, 2016	Rev 00	Add Chamfer

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