

## General Description

The 9DMU0431 is a member of IDT's SOC-Friendly 1.5V Ultra-Low-Power (ULP) PCIe Gen1-2-3 family. Each of the 4 outputs has its own dedicated OE# pin for optimal system control and power management. The part provides asynchronous and glitch-free switching modes.

## Recommended Application

2:4 PCIe Gen1-2-3 clock multiplexer

## Output Features

- 4 – Low-Power (LP) HCSL DIF pair

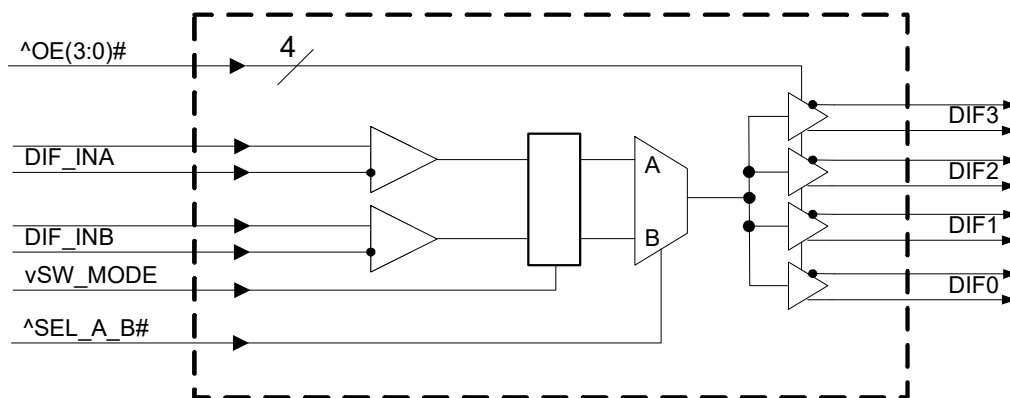
## Key Specifications

- DIF *additive* cycle-to-cycle jitter <5ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Additive phase jitter @ 125MHz: 535fs rms typical (12kHz to 20MHz)
- DIF output-to-output skew <50ps

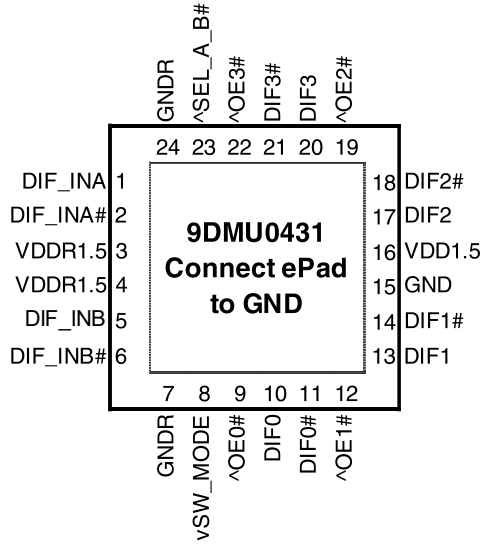
## Features/Benefits

- LP-HCSL outputs; save 8 resistors compared to standard HCSL outputs
- 1.5V operation; 31mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Spread Spectrum Compatible; supports EMI reduction
- OE# pins; support DIF power management
- HCSL differential inputs; can be driven by common clock sources
- 1MHz to 167MHz operating frequency
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

## Block Diagram



## Pin Configuration



**24 VFQFPN, 4x4 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor  
v prefix indicates internal 120KOhm pull down resistor

### Power Management Table

| OEx# Pin | DIF_IN  | DIFx     |           |
|----------|---------|----------|-----------|
|          |         | True O/P | Comp. O/P |
| 0        | Running | Running  | Running   |
| 1        | Running | Low      | Low       |

### Power Connections

| Pin Number |     | Description             |
|------------|-----|-------------------------|
| VDD        | GND |                         |
| 3          | 24  | Input A receiver analog |
| 4          | 7   | Input B receiver analog |
| 16         | 15  | DIF outputs             |

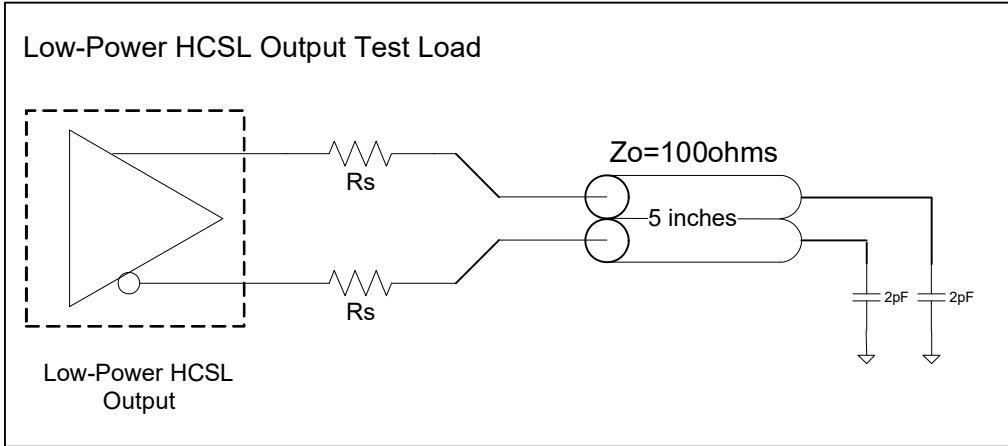
## Pin Descriptions

| Pin# | Pin Name | Type | Pin Description  |
|------|----------|------|--|
| 1    | DIF_INA  | IN   | HCSL Differential True input   |
| 2    | DIF_INA# | IN   | HCSL Differential Complement Input   |
| 3    | VDDR1.5  | PWR  | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.   |
| 4    | VDDR1.5  | PWR  | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.   |
| 5    | DIF_INB  | IN   | HCSL Differential True input   |
| 6    | DIF_INB# | IN   | HCSL Differential Complement Input   |
| 7    | GNDR     | GND  | Analog Ground pin for the differential input (receiver)  |
| 8    | vSW_MODE | IN   | Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms.<br>0 = asynchronous mode<br>1 = glitch-free mode |
| 9    | ^OE0#    | IN   | Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor.<br>1 =disable outputs, 0 = enable outputs   |
| 10   | DIF0     | OUT  | Differential true clock output   |
| 11   | DIF0#    | OUT  | Differential Complementary clock output  |
| 12   | ^OE1#    | IN   | Active low input for enabling DIF pair 1. This pin has an internal pull-up resistor.<br>1 =disable outputs, 0 = enable outputs   |
| 13   | DIF1     | OUT  | Differential true clock output   |
| 14   | DIF1#    | OUT  | Differential Complementary clock output  |
| 15   | GND      | GND  | Ground pin.  |

## Pin Descriptions (cont.)

| Pin# | Pin Name  | Type | Pin Description   |
|------|-----------|------|---|
| 16   | VDD1.5    | PWR  | Power supply, nominally 1.5V  |
| 17   | DIF2      | OUT  | Differential true clock output  |
| 18   | DIF2#     | OUT  | Differential Complementary clock output   |
| 19   | ^OE2#     | IN   | Active low input for enabling DIF pair 2. This pin has an internal pull-up resistor.<br>1 =disable outputs, 0 = enable outputs  |
| 20   | DIF3      | OUT  | Differential true clock output  |
| 21   | DIF3#     | OUT  | Differential Complementary clock output   |
| 22   | ^OE3#     | IN   | Active low input for enabling DIF pair 3. This pin has an internal pull-up resistor.<br>1 =disable outputs, 0 = enable outputs  |
| 23   | ^SEL_A_B# | IN   | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor.<br>0 = Input B selected, 1 = Input A selected. |
| 24   | GNDR      | GND  | Analog Ground pin for the differential input (receiver)   |
| 25   | EPAD      | GND  | Connect to Ground.  |

## Test Loads

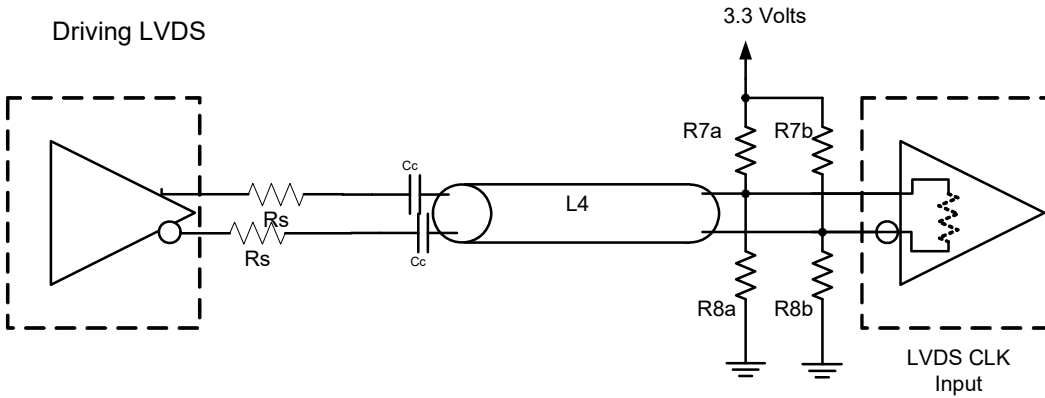


### Alternate Differential Output Terminations

| $R_s$ | $Z_o$ | Units |
|-------|-------|-------|
| 33    | 100   | Ohms  |
| 27    | 85    |       |

## Driving LVDS

### Driving LVDS



### Driving LVDS inputs

| Component | Value                    |                                    | Note |
|-----------|--------------------------|------------------------------------|------|
|           | Receiver has termination | Receiver does not have termination |      |
| R7a, R7b  | 10K ohm                  | 140 ohm                            |      |
| R8a, R8b  | 5.6K ohm                 | 75 ohm                             |      |
| Cc        | 0.1 uF                   | 0.1 uF                             |      |
| Vcm       | 1.2 volts                | 1.2 volts                          |      |

## Electrical Characteristics–Absolute Maximum Ratings

| PARAMETER                 | SYMBOL             | CONDITIONS                | MIN  | TYP | MAX                  | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|----------------------|-------|-------|
| Supply Voltage            | VDDx               |                           | -0.5 |     | 2                    | V     | 1,2   |
| Input Voltage             | V <sub>IN</sub>    |                           | -0.5 |     | V <sub>DD</sub> +0.5 | V     | 1,3   |
| Input High Voltage, SMBus | V <sub>IHSMB</sub> | SMBus clock and data pins |      |     | 3.3                  | V     | 1     |
| Storage Temperature       | T <sub>S</sub>     |                           | -65  |     | 150                  | °C    | 1     |
| Junction Temperature      | T <sub>J</sub>     |                           |      |     | 125                  | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model          | 2000 |     |                      | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup>Not to exceed 2.0V.

## Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

T<sub>A</sub> = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                              | SYMBOL                 | CONDITIONS  | MIN                  | TYP | MAX                   | UNITS  | NOTES |
|--|------------------------|---|----------------------|-----|-----------------------|--------|-------|
| Supply Voltage                         | VDDx                   | Supply voltage for core and analog  | 1.425                | 1.5 | 1.575                 | V      |       |
| Ambient Operating Temperature          | T <sub>AMB</sub>       | Industrial range  | -40                  | 25  | 85                    | °C     | 1     |
| Input High Voltage                     | V <sub>IH</sub>        | Single-ended inputs, except SMBus   | 0.75 V <sub>DD</sub> |     | V <sub>DD</sub> + 0.3 | V      |       |
| Input Low Voltage                      | V <sub>IL</sub>        | Single-ended inputs, except SMBus   | -0.3                 |     | 0.25 V <sub>DD</sub>  | V      |       |
| Input Current                          | I <sub>IN</sub>        | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5                   |     | 5                     | µA     |       |
|  | I <sub>INP</sub>       | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200                 |     | 200                   | µA     |       |
| Input Frequency                        | F <sub>in</sub>        |   | 1                    |     | 167                   | MHz    | 2     |
| Pin Inductance                         | L <sub>pin</sub>       |   |                      |     | 7                     | nH     | 1     |
| Capacitance                            | C <sub>IN</sub>        | Logic Inputs, except DIF_IN   | 1.5                  |     | 5                     | pF     | 1     |
|  | C <sub>INDIF_IN</sub>  | DIF_IN differential clock inputs  | 1.5                  |     | 2.7                   | pF     | 1,4   |
|  | C <sub>OUT</sub>       | Output pin capacitance  |                      |     | 6                     | pF     | 1     |
| Clk Stabilization                      | T <sub>STAB</sub>      | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |                      |     | 1                     | ms     | 1,2   |
| Input SS Modulation Frequency PCIe     | f <sub>MODINPCIe</sub> | Allowable Frequency for PCIe Applications (Triangular Modulation)   | 30                   |     | 33                    | kHz    |       |
| Input SS Modulation Frequency non-PCIe | f <sub>MODIN</sub>     | Allowable Frequency for non-PCIe Applications (Triangular Modulation)   | 0                    |     | 66                    | kHz    |       |
| OE# Latency                            | t <sub>LATOE#</sub>    | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 1                    |     | 3                     | clocks | 1,3   |
| Tfall                                  | t <sub>F</sub>         | Fall time of single-ended control inputs  |                      |     | 5                     | ns     | 2     |
| Trise                                  | t <sub>R</sub>         | Rise time of single-ended control inputs  |                      |     | 5                     | ns     | 2     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup> DIF\_IN input

## Electrical Characteristics–Clock Input Parameters

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                          | SYMBOL             | CONDITIONS  | MIN                   | TYP | MAX  | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN        | V <sub>IHDIF</sub> | Differential inputs<br>(single-ended measurement)             | 300                   | 750 | 1150 | mV    | 1     |
| Input Low Voltage - DIF_IN         | V <sub>ILDIF</sub> | Differential inputs<br>(single-ended measurement)             | V <sub>SS</sub> - 300 | 0   | 300  | mV    | 1     |
| Input Common Mode Voltage - DIF_IN | V <sub>COM</sub>   | Common Mode Input Voltage                                     | 200                   |     | 725  | mV    | 1     |
| Input Amplitude - DIF_IN           | V <sub>SWING</sub> | Peak to Peak value (V <sub>IHDIF</sub> - V <sub>ILDIF</sub> ) | 300                   |     | 1450 | mV    | 1     |
| Input Slew Rate - DIF_IN           | dv/dt              | Measured differentially                                       | 0.35                  |     | 8    | V/ns  | 1,2   |
| Input Leakage Current              | I <sub>IN</sub>    | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND     | -5                    |     | 5    | uA    |       |
| Input Duty Cycle                   | d <sub>in</sub>    | Measurement from differential waveform                        | 45                    | 50  | 55   | %     | 1     |
| Input Jitter - Cycle to Cycle      | J <sub>DIFin</sub> | Differential Measurement                                      | 0                     |     | 150  | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

## Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL                 | CONDITIONS  | MIN  | TYP  | MAX  | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------|-------|
| Slew rate              | dV/dt                  | Scope averaging on, fast setting  | 1.2  | 2.5  | 4.2  | V/ns  | 1,2,3 |
| Slew rate matching     | ΔdV/dt                 | Slew rate matching, Scope averaging on  |      | 10   | 20   | %     | 1,2,4 |
| Voltage High           | V <sub>HIGH</sub>      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 550  | 761  | 850  | mV    |       |
| Voltage Low            | V <sub>LOW</sub>       |   | -150 | 33   | 150  |       |       |
| Max Voltage            | V <sub>max</sub>       | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      | 800  | 1150 | mV    |       |
| Min Voltage            | V <sub>min</sub>       |   | -300 | -1   |      |       |       |
| Vswing                 | Vswing                 | Scope averaging off   | 300  | 1457 |      | mV    | 1,2   |
| Crossing Voltage (abs) | V <sub>cross_abs</sub> | Scope averaging off   | 250  | 404  | 550  | mV    | 1,5   |
| Crossing Voltage (var) | Δ-V <sub>cross</sub>   | Scope averaging off   |      | 15   | 140  | mV    | 1,6   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting Δ-V<sub>cross</sub> to be smaller than V<sub>cross</sub> absolute.

## Electrical Characteristics–Current Consumption

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                | SYMBOL            | CONDITIONS                      | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------|---------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I <sub>DD</sub>   | VDD, All outputs active @100MHz |     | 19  | 27  | mA    | 1     |
| Powerdown Current        | I <sub>DDPD</sub> | VDD, all outputs disabled       |     | 1.4 | 2.5 | mA    | 1, 2  |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input clock stopped.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL               | CONDITIONS                                   | MIN  | TYP   | MAX  | UNITS | NOTES |
|------------------------|----------------------|--|------|-------|------|-------|-------|
| Duty Cycle Distortion  | t <sub>DCD</sub>     | Measured differentially, Bypass Mode @100MHz | -1   | -0.05 | 1    | %     | 1,3   |
| Skew, Input to Output  | t <sub>pdBYP</sub>   | Bypass Mode, V <sub>T</sub> = 50%            | 2046 | 2864  | 4010 | ps    | 1     |
| Skew, Output to Output | t <sub>sk3</sub>     | V <sub>T</sub> = 50%                         |      | 19    | 50   | ps    | 1,4   |
| Jitter, Cycle to cycle | t <sub>jyc-cyc</sub> | Additive Jitter in Bypass Mode               |      | 0.1   | 5    | ps    | 1,2   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

Measured from differential waveform

<sup>4</sup> All outputs at default slew rate

<sup>5</sup> The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics–Phase Jitter Parameters

TA = T<sub>AMB</sub>, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                          | SYMBOL  | CONDITIONS  | MIN | TYP   | MAX | INDUSTRY LIMIT | UNITS    | Notes     |
|------------------------------------|---|---|-----|-------|-----|----------------|----------|-----------|
| Additive Phase Jitter, Bypass Mode | t <sub>jphPCleG1</sub>  | PCIe Gen 1  |     | 1.3   | 5   | N/A            | ps (p-p) | 1,2,3,5   |
|                                    | t <sub>jphPCleG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz  |     | 0.1   | 0.5 | N/A            | ps (rms) | 1,2,3,4,5 |
|                                    |   | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)                                  |     | 0.1   | 0.6 | N/A            | ps (rms) | 1,2,3,4   |
|                                    | t <sub>jphPCleG3</sub>  | PCIe Gen 3<br>(PLL BW of 2-4 or 2-5MHz, CDR = 10MHz)                                  |     | 0.170 | 0.3 | N/A            | ps (rms) | 1,2,3,4   |
|                                    | t <sub>jph125M0</sub>   | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz |     | 365   | 380 | N/A            | fs (rms) | 1,6       |
| t <sub>jph125M1</sub>              | 125MHz, 12KHz to 20MHz, -20dB/decade rollover < 12kHz, -40db/decade rolloff > 20MHz |   | 535 | 550   | N/A | fs (rms)       | 1,6      |           |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

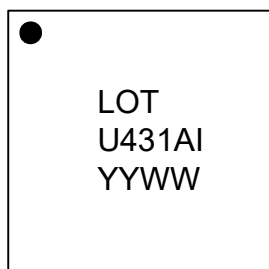
<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>]

<sup>5</sup> Driven by 9FGU0831 or equivalent

<sup>6</sup> Rohde&Schartz SMA100

## Marking Diagrams



### Notes:

1. "LOT" denotes the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. Line 2: truncated part number
4. "I" denotes industrial temperature grade.

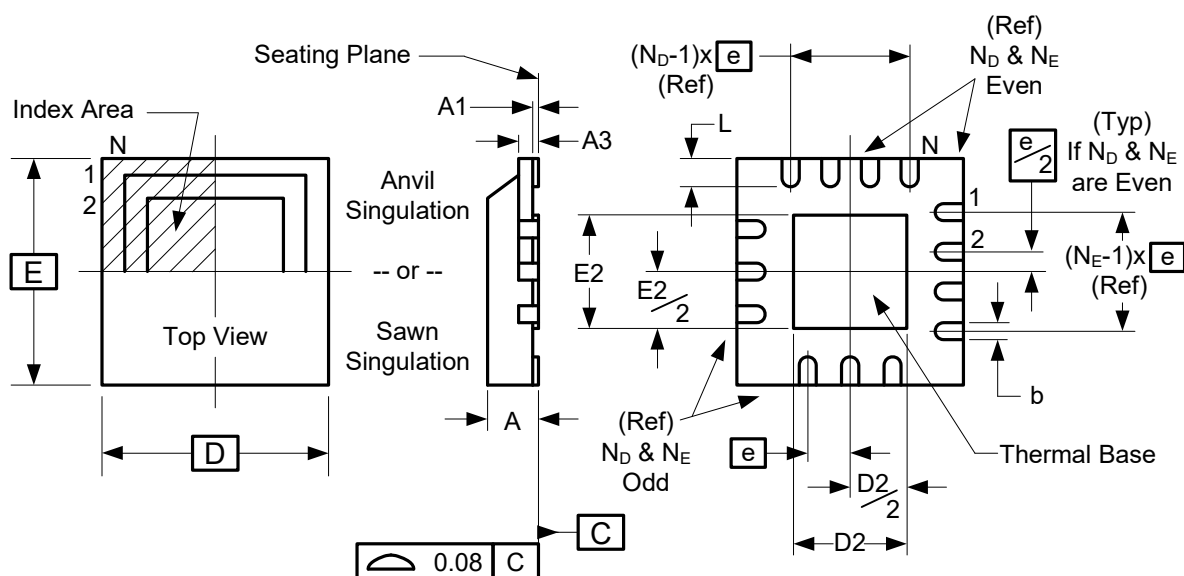
## Thermal Characteristics

| PARAMETER          | SYMBOL         | CONDITIONS                      | PKG   | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | $\theta_{JC}$  | Junction to Case                | NLG24 | 42        | °C/W  | 1     |
|                    | $\theta_{Jb}$  | Junction to Base                |       | 2.4       | °C/W  | 1     |
|                    | $\theta_{JA0}$ | Junction to Air, still air      |       | 39        | °C/W  | 1     |
|                    | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow |       | 33        | °C/W  | 1     |
|                    | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow |       | 28        | °C/W  | 1     |
|                    | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow |       | 27        | °C/W  | 1     |

<sup>1</sup>ePad soldered to board



## Package Outline and Package Dimensions (NLG24)



| Symbol       | Millimeters    |      |
|--------------|----------------|------|
|              | Min            | Max  |
| A            | 0.80           | 1.00 |
| A1           | 0              | 0.05 |
| A3           | 0.25 Reference |      |
| b            | 0.18           | 0.30 |
| e            | 0.50 BASIC     |      |
| D x E BASIC  | 4.00 x 4.00    |      |
| D2 MIN./MAX. | 2.3            | 2.55 |
| E2 MIN./MAX. | 2.3            | 2.55 |
| L MIN./MAX.  | 0.30           | 0.50 |
| N            | 24             |      |
| ND           | 6              |      |
| NE           | 6              |      |

## Ordering Information

| Part / Order Number | Shipping Packaging | Package       | Temperature   |
|---------------------|--------------------|---------------|---------------|
| 9DMU0431AKILF       | Tubes              | 24-pin VFQFPN | -40 to +85° C |
| 9DMU0431AKILFT      | Tape and Reel      | 24-pin VFQFPN | -40 to +85° C |

"LF" to the suffix denotes Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

## Revision History

| Rev. | Initiator | Issue Date | Description  | Page # |
|------|-----------|------------|--|--------|
| A    | RDW       | 9/24/2014  | 1. Updated additive phase jitter and General Description<br>2. Move to final | 1,7    |



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[AD9513BCPZ-REEL7](#) [ADCLK950BCPZ-REEL7](#) [ADCLK950BCPZ](#) [AD9553BCPZ](#) [HMC940LC4B](#) [HMC6832ALP5LE](#) [CSPUA877ABVG8](#)  
[9P936AFLFT](#) [49FCT3805ASOG](#) [49FCT3805DQGI](#) [49FCT3805EQGI](#) [49FCT805CTQG](#) [74FCT3807EQGI](#) [74FCT388915TEPYG](#)  
[853S013AMILF](#) [853S058AGILF](#) [8SLVD1208-33NBGI](#) [8V79S680NLGI](#) [ISPPAC-CLK5312S-01TN48I](#) [ISPPAC-CLK5520V-01TN100I](#)