8 OUTPUT LOW-POWER PCIE GEN1-2-3 CLOCK GENERATOR W/ZO=100OHMS 9FGL839

Description

The 9FGL839 is an 8-output clock generator for PCI Express Gen1, Gen2, and Gen3 applications. It has integrated terminations providing direction connection to 100ohm transmission lines and saving 32 resistors compared to standard HCSL outputs. The 9FGL839 supports Common, Data and Separate Reference no-Spread (SRnS) PCIe clock architectures.

Recommended Application

100MHz PCIe Gen1-2-3 clock generator

Output Features

- 8 - Low-Power (LP) HCSL output pairs @ 100MHz

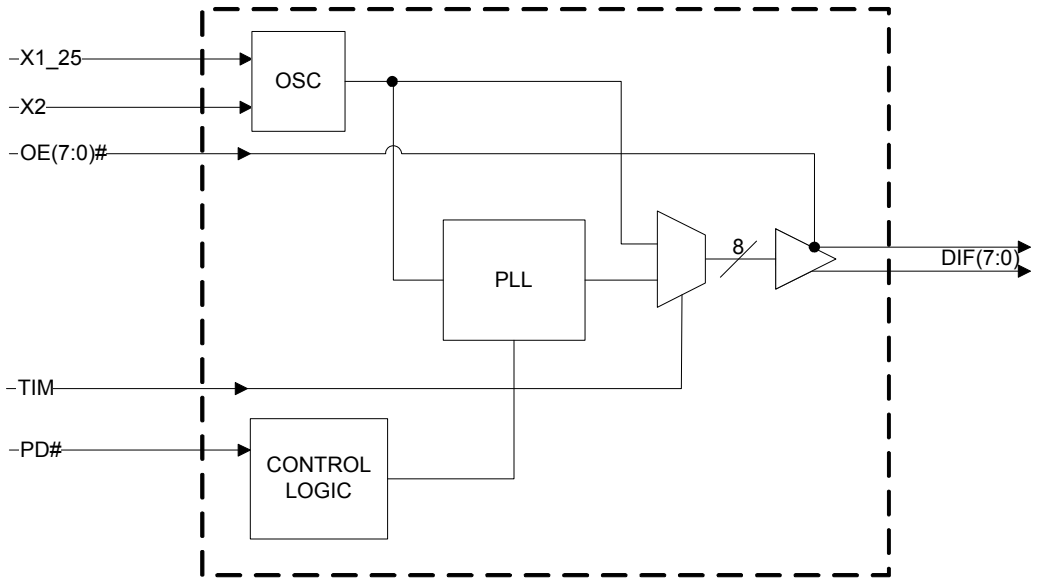
Features/Benefits

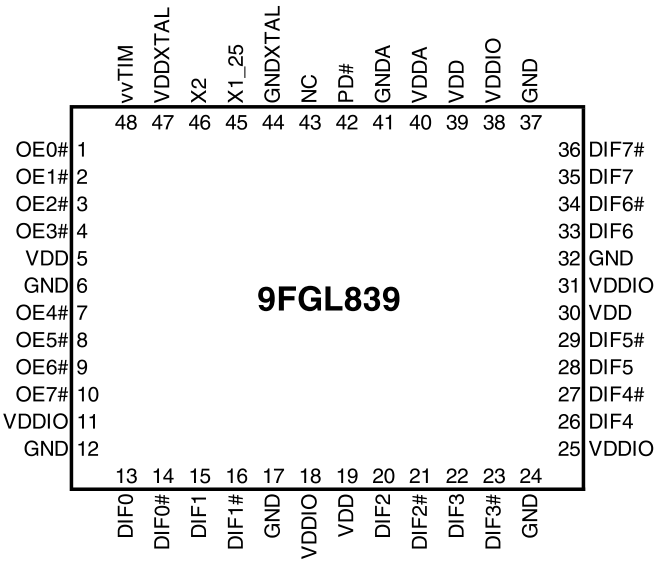
- Integrated terminations; save 32 resistors compared to standard HCSL outputs
- LP-HCSL outputs; support separate VDDIO rail and 130mW typical power consumption
- 8 OE# pins; Hardware control of each output
- 25MHz crystal input; exact synthesis
- 100MHz operation; supports PCIe and SATA applications
- VDDIO; allows outputs to run from lower voltage rail to save power
- OE# pins have 1.5V high input threshold; direct interface to 1.8-3.3V systems
- Packaged in 48-pin VFQFPN

Key Specifications

- <130mW power consumption (typical)
- Cycle-to-cycle jitter <50ps
- Output-to-output skew <100 ps
- PCIe Gen2 phase jitter <3.0ps RMS
- PCIe Gen3 phase jitter <1.0ps RMS
- PCIe Gen3 SRnS clock phase jitter <0.7ps RMS

Block Diagram





48-pin VFQFPN, 6x6 mm, 0.4mm pitch

v prefix indicates internal 120KOhm pull down resistor
vv prefix indicates internal 60KOhm pull down resistor
^ prefix indicates internal 120KOhm pull up resistor

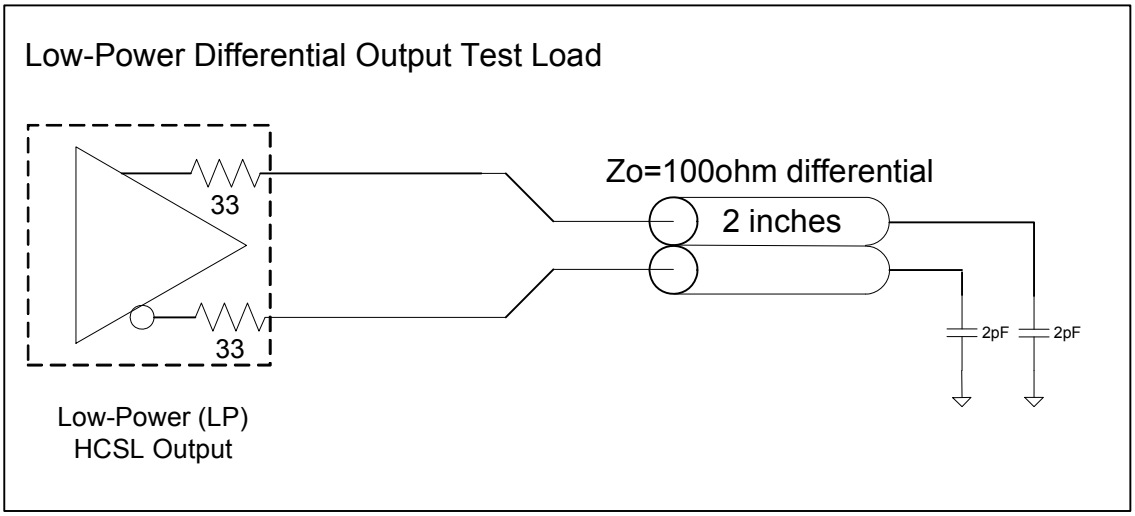
Power Management Table

Inputs	Control Bits/Pins	Outputs	PLL State
PD#	OE# Pin	DIFx/DIFx#	
0	X	Low/Low	OFF
1	0	Running	ON
1	1	Low/Low	ON

MLF Power Connections Table

Pin Number				Description
VDDA	VDD	VDDIO	GND	
40			41	Analog PLL
47			44	XTAL
	5		6	Inputs
	19, 30, 39	11, 18, 25, 31, 38	12, 17, 24, 32, 37	DIF clocks

PIN #	PIN NAME	TYPE	DESCRIPTION
1	OE0#	IN	Active low input for enabling DIF pair 0. 1 =disable outputs, 0 = enable outputs
2	OE1#	IN	Active low input for enabling DIF pair 1. 1 =disable outputs, 0 = enable outputs
3	OE2#	IN	Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs
4	OE3#	IN	Active low input for enabling DIF pair 3. 1 =disable outputs, 0 = enable outputs
5	VDD	PWR	Power supply, nominal 3.3V
6	GND	PWR	Ground pin.
7	OE4#	IN	Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs
8	OE5#	IN	Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs
9	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
10	OE7#	IN	Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs
11	VDDIO	PWR	Power supply for differential outputs
12	GND	PWR	Ground pin.
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
15	DIF1	OUT	Differential true clock output
16	DIF1#	OUT	Differential Complementary clock output
17	GND	PWR	Ground pin.
18	VDDIO	PWR	Power supply for differential outputs
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF2	OUT	Differential true clock output
21	DIF2#	OUT	Differential Complementary clock output
22	DIF3	OUT	Differential true clock output
23	DIF3#	OUT	Differential Complementary clock output
24	GND	PWR	Ground pin.
25	VDDIO	PWR	Power supply for differential outputs
26	DIF4	OUT	Differential true clock output
27	DIF4#	OUT	Differential Complementary clock output
28	DIF5	OUT	Differential true clock output
29	DIF5#	OUT	Differential Complementary clock output
30	VDD	PWR	Power supply, nominal 3.3V
31	VDDIO	PWR	Power supply for differential outputs
32	GND	PWR	Ground pin.
33	DIF6	OUT	Differential true clock output
34	DIF6#	OUT	Differential Complementary clock output
35	DIF7	OUT	Differential true clock output
36	DIF7#	OUT	Differential Complementary clock output
37	GND	PWR	Ground pin.
38	VDDIO	PWR	Power supply for differential outputs
39	VDD	PWR	Power supply, nominal 3.3V
40	VDDA	PWR	3.3V power for the PLL core.
41	GNDA	PWR	Ground pin for the PLL core.
42	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.
43	NC	N/A	No Connection.
44	GNDXTAL	PWR	GND for XTAL
45	X1_25	IN	Crystal input, Nominally 25.00MHz.
46	X2	OUT	Crystal output.
47	VDDXTAL	PWR	Power supply for XTAL, nominal 3.3V
48	vvTIM	IN	This pin is the Test Input Mode pin. A '0' on this pin puts the part in normal operating mode. A '1' on this pin puts the part in Test Input Mode, bypassing the PLL. This pin should be either pulled to ground with an external 10Kohm resistor or grounded



Stresses above the ratings listed below can cause permanent damage to the 9FGL839. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDD, VDDA	VDD for core logic and PLL			4.6	V	1,2
IO Supply Voltage	VDDIO	VDD for differential IO			4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins (if present)			5.5	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Input/Supply/Common Parameters

$T_A = T_{COM}$ or T_{IND}; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%, VDDIO = 1.05V to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
	T_{IND}	Industriall range	-40		85	°C	1
Input High Voltage	V_{IHOE}	OE# pins	1.5		V_{DD} + 0.3	V	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5	+/-3	5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200	+/-75	200	uA	1
Input Frequency	Fin	V_{DDA}, V_{DD}		25		MHz	2
Pin Inductance	L_{pin}			6	7	nH	1
Capacitance	C_{IN}	Logic Inputs	1.5	4	5	pF	1
	C_{OUT}	Output pin capacitance		5	6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.5	1	ms	1,2
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	4	clocks	1
Tfall	t_F	Fall time of control inputs			10	ns	1,2
Trise	t_R	Rise time of control inputs			10	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

$T_A = T_{COM\ or}\ T_{IND}$; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%, VDDIO = 1.05V to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2	3	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		7.6	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	480	590	850	mV	1
Voltage Low	VLow		-150	9	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		609	1150	mV	1
Min Voltage	Vmin		-300	-19			1
Vswing	Vswing	Scope averaging off	300	1162		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	292	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		23	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF. (100Ω differential trace impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross abs.

Electrical Characteristics–Current Consumption

$T_A = T_{COM\ or}\ T_{IND}$; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%, VDDIO = 1.05V to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Current	$I_{DDVDD,\ VDDA}$	C_L = 2pF; VDD/VDDA rail, all outputs on		35	42	mA	1
	$I_{DDVDDIO}$	C_L = 2pf; VDDIO rail, all outputs on		14	20	mA	1
Powerdown Current	$I_{DDVDD,\ VDDA}$	Power Down, VDD/VDDA Rail		5.3	8	mA	1
	$I_{DDVDDIO}$	Power Down, VDDIO Rail		0.001	0.1	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Skew and Differential Jitter Parameters

$T_A = T_{COM\ or}\ T_{IND}$; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%, VDDIO = 1.05V to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
DIF{x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs		50	100	ps	1,2,3
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	49.4	55	%	1,3
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		17.5	50	ps	1,3,4

Notes for preceding table:

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] Guaranteed by design and characterization, not 100% tested in production.

[4] Measured from differential waveform

T_A = $T_{COM\ or}$ T_{IND}; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%, VDDIO = 1.05V to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1		23	40	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.6	0.8	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.9	2.5	3.1	ps (rms)	1,2
	$t_{jphPCIeG3COM}$	PCIe Gen3, (Common Clock and Data Clock)		0.4	0.6	1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen3 (Separate Reference no Spread - SRnS)		0.4	0.6	0.7	ps (rms)	1,2

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

Clock Periods–Differential Outputs

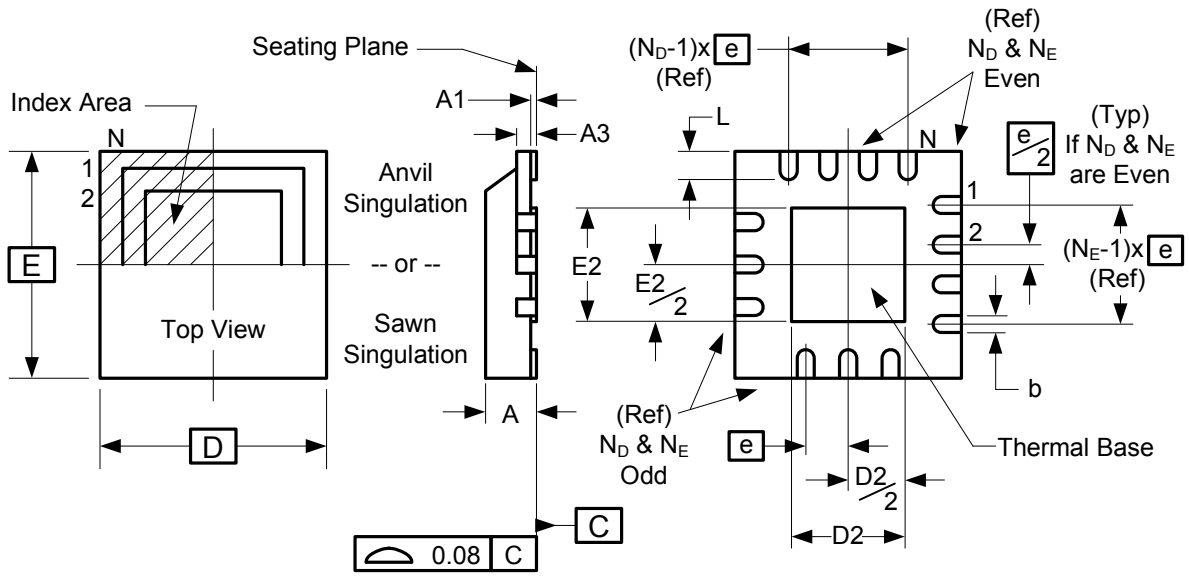
SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.91450		9.99950	10.00000	10.00050		10.08550	ns	1,2,3

Notes:

1. “LOT” is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “L” denotes RoHS compliant package.
4. “I” denotes industrial temperature range.
4. “COO” denotes country of origin.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		34		°C/W
	θ_{JA}	1 m/s air flow		31		°C/W
	θ_{JA}	2 m/s air flow		29		°C/W
Thermal Resistance Junction to Case	θ_{JC}			31.7		°C/W



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.15	0.25
e	0.40 BASIC	
D x E BASIC	6.00 x 6.00	
D2 MIN./MAX.	4.10	4.30
E2 MIN./MAX.	4.10	4.30
L MIN./MAX.	0.35	0.45
N	48	
N_D	12	
N_E	12	

Ordering Information

Part / Order Number	Shipping Package	Package	IDT Package Code	Temperature
9FGL839AKLF	Trays	48-pin VFQFPN	NDG48	0 to +70°C
9FGL839AKLFT	Tape and Reel	48-pin VFQFPN	NDG48	0 to +70°C
9FGL839AKILF	Trays	48-pin VFQFPN	NDG48	-40 to +85°C
9FGL839AKILFT	Tape and Reel	48-pin VFQFPN	NDG48	-40 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Rev.	Issuer	Issue Date	Description	Page #
A	RDW	1/6/2012	1. Updated Features/Benefits 2. Updated Power Connections Table 3. Updated Electrical Tables to Final, removed references to 125M 4. Adding mark information and Thermal Data	1,2, 5-8
B	RDW	7/21/2014	1a. Updated DS title from "Frequency Synthesizer" to "Clock Generator" and updated "PCIe Gen2/3" to "PCIe Gen1-2-3". 1b. Updated general description and features/benefits 2. Updated IDDVDD, VDDA max parameter from 40mA to 42mA. 3. Updated IDDVDD, VDDA power down max parameter from 6mA to 8mA. 4. Reduced max cycle to cycle jitter from 85ps to 50ps. 5. Added INDUSTRY LIMIT to phase jitter table and specified MAX separately. Added separate line for SRnS spec. 6. Reduced VHigh min from 500mV to 480mV. Min Vswing is still >1000mV against PCIe SIG 300mV limit	1, 5-8

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