

Description

The 9ZXL1930 is a low power version of the Intel DB1900Z Differential Buffer utilizing Low-Power HCSL (LP-HCSL) outputs to reduce power consumption more than 50% from the original IDT9ZX21901. It is suitable for PCI-Express Gen1/2/3 or QPI/UPI applications, and uses a fixed external feedback to maintain low drift for demanding QPI/UPI applications.

Recommended Application

Buffer for Romley, Grantley and Purley Servers

Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: <85ps
- Input-to-output delay: Fixed at 0 ps
- Input-to-output delay variation: <50ps
- Phase jitter: PCIe Gen3 < 1ps rms
- Phase jitter: QPI/UPI 9.6GB/s < 0.2ps rms

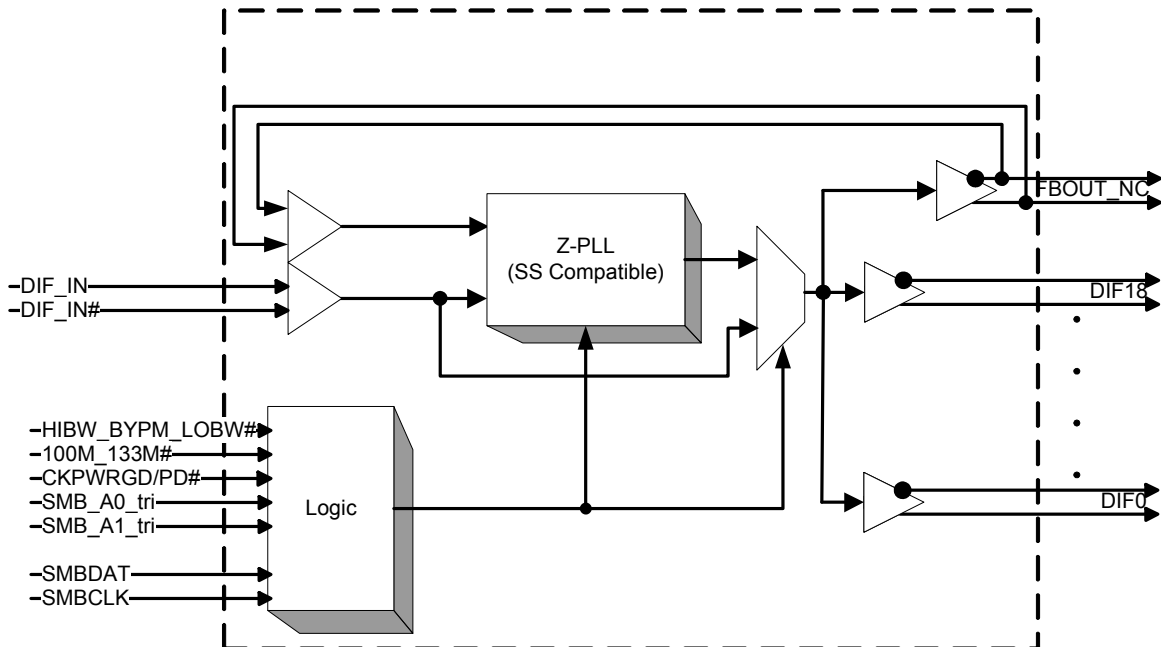
Features/Benefits

- Fixed feedback path; 0ps input-to-output delay
- 9 Selectable SMBus addresses; Multiple devices can share same SMBus segment
- Separate VDDIO for outputs; allows maximum power savings
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL BW; minimizes jitter peaking in downstream PLL's
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus Interface; unused outputs can be disabled
- 100MHz & 133.33MHz PLL mode; Legacy QPI/UPI support
- Differential outputs are Low/Low in power down; Maximum power savings

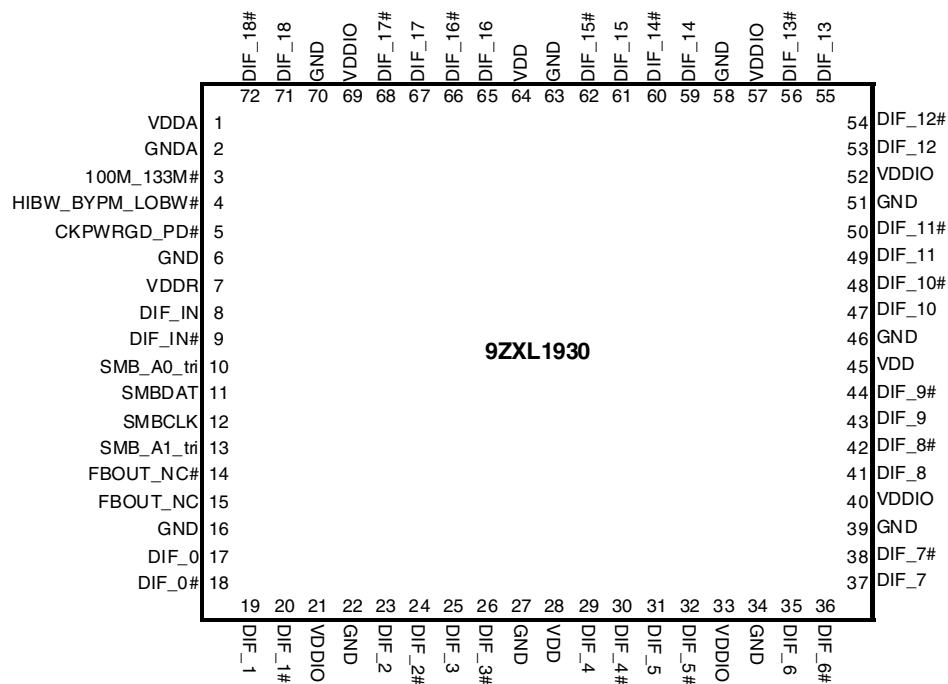
Output Features

- 19 - LP-HCSL Differential Output Pairs

Block Diagram



Pin Configuration



Power Management Table

| Inputs | | Control Bits | Outputs | | PLL State |
|-------------|--------------------|-----------------|------------------|-------------------------|-----------|
| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | DIF_x/ DIF_x# | FBOUT_NC/ FB_OUT_NC# | |
| 0 | X | X | Low/Low | Low/Low | OFF |
| 1 | Running | 0 | Low/Low | Running | ON |
| | | 1 | Running | Running | ON |

Power Connections

| Pin Number | | | Description |
|------------|---------------------------|--|--------------|
| VDD | VDDIO | GND | |
| 1 | | 2 | Analog PLL |
| 7 | | 6 | Analog Input |
| 28, 45, 64 | 21, 33, 40, 52, 57, 69 | 16, 22, 27, 34, 39, 46, 51, 58, 63, 70 | DIF clocks |

Functionality at Power-up (PLL mode)

| 100M_133M# | DIF_IN (MHz) | DIFx (MHz) |
|------------|-----------------|---------------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

PLL Operating Mode Table

| HiBW_BypM_LoBW# | Byte0, bit (7:6) |
|--------------------|------------------|
| Low (PLL Low BW) | 00 |
| Mid (Bypass) | 01 |
| High (PLL High BW) | 11 |

NOTE: PLL is off in Bypass mode

Tri-Level Input Thresholds

| Level | Voltage |
|-------|--------------|
| Low | <0.8V |
| Mid | 1.2<Vin<1.8V |
| High | Vin > 2.2V |

Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-----------------|----------|---|
| 1 | VDDA | PWR | 3.3V power for the PLL core. |
| 2 | GNDA | PWR | Ground pin for the PLL core. |
| 3 | 100M_133M# | IN | 3.3V Input to select operating frequency See Functionality Table for Definition |
| 4 | HIBW_BYPM_LOBW# | IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 5 | CKPWRGD_PD# | IN | Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 6 | GND | PWR | Ground pin. |
| 7 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 8 | DIF_IN | IN | 0.7 V Differential TRUE input |
| 9 | DIF_IN# | IN | 0.7 V Differential Complementary Input |
| 10 | SMB_A0_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. |
| 11 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 12 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 13 | SMB_A1_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses. |
| 14 | FBOUT_NC# | OUT | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 15 | FBOUT_NC | OUT | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 16 | GND | PWR | Ground pin. |
| 17 | DIF_0 | OUT | 0.7V differential true clock output |
| 18 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 19 | DIF_1 | OUT | 0.7V differential true clock output |
| 20 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 21 | VDDIO | PWR | Power supply for differential outputs |
| 22 | GND | PWR | Ground pin. |
| 23 | DIF_2 | OUT | 0.7V differential true clock output |
| 24 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 25 | DIF_3 | OUT | 0.7V differential true clock output |
| 26 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 27 | GND | PWR | Ground pin. |
| 28 | VDD | PWR | Power supply, nominal 3.3V |
| 29 | DIF_4 | OUT | 0.7V differential true clock output |
| 30 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 31 | DIF_5 | OUT | 0.7V differential true clock output |
| 32 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 33 | VDDIO | PWR | Power supply for differential outputs |
| 34 | GND | PWR | Ground pin. |
| 35 | DIF_6 | OUT | 0.7V differential true clock output |
| 36 | DIF_6# | OUT | 0.7V differential Complementary clock output |

Pin Descriptions (cont.)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|--|
| 37 | DIF_7 | OUT | 0.7V differential true clock output |
| 38 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 39 | GND | PWR | Ground pin. |
| 40 | VDDIO | PWR | Power supply for differential outputs |
| 41 | DIF_8 | OUT | 0.7V differential true clock output |
| 42 | DIF_8# | OUT | 0.7V differential Complementary clock output |
| 43 | DIF_9 | OUT | 0.7V differential true clock output |
| 44 | DIF_9# | OUT | 0.7V differential Complementary clock output |
| 45 | VDD | PWR | Power supply, nominal 3.3V |
| 46 | GND | PWR | Ground pin. |
| 47 | DIF_10 | OUT | 0.7V differential true clock output |
| 48 | DIF_10# | OUT | 0.7V differential Complementary clock output |
| 49 | DIF_11 | OUT | 0.7V differential true clock output |
| 50 | DIF_11# | OUT | 0.7V differential Complementary clock output |
| 51 | GND | PWR | Ground pin. |
| 52 | VDDIO | PWR | Power supply for differential outputs |
| 53 | DIF_12 | OUT | 0.7V differential true clock output |
| 54 | DIF_12# | OUT | 0.7V differential Complementary clock output |
| 55 | DIF_13 | OUT | 0.7V differential true clock output |
| 56 | DIF_13# | OUT | 0.7V differential Complementary clock output |
| 57 | VDDIO | PWR | Power supply for differential outputs |
| 58 | GND | PWR | Ground pin. |
| 59 | DIF_14 | OUT | 0.7V differential true clock output |
| 60 | DIF_14# | OUT | 0.7V differential Complementary clock output |
| 61 | DIF_15 | OUT | 0.7V differential true clock output |
| 62 | DIF_15# | OUT | 0.7V differential Complementary clock output |
| 63 | GND | PWR | Ground pin. |
| 64 | VDD | PWR | Power supply, nominal 3.3V |
| 65 | DIF_16 | OUT | 0.7V differential true clock output |
| 66 | DIF_16# | OUT | 0.7V differential Complementary clock output |
| 67 | DIF_17 | OUT | 0.7V differential true clock output |
| 68 | DIF_17# | OUT | 0.7V differential Complementary clock output |
| 69 | VDDIO | PWR | Power supply for differential outputs |
| 70 | GND | PWR | Ground pin. |
| 71 | DIF_18 | OUT | 0.7V differential true clock output |
| 72 | DIF_18# | OUT | 0.7V differential Complementary clock output |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1930. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA, R | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| I/O Supply Voltage | VDDIO | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics—DIF_IN Clock Input Parameters

T_A = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Cross Over Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{in} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Output Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 33 | | 150 | MHz | 2 |
| | F _{ipl} | V _{DD} = 3.3 V, 100MHz PLL mode | 90 | 100.00 | 110 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 133.33MHz PLL mode | 120 | 133.33 | 147 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 12 | clocks | 1 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF Low-Power HCSL Differential Outputs

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------|---|------|-----|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 3 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 7.6 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 757 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 16 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 857 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -36 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 300 | 469 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 14 | 140 | mV | 1, 6 |

¹ Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 33Ω for Z_o = 50Ω (100Ω differential trace impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------------|---|-----|------|-----|-------|-------|
| Operating Supply Current | I _{DDVDD} | All outputs @100MHz, C _L = 2pF; Z _o =85 Ω | | 23 | 35 | mA | 1 |
| | I _{DDVDDA/R} | All outputs @100MHz, C _L = 2pF; Z _o =85 Ω | | 12 | 20 | mA | 1 |
| | I _{DDVDDIO} | All outputs @100MHz, C _L = 2pF; Z _o =85 Ω | | 151 | 175 | mA | 1 |
| Powerdown Current | I _{DDVDDPD} | All differential pairs low/low | | 2.9 | 6 | mA | 1,2 |
| | I _{DDVDDA/RPD} | All differential pairs low/low | | 4.4 | 6 | mA | 1,2 |
| | I _{DDVDDIOPD} | All differential pairs low/low | | 0.05 | 1.5 | mA | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² With input clock running. Stopping the input clock will result in lower numbers.

Electrical Characteristics—Skew and Differential Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|-----|-------------|-----------|
| CLK_IN, DIF[x:0] | t _{SPO_PLL} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | -100 | -44 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 2.5 | 3.6 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | -50 | -2 | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | -250 | | 250 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random Differential Tracking error between two 9ZX devices in Hi BW Mode | | 3 | 5 | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode | | 15 | 75 | ps | 1,2,3,5,8 |
| DIF[x:0] | t _{SKEW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 76 | 85 | ps | 1,2,3,8 |
| PLL Jitter Peaking | j _{peak-hibw} | LOBW#_BYPASS_HIBW = 1 | 0 | 1.75 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | j _{peak-lobw} | LOBW#_BYPASS_HIBW = 0 | 0 | 0.75 | 2 | dB | 7,8 |
| PLL Bandwidth | p _{ll_HIBW} | LOBW#_BYPASS_HIBW = 1 | 2 | 3.33 | 4 | MHz | 8,9 |
| PLL Bandwidth | p _{ll_LOBW} | LOBW#_BYPASS_HIBW = 0 | 0.7 | 1.18 | 1.4 | MHz | 8,9 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 50.4 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, Bypass Mode @100MHz | -2 | 0 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | PLL mode | | 24 | 50 | ps | 1,11 |
| | | Additive Jitter in Bypass Mode | | 0 | 50 | ps | 1,11 |

Notes for preceding table:

- ¹ Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- ² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- ³ All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- ⁴ This parameter is deterministic for a given device
- ⁵ Measured with scope averaging on to find mean value.
- ⁶ t is the period of the input clock
- ⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- ⁸ Guaranteed by design and characterization, not 100% tested in production.
- ⁹ Measured at 3 db down or half power point.
- ¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
- ¹¹ Measured from differential waveform

Electrical Characteristics—Phase Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|-------------------------|--|-----|------|-----|----------|---------|
| Phase Jitter, PLL Mode | t _{jphPCleG1} | PCIe Gen 1 | | 30 | 86 | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.0 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 1.7 | 3.1 | ps (rms) | 1,2 |
| | t _{jphPCleG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.38 | 1 | ps (rms) | 1,2,4 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.18 | 0.5 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.13 | 0.3 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.10 | 0.2 | ps (rms) | 1,5 |
| Additive Phase Jitter, Bypass mode | t _{jphPCleG1} | PCIe Gen 1 | | 0 | 10 | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.0 | 0.3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.0 | 0.7 | ps (rms) | 1,2,6 |
| | t _{jphPCleG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.0 | 0.3 | ps (rms) | 1,2,4,6 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.12 | 0.3 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.00 | 0.1 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.00 | 0.1 | ps (rms) | 1,5,6 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final ratification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

⁶ For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)² = (total jitter)² - (input jitter)²

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1 μ s | 0.1 s | 0.1s | 0.1s | 1 μ s | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2,3 |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2,4 |

Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1 μ s | 0.1 s | 0.1s | 0.1s | 1 μ s | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

Notes:

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1930 itself does not contribute to ppm error.

³ Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

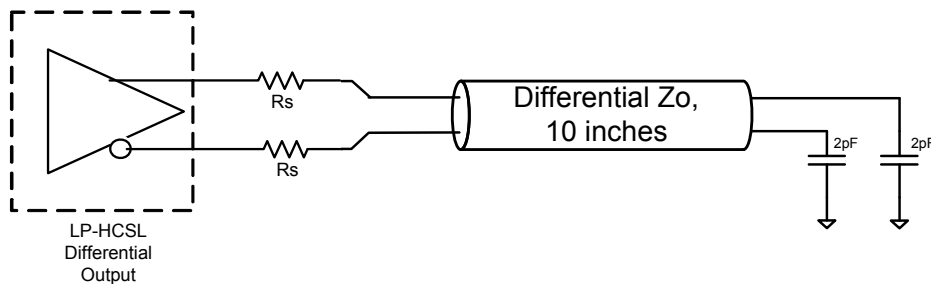
⁴ Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Test Loads

Differential Output Terminations

| DIF Zo (Ω) | Rs (Ω) |
|---------------------|-----------------|
| 100 | 33 |
| 85 | 27 |

9ZXL Differential Test Loads



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| ACK | | X Byte | Data Byte Count=X |
| ACK | | | Beginning Byte N |
| O | | | O |
| O | | | O |
| | | | O |
| ACK | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

9ZXL1930 SMBus Addressing

| SMB_A(1:0)_tri | SMBus Address (Rd/Wrt bit = 0) |
|----------------|--------------------------------|
| 00 | D8 |
| 0M | DA |
| 01 | DE |
| M0 | C2 |
| MM | C4 |
| M1 | C6 |
| 10 | CA |
| 1M | CC |
| 11 | CE |

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------|----------------------------------|------|---------------------------------------|--------|---------|
| Bit 7 | 4 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 6 | 4 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | | | Latch |
| Bit 5 | 72/71 | DIF_18_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 4 | 68/67 | DIF_17_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 3 | 66/65 | DIF_16_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | 3 | 100M_133M# | Frequency Select Readback | R | 133MHz | 100MHz | Latch |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|----------------------------------|------|---------|--------|---------|
| Bit 7 | 38/37 | DIF_7_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 6 | 35/36 | DIF_6_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | 31/32 | DIF_5_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | 29/30 | DIF_4_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | 25/26 | DIF_3_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | 23/24 | DIF_2_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | 19/20 | DIF_1_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | 17/18 | DIF_0_En | Output Control overrides OE# pin | RW | | | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|----------------------------------|------|---------|--------|---------|
| Bit 7 | 62/61 | DIF_15_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 6 | 60/59 | DIF_14_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | 56/55 | DIF_13_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | 54/53 | DIF_12_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | 50/49 | DIF_11_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | 48/47 | DIF_10_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | 44/43 | DIF_9_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | 42/41 | DIF_8_En | Output Control overrides OE# pin | RW | | | 1 |

SMBusTable: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|--------------------------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | A rev = 0000 B rev = 0001 etc. | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-------------------|------|----------------------------------|---|---------|
| Bit 7 | - | | Device ID 7 (MSB) | R | 1930 is 193 Decimal or C1 Hex | | 1 |
| Bit 6 | - | | Device ID 6 | R | | | X |
| Bit 5 | - | | Device ID 5 | R | | | X |
| Bit 4 | - | | Device ID 4 | R | | | X |
| Bit 3 | - | | Device ID 3 | R | | | X |
| Bit 2 | - | | Device ID 2 | R | | | 0 |
| Bit 1 | - | | Device ID 1 | R | | | 0 |
| Bit 0 | - | | Device ID 0 | R | | | 1 |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

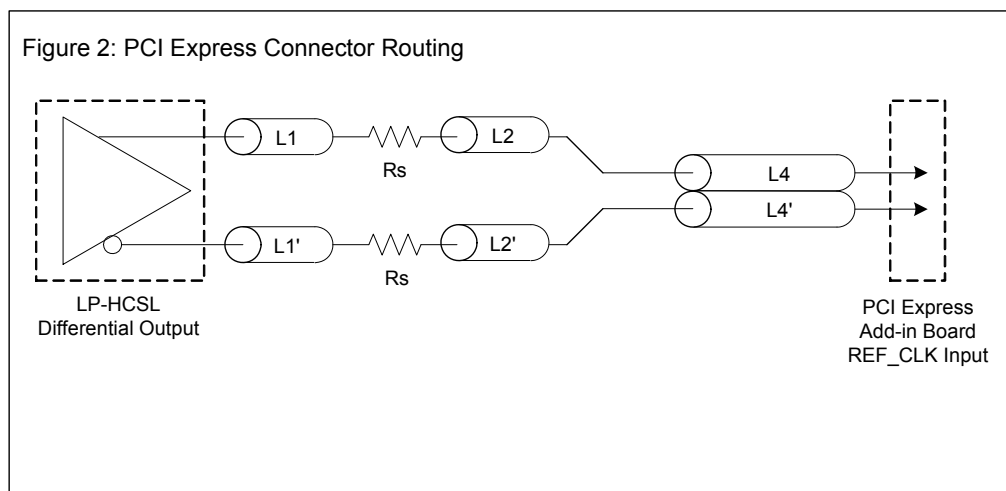
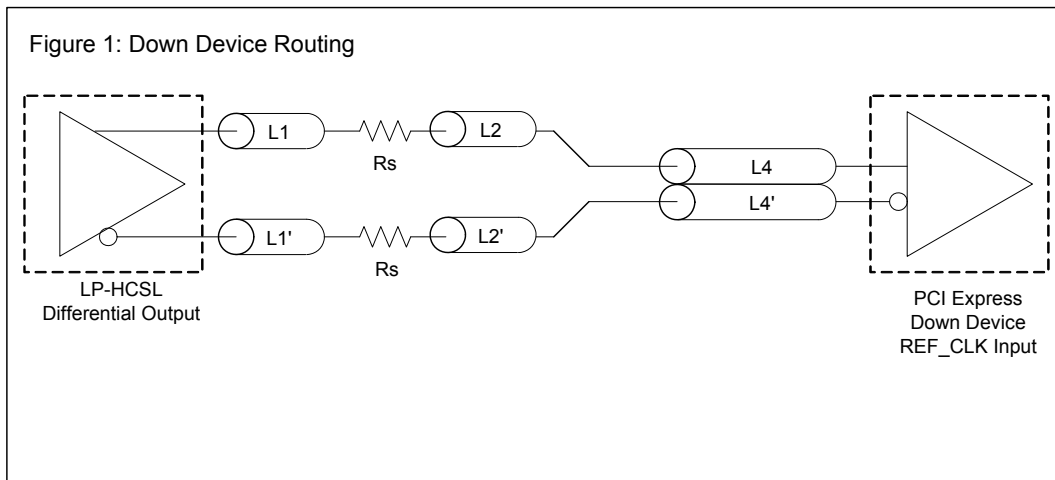
SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

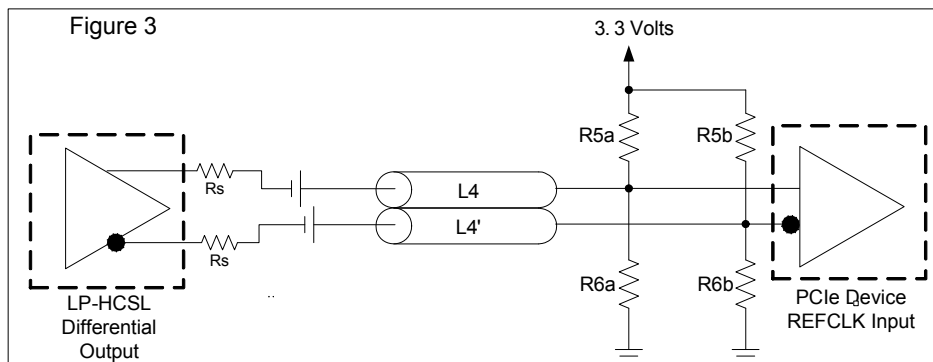
| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs (100 ohm differential traces) | 33 | ohm | 1 |
| Rs (85 ohm differential traces) | 27 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|--------|---|
| Dimension or Value | Unit | Figure | |
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

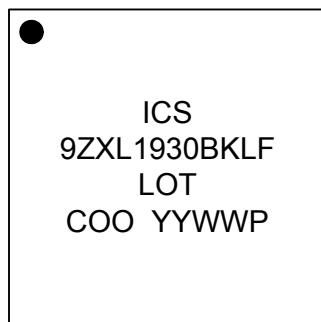
| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|--------|---|
| Dimension or Value | Unit | Figure | |
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |



| Cable Connected AC Coupled Application (Figure 3) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



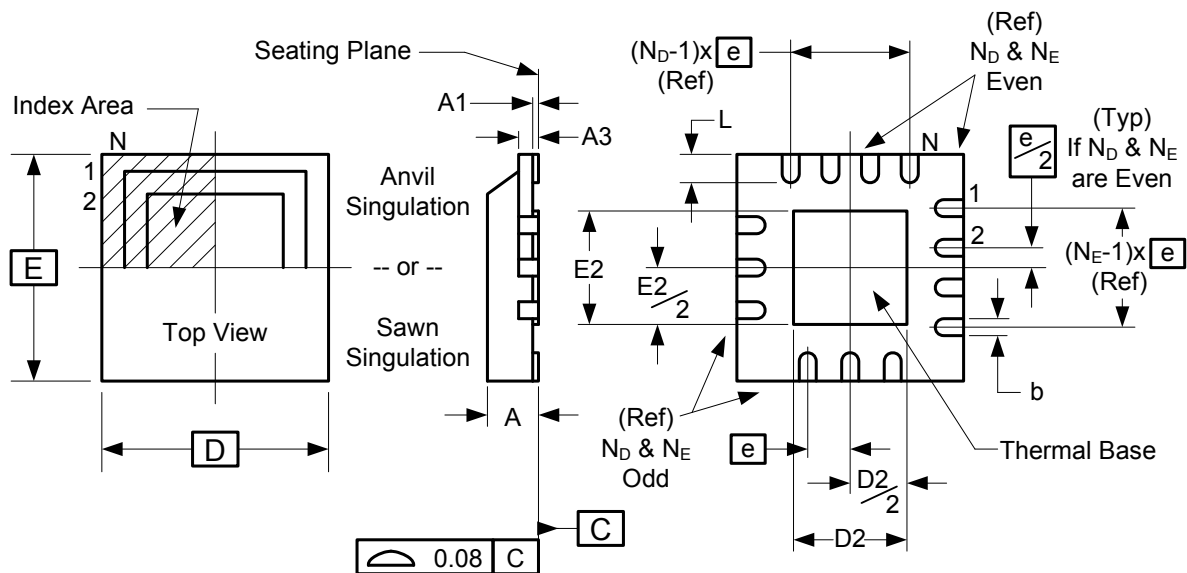
Marking Diagram



Notes:

1. 'LOT' is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes RoHS compliant package.
4. 'COO' denotes country of origin.

Package Outline and Package Dimensions (72-pin MLF)



| Symbol | Millimeters | |
|--------------|----------------|------|
| | Min | Max |
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 10.00 x 10.00 | |
| D2 MIN./MAX. | 5.75 | 6.15 |
| E2 MIN./MAX. | 5.75 | 6.15 |
| L MIN./MAX. | 0.3 | 0.5 |
| ND | 18 | |
| NE | 18 | |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|------------|-------------|
| 9ZXL1930BKLF | see page 15 | Tray | 72-pin MLF | 0 to +70° C |
| 9ZXL1930BKLF | | Tape and Reel | 72-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate with the datasheet revision).

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

| Rev. | Issuer | Issue Date | Description | Page # |
|------|--------|------------|---|-----------|
| A | RDW | 12/8/2011 | <ol style="list-style-type: none"> 1. Updated key specifications table Output to Output skew to 85ps 2. Updated Electrical Tables with typical specs 3. Updated Byte 5 for REV ID 4. Moved to Final | 1,6-9,13 |
| B | RDW | 3/12/2012 | <ol style="list-style-type: none"> 1. Various typo fixes, changed output references to LP-HCSL. 2. Added Test Loads figure and table. | 1,9,10,14 |
| C | RDW | 6/25/2014 | <ol style="list-style-type: none"> 1. Slightly increased MAX power down currents. 2. Clarified block diagram to indicate that there are multiple outputs. 3. Changed title of output characteristics table to "Electrical Characteristics - DIF Low-Power HCSL Differential Outputs" to follow new standard. 4. Reformatted Figures 2 and 3 for consistency/clarity | 1,7,14,15 |
| D | RDW | 11/20/2015 | <ol style="list-style-type: none"> 1. Updated QPI references to QPI/UPI 2. Updated DIF_IN table to match PCI SIG specification, no silicon change | 1,5 |

9ZXL1930

19-OUTPUT DB1900Z LOW-POWER DERIVATIVE

SYNTHESIZERS

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Clock Buffer](#) category:

Click to view products by [Renesas](#) manufacturer:

Other Similar products are found below :

[MPC962309EJ-1H](#) [NB4N121KMNG](#) [IDT49FCT805ASO](#) [MK2308S-1HILF](#) [PL133-27GI-R](#) [NB3L02FCT2G](#) [NB3L03FCT2G](#)
[ZL40203LDG1](#) [ZL40200LDG1](#) [ZL40205LDG1](#) [9FG1200DF-1LF](#) [9FG1001BGLF](#) [ZL40202LDG1](#) [PI49FCT20802QE](#) [SL2305SC-1T](#)
[PI6C4931502-04LIE](#) [NB7L1008MNG](#) [NB7L14MN1G](#) [PI49FCT20807QE](#) [PI6C4931502-04LIEX](#) [ZL80002QAB1](#) [PI6C4931504-04LIEX](#)
[PI6C10806BLEX](#) [ZL40226LDG1](#) [ZL40219LDG1](#) [8T73S208B-01NLGI](#) [SY75578LMG](#) [PI49FCT32805QEX](#) [PL133-27GC-R](#)
[CDCV304PWG4](#) [MC10LVEP11DG](#) [MC10EP11DTG](#) [MC100LVEP11DG](#) [MC100E111FNG](#) [MC100EP11DTG](#) [NB6N11SMNG](#)
[NB7L14MMNG](#) [NB3N2304NZDTR2G](#) [NB6L11MMNG](#) [NB6L14MMNR2G](#) [NB6L611MNG](#) [PL123-02NGI-R](#) [NB3N111KMNR4G](#)
[ADCLK944BCPZ-R7](#) [ZL40217LDG1](#) [NB7LQ572MNG](#) [HMC940LC4BTR](#) [ADCLK946BCPZ-REEL7](#) [ADCLK946BCPZ](#)
[ADCLK846BCPZ-REEL7](#)