EL5111, EL5211, EL5411

60MHz Rail-to-Rail Input-Output Op Amps

FN7119
Rev 8.00
August 27, 2015

The EL5111, EL5211, and EL5411 are low power, high voltage rail-to-rail input-output amplifiers. The EL5111 represents a single amplifier, the EL5211 contains two amplifiers, and the EL5411 contains four amplifiers. Operating on supplies ranging from 5V to 15V, while consuming only 2.5mA per amplifier, the EL5111, EL5211, and EL5411 have a bandwidth of 60MHz (-3dB). They also provide common mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables these amplifiers to offer maximum dynamic range at any supply voltage.

The EL5111, EL5211, and EL5411 also feature fast slewing and settling times, as well as a high output drive capability of 65mA (sink and source). These features make these amplifiers ideal for high speed filtering and signal conditioning application. Other applications include battery power, portable devices, and anywhere low power consumption is important.

The EL5111 is available in 5 Ld TSOT and 8 Ld HMSOP packages. The EL5211 is available in the 8 Ld HMSOP package. The EL5411 is available in space-saving 14 Ld HTSSOP packages. All feature a standard operational amplifier pinout. These amplifiers operate over a temperature range of -40°C to +85°C.

Features

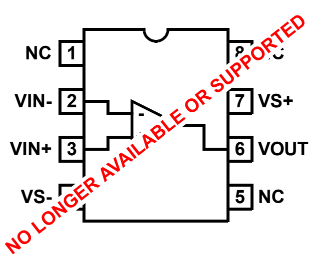
- Pb-free plus anneal available (RoHS compliant)
- 60MHz (-3dB) bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 75V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- ±180mA output short current

Applications

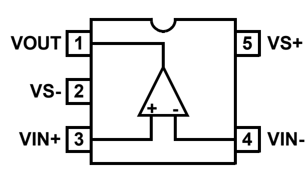
- TFT-LCD panels
- V_{COM} amplifiers
- Drivers for A/D converters
- Data acquisition
- Video processing
- Audio processing
- Active filters
- Test equipment
- Battery-powered applications
- Portable equipment

Pinouts

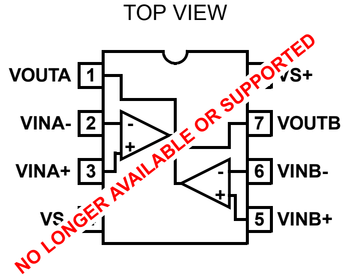
EL5111
(8 LD HMSOP)
TOP VIEW



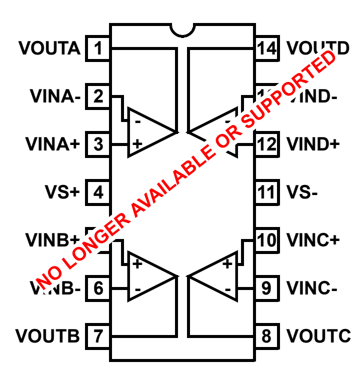
EL5111
(5 LD TSOT)
TOP VIEW



EL5211
(8 LD HMSOP)
TOP VIEW



EL5411
(14 LD HTSSOP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5111IWTZ-T7 (Note)	BAAG	7" (3k pcs)	5 Ld TSOT (Pb-free)	MDP0049
EL5111IWTZ-T7A (Note)	BAAG	7" (250 pcs)	5 Ld TSOT (Pb-free)	MDP0049
EL5111IYEZ (Note) **(No longer available or supported)**	BAAJA	-	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5111IYEZ-T7 (Note) **(No longer available or supported)**	BAAJA	7"	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5111IYEZ-T13 (Note) **(No longer available or supported)**	BAAJA	13"	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5211IYEZ (Note) **(No longer available or supported)**	BAATA	-	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5211IYEZ-T7 (Note) **(No longer available or supported)**	BAATA	7"	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5211IYEZ-T13 (Note) **(No longer available or supported)**	BAATA	13"	8 Ld HMSOP (Pb-free) (3.0mm)	MDP0050
EL5411IREZ (Note) **(No longer available or supported)**	5411IREZ	-	14 Ld HTSSOP (Pb-free) (4.4mm)	MDP0048
EL5411IREZ-T7 (Note) **(No longer available or supported)**	5411IREZ	7"	14 Ld HTSSOP (Pb-free) (4.4mm)	MDP0048
EL5411IREZ-T13 (Note) **(No longer available or supported)**	5411IREZ	13"	14 Ld HTSSOP (Pb-free) (4.4mm)	MDP0048
EL5411IRZ (Note) **(No longer available or supported)**	5411IRZ	-	14 Ld TSSOP (Pb-free) (4.4mm)	M14.173
EL5411IRZ-T7 (Note) **(No longer available or supported)**	5411IRZ	7"	14 Ld TSSOP (Pb-free) (4.4mm)	M14.173
EL5411IRZ-T13 (Note) **(No longer available or supported)**	5411IRZ	13"	14 Ld TSSOP (Pb-free) (4.4mm)	M14.173

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . .+18V
Input Voltage . . . . V_S- - 0.5V, V_S +0.5V
Maximum Continuous Output Current 65mA
Maximum Die Temperature . . . .+150°C

Thermal Information

Storage Temperature . . . .-65°C to +150°C
Ambient Operating Temperature . . . .-40°C to +85°C
Power Dissipation . . . . See Curves
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 1kΩ to 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	62	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.92	-4.85	V
V_{OH}	Output Swing High	I_L = 5mA	4.85	4.92		V
I_{SC}	Short-Circuit Current			±180		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current	No load (EL5111)		2.5	4.5	mA
		No load (EL5211)		5	7.5	mA
		No load (EL5411)		10	15	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz (EL5211 and EL5411 only)		110		dB
d_G	Differential Gain (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.17		%
d_P	Differential Phase (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.24		°

NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.
3. NTSC signal generator used.

Electrical Specifications V_S+ = +5V, V_S- = 0V, R_L = 1kΩ to 2.5V, T_A = +25°C, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 4)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 2.5V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	45	66		dB
A_{VOL}	Open-Loop Gain	0.5V ≤ V_{OUT} ≤ 4.5V	62	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		80	150	mV
V_{OH}	Output Swing High	I_L = 5mA	4.85	4.92		V
I_{SC}	Short-circuit Current			±180		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load (EL5111)		2.5	4.5	mA
		No load (EL5211)		5	7.5	mA
		No load (EL5411)		10	15	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 5)	1V ≤ V_{OUT} ≤ 4V, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz (EL5211 and EL5411 only)		110		dB
d_G	Differential Gain (Note 6)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.17		%
d_P	Differential Phase (Note 6)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.24		°

NOTES:

4. Measured over operating temperature range.
5. Slew rate is measured on rising and falling edges.
6. NTSC signal generator used.

Electrical Specifications

$V_S+ = +15V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 7.5V, $T_A = +25°C$, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 7)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 15.5V	53	72		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUT} \le 14.5V$	62	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		80	150	mV
V_{OH}	Output Swing High	I_L = 5mA	14.85	14.92		V
I_{SC}	Short-circuit Current			±180		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current	No load (EL5111)		2.5	4.5	mA
		No load (EL5211)		5	7.5	mA
		No load (EL5411)		10	15	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 8)	$1V \le V_{OUT} \le 14V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz (EL5211 and EL5411 only)		110		dB
d_G	Differential Gain (Note 9)	$R_F = R_G = 1k\Omega$ and V_{OUT} = 1.4V		0.16		%
d_P	Differential Phase (Note 9)	$R_F = R_G = 1k\Omega$ and V_{OUT} = 1.4V		0.22		°

NOTES:

7. Measured over operating temperature range
8. Slew rate is measured on rising and falling edges
9. NTSC signal generator used

Typical Performance Curves

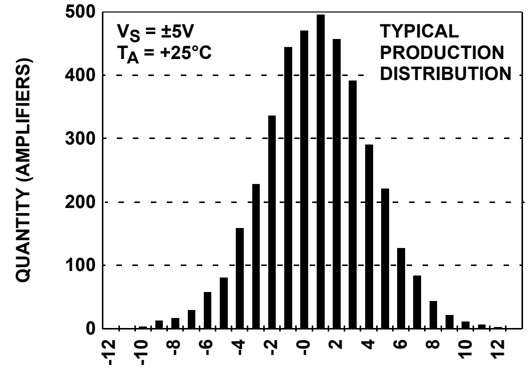


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

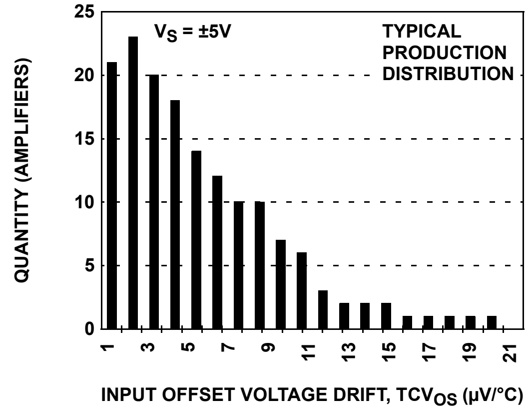


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

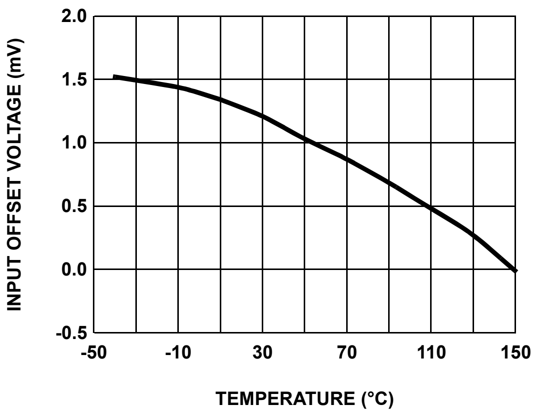


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

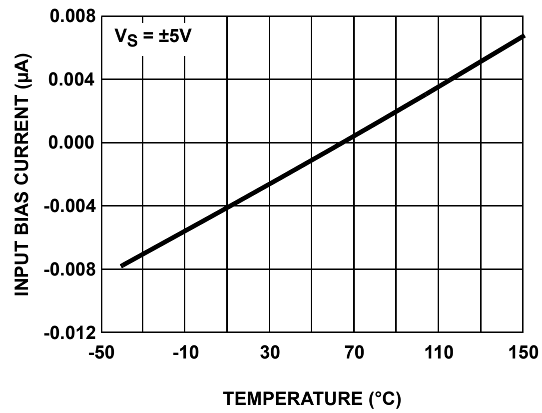


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

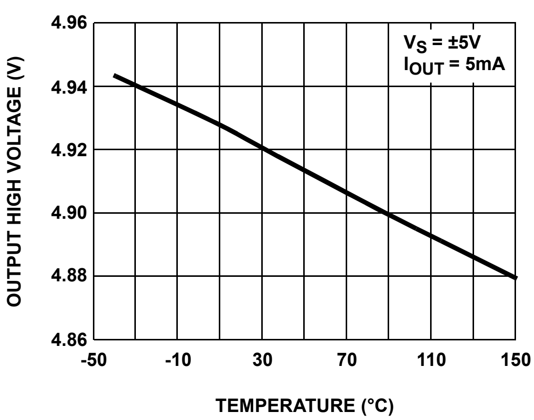


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

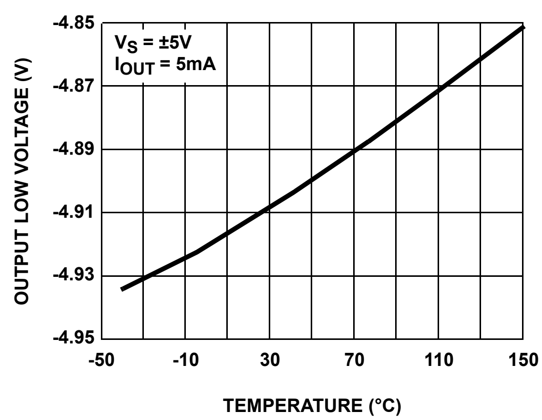


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

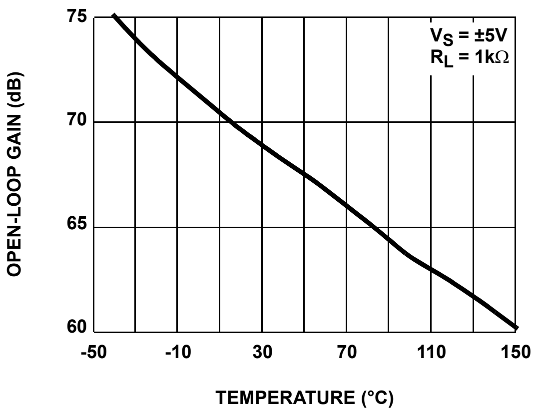


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

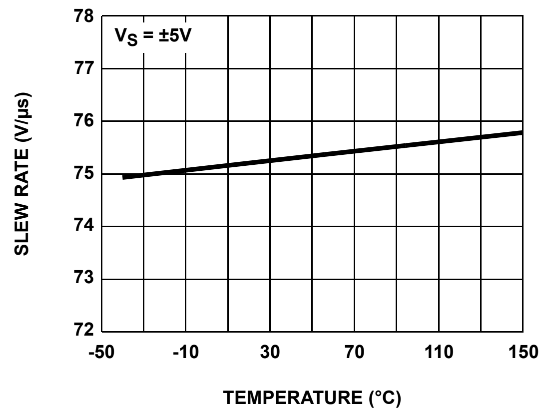


FIGURE 8. SLEW RATE vs TEMPERATURE

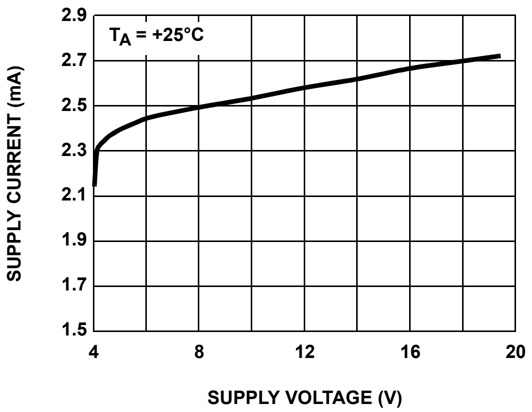


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

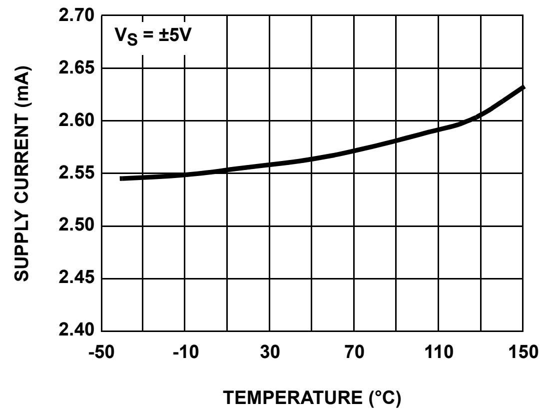


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

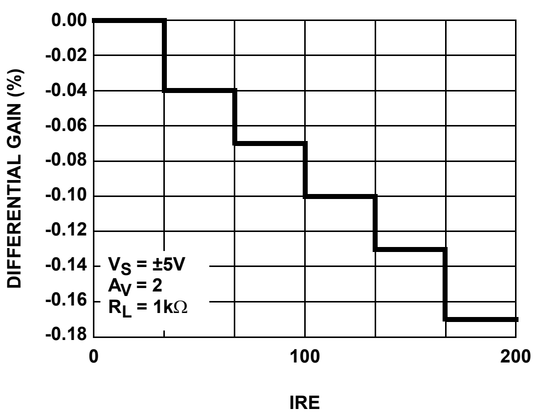


FIGURE 11. DIFFERENTIAL GAIN

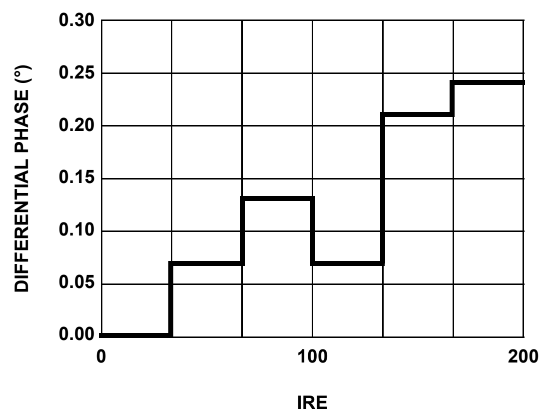


FIGURE 12. DIFFERENTIAL PHASE

Typical Performance Curves (Continued)

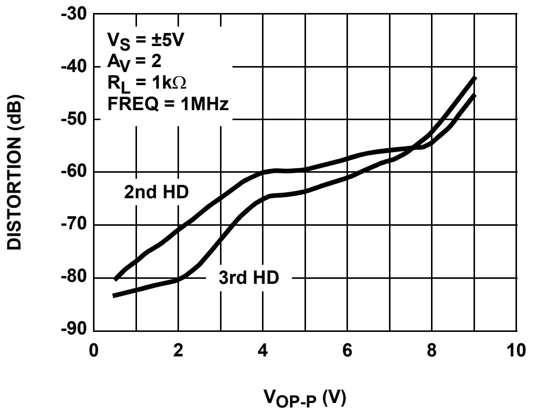


FIGURE 13. HARMONIC DISTORTION vs V_{OP-P}

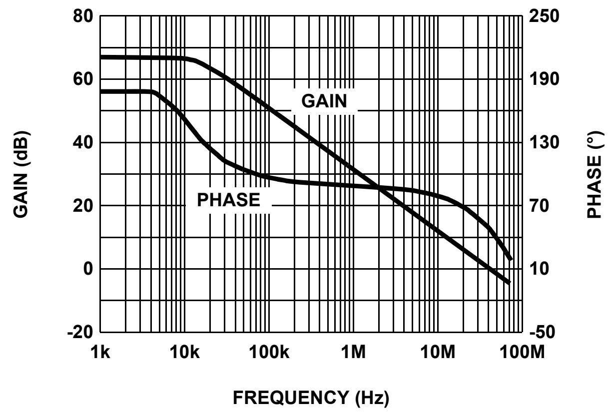


FIGURE 14. OPEN LOOP GAIN AND PHASE

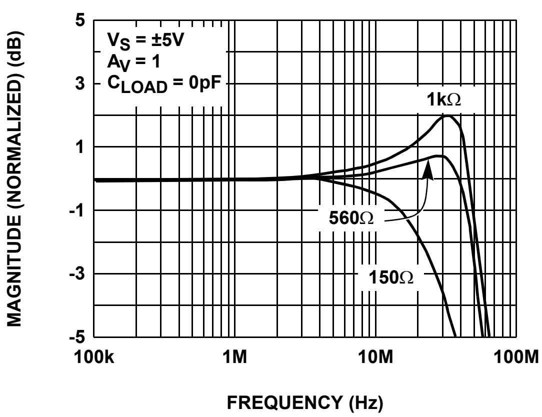


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L

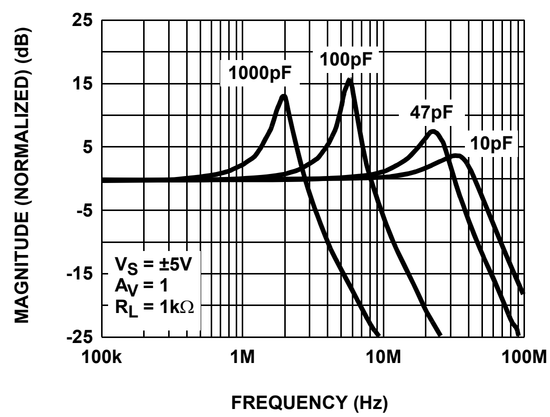


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L

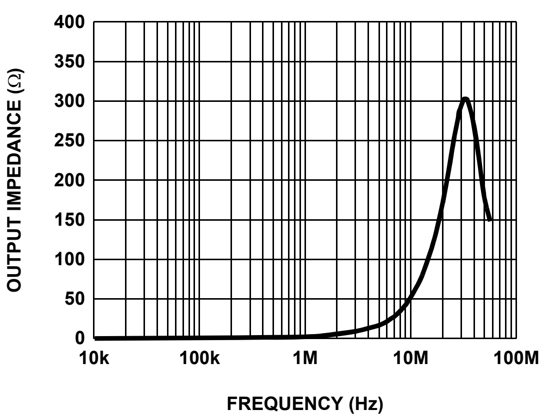


FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE

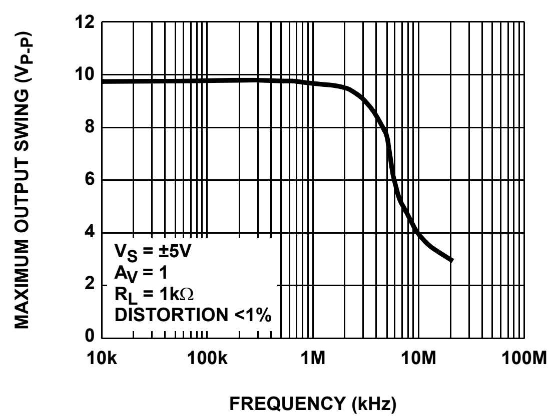


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

Typical Performance Curves (Continued)

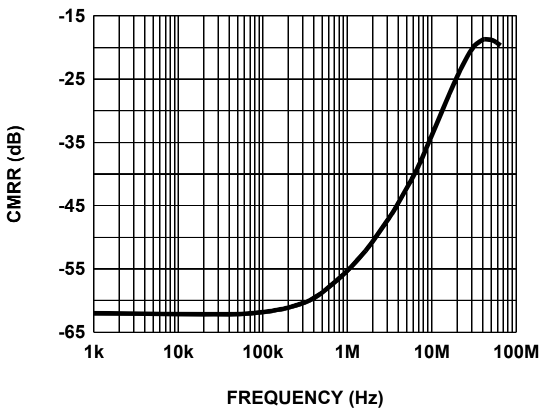


FIGURE 19. CMRR

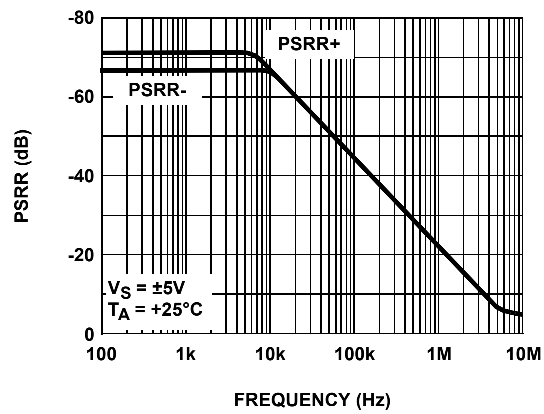


FIGURE 20. PSRR

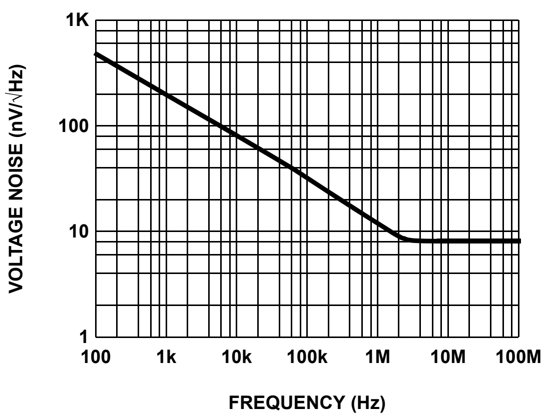


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY

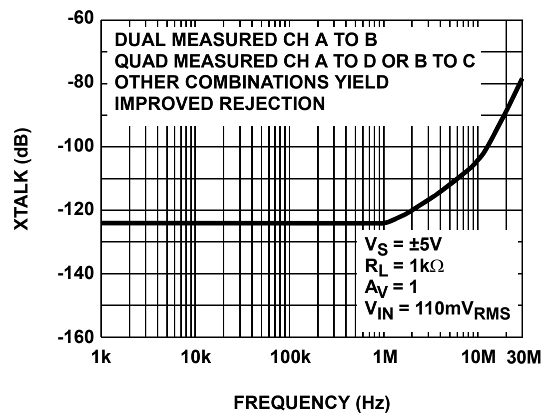


FIGURE 22. CHANNEL SEPARATION

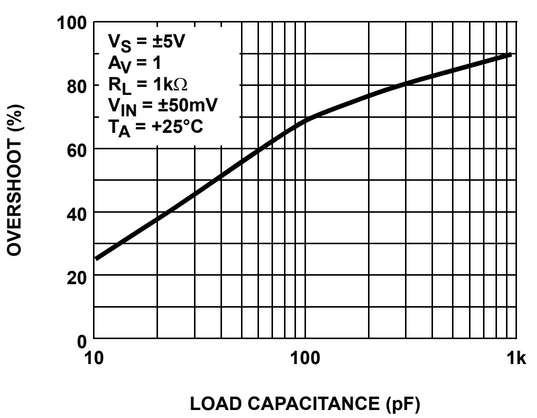


FIGURE 23. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

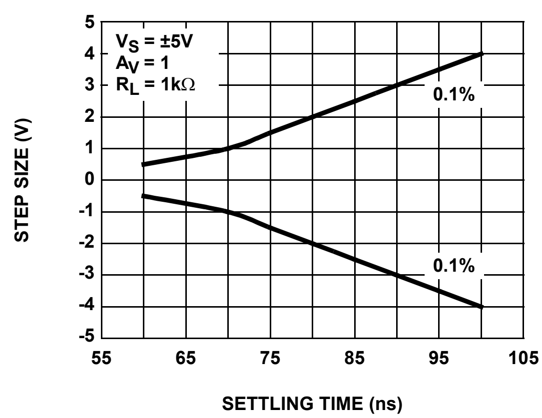


FIGURE 24. SETTLING TIME vs STEP SIZE

Typical Performance Curves (Continued)

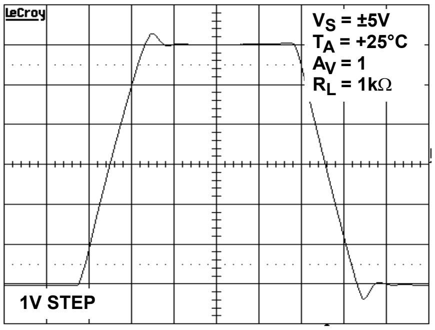


FIGURE 25. LARGE SIGNAL TRANSIENT RESPONSE

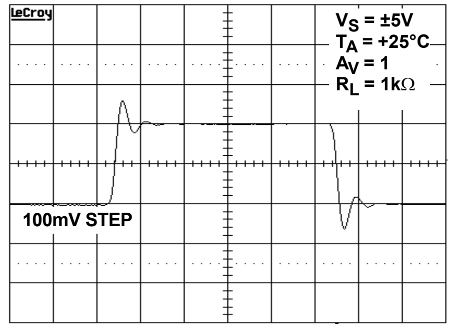
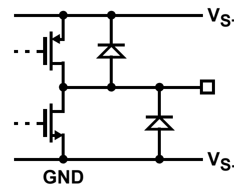
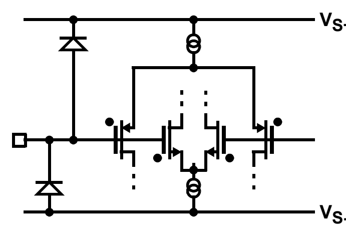


FIGURE 26. SMALL SIGNAL TRANSIENT RESPONSE

Pin Descriptions

EL5111 (TSOT-5)	EL5111 (HMSOP8)	EL5211 (HMSOP8)	EL5411 (HTSSOP14)	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	6	1	1	VOUTA	Amplifier A output	 CIRCUIT 1
4	2	2	2	VINA-	Amplifier A inverting input	 CIRCUIT 2
3	3	3	3	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
5	7	8	4	VS+	Positive power supply	
		5	5	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
		6	6	VINB-	Amplifier B inverting input	(Reference Circuit 2)
		7	7	VOUTB	Amplifier B output	(Reference Circuit 1)
			8	VOUTC	Amplifier C output	(Reference Circuit 1)
			9	VINC-	Amplifier C inverting input	(Reference Circuit 2)
			10	VINC+	Amplifier C non-inverting input	(Reference Circuit 2)
2	4	4	11	VS-	Negative power supply	
			12	VIND+	Amplifier D non-inverting input	(Reference Circuit 2)
			13	VIND-	Amplifier D inverting input	(Reference Circuit 2)
			14	VOUTD	Amplifier D output	(Reference Circuit 1)
	1, 5, 8			NC	Not connected	

Applications Information

Product Description

The EL5111, EL5211, and EL5411 voltage feedback amplifiers are fabricated using a high voltage CMOS process. They exhibit rail-to-rail input and output capability, are unity gain stable and have low power consumption (2.5mA per amplifier). These features make the EL5111, EL5211, and EL5411 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1kΩ, the EL5111, EL5211, and EL5411 have a -3dB bandwidth of 60MHz while maintaining a 75V/µs slew rate. The EL5111 is a single amplifier, the EL5211 a dual amplifier, and the EL5411 a quad amplifier.

Operating Voltage, Input, and Output

The EL5111, EL5211, and EL5411 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5111, EL5211, and EL5411 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The input common-mode voltage range of the EL5111, EL5211, and EL5411 extends 500mV beyond the supply rails. The output swings of the EL5111, EL5211, and EL5411 typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 27 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

V_S = ±5V, T_A = +25°C, A_V = 1, V_{IN} = $10V_{P-P}$

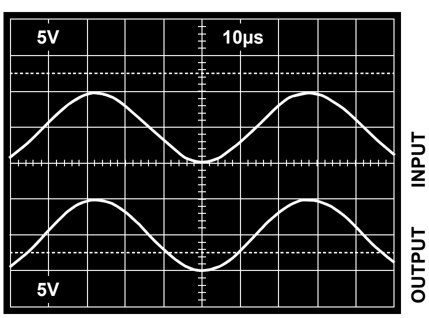


FIGURE 27. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5111, EL5211, and EL5411 will limit the short circuit current to ±180mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±65mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5111, EL5211, and EL5411 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 28 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

V_S = ±2.5V, T_A = +25°C, A_V = 1, V_{IN} = $6V_{P-P}$

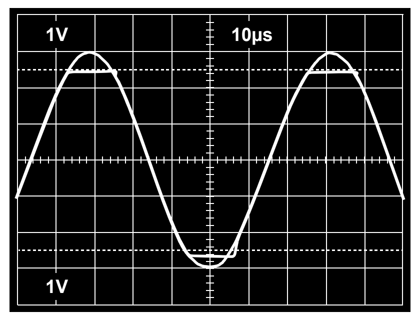


FIGURE 28. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5111, EL5211, and EL5411 amplifiers, it is possible to exceed the +125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT} i) \times I_{LOAD} i] \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT} i - V_S -) \times I_{LOAD} i] \quad \text{(EQ. 3)}$$

when sinking,

where:

- i = 1 to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- $V_{OUT}i$ = Maximum output voltage of the application
- $I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figures 29 through 36 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 29 through 36.

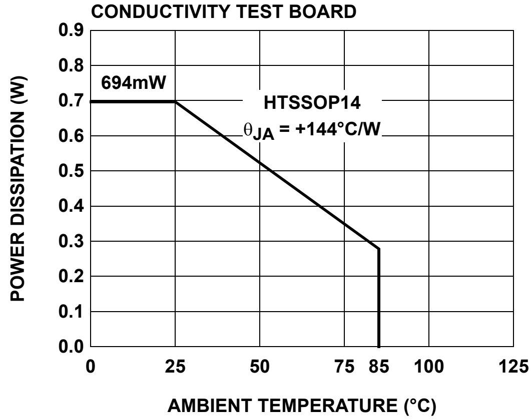


FIGURE 29. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

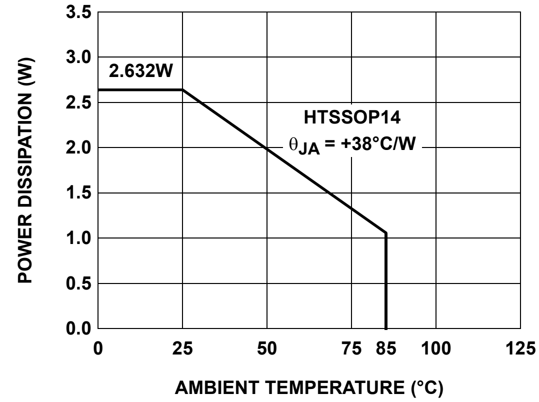


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

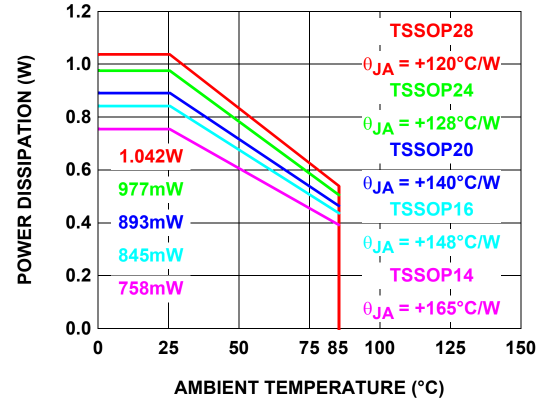


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

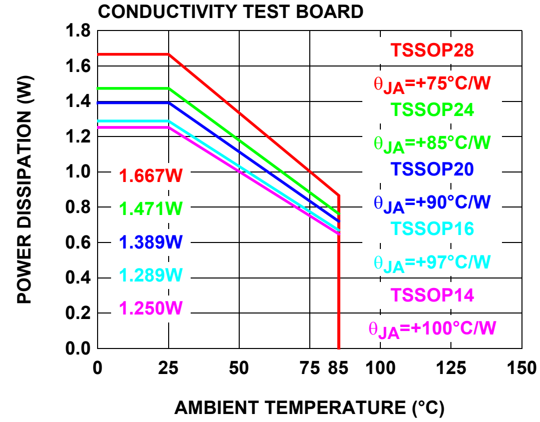


FIGURE 32. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

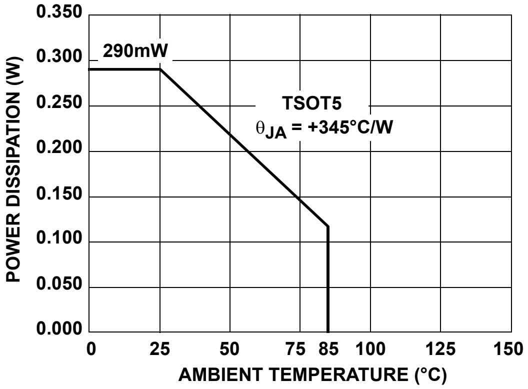


FIGURE 33. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

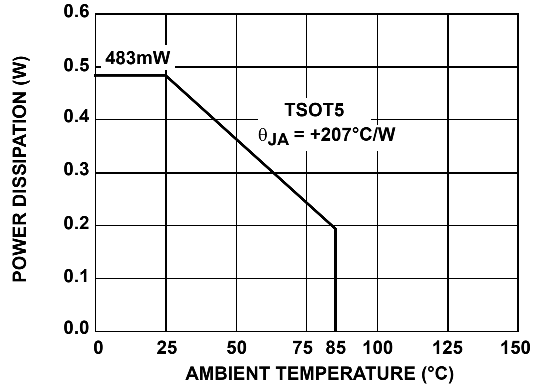


FIGURE 34. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

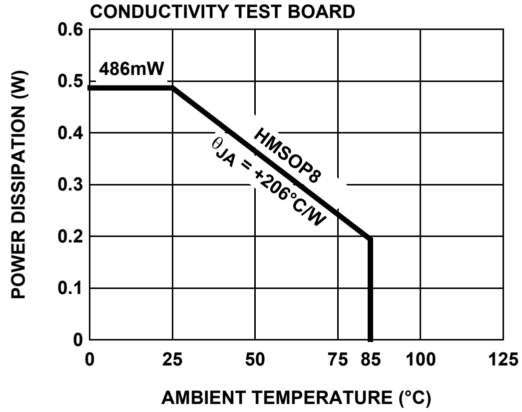


FIGURE 35. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

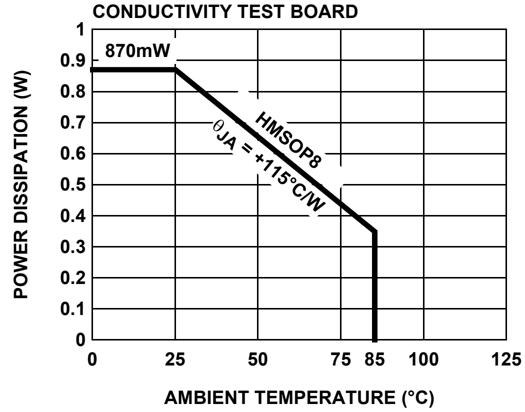


FIGURE 36. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Unused Amplifiers

It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5111, EL5211, and EL5411 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ to pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 27, 2015	FN7119.8	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections.

About Intersil

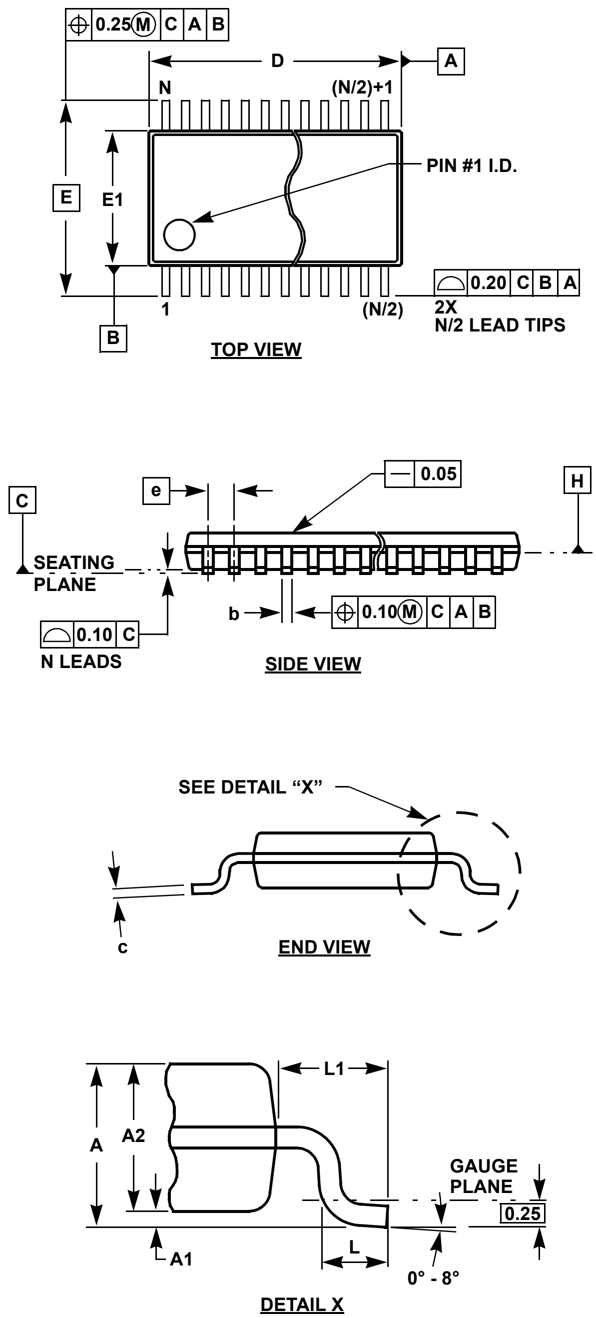
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Thin Shrink Small Outline Package Family (TSSOP)



MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

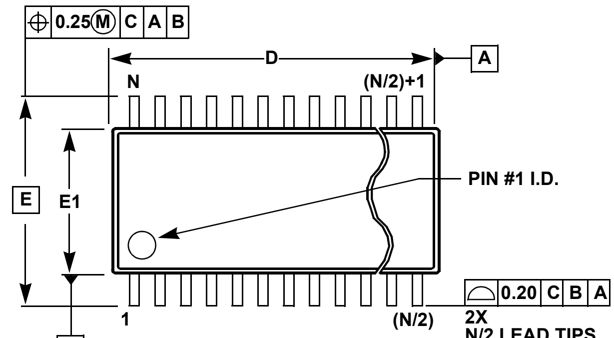
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

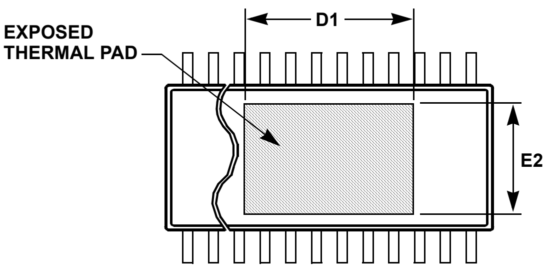
NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

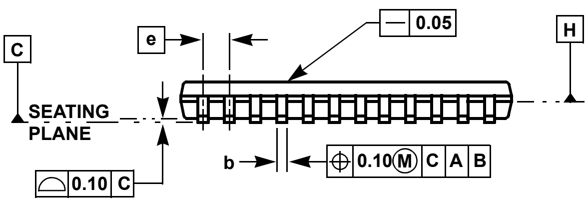
HTSSOP (Heat-Sink TSSOP) Family



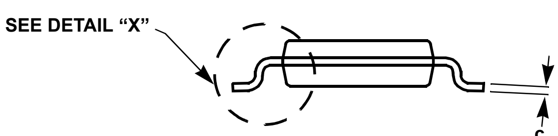
TOP VIEW



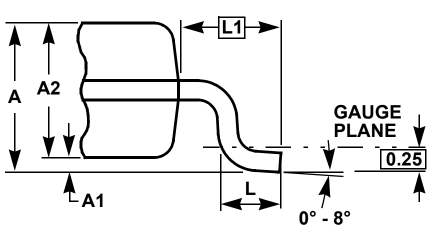
BOTTOM VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

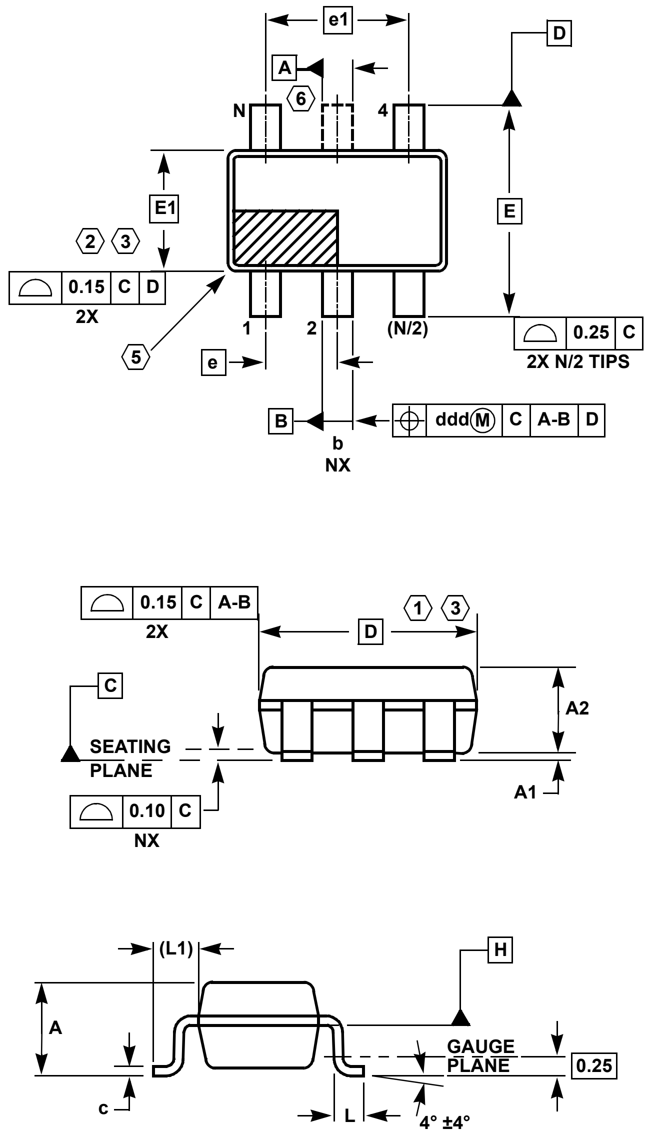
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

TSOT Package Family



MDP0049

TSOT PACKAGE FAMILY

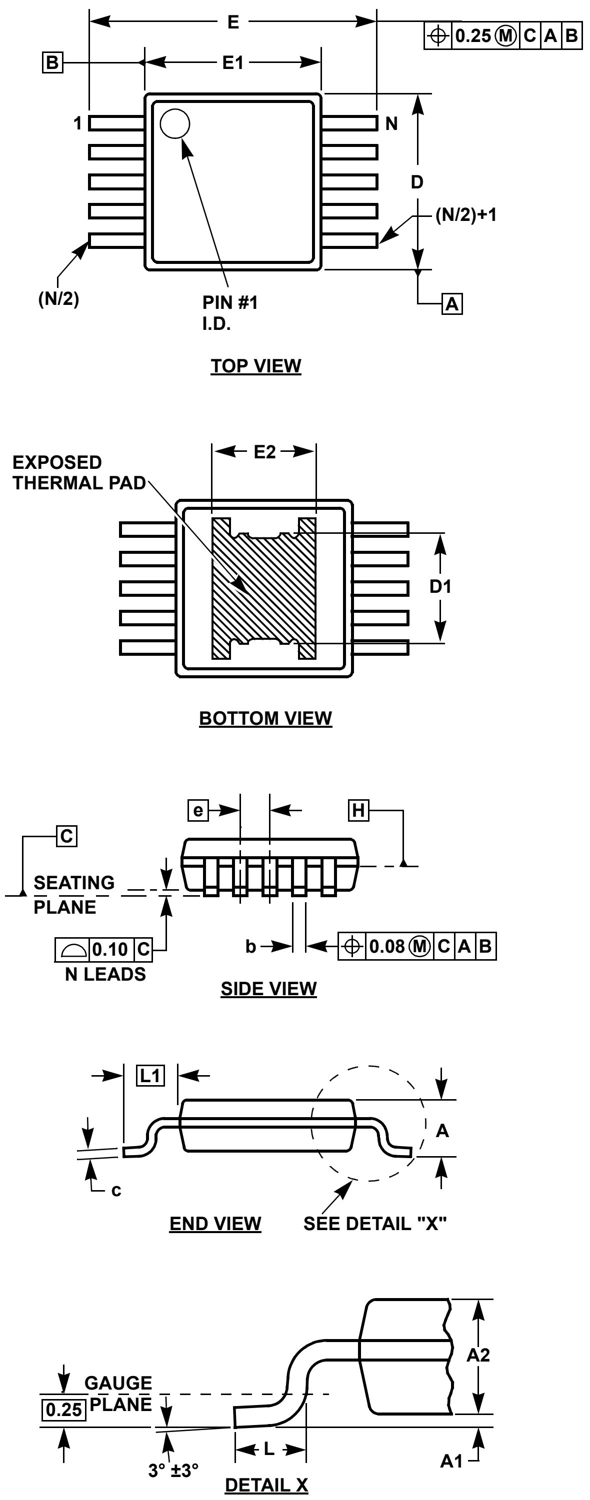
SYMBOL	MILLIMETERS			TOLERANCE
	TSOT5	TSOT6	TSOT8	
A	1.00	1.00	1.00	Max
A1	0.05	0.05	0.05	±0.05
A2	0.87	0.87	0.87	±0.03
b	0.38	0.38	0.29	±0.07
c	0.127	0.127	0.127	+0.07/-0.007
D	2.90	2.90	2.90	Basic
E	2.80	2.80	2.80	Basic
E1	1.60	1.60	1.60	Basic
e	0.95	0.95	0.65	Basic
e1	1.90	1.90	1.95	Basic
L	0.40	0.40	0.40	±0.10
L1	0.60	0.60	0.60	Reference
ddd	0.20	0.20	0.13	-
N	5	6	8	Reference

Rev. B 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.15mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (TSOT6 AND TSOT8 only).
6. TSOT5 version has no center lead (shown as a dashed line).

HMSOP (Heat-Sink MSOP) Package Family



MDP0050

HMSOP (HEAT-SINK MSOP) PACKAGE FAMILY

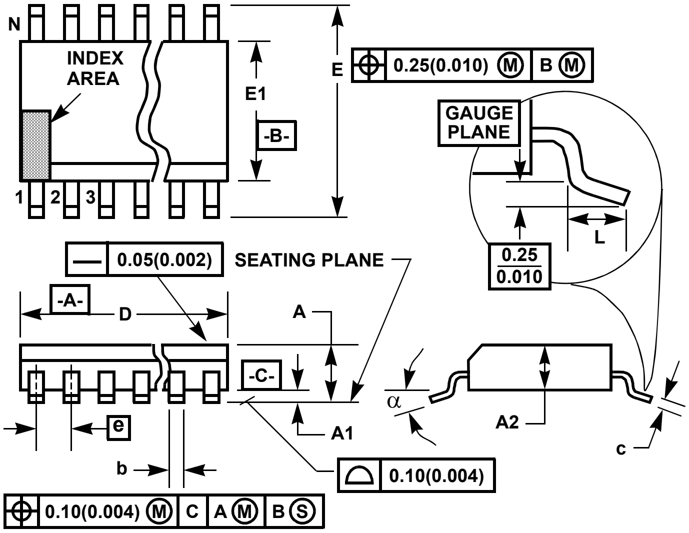
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	HMSOP8	HMSOP10		
A	1.00	1.00	Max.	-
A1	0.075	0.075	+0.025/-0.050	-
A2	0.86	0.86	±0.09	-
b	0.30	0.20	+0.07/-0.08	-
c	0.15	0.15	±0.05	-
D	3.00	3.00	±0.10	1, 3
D1	1.85	1.85	Reference	-
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
E2	1.73	1.73	Reference	-
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. 1 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Thin Shrink Small Outline Plastic Packages (TSSOP)



M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)