EL5177

550MHz Differential Twisted-Pair Driver

FN7344
Rev 6.00
August 28, 2012

The EL5177 is a high bandwidth amplifier with an output in differential form. It is primarily targeted for applications such as driving twisted-pair lines or any application where common mode injection is likely to occur. The input signal can be in either single-ended or differential form but the output is always in differential form.

On the EL5177, two feedback inputs provide the user with the ability to set the device gain (stable at a minimum gain of 1).

The output common mode level is set by the reference pin (REF), which has a -3dB bandwidth of 110MHz. Generally, this pin is grounded but it can be tied to any voltage reference.

Both outputs (OUT+, OUT-) are short circuit protected to withstand temporary overload condition.

The EL5177 is available in the 10 Ld MSOP package and is specified for operation over the full -40°C to +85°C temperature range.

See also EL5174 (EL5177 in 8 Ld MSOP).

Features

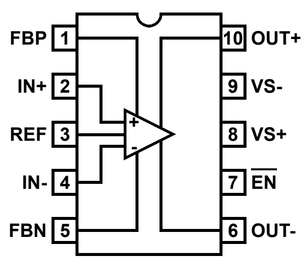
- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 550MHz 3dB bandwidth
- 1100V/µs slew rate
- Low distortion at 20MHz
- Single 5V or dual ±5V supplies
- 40mA maximum output current
- Low power, 12.5mA typical supply current
- Pb-free (RoHS compliant)

Applications

- Twisted-pair drivers
- Differential line drivers
- VGA over twisted-pair
- ADSL/HDSL drivers
- Single-ended to differential amplification
- Transmission of analog signals in a noisy environment

Pinout

EL5177
(10 LD MSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	FBP	Non-inverting feedback input; resistor R_{F1} must be connected from this pin to V_{OUT}
2	IN+	Non-inverting input
3	REF	Output common-mode control; the common-mode voltage of V_{OUT} will follow the voltage on this pin
4	IN-	Inverting input
5	FBN	Inverting feedback input; resistor R_{F2} must be connected from this pin to V_{OUT}
6	OUT-	Inverting output
7	$\overline{EN}$	Enabled when this pin is floating or the applied voltage $\leq V_S + -1.5$
8	VS+	Positive supply
9	VS-	Negative supply
10	OUT+	Non-inverting output

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
EL5177IYZ	BAAKA	10 Ld MSOP (3.0mm)	M10.118A

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5177. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S+ to V_S-) 12V
V_{IN}, V_{INB}, V_{REF} . . . . V_S- + 0.8V (min) to V_S+ - 0.8V (max)
V_{IN} - V_{INB} . . . . ±5
Supply Voltage Rate-of-rise (dV/dT) 1V/µs
Input Voltage (IN+, IN- to V_S+, V_S-) . . . . V_S- - 0.3V to V_S+ + 0.3V
Differential Input Voltage (IN+ to IN-) . . . . ±4.8V
Maximum Output Current . . . . ±60mA

Thermal Information

Recommended Operating Temperature . . . . -40°C to +85°C
Operating Junction Temperature . . . . +135°C
Storage Temperature Range . . . . -65°C to +150°C
Power Dissipation . . . . See Curves
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = +25°C, V_{IN} = 0V, R_{LD} = 1kΩ, R_F = 0, R_G = OPEN, C_{LD} = 2.7pF, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = 1, C_{LD} = 2.7pF		550		MHz
		A_V = 2, R_F = 500, C_{LD} = 2.7pF		130		MHz
		A_V = 10, R_F = 500, C_{LD} = 2.7pF		20		MHz
BW	±0.1dB Bandwidth	A_V = 1, C_{LD} = 2.7pF		120		MHz
SR	Slew Rate	V_{OUT} = 3V_{P-P}, 20% to 80%	800	1100		V/µs
t_{STL}	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}		10		ns
t_{OVR}	Output Overdrive Recovery Time			20		ns
GBWP	Gain Bandwidth Product			200		MHz
V_{REF}BW (-3dB)	V_{REF} -3dB Bandwidth	A_V =1, C_{LD} = 2.7pF		110		MHz
V_{REF}SR+	V_{REF} Slew Rate - Rise	V_{OUT} = 2V_{P-P}, 20% to 80%		134		V/µs
V_{REF}SR-	V_{REF} Slew Rate - Fall	V_{OUT} = 2V_{P-P}, 20% to 80%		70		V/µs
V_N	Input Voltage Noise	at 10kHz		21		nV/√Hz
I_N	Input Current Noise	at 10kHz		2.7		pA/√Hz
HD2	Second Harmonic Distortion	V_{OUT} = 2V_{P-P}, 5MHz		-95		dBc
		V_{OUT} = 2V_{P-P}, 20MHz		-94		dBc
HD3	Third Harmonic Distortion	V_{OUT} = 2V_{P-P}, 5MHz		-88		dBc
		V_{OUT} = 2V_{P-P}, 20MHz		-87		dBc
dG	Differential Gain at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.06		%
dθ	Differential Phase at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.13		°
INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage			±1.4	±25	mV
I_{IN}	Input Bias Current (V_{IN}+, V_{IN}-)		-30	-14	-7	µA
I_{REF}	Input Bias Current (V_{REF})		0.5	2.3	4	µA
R_{IN}	Differential Input Resistance			150		kΩ
C_{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Mode Input Range		±2.1	±2.3	±2.5	V
CMIR+	Common Mode Positive Input Range at V_{IN}+, V_{IN}-			3.4		V

Electrical Specifications

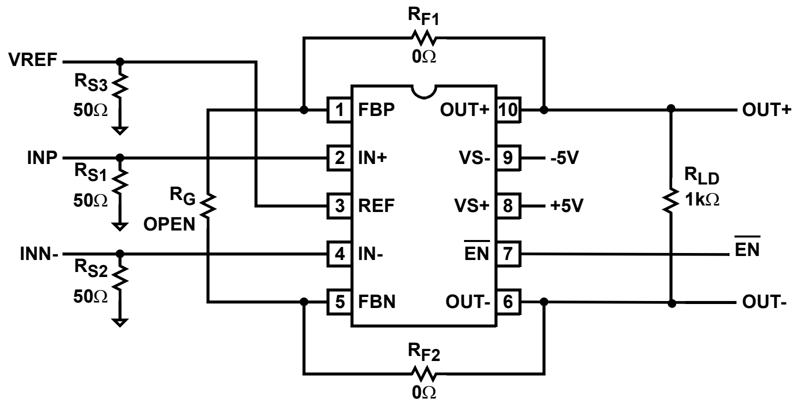
V_S+ = +5V, V_S- = -5V, T_A = +25°C, V_{IN} = 0V, R_{LD} = 1kΩ, R_F = 0, R_G = OPEN, C_{LD} = 2.7pF, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
CMIR-	Common Mode Negative Input Range at $V_{IN}+$, $V_{IN}-$			-4.3		V
$V_{REFIN}+$	Positive Reference Input Voltage Range	$V_{IN}+$ = $V_{IN}-$ = 0V	3.4	3.7		V
$V_{REFIN}-$	Negative Reference Input Voltage Range	$V_{IN}+$ = $V_{IN}-$ = 0V		-3.3	-3	V
V_{REFOS}	Output Offset Relative to V_{REF}			±50	±100	mV
CMRR	Input Common Mode Rejection Ratio	V_{IN} = ±2.5V	65	78		dB
Gain	Gain Accuracy	V_{IN} = 1V	0.980	0.995	1.010	V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Voltage Swing	R_L = 500Ω to GND	±3.6	±3.8		V
$I_{OUT}+$(Max)	Maximum Source Output Current	R_L = 10Ω, $V_{IN}+$ = 1.1V, $V_{IN}-$ = -1.1V, V_{REF} = 0	35	50		mA
$I_{OUT}-$(Max)	Maximum Sink Output Current			-40	-30	mA
R_{OUT}	Output Impedance			130		mΩ
SUPPLY						
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	4.75		11	V
$I_{S(ON)}$	Power Supply Current - Per Channel		10	12.5	14	mA
$I_{S(OFF)}+$	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V		76	120	µA
$I_{S(OFF)}-$	Negative Power Supply Current - Disabled		-200	-120		µA
PSRR	Power Supply Rejection Ratio	V_S from ±4.5V to ±5.5V	60	75		dB
ENABLE						
t_{EN}	Enable Time			130		ns
t_{DS}	Disable Time			1.2		µs
V_{IH}	$\overline{EN}$ Pin Voltage for Power-Up				V_S+ -1.5	V
V_{IL}	$\overline{EN}$ Pin Voltage for Shutdown		V_S+ -0.5			V
I_{IH-EN}	$\overline{EN}$ Pin Input Current High	At V_{EN} = 5V		40	50	µA
I_{IL-EN}	$\overline{EN}$ Pin Input Current Low	At V_{EN} = 0V	-6	-2.5		µA

NOTE:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Connection Diagram



Typical Performance Curves

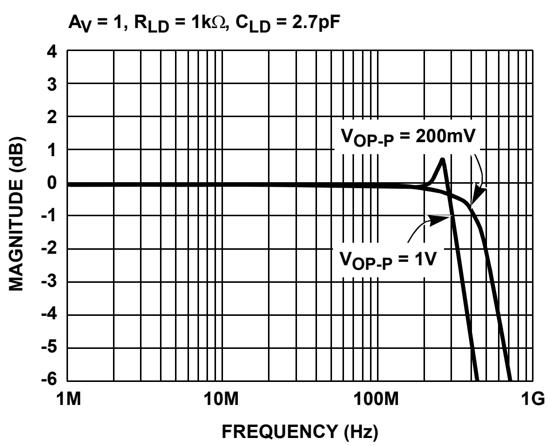


FIGURE 1. FREQUENCY RESPONSE

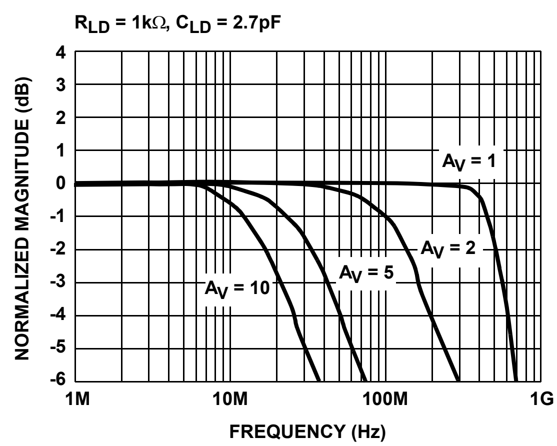


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS GAIN

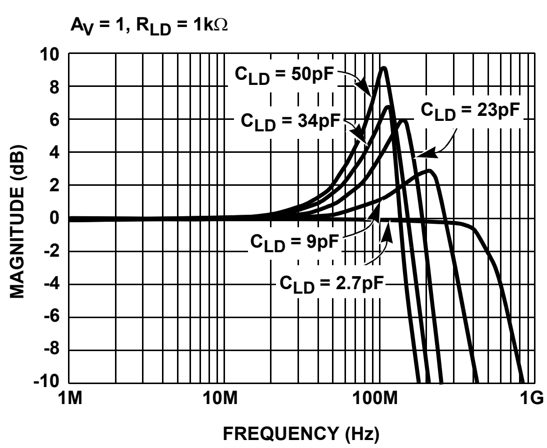


FIGURE 3. FREQUENCY RESPONSE vs C_{LD}

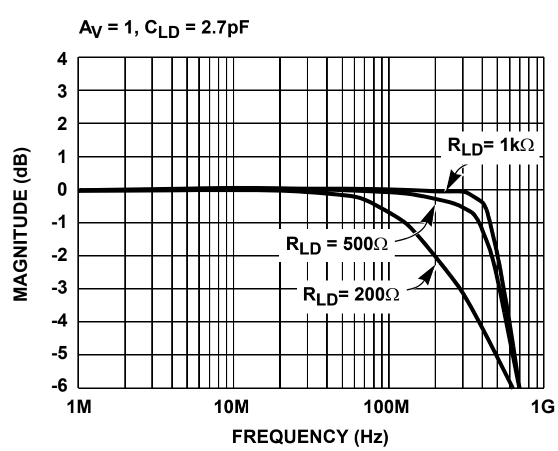


FIGURE 4. FREQUENCY RESPONSE vs R_{LD}

Typical Performance Curves (Continued)

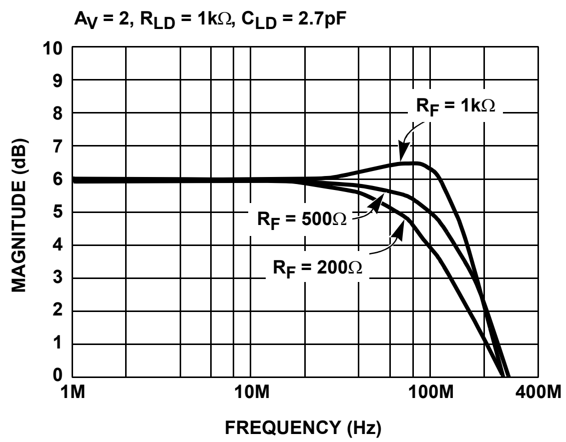


FIGURE 5. FREQUENCY RESPONSE

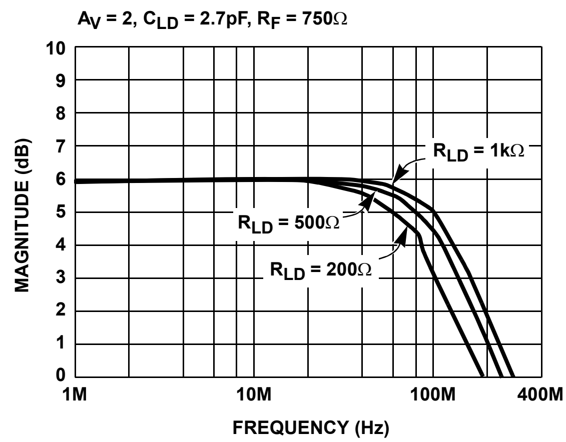


FIGURE 6. FREQUENCY RESPONSE vs R_{LD}

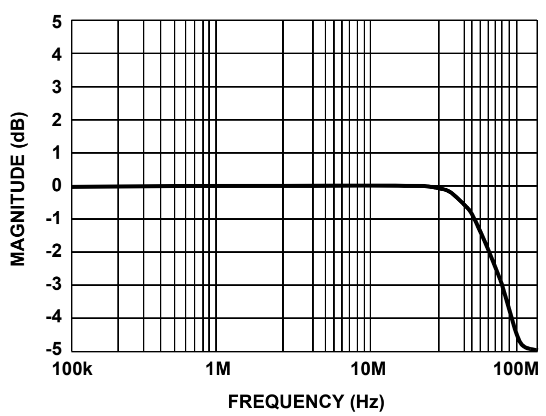


FIGURE 7. FREQUENCY RESPONSE - V_{REF}

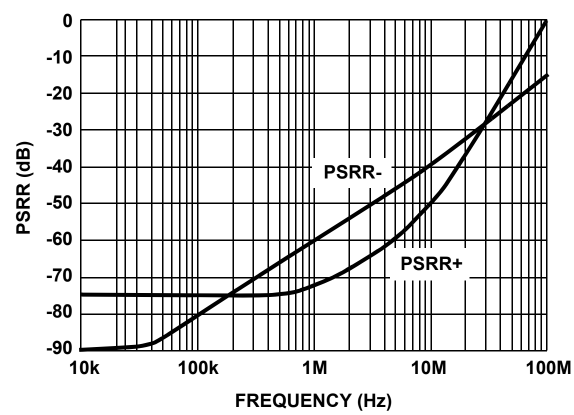


FIGURE 8. PSRR vs FREQUENCY

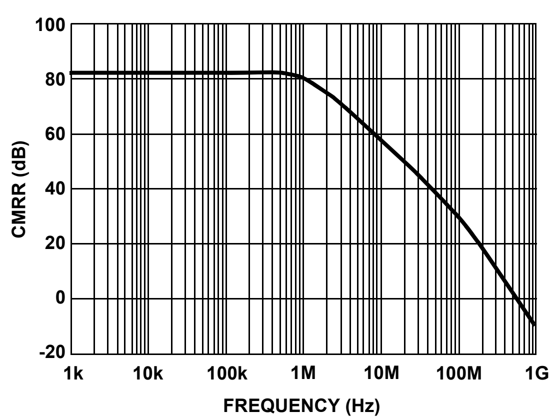


FIGURE 9. CMRR vs FREQUENCY

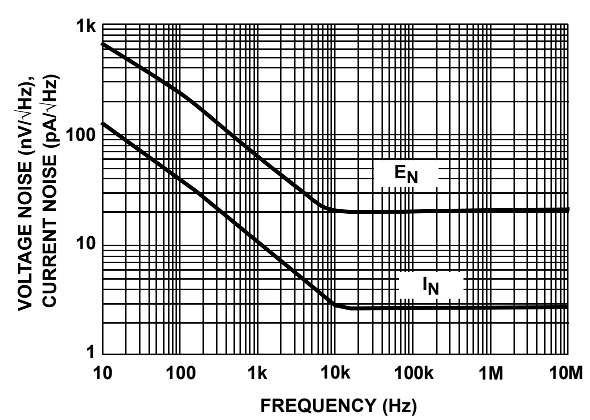


FIGURE 10. VOLTAGE AND CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

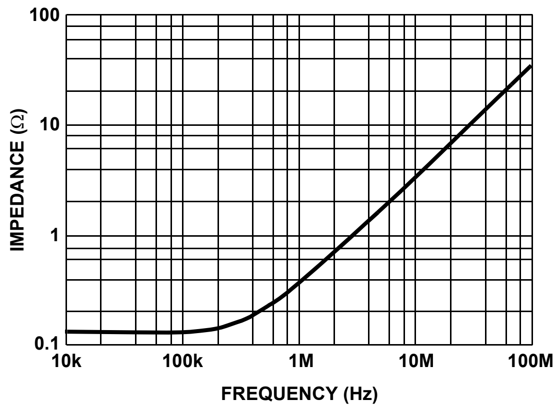


FIGURE 11. OUTPUT IMPEDANCE vs FREQUENCY

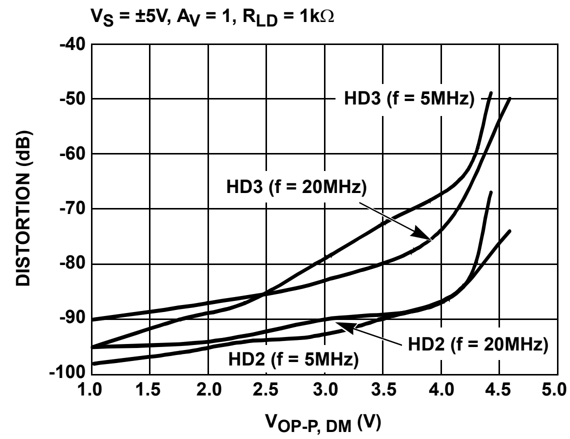


FIGURE 12. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

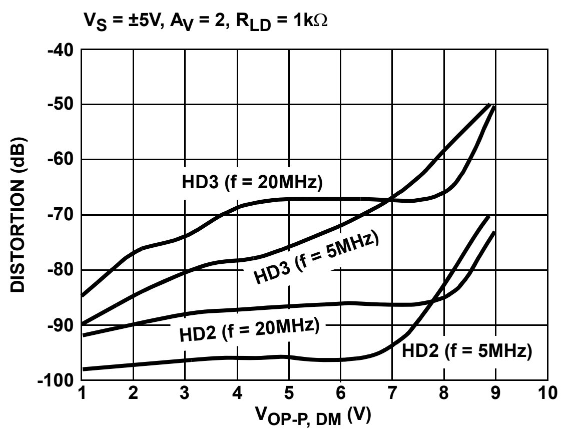


FIGURE 13. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

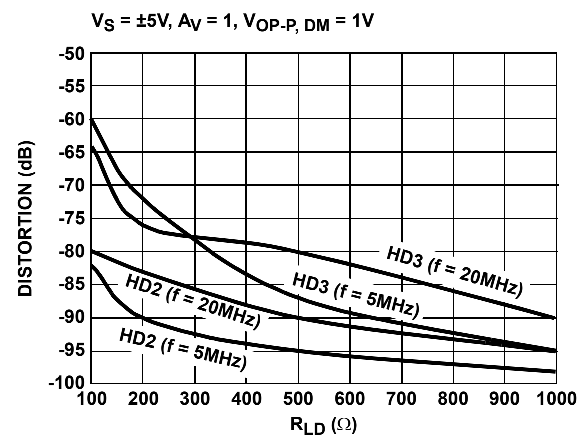


FIGURE 14. HARMONIC DISTORTION vs R_{LD}

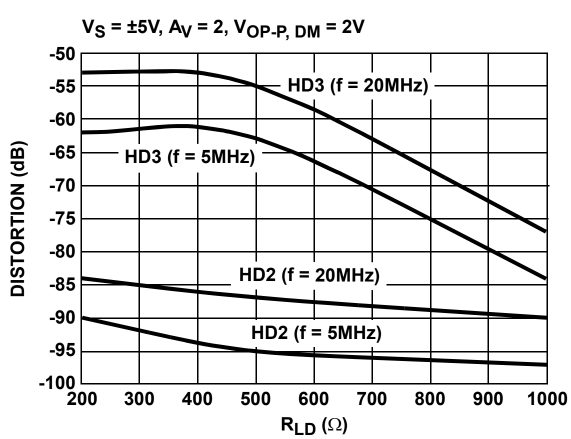


FIGURE 15. HARMONIC DISTORTION vs R_{LD}

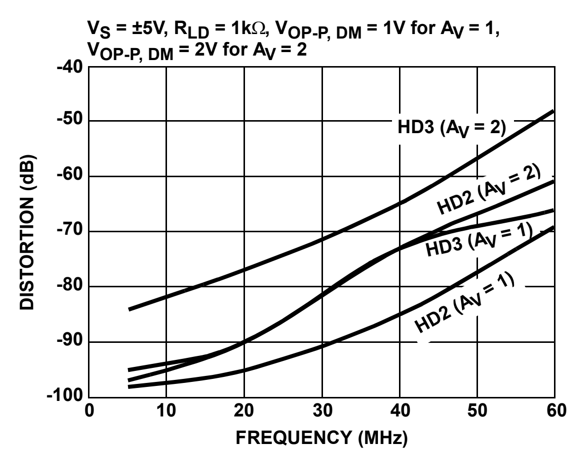


FIGURE 16. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves (Continued)

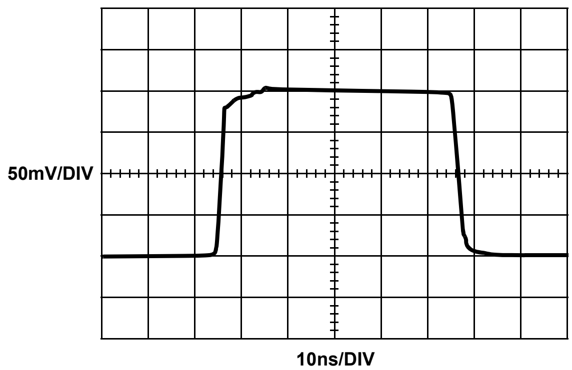


FIGURE 17. SMALL SIGNAL TRANSIENT RESPONSE

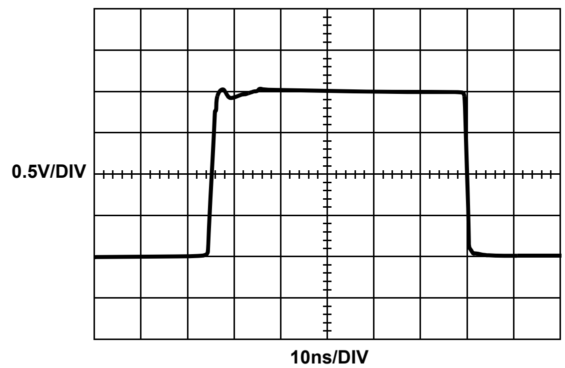


FIGURE 18. LARGE SIGNAL TRANSIENT RESPONSE

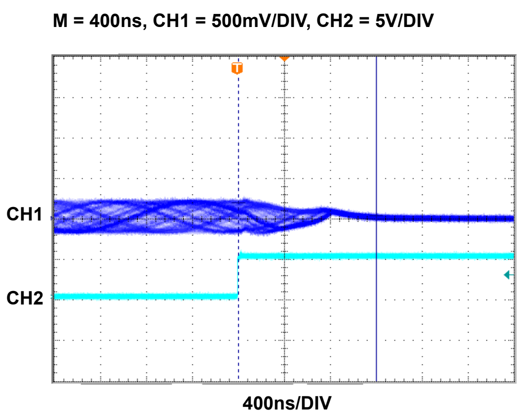


FIGURE 19. ENABLED RESPONSE

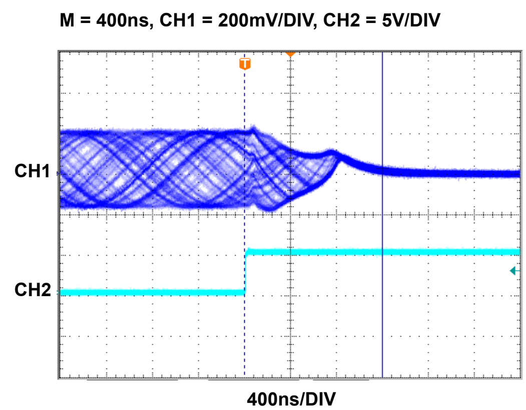


FIGURE 20. DISABLED RESPONSE

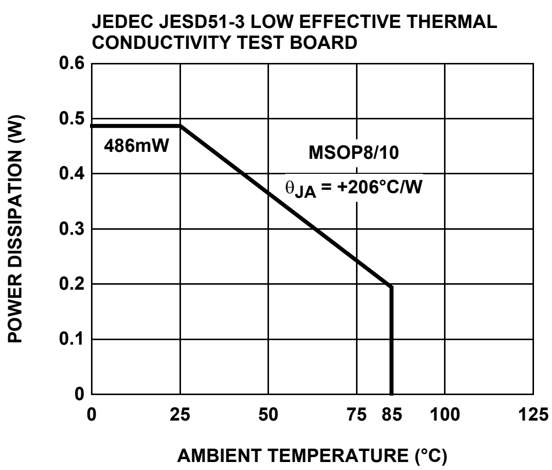


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

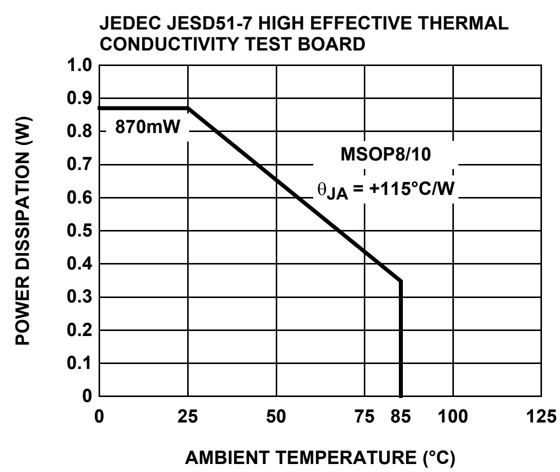
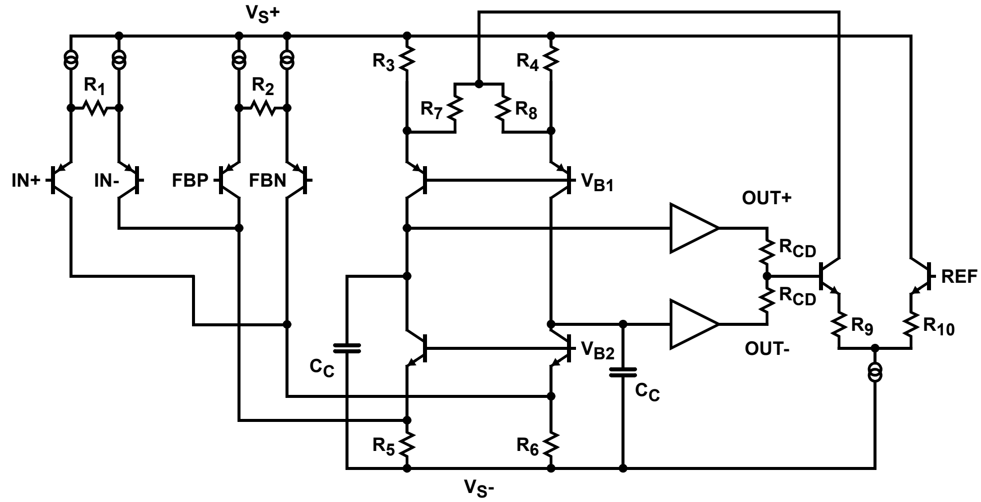


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5177 is a wide bandwidth, low power and single/differential ended to differential output amplifier. It can be used as single/differential ended to differential converter. The EL5177 is internally compensated for closed loop gain of +1 or greater. Connected in gain of 1 and driving a 1kΩ differential load, the EL5177 has a -3dB bandwidth of 550MHz. Driving a 200Ω differential load at gain of 2, the bandwidth is about 130MHz. The EL5177 is available with a power-down feature to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The EL5177 has been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.3V to 3.4V for ±5V supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal to become distorted.

The output of the EL5177 can swing from -3.8V to +3.8V at a 1kΩ differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

The voltage applied at REF pin can set the output common mode voltage and the gain is one. The differential gain is set by the R_F and R_G network.

The gain setting for EL5177 is expressed in Equation 1:

$$V_{ODM} = (V_{IN}+ - V_{IN}-) \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G}\right)$$

$$V_{ODM} = (V_{IN}+ - V_{IN}-) \times \left(1 + \frac{2R_F}{R_G}\right) \quad \text{(EQ. 1)}$$

$$V_{OCM} = V_{REF}$$

Where:

$R_{F1} = R_{F2} = R_F$

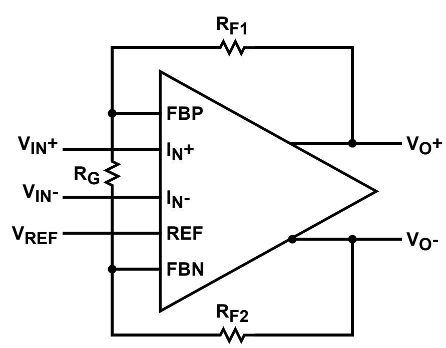


FIGURE 23.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the OUT+ pin to FBP pin and OUT- pin to FBN pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5177 depends on the load and the feedback network. R_F and R_G appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum bandwidth performance. For gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F between 500Ω to 1kΩ.

The EL5177 has a gain bandwidth product of 200MHz for R_{LD} = 1kΩ. For gains ≥5, its bandwidth can be predicted by Equation 2:

$$Gain \times BW = 200MHz \quad \text{(EQ. 2)}$$

Driving Capacitive Loads and Cables

The EL5177 can drive a 23pF differential capacitor in parallel with a 1kΩ differential load with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL5177 can be disabled and its outputs placed in a high impedance state. The turn-off time is about 1.2µs and the turn-on time is about 130ns. When disabled, the amplifier's supply current is reduced to 1.7µA for I_S+ and 120µA for I_S- typically, thereby effectively eliminating the power consumption. The amplifier's power-down can be controlled by standard CMOS signal levels at the EN pin. The applied logic signal is relative to V_S+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below V_S+ will enable the amplifier. The amplifier will be disabled when the signal at the $\overline{EN}$ pin is above V_S+ - 0.5V.

Output Drive Capability

The EL5177 has internal short circuit protection. Its typical short circuit current is ±40mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnect.

Power Dissipation

With the high output drive capability of the EL5177, it is possible to exceed the +135°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 3:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 3)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = i \times \left(V_{STOT} \times I_{SMAX} + (V_{STOT} - \Delta V_O) \times \frac{\Delta V_O}{R_{LD}}\right) \quad \text{(EQ. 4)}$$

Where:

V_{STOT} = Total supply voltage = V_S+ - V_S-

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate this loss is to boost the high frequency gain at the receiver side.

Typical Applications

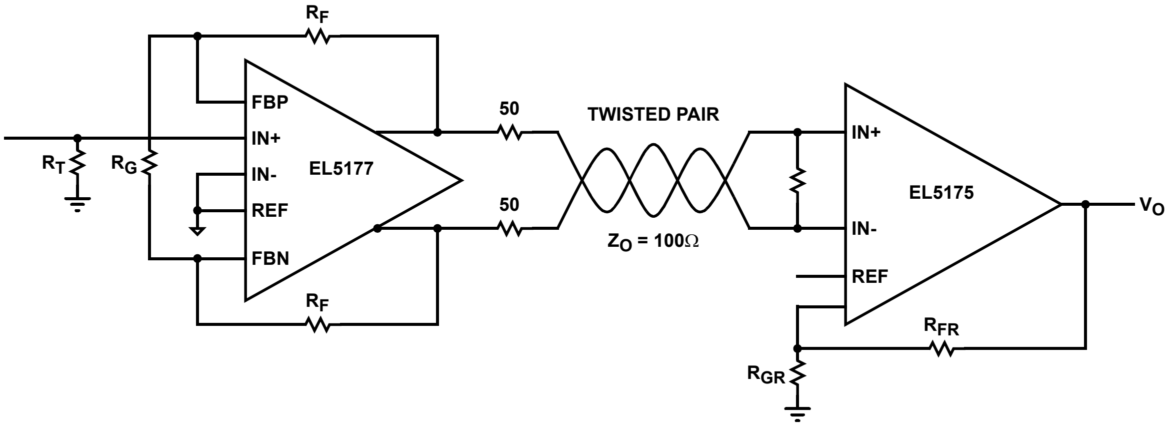
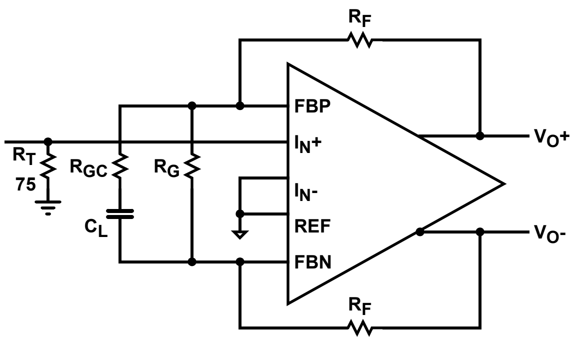
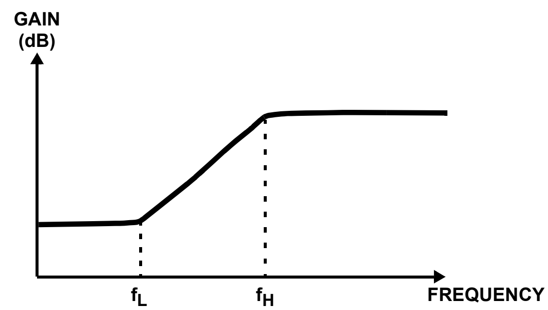


FIGURE 24. TWISTED PAIR CABLE RECEIVER



$$\text{DC Gain} = 1 + \frac{2R_F}{R_G}$$

$$(\text{HF})\text{Gain} = 1 + \frac{2R_F}{R_G \parallel R_{GC}}$$



$$f_L \cong \frac{1}{2\pi R_G C_C}$$

$$f_H \cong \frac{1}{2\pi R_{GC} C_C}$$

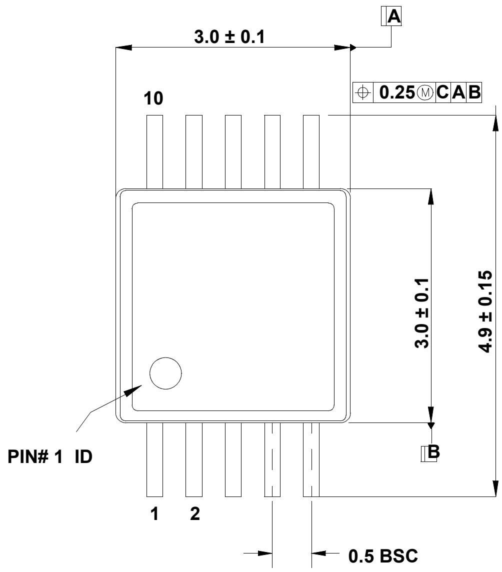
FIGURE 25. TRANSMIT EQUALIZER

Package Outline Drawing

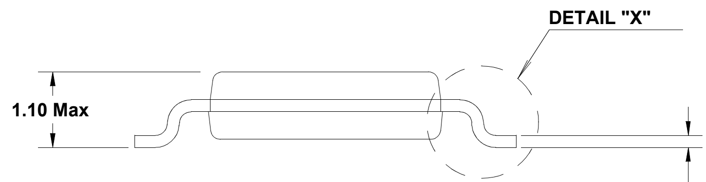
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

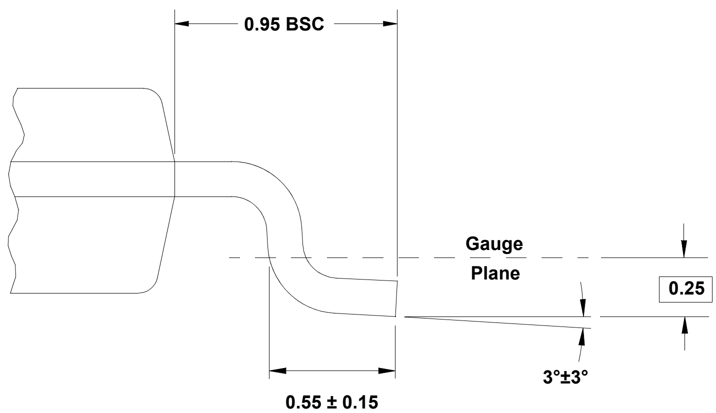
Rev 0, 9/09



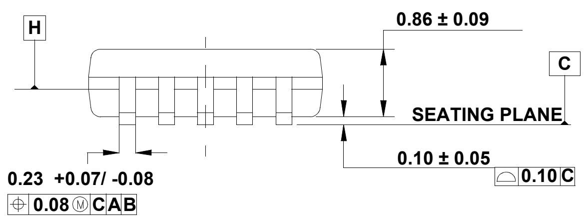
TOP VIEW



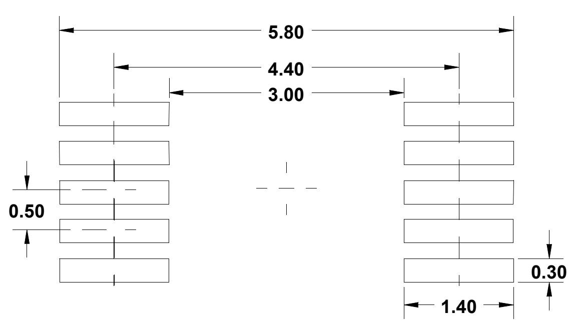
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.