RENESAS

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POSSIBLE SUBSTITUTE PRODUCT
(NOT PIN-FOR-PIN) ISL8002, ISL8002A

DATASHEET

EL7532

Monolithic 2A Step-Down Regulator

FN7435
Rev 9.00
December 9, 2015

The EL7532 is a synchronous, integrated FET 2A step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a single Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider.

The EL7532 features PWM mode control. The operating frequency is typically 1.5MHz. Additional features include a 100ms Power-On-Reset output, <1µA shut-down current and over-temperature protection.

The EL7532 is available in the 10-pin MSOP package, making the entire converter occupy less than 0.18 in^2 of PCB area with components on one side only. The package is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

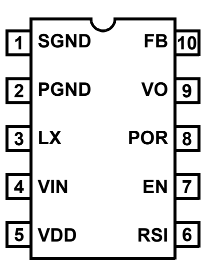
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
EL7532IYZ (Note)	BAARA	-40 to +85	10 Ld MSOP (Pb-free)	MDP0043

*Add -T7 suffix for 1k unit or -T13 suffix for 2.5k unit tape and reel options. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

EL7532
(10 LD MSOP)
TOP VIEW



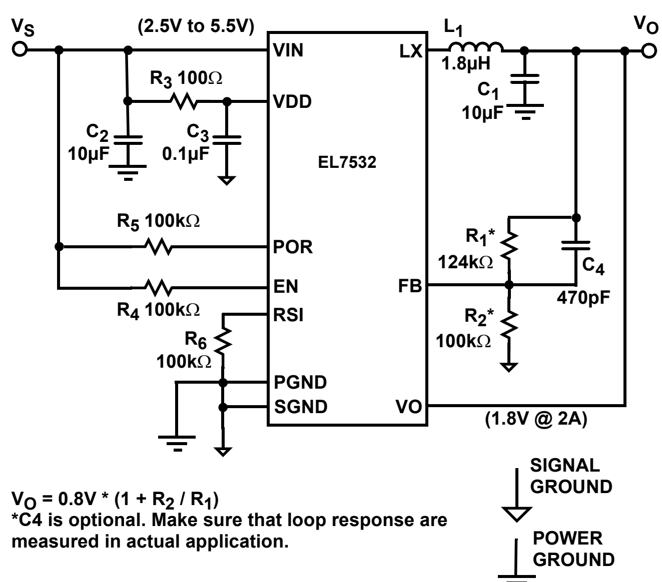
Features

- 2A continuous current (from -40°C to +85°C)
- Less than 0.18 in^2 footprint for the complete 2A converter
- Max height 1.1mm MSOP10
- 1.5MHz (typ.) switching frequency
- 100ms Power-On-Reset output (POR)
- Internally-compensated voltage mode controller
- Up to 94% efficiency
- <1µA shut-down current
- Over-temperature protection
- Pb-free available (RoHS compliant)

Applications

- PDA and pocket PC computers
- Bar code readers
- ADSL modems
- Portable instruments
- Li-Ion battery powered devices
- ASIC/FPGA/DSP supplies
- Set top boxes

Typical Application Schematic



$V_O = 0.8V * (1 + R_2 / R_1)$
*C4 is optional. Make sure that loop response are measured in actual application.

Absolute Maximum Ratings (T_A = +25°C)

V_{IN}, V_{DD}, POR to SGND . . . . -0.3V to +6.5V
LX to PGND . . . . -0.3V to (V_{IN} + +0.3V)
RSI, EN, V_O, FB to SGND . . . . -0.3V to (V_{IN} + +0.3V)
PGND to SGND . . . . -0.3V to +0.3V
Peak Output Current 2.4A
ESD Classification
Human Body Model (Per JESD22-A114-B) . . . . Class 2

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
MSOP10 Package (Note 1)	115

Operating Ambient Temperature . . . . -40°C to +85°C
Storage Temperature . . . . -65°C to +150°C
Junction Temperature . . . . +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_{DD} = V_{IN} = V_{EN}$ = 3.3V, C1 = C2 = 10µF, L = 1.8µH, V_O = 1.8V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{FB}	Feedback Input Voltage		790	800	810	mV
I_{FB}	Feedback Input Current				250	nA
V_{IN}, V_{DD}	Input Voltage		2.5		5.5	V
$V_{IN,OFF}$	Minimum Voltage for Shut-down	V_{IN} falling	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Start-up	V_{IN} rising	2.2		2.4	V
I_{DD}	Supply Current	PWM, $V_{IN} = V_{DD}$ = 5V		400	500	µA
		EN = 0, $V_{IN} = V_{DD}$ = 5V		0.1	1	µA
$R_{DS(ON)-PMOS}$	PMOS FET Resistance	V_{DD} = 5V, wafer test only		52	80	mΩ
$R_{DS(ON)-NMOS}$	NMOS FET Resistance	V_{DD} = 5V, wafer test only		35	65	mΩ
$T_{OT,OFF}$	Over-temperature Threshold (Note 2)	T rising		145		°C
$T_{OT,ON}$	Over-temperature Hysteresis (Note 2)	T falling		130		°C
I_{EN}, I_{RSI}	EN, RSI Current	V_{EN}, V_{RSI} = 0V and 3.3V	-1		1	µA
V_{EN1}, V_{RSI1}	EN, RSI Rising Threshold	V_{DD} = 3.3V			2.4	V
V_{EN2}, V_{RSI2}	EN, RSI Falling Threshold	V_{DD} = 3.3V	0.8			V
V_{POR}	Minimum V_{FB} for POR, WRT Targeted V_{FB} Value	V_{FB} rising			95	%
		V_{FB} falling	86			%
V_{OLPOR}	POR Voltage Drop	I_{SINK} = 5mA		35	70	mV
$V_{LINEREG}$	Line Regulation (Note 2)	V_{IN} = 2.5V to 6V, I_{OUT} = 2A, V_{OUT} = 1.8V		0.1		%/V
$V_{LOADREG}$	Load Regulation (Note 2)	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0 to 2A		0.5		%
AC CHARACTERISTICS						
F_{PWM}	PWM Switching Frequency		1.35	1.5	1.65	MHz
t_{RSI}	Minimum RSI Pulse Width (Note 2)			25	50	ns
t_{SS}	Soft-start Time (Note 2)			650		µs
t_{POR}	Power On Reset Delay Time (Note 2)		80	100	120	ms

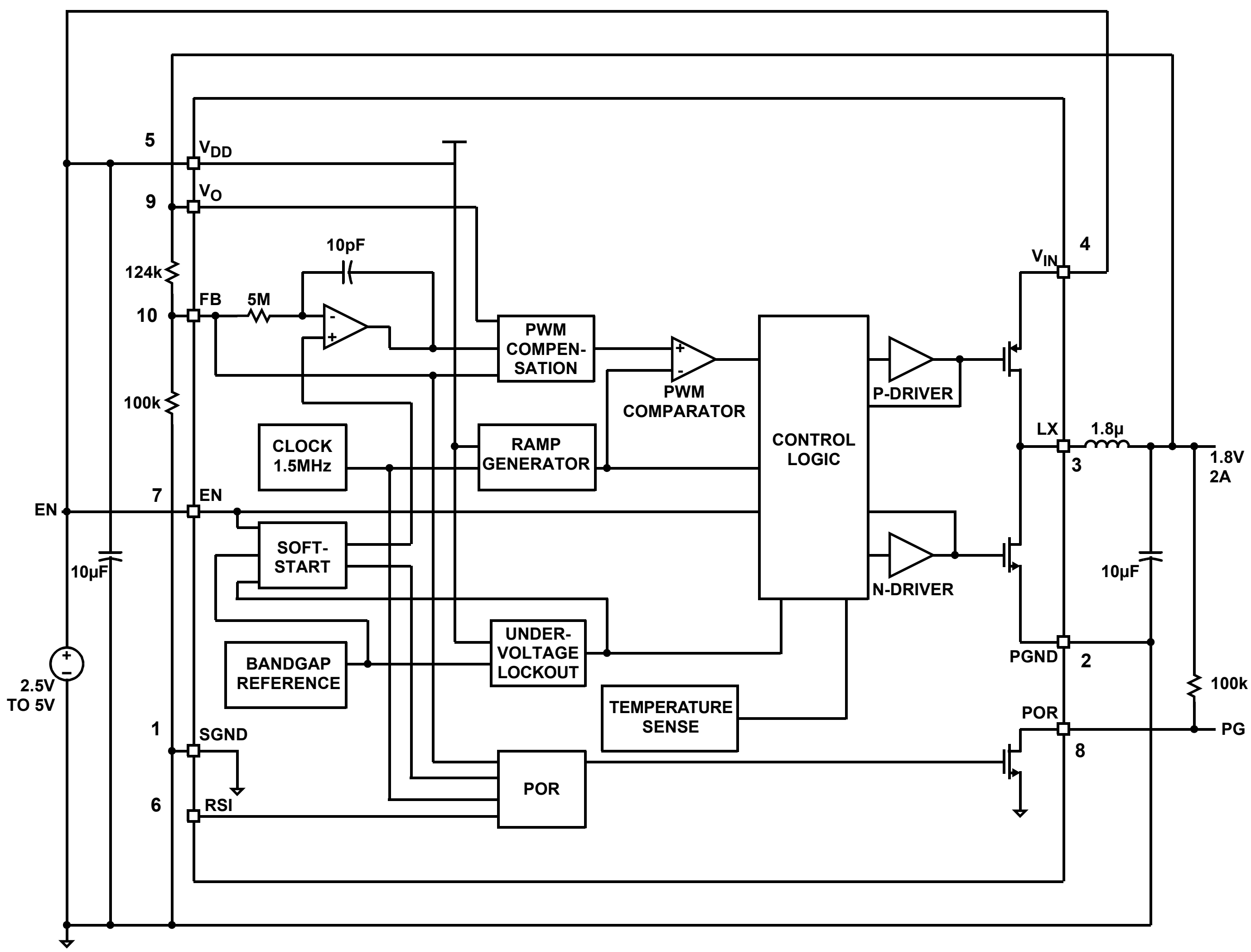
NOTE:

2. Not production tested.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	RSI	Resets POR timer; Connect to ground if not used
7	EN	Enable; Can be connected directly to the VIN for enable
8	POR	Power on reset open drain output; Leave open if not used
9	VO	Output voltage sense pin
10	FB	Voltage feedback input; connected to an external resistor divider between V_O and SGND for variable output

Block Diagram



Typical Performance Curves

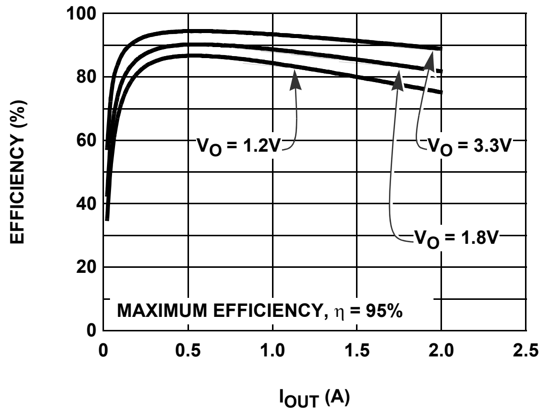


FIGURE 1. EFFICIENCY vs I_{OUT} @ V_{IN} = 5V

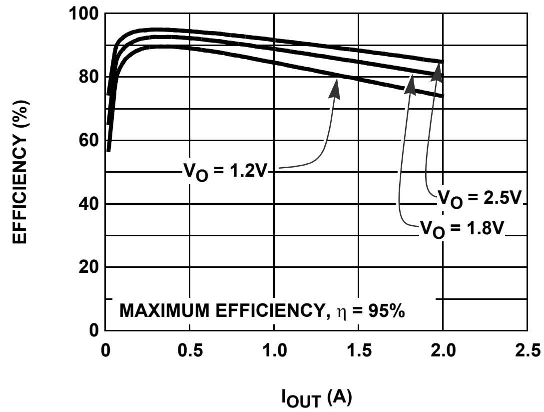


FIGURE 2. EFFICIENCY vs I_{OUT} @ V_{IN} = 3.3V

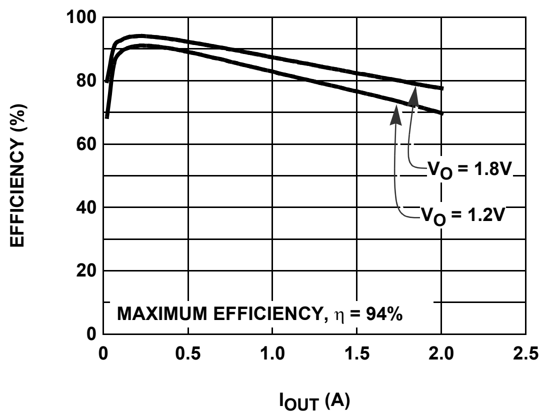


FIGURE 3. EFFICIENCY vs I_{OUT} @ V_{IN} = 2.5V

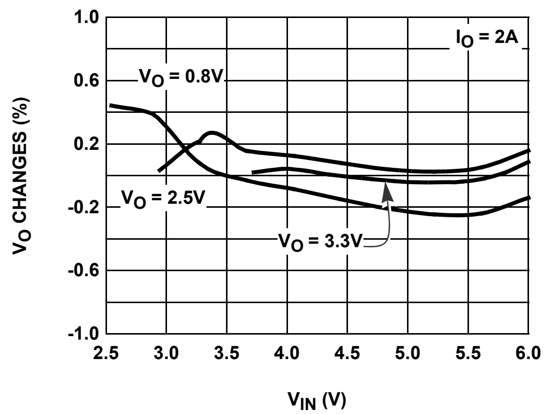


FIGURE 4. LINE REGULATION

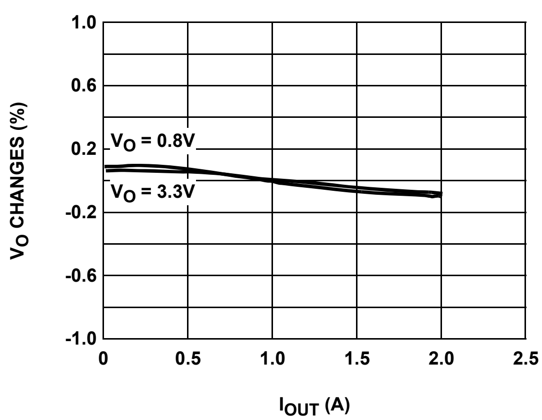


FIGURE 5. LOAD REGULATION @ V_{IN} = 5V

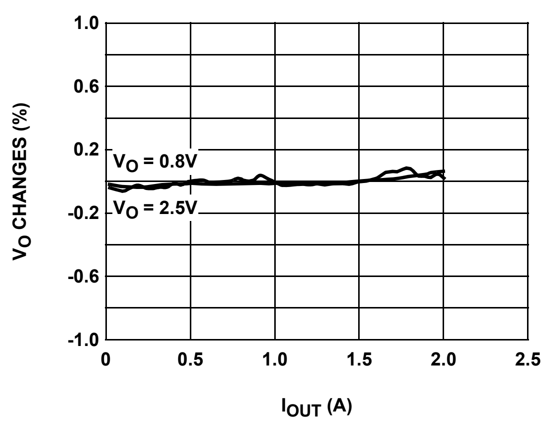


FIGURE 6. LOAD REGULATION @ V_{IN} = 3.3V

Typical Performance Curves (Continued)

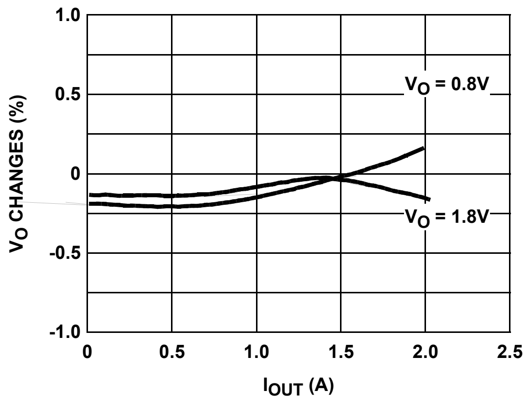


FIGURE 7. LOAD REGULATION @ V_{IN} = 2.5V

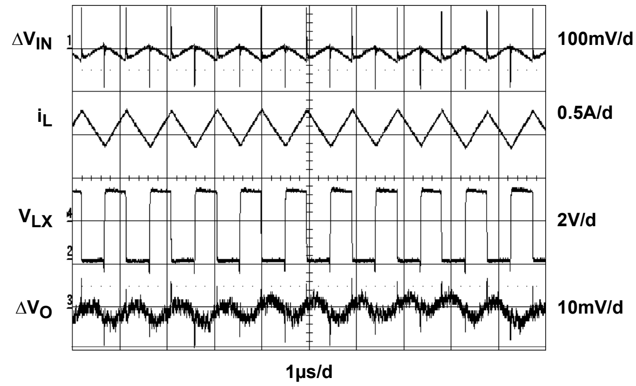


FIGURE 8. LOAD REGULATION @ V_{IN} = 2.5V

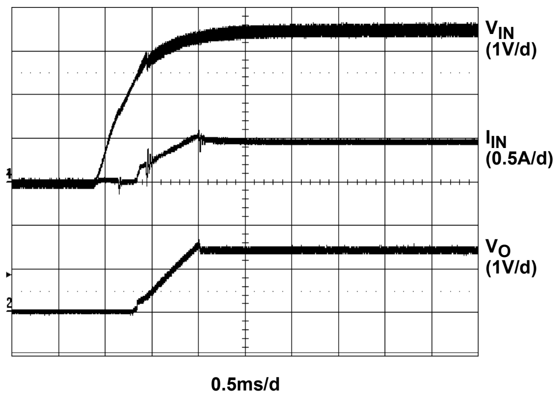


FIGURE 9. START-UP 1

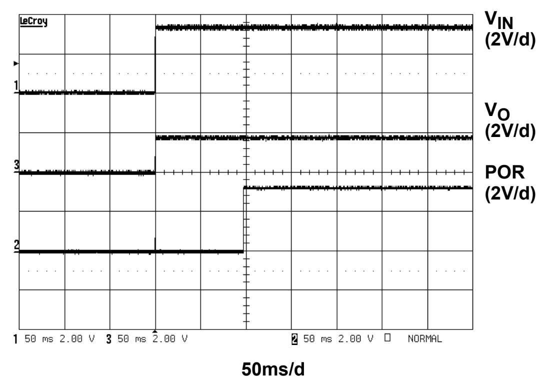


FIGURE 10. START-UP 2

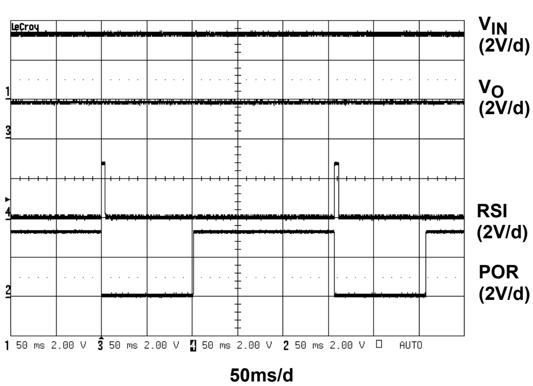


FIGURE 11. POR FUNCTION

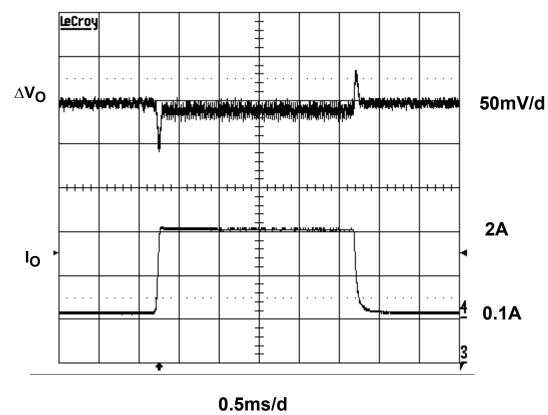


FIGURE 12. TRANSIENT RESPONSE

Applications Information

Product Description

The EL7532 is a synchronous, integrated FET 2A step-down regulator which operates from an input of 2.5V to 5.5V. The output voltage is user-adjustable with a pair of external resistors.

The internally-compensated controller makes it possible to use only two ceramic capacitors and one inductor to form a complete, very small footprint 2A DC/DC converter.

Start-Up and Shut-Down

When the EN pin is tied to V_{IN}, and V_{IN} reaches approximately 2.4V, the regulator begins to switch. The output voltage is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the EL7532 is in the shut-down mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 1µA.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

PWM Operation

In the PWM mode, the P-Channel MOSFET and N-Channel MOSFET always operate complementary. When the PMOSFET is on and the NMOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P-Channel MOSFET is off and the N-Channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to V_O divided by V_{IN}.

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10µF to 22µF ceramic. The inductor is nominally 1.8µH, though 1.5µH to 2.2µH can be used.

100% Duty Ratio Operation

EL7532 utilizes CMOS power FET's as the internal synchronous power switches. The upper switch is a PMOS and lower switch a NMOS. This not only saves a boot capacitor, it also allows 100% turn-on of the upper PFET switch, achieving V_O close to V_{IN}. The maximum achievable V_O is:

$$V_O = V_{IN} - (R_L + r_{DS(ON1)}) \times I_O \quad \text{(EQ. 1)}$$

Where RL is the DC resistance on the inductor and $r_{DS(ON1)}$ the PFET on-resistance, nominal 70mΩ at room temperature with tempco of 0.2mΩ/°C.

As the input voltage drops gradually close or even below the preset V_O, the converter gets into 100% duty ratio. At this condition, the upper PFET needs some minimum turn-off time if it is turned off. This off-time is related to input/output conditions. This makes the duty ratio appear randomly and increases the output ripple somewhat until the 100% duty ratio is reached. A larger output capacitor could reduce the random-looking ripple. Users need to verify if this condition has an adverse effect on the overall circuit if close to 100% duty ratio is expected.

RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for about 100ms after V_O reaches the preset voltage. When the active-HI reset signal RSI is issued, POR goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected. (Please refer to the timing diagram). When the function is not used, connect RSI to ground and leave open the pull-up resister R_4 at POR pin.

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resister R_4 is installed. The RSI pin needs to be directly (or indirectly through a resister R_5) connected to Ground for this to function properly.

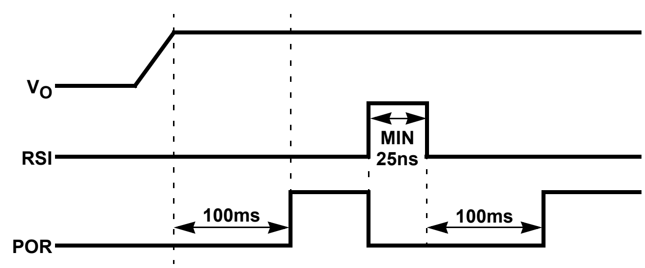


FIGURE 13. RSI AND POR TIMING DIAGRAM

Output Voltage Selection

Users can set the output voltage of the converter with a resister divider, which can be chosen based on Equation 2:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 2)}$$

Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. We recommend 10µF to 22µF multi-layer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and 1.5µH to 2.2µH inductance for the inductor.

At extreme conditions (V_{IN} < 3V, I_O > 0.7A, and junction temperature higher than +75°C), input cap C_1 is recommended to be 22µF. Otherwise, if any of the above 3 conditions is not true, C_1 can remain as low as 10µF.

The RMS current present at the input capacitor is decided by Equation 3:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O \qquad \text{(EQ. 3)}$$

This is about half of the output current I_O for all the V_O. This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S} \qquad \text{(EQ. 4)}$$

- L is the inductance
- f_S the switching frequency (nominally 1.5MHz)

The inductor must be able to handle I_O for the RMS load current, and to assure that the inductor is reliable, it must handle the 3A surge current that can occur during a current limit condition.

In addition to decoupling capacitors and inductor value, it is important to properly size the phase-lead capacitor C_4 (Refer to the Typical Application Diagram). The phase-lead capacitor creates additional phase margin in the control loop by generating a zero and a pole in the transfer function. As a general rule of thumb, C_4 should be sized to start the phase-lead at a frequency of ~2.5kHz. The zero will always appear at lower frequency than the pole and follow Equation 5:

$$f_Z = \frac{1}{2\pi R_2 C_4} \qquad \text{(EQ. 5)}$$

Over a normal range of R_2 (~10k to 100k), C_4 will range from ~470pF to 4700pF. The pole frequency cannot be set once the zero frequency is chosen as it is dictated by the ratio of R_1 and R_2, which is solely determined by the desired output set point. Equation 6 shows the pole frequency relationship:

$$f_P = \frac{1}{2\pi(R_1 || R_2)C_4} \qquad \text{(EQ. 6)}$$

Thermal Shut-Down

Once the junction reaches about +145°C, the regulator shuts down. Both the P-Channel and the N-Channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will soon cool down. Once the junction temperature drops to about +130°C, the regulator will restart again in the same manner as the EN pin connects to logic HI.

Thermal Performance

The EL7532 is in a fused-lead MSOP10 package. Compared to the regular MSOP10 package, the fused-lead package provides lower thermal resistance. The typical θ_{JA} of +115°C/W (See Thermal Information section in spec table) can be improved by maximizing the copper area around the pins. A θ_{JA} of +100°C/W can be achieved on a 4-layer board and +125°C/W on a 2-layer board. Refer to Intersil's Tech Brief, TB379, for more information on thermal resistance.

Layout Considerations

The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

- Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the pins
- Place the input capacitor as close to V_{IN} and PGND pins as possible
- Make the following PC traces as small as possible:
  - from L_X pin to L
  - from C_O to PGND
- If used, connect the trace from the FB pin to R_1 and R_2 as close as possible
- Maximize the copper area around the PGND pin
- Place several via holes under the chip to additional ground plane to improve heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the EL7532 Application Brief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 09, 2015	FN7435.9	Updated the Ordering Information table on page 1. Added Revision History and About Intersil sections.

About Intersil

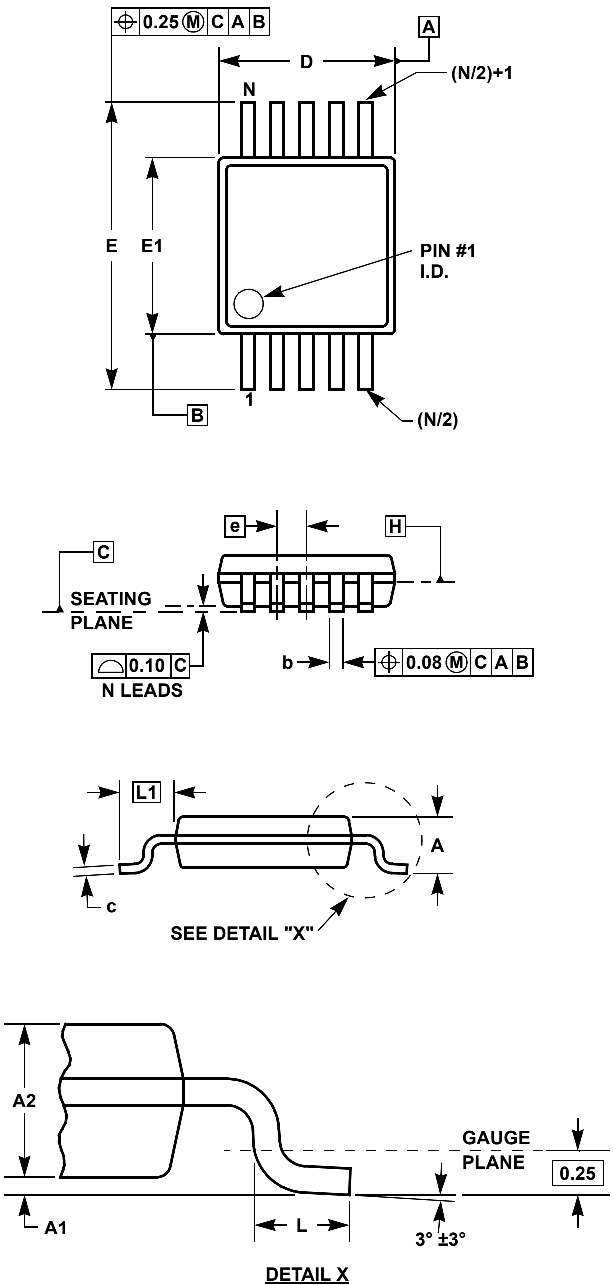
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.