General Description

This document describes the specification for the IDT F1912 Digital Step Attenuator. The F1912 is part of a family of *Glitch-Free™* DSAs optimized for the demanding requirements of Base Station (BTS) radio cards and numerous other non-BTS applications. These devices are offered in a compact 4mm x 4mm 20 pin QFN package with 50Ω impedances for ease of integration.

Competitive Advantage

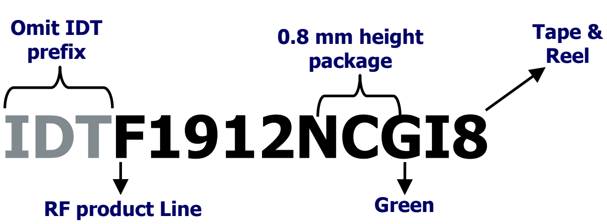
Digital step attenuators are used in receivers and transmitters to provide gain control. The F1912 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (> +60 dBm IIP3). The device has pinpoint accuracy. Most importantly, the F1912 includes IDT's *Glitch-Free™* technology, which results in low overshoot and ringing during MSB transitions.

- ✓ *Glitch-Free™* technology so PA or ADC will not be damaged during when transitions.
- ✓ Extremely accurate with low distortion.
- ✓ Lowest insertion loss for best SNR

Applications

- Base Station 2G, 3G, 4G, TDD radio cards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID Handheld and Portable Readers
- Cable Infrastructure

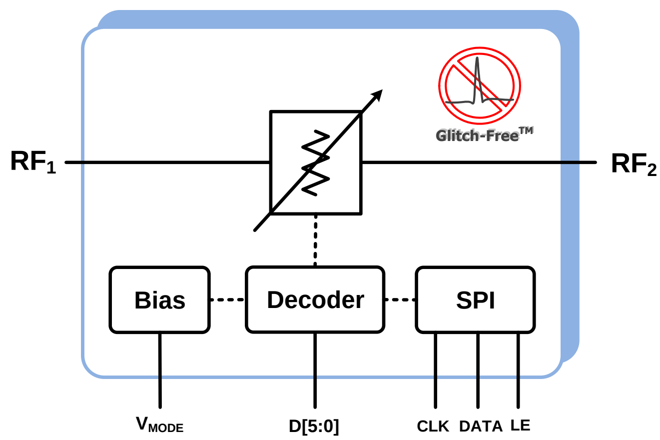
Ordering Information



Features

- Serial and 6 bit Parallel Interface
- 31.5 dB Control Range
- 0.5 dB step
- *Glitch-Free™*, low transient overshoot
- 3.0 V to 5.25 V supply
- 1.8 V or 3.3 V control logic
- Attenuation Error < 0.20 dB @ 2 GHz
- Low Insertion Loss < 1.4 dB @ 2 GHz
- Ultra Linear IIP3 > +60 dBm
- IIP2 = +110 dBm typical
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 550 µA typical
- -40 °C to +105 °C operating temperature
- 4mm x 4mm Thin QFN 20 pin package

Functional Block Diagram



Part# Details

Part#	Freq Range (MHz)	Resolution / Range (dB)	Control	IL (dB)	Pinout
F1950	150 - 4000	0.25 / 31.75	Parallel & Serial	1.3	PE43702 PE43701
F1951	100 - 4000	0.50 / 31.5	Serial Only	1.2	HMC305
F1952	100 – 4000	0.50 / 15.5	Serial Only	0.9	HMC305
F1953	400 – 4000	0.50 / 31.5	Parallel & Serial	1.3	PE4302 DAT-31R5
F1956	1 - 4000	0.25 / 31.75	Parallel & Serial	1.4	PE43705, RFSA3715
F1912	**1 – 4000**	**0.50 / 31.5**	**Parallel & Serial**	**1.4**	**PE4312 PE4302**

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
V_{DD} to GND	V_{DD}	-0.3	+5.5	V
DATA, LE, CLK, D[5:0]	V_{Logic}	-0.3	Lower of (V_{DD}+0.3, 3.9)	V
RF1, RF2	V_{RF}	-0.3	+0.3	V
Maximum Input Power applied to RF1 or RF2 (>100 MHz)	P_{RF}		+34	dBm
Operating Case Temperature			+105	°C
Maximum Junction Temperature	T_{Jmax}		+140	°C
Junction Temperature	T_{jmax}		140	°C
Continuous Power Dissipation			1.5	W
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	Volts
ESD Voltage – CDM (Per JESD22-C101F)	V_{ESDCDM}		500 (Class C2)	Volts

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	50 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	3 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1912 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{DD}		3		5.25	V
Frequency Range	F_{RF}		1		4000	MHz
Operating Temperature Range	T_{CASE}	Exposed Paddle	-40		105	°C
RF CW Input Power	PCW	RF1 or RF2			See Figure 1	dBm
Source Impedance	Z_{Source}	Single Ended		50		Ω
Load Impedance	Z_{Load}	Single Ended		50		Ω

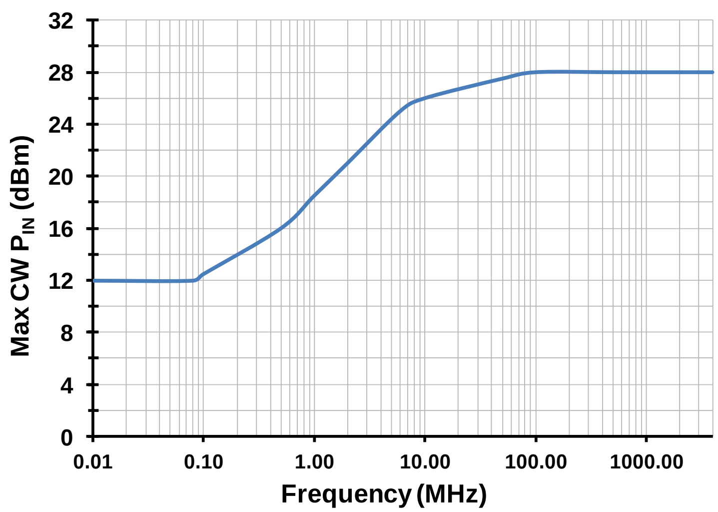


Figure 1 Maximum Continuous Operating RF input power versus Input Frequency

F1912 Specification

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25 °C, F_{RF} = 2000 MHz, P_{IN} = 0 dBm, Serial Mode (V_{MODE} > V_{IH}), Z_{source} = Z_{Load} = 50 Ω unless otherwise noted. EVKit losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High [5]	V_{IH}	All Control Pins				
		V_{DD} > 3.9 V	***1.17***[1]		***3.6***	V
		3.0 ≤ V_{DD} ≤ 3.9 V	***1.17***		Lower of (V_{DD}+0.3, 3.6)	V
Logic Input Low [5]	V_{IL}	All Control Pins			***0.63***	V
Logic Current	I_{IH}, I_{IL}	All Control Pins	***-35***		***+35***	µA
Supply Current	I_{DD}	V_{DD} = 3.3 V		550	***830***	µA
		V_{DD} = 5.0 V		620	***900***	
RF1 Return Loss	S_{11}			18		dB
RF2 Return Loss	S_{22}			18		dB
Attenuation Step	LSB	Least Significant Bit		0.5		dB
Insertion Loss (Minimum Attenuation)	A_{MIN}	D[5:0]=[000000] (IL State)		1.4	***2.0***	dB
Insertion Loss (Maximum Attenuation)	A_{MAX}	D[5:0]=[111111]=31.5 dB	32[2]	33.0		dB
Step Error	DNL			0.10		dB
Absolute Error	INL	D[5:0]=[100111]= 19.5 dB	***-0.7***		***+0.5***	dB
Relative Phase (max to min attenuation)	Φ_{Δ}	At 2 GHz		27		Deg
		At 4 GHz		55		
Input IP3	IIP3	P_{IN} = +10 dBm/tone, Tone Spacing = 50 MHz				
		Attn = 0.0 dB, RF_{in} = RF1	60	64.0		dBm
		Attn = 0.0 dB, RF_{in} = RF2	56	60.5		
		Attn =15.5 dB, RF_{in} = RF1	56	61.0		
		Attn =15.5 dB, RF_{in} = RF2	57	61.5		
	IIP3	Attn = 0.00 dB, RF_{in} = RF1 P_{IN} = +22 dBm per tone 1 MHz Tone Separation				
		F_{RF} = 0.7 GHz	60	62.5		dBm
		F_{RF} = 1.8 GHz	58	61.5		
		F_{RF} = 2.2 GHz	58	61.0		
		F_{RF} = 2.6 GHz	57	60.5		
Input IP2	IIP2	P_{IN} = +12dBm/tone, V_{DD}=5.0V F1=945 MHz, F2= 949 MHz F1+F2 = 1894 MHz RF_{IN}= RF1		110		dBm
0.1dB Compression[3]	$P_{0.1}$	D[5:0] = [000000] = 0 dB		31		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
Note 5: The power supply voltage must be applied before all other voltages. See Applications Information.

F1912 SPECIFICATION (CONTINUED)

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25 °C, F_{RF} = 2000 MHz, P_{IN} = 0 dBm, Serial Mode (V_{MODE} > V_{IH}), Z_{source} = Z_{Load} = 50 Ω unless otherwise noted. EVKit losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MSB Step Time	t_{LSB}	LE rising edge to within ±0.10 dB Pout settling for 15.5 dB to 16.0 dB transition		500		ns
Maximum spurious level on any RF port[4]	$Spur_{MAX}$			-140		dBm
Maximum Switching Frequency	SW_{FREQ}			25		kHz
DSA Settling time	τ_{SET}	Max to Min Attenuation to settle to within 0.5 dB of final value		0.9		µs
		Min to Max Attenuation to settle to within 0.5 dB of final value		1.8		
Control Interface	SPI_{BIT}			6		bit
Serial Clock Speed	SPI_{CLK}				***25***	MHz

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
Note 5: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).

PROGRAMMING OPTIONS

F1912 can be programmed using either the parallel or serial interface, which is selectable via V_{MODE} (pin 13). Serial mode is selected by floating V_{MODE} or pulling it to a voltage logic high (greater than V_{IH}) and parallel mode is selected by setting V_{MODE} to logic low (less than V_{IL}).

SERIAL CONTROL MODE

F1912 Serial mode is selected by floating V_{MODE} (pin 13) or pulling it to a voltage > V_{IH}. The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (1, 15, 16, 17, 19, 20) **must** be grounded.

Table 1 - 6 Bit SPI Word Sequence

D5	Attenuation 16 dB Control Bit
D4	Attenuator 8 dB Control Bit
D3	Attenuator 4 dB Control Bit
D2	Attenuator 2 dB Control Bit
D1	Attenuator 1 dB Control Bit
D0	Attenuator 0.5 dB Control Bit

Table 2 - Truth Table for Serial Control Word

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

SERIAL MODE REGISTER TIMING DIAGRAM: (Note The Timing Spec Intervals In Blue)

With serial control, the F1912 can be programmed via the serial port on the rising edge of Latch Enable (LE), which loads the last 6 DATA line bits [formatted MSB (D5) first] resident in the SHIFT register followed by the next 5 bits.

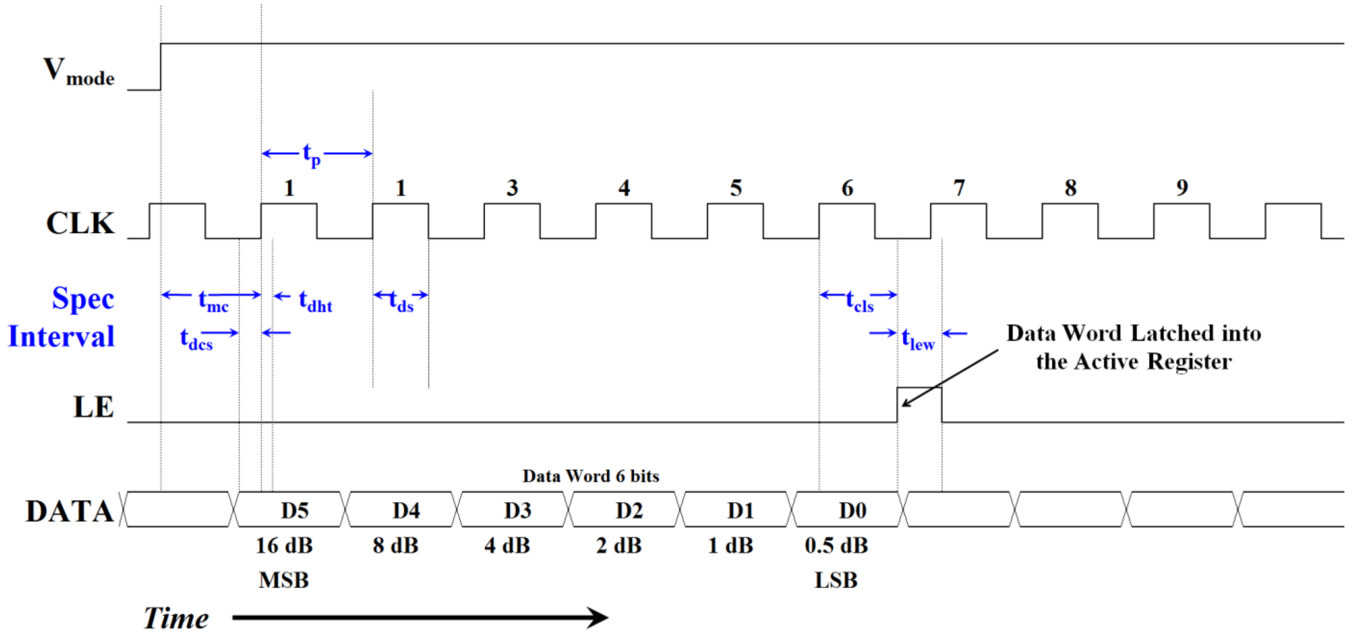


Figure 2 - Serial Register Timing Diagram

Note *- When Latch enable is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch enable be left high when the device is not being programmed.*

Table 3 - Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{mc}	Parallel to Serial Setup Time - From rising edge of V_{MODE} to rising edge of CLK for D5	***100***		ns
t_{ds}	Clock high pulse width	***10***		ns
t_{cls}	LE Setup Time - From the rising edge of CLK pulse for D0 to LE rising edge minus half the clock period.	***10***		ns
t_{lew}	LE pulse width	***30***		ns
t_{dsc}	Data Setup Time - From the starting edge of Data bit to rising edge of CLK	***10***		ns
t_{dht}	Data Hold Time - From rising edge of CLK to falling edge of the Data bit.	***10***		ns

Serial Mode Default Startup Condition:

When the device is first powered up it will default to the Maximum Attenuation of 31.5 dB independent of the V_{MODE} and parallel pin [D5:D0] conditions.

Table 4 - Default Control Word for the Serial Mode

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
1	1	1	1	1	1	31.5

PARALLEL CONTROL MODE

For the F1912 the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode:

Direct Parallel Mode is selected when V_{MODE} (pin 13) is less than V_{IL} and LE (pin 5) is greater than V_{IH}. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 15, 16, 17, 19, 20]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode:

Latched Parallel Mode is selected when V_{MODE} is less than V_{IL} and LE (pin 5) is toggled from less than V_{IL} to greater than V_{IH}. To utilize Latched Parallel Mode:

- Set LE < V_{IL}
- Adjust pins [pins 1, 15, 16, 17, 19, 20] to the desired attenuation setting. (Note the device will not react to these pins while LE < V_{IL}.)
- Pull LE > V_{IH}. The device will then transition to the attenuation settings reflected by pins D5 – D0.

Latched Parallel Mode implies a default state for when the device is first powered up with VMODE < V_{IL} and LE < V_{IL}. In this case the default setting is MAXIMUM Attenuation.

Table 5 - Truth Table for the Parallel Control Word

D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

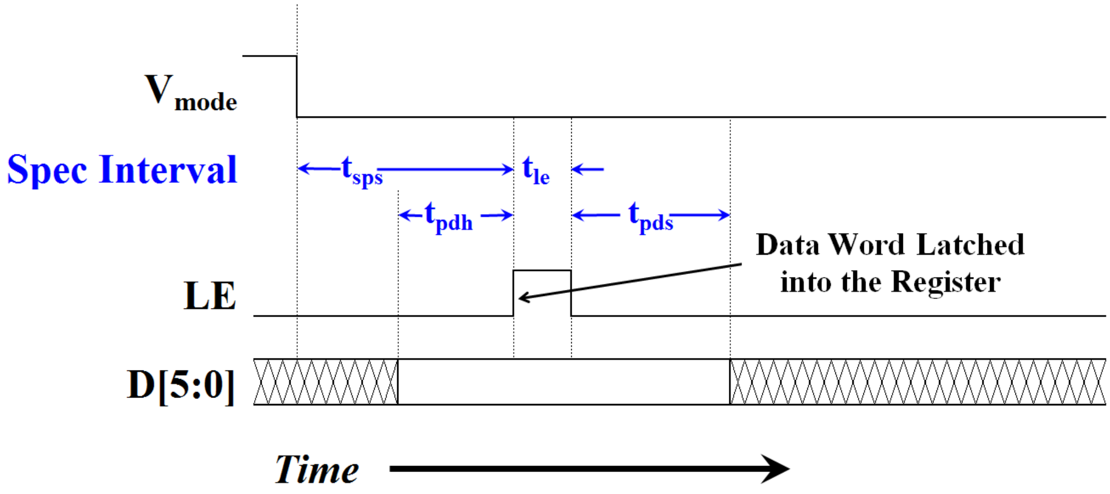


Figure 3 - Latched Parallel Mode Timing Diagram

Table 6 - Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{sps}	Serial to Parallel Mode Setup Time	100		ns
t_{pdh}	Parallel Data Hold Time	10		ns
t_{pds}	LE minimum pulse width	10		ns
t_{le}	Parallel Data Setup Time	10		ns

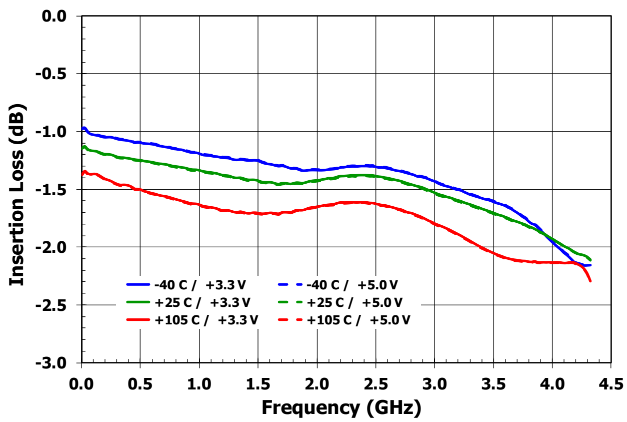
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

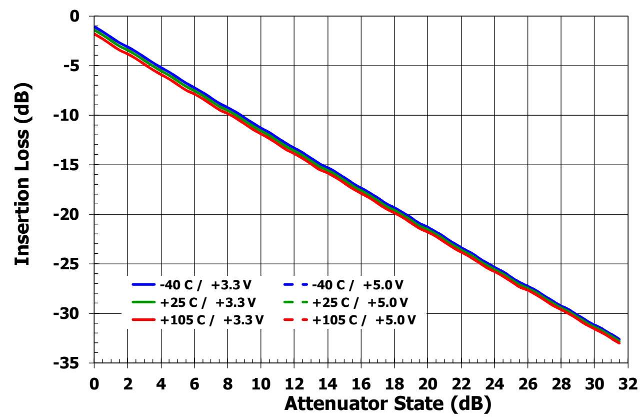
- **V_{DD} = +3.30 V**
- **T_{CASE} = +25 °C**
- **F_{RF} = 2 GHz**
- **P_{IN} = 0 dBm for single tone measurements**
- **P_{IN} = +10 dBm/tone for multi-tone measurements**
- **Tone Spacing = 50 MHz**
- **EVKit connector and board losses are de-embedded**

TYPICAL OPERATING CONDITIONS (- 1 -)

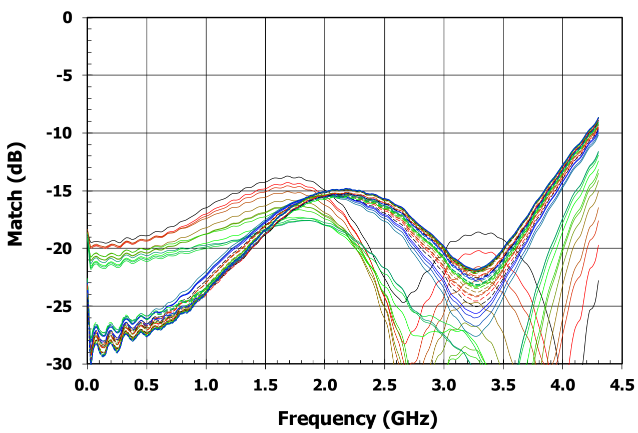
Insertion Loss vs Frequency



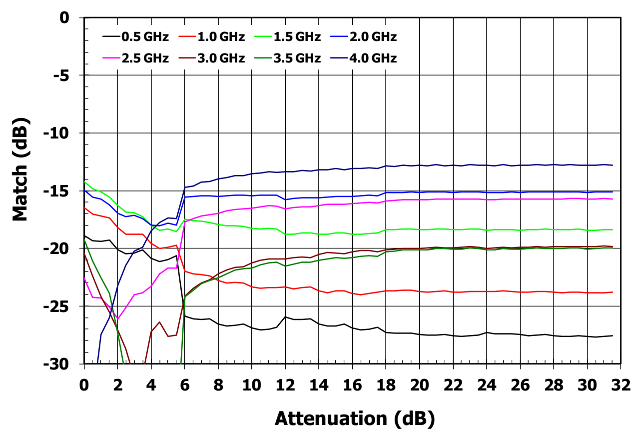
Insertion Loss vs Attenuation State



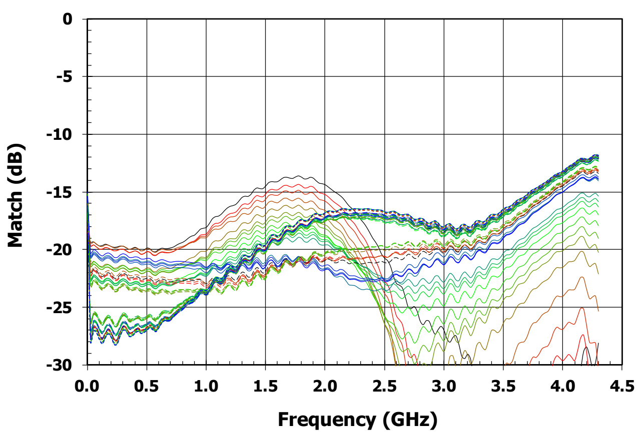
RF1 (Input) Return Loss vs Frequency [All States]



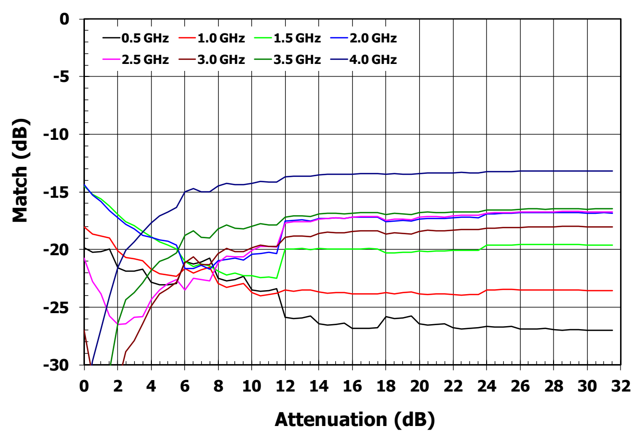
RF1 (Input) Return Loss vs Attenuation State



RF2 (Output) Return Loss vs Frequency [All States]

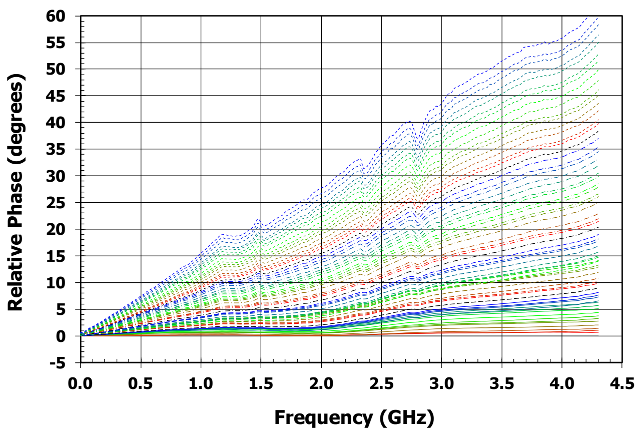


RF2 (Output) Return Loss vs Attenuation State

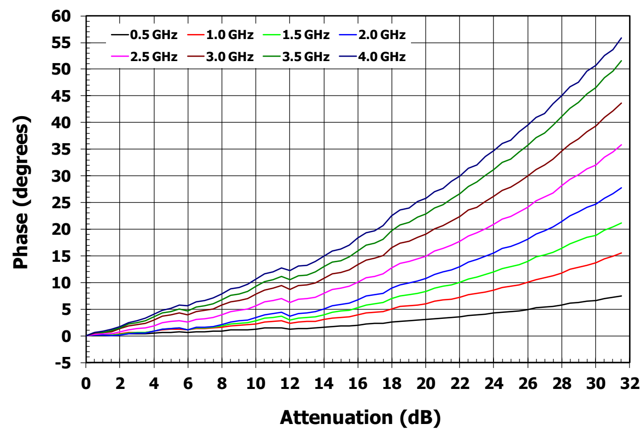


TYPICAL OPERATING CONDITIONS (- 2 -)

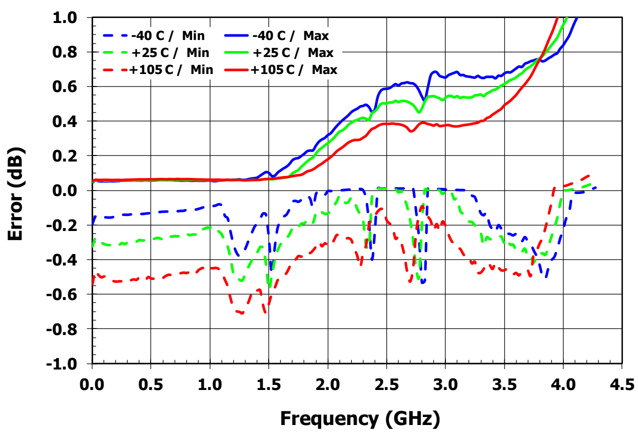
Relative Insertion Phase vs Frequency



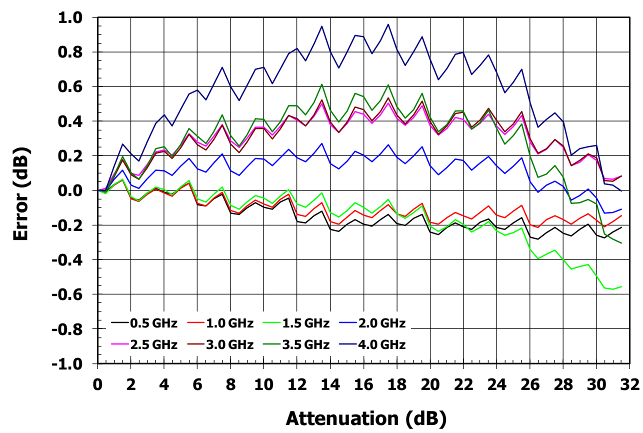
Relative Insertion Phase vs Attenuation



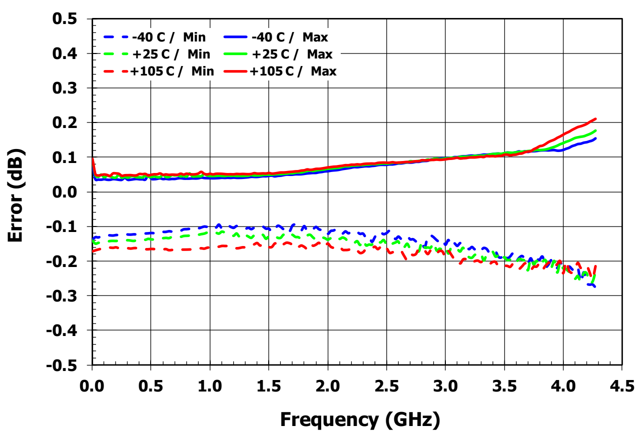
Worst Case Absolute Accuracy vs Frequency



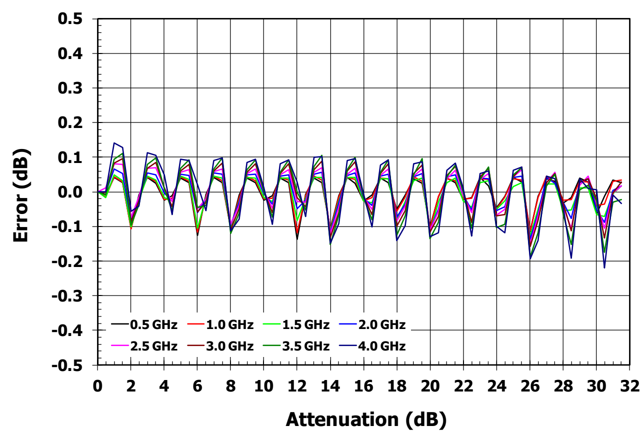
Absolute Accuracy vs Attenuation



Worst Case Step Accuracy vs Frequency

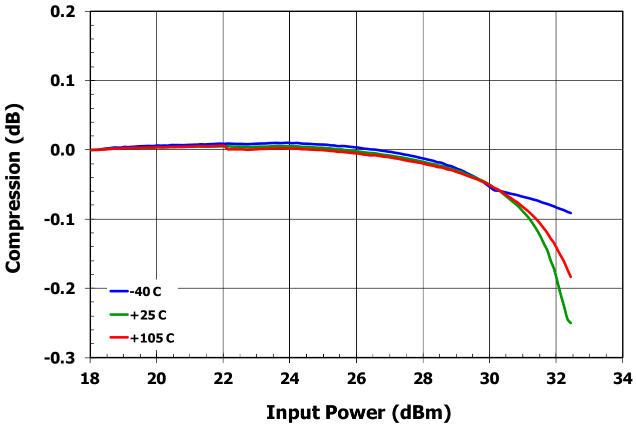


Step Accuracy vs Attenuation

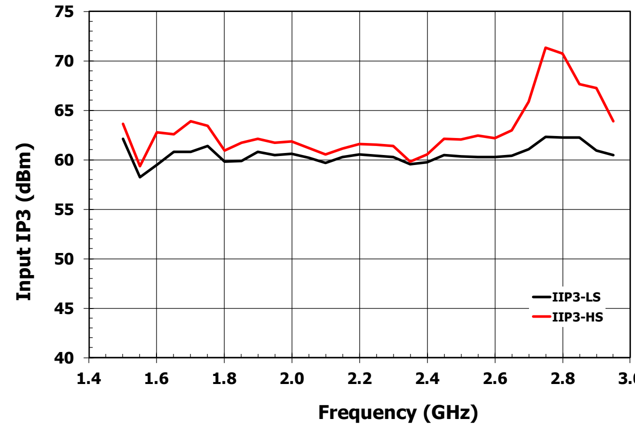


TYPICAL OPERATING CONDITIONS (- 3 -)

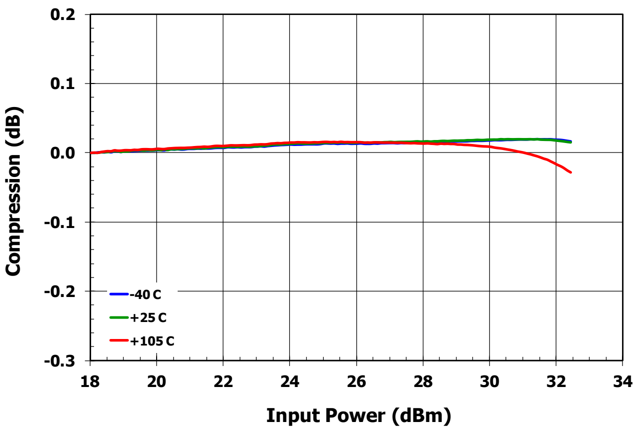
Compression at 0 dB and 2 GHz



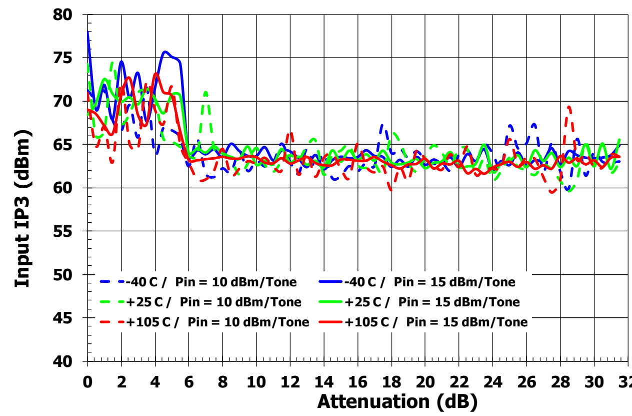
Input IP3 - 0 dB, +22 dBm, 1 MHz Tone Delta, RF1



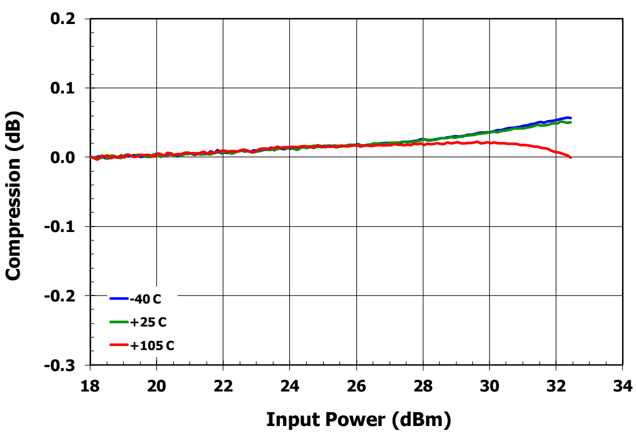
Compression at 15.5 dB and 2 GHz



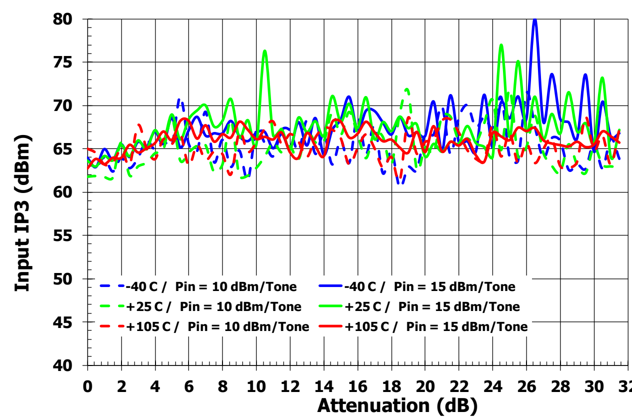
Input IP3 (Low Side) vs attenuation at 2GHz



Compression at 31.5 dB and 2 GHz

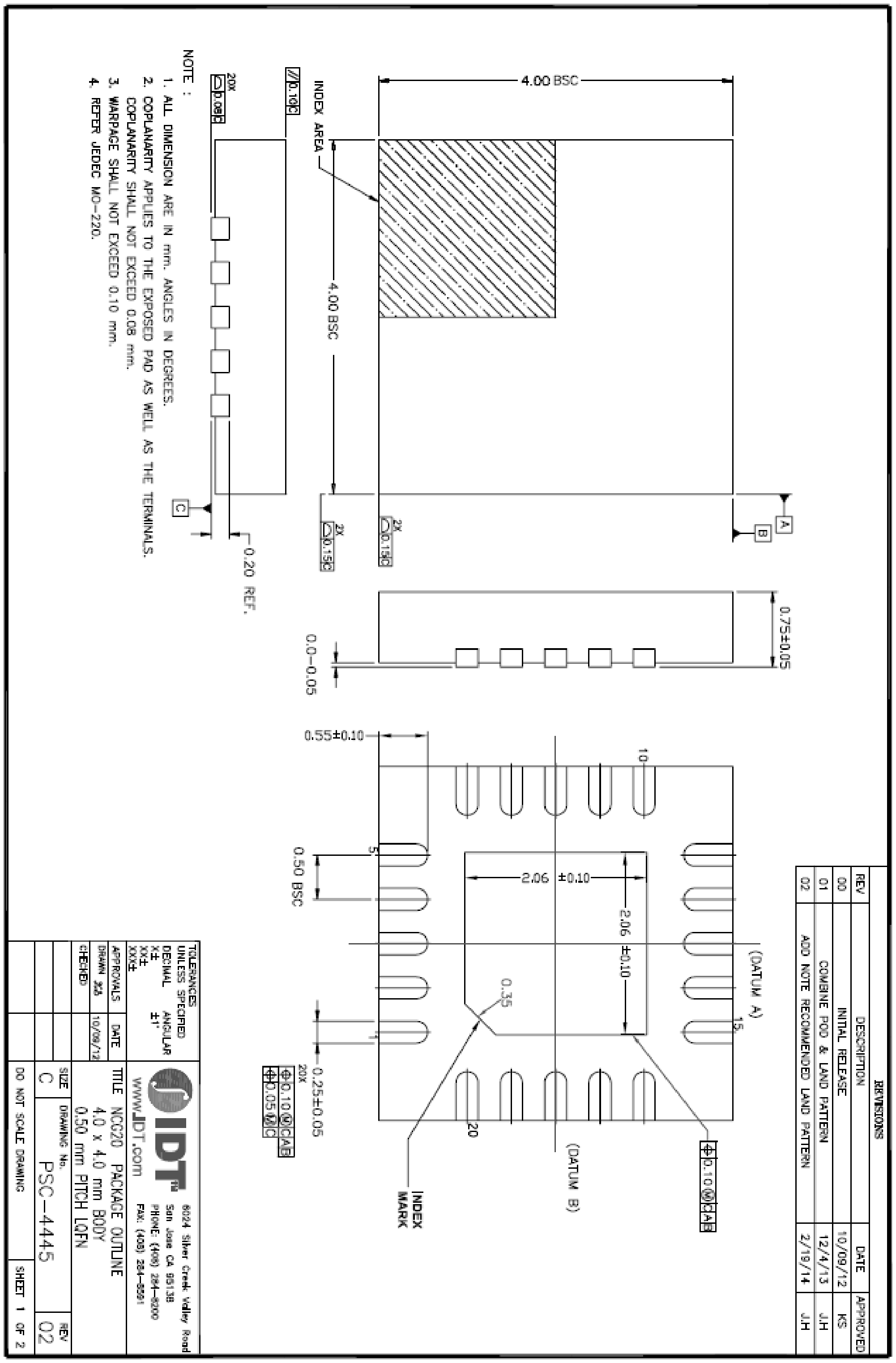


Input IP3 (High Side) vs attenuation at 2GHz

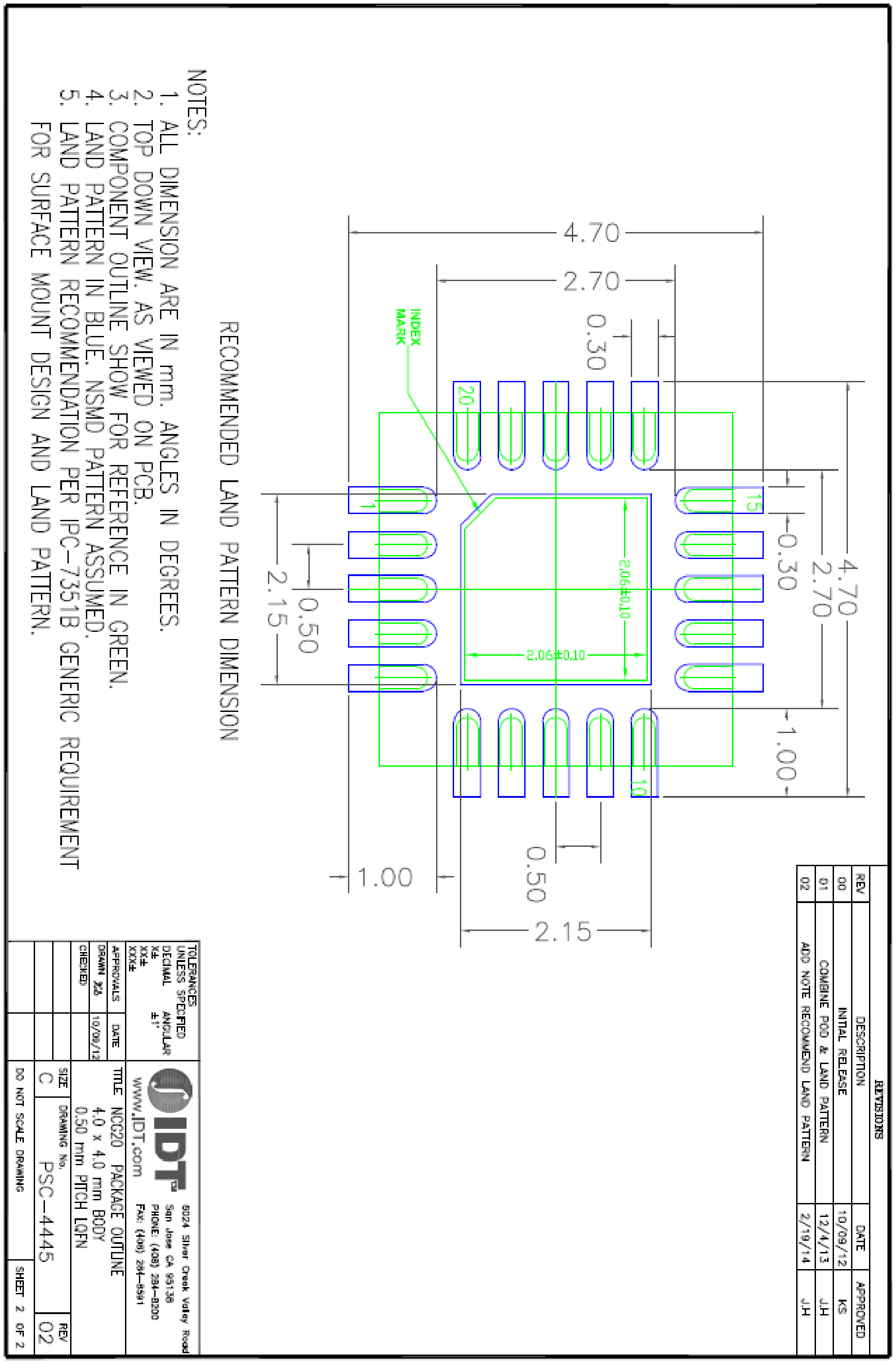


PACKAGE DRAWING

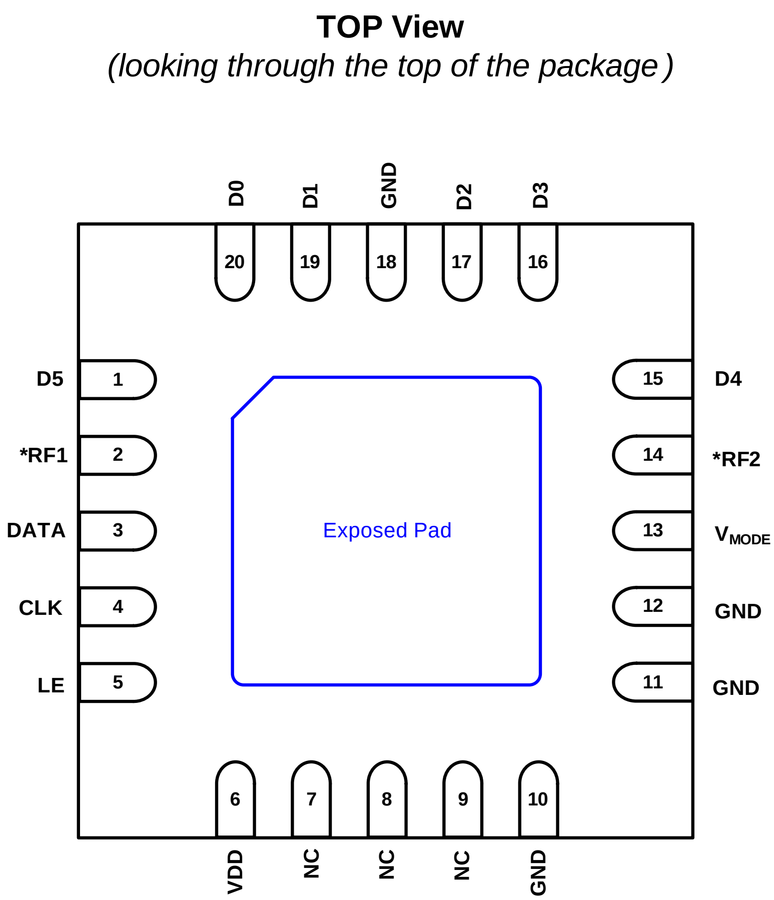
(4 mm x 4 mm 20-pin TQFN), **NCG20**



LAND PATTERN DIMENSION



PIN DIAGRAM

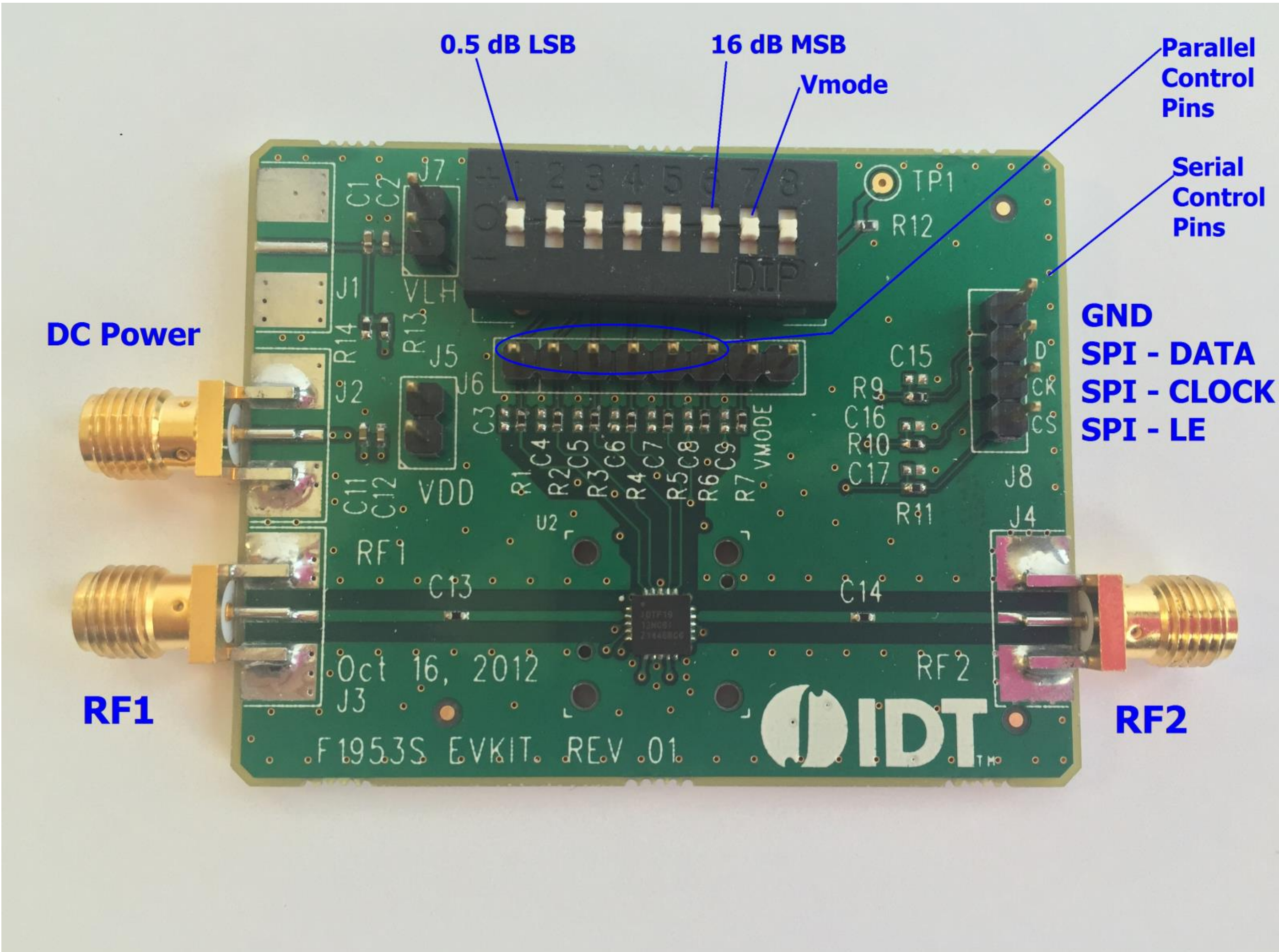


* Device is RF Bi-Directional

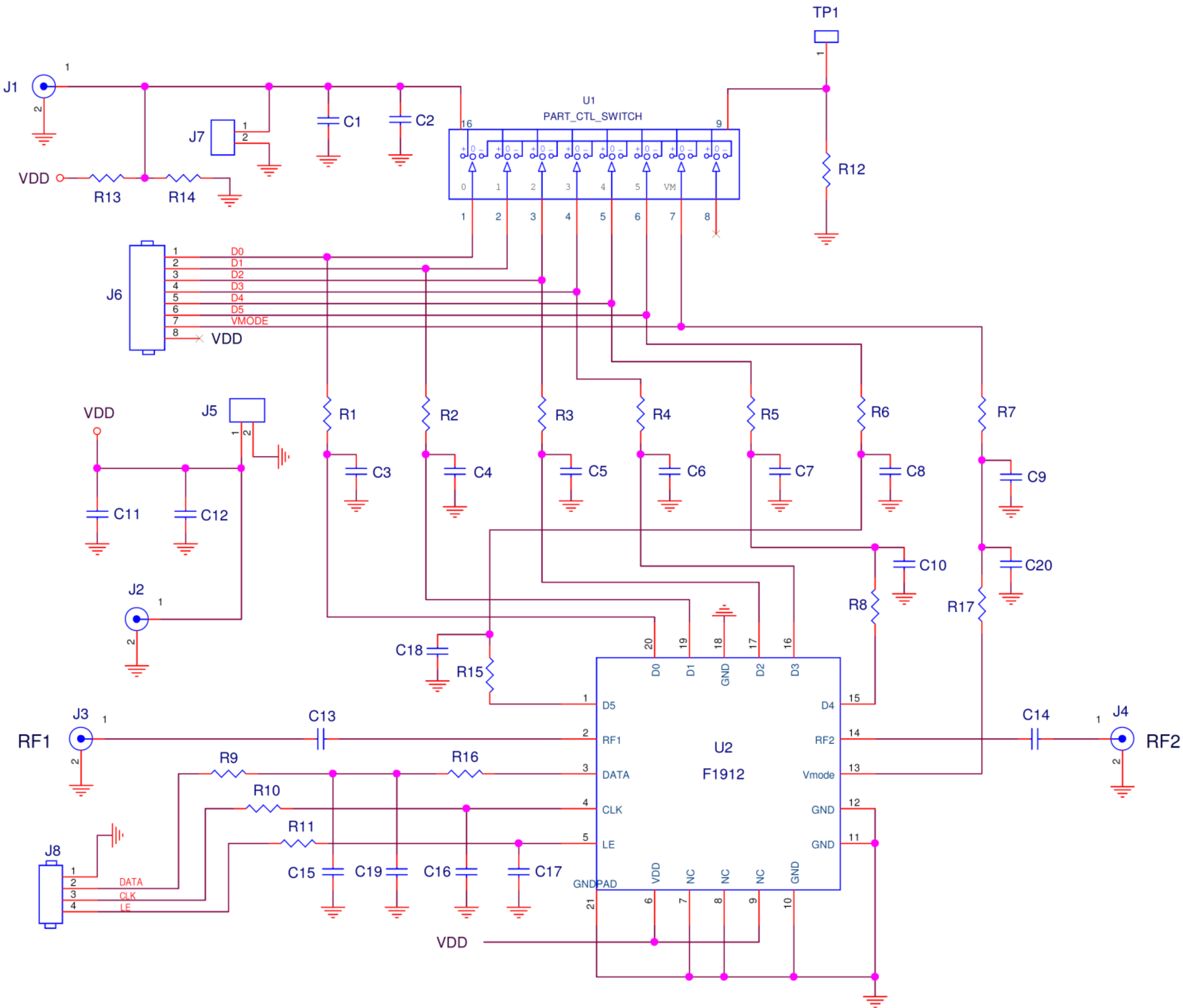
PIN DESCRIPTION

PIN	NAME	FUNCTION
1	D5	16 dB Attenuation Control Bit. Pull high for 16 dB ATTN.
2	RF1	Device RF input or output (bi-directional). Internally DC blocked.
3	DATA	Serial interface Data Input.
4	CLK	Serial interface Clock Input.
5	LE	Serial interface Latch Enable Input. Internal pullup (100K ohm).
6	VDD	Power supply pin.
7	NC	Internally unconnected.
8	NC	Internally unconnected.
9	NC	Internally unconnected.
10	GND	Connect to Ground. This pin is internally connected to the exposed paddle.
11	GND	Connect to Ground. This pin is internally connected to the exposed paddle.
12	GND	Connect to Ground. This pin is internally unconnected.
13	VMODE	Pull high for serial control mode. Ground for parallel control mode.
14	RF2	Device RF input or output (bi-directional). Internally DC blocked.
15	D4	8 dB Attenuation Control Bit. Pull high for 8 dB ATTN.
16	D3	4 dB Attenuation Control Bit. Pull high for 4 dB ATTN.
17	D2	2 dB Attenuation Control Bit. Pull high for 2 dB ATTN.
18	GND	Connect to Ground. This pin is internally unconnected.
19	D1	1 dB Attenuation Control Bit. Pull high for 1 dB ATTN.
20	D0	0.5 dB Attenuation Control Bit. Pull high for 0.5 dB ATTN.
EPAD	Exposed Paddle	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.

EVKIT PICTURE



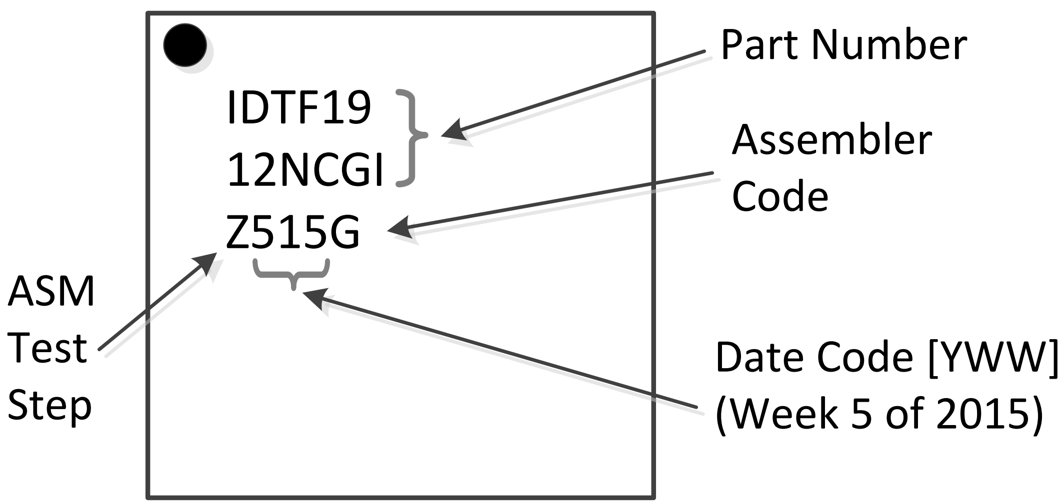
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1, C11	2	100nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H104K	MURATA
2	C2, C12	2	10nF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM155R71H103J	MURATA
3	R12, C13, C14	3	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
4	R1-R7	7	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
5	R9, R10, R11	3	3kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
6	R8, R15, R16, R17	4	10kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
7	R13	1	100KΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	PANASONIC
8	R14	1	267KΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2673X	PANASONIC
9	J5, J7	2	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
10	J8	1	CONN HEADER VERT SGL 4 X 1 POS GOLD	961104-6404-AR	3M
11	J6	1	CONN HEADER VERT SGL 8 X 1 POS GOLD	961108-6404-AR	3M
12	J2, J3, J4	3	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
13	U1	1	SWITCH 8 POSITION DIP SWITCH	KAT1108E	E-Switch
14	U2	1	DSA	F1912Z	IDT
15		1	Printed Circuit Board (Rev 01)	F1953S EVKit Rev 01	IDT
16			Bill Of Material (Rev 01)		

TOP MARKINGS



APPLICATIONS INFORMATION

F1912 Digital Pin Voltage & Resistance Values (pins not connected)

The following table lists the resistance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC these same pins should have the measured voltage to ground.

Pin	Name	DC voltage (volts)	Resistance (ohms)
13	V_{MODE}	2.5V	100 kΩ pullup resistor to internally regulated 2.5 V
3, 4, 5	DATA, CLK, LE	2.5V	100 kΩ pullup resistor to internally regulated 2.5 V

Logic Voltage applied before Power Supply

Due to on-chip ESD protection circuitry, the V_{DD} supply voltage is required to be present before the logic voltages can be applied to the logic pins (V_{MODE}, DATA, LE, CLK, D[5:0]). If in the application this is not possible, then a series resistor of 3kΩ needs to be added in line with each of the logic pins, D0-D3. The other logic pins (V_{MODE}, DATA, LE, CLK, D4, D5) already have a significant resistor value per the Bill Of Material (BOM). This resistor limits the current into the logic pin to a safe level when V_{DD} is not present. The resistor should be placed close to the device to minimize the impact on switching speed due to stray PCB parasitics.

Revision History

Revision	Revision Date	Description of Change
2	2017-July-10	Corrected logic voltages in absolute maximum rating table (Page 2) and operating condition table (Page 4). Added paragraph in Application Information (page 21) with respect to the logic and power supply voltages.
1	2017-May-26	Corrected pin label on Page 16.
O	2015-June-06	Initial release of the datasheet.

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