# IDTF2258NLGK Datasheet

*Voltage Variable RF Attenuator* *50 to 6000 MHz*

## General Description

The F2258 is a low insertion loss **V**oltage **V**ariable RF **A**ttenuator (VVA) designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50 MHz to 6000 MHz. In addition to providing low insertion loss, the F2258 provides excellent linearity performance over its entire voltage control and attenuation range.

The F2258 uses a single positive supply voltage of 3.15 V to 5.25 V. Another feature includes multi-directional operation meaning the RF input can be applied to either RF1 or RF2 pins. Control voltage ranges from 0 V to 3.6 V.

## Competitive Advantage

F2258 provides extremely low insertion loss and superb IP3, IP2, Return Loss and Slope Linearity across the control range. Comparing to the previous state-of-the-art for silicon VVAs this device is better as follows:

- ✓ Insertion Loss:
  @ 2000 MHz: 1.4 dB vs. 2.8 dB
  @ 6000 MHz: 2.7 dB vs. 7.0 dB
- ✓ Maximum Attenuation Slope:
  33 dB/Volt vs. 53 dB/Volt
- ✓ Minimum Return Loss up to 6000 MHz:
  12.5 dB vs. 7 dB
- ✓ Minimum Output IP3:
  31 dBm vs. 15 dBm
- ✓ Minimum Input IP2:
  87 dBm vs. 80 dBm
- ✓ Maximum Operating Temperature:
  +105 °C vs. +85 °C

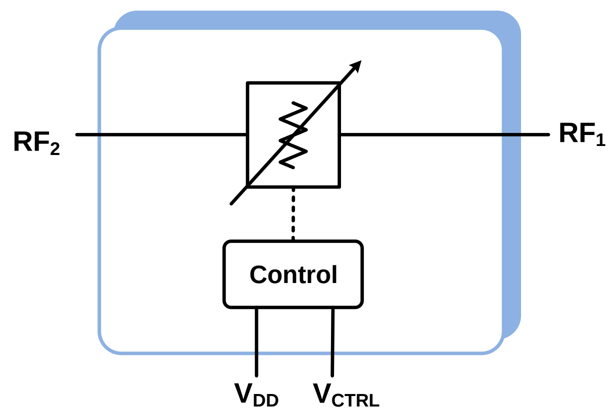
## Applications

- Base Station 2G, 3G, 4G,
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- Satellite Receivers and Modems
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

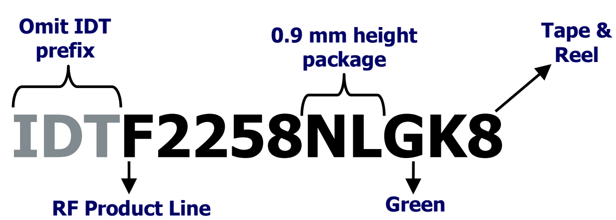
## Features

- Low Insertion Loss: 1.4 dB @ 2000 MHz
- Typical / Min IIP3: 65 dBm / 47 dBm
- Typical / Min IIP2: 95 dBm / 87 dBm
- 33.6 dB Attenuation Range
- Bi-directional RF ports
- +34.4 dBm Input P1dB compression
- Linear-in-dB attenuation characteristic
- Supply voltage: 3.15 V to 5.25 V
- $V_{CTRL}$ range: 0 V to 3.6 V using 5 V supply
- +105 °C max operating temperature
- 3 mm x 3 mm, 16-pin QFN package

## Functional Block Diagram




## Ordering Information



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ to GND | $V_{DD}$ | -0.3 | +5.5 | V |
| $V_{CTRL}$ to GND (with 0 V ≤ $V_{DD}$ ≤ 5.25 V) | $V_{CTRL}$ | -0.3 | Minimum ($V_{DD}$, +4.0) | V |
| RF1, RF2 to GND | $V_{RF}$ | -0.3 | 0.3 | V |
| RF1 or RF2 Input Power applied for 24 hours maximum ($V_{DD}$ applied @ 2000 MHz and $T_{case}$=+85°C) | $P_{MAX24}$ | | 30 | dBm |
| Junction Temperature | $T_j$ | | 150 | °C |
| Storage Temperature Range | $T_{st}$ | -65 | 150 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012) | $V_{ESDHBM}$ | | (Class 1C) | |
| ElectroStatic Discharge – CDM (JEDEC 22-C101F) | $V_{ESDCDM}$ | | (Class C3) | |

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|---|
| $\theta_{JA}$ (Junction – Ambient) | 80.6 °C/W |
| $\theta_{JC}$ (Junction – Case) [The Case is defined as the exposed paddle] | 5.1 °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL1 |

## F2258 Recommended Operating Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 3.15 | | 5.25 | V |
| Control Voltage | $V_{CTRL}$ | $V_{DD}$ = 3.90 V to 5.25 V | 0 | | 3.6 | V |
| | | $V_{DD}$ = 3.15 V to 3.90 V | 0 | | $V_{DD}$-0.3 | |
| Operating Temperature Range | $T_{CASE}$ | Exposed Paddle | -40 | | +105 | °C |
| Frequency Range | $F_{RF}$ | | 50 | | 6000 | MHz |
| RF Operating Power | $P_{MAX, CW}$ | Power can be applied to RF1 or RF2 | | | See Figure 1 | dBm |
| RF1 Port Impedance | $Z_{RF1}$ | Single Ended | | 50 | | Ω |
| RF2 Port Impedance | $Z_{RF2}$ | Single Ended | | 50 | | Ω |

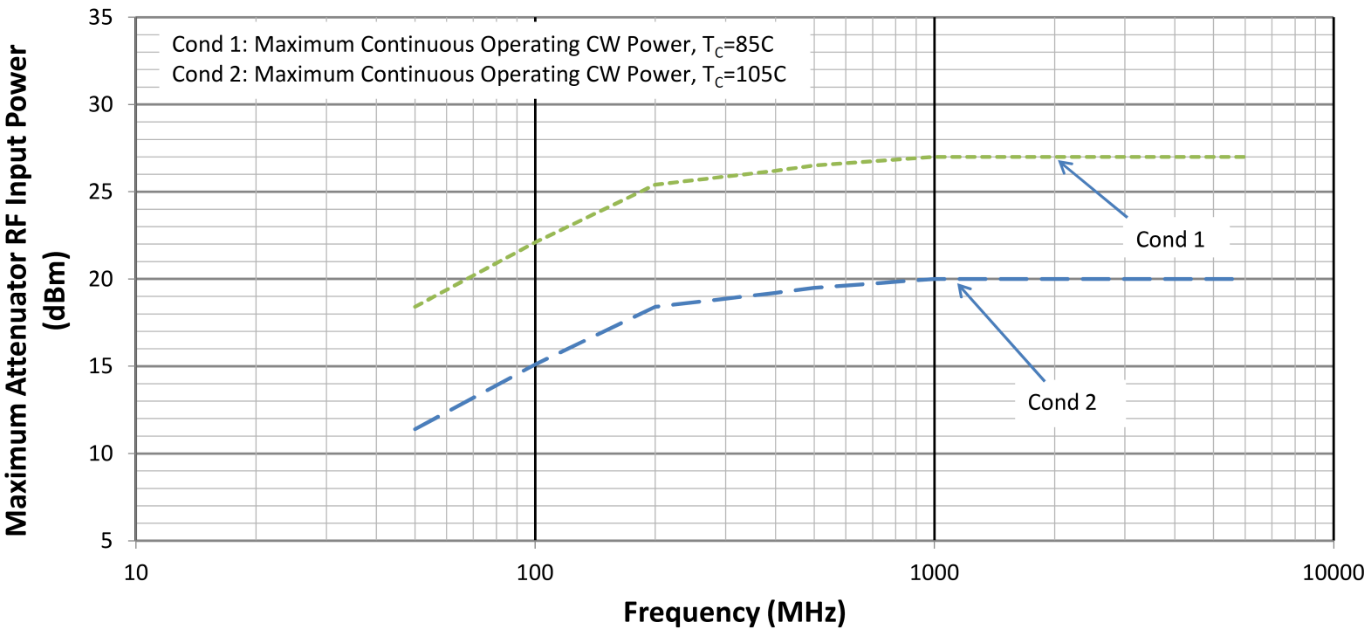



**Figure 1 - MAXIMUM RF INPUT POWER VS. RF FREQUENCY**

## F2258 Specification

Refer to EVKit / Applications Circuit, $V_{DD}$ = +3.3 V, $T_{CASE}$ = +25 °C, signal applied to RF1 input, $F_{RF}$ = 2000 MHz, minimum attenuation, $P_{IN}$ = 0 dBm for small signal parameters, +20 dBm for single tone linearity tests, +20 dBm per tone for two tone tests, two tone delta frequency = 50 MHz, PCB board traces and connector losses are de-embedded unless otherwise noted. Refer to Typical Operating Curves for performance over entire frequency band.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | ***0.5*** [1] | 1.17 | ***2*** | mA |
| $I_{CTRL}$ Current | $I_{CTRL}$ | | ***-1.0*** | | ***14*** | µA |
| Insertion Loss, IL | $A_{MIN}$ | Minimum Attenuation | | 1.4 | ***1.9*** | dB |
| Maximum Attenuation | $A_{MAX}$ | | 34 [2] | 35 | | dB |
| Insertion Phase Δ | $\Phi_{\Delta MAX}$ | At 36 dB attenuation relative to Insertion Loss | | 27 | | Deg |
| | $\Phi_{\Delta MID}$ | At 18 dB attenuation relative to Insertion Loss | | 10 | | |
| Input 1dB Compression [3] | P1dB | | | 34.4 | | dBm |
| Minimum RF1 Return Loss over control voltage range | $S_{11}$ | 50 MHz[4] | | 16 | | dB |
| | | 700 MHz | | 17 | | |
| | | 2000 MHz | | 17 | | |
| | | 6000 MHz | | 15 | | |
| Minimum RF2 Return Loss over control voltage range | $S_{22}$ | 50 MHz[4] | | 16 | | dB |
| | | 700 MHz | | 15 | | |
| | | 2000 MHz | | 16 | | |
| | | 6000 MHz | | 13 | | |
| Input IP3 | IIP3 | | | 65 | | dBm |
| | $IIP3_{MIN}$ | All attenuation settings | 44 | 47 | | |
| Output IP3 | $OIP3_{MIN}$ | Maximum attenuation | | 35 | | dBm |
| Input IP2 | IIP2 | $P_{IN}$ + $IM2_{dBc}$,<br>IM2 term is F1+F2 | | 95 | | dBm |
| | $IIP2_{MIN}$ | All attenuation settings | | 87 | | |
| Input IH2 | HD2 | $P_{IN}$ + $H2_{dBc}$ | | 90 | | dBm |
| Input IH3 | HD3 | $P_{IN}$ + ($H3_{dBc}$/2) | | 54 | | dBm |
| Settling Time | $T_{SETTL0.1dB}$ | Any 1 dB step in the 0 dB to 33 dB control range<br>50% $V_{CTRL}$ to RF settled to within ± 0.1 dB | | 15 | | µs |

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section along with Figure 1 for the maximum RF input power vs. RF frequency.
Note 4: Set blocking capacitors C1 & C2 to 0.01uF to achieve best return loss performance at 50 MHz.

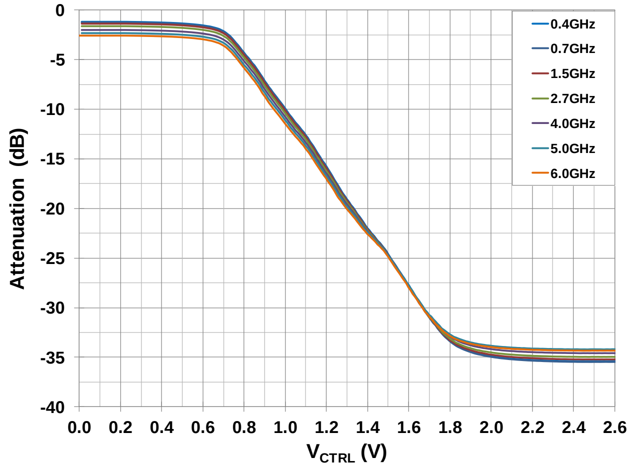
## TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

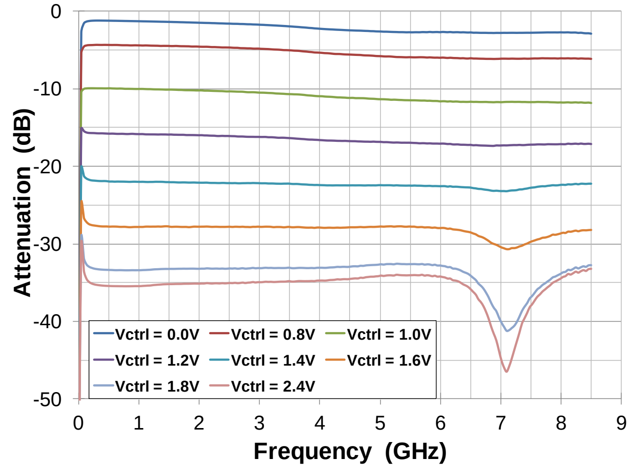
- **$V_{DD}$ = +3.3 V or +5.0 V**
- **$T_{CASE}$ = +25 °C**
- **$F_{RF}$ = 2000 MHz**
- **RF trace and connector losses are de-embedded for S-parameters**
- **Pin = 0 dBm for all small signal tests**
- **Pin = +20 dBm for single tone linearity tests (RF1 port driven)**
- **Pin = +20 dBm/tone for two tone linearity tests (RF1 port driven)**
- **Two tone frequency spacing = 50 MHz**

## TYPICAL OPERATING CONDITIONS [S2P BROADBAND PERFORMANCE] (- 1 -)

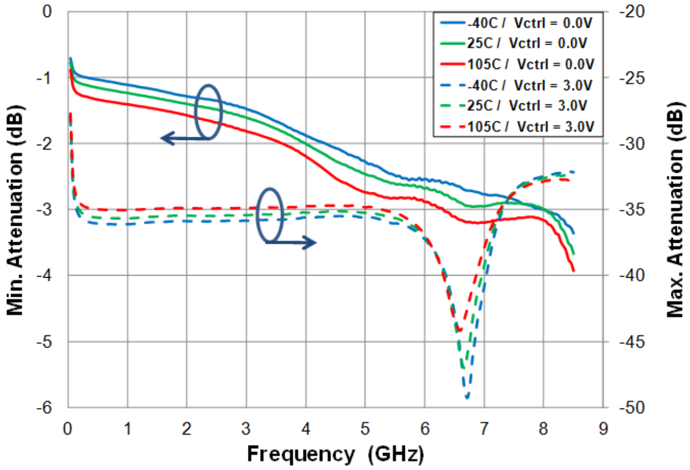
### Attenuation vs. $V_{CTRL}$



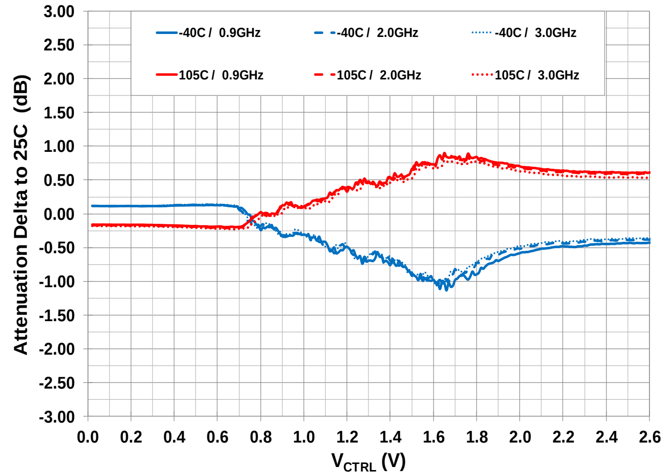

### Attenuation vs. Frequency




### Min. & Max. Attenuation vs. Frequency

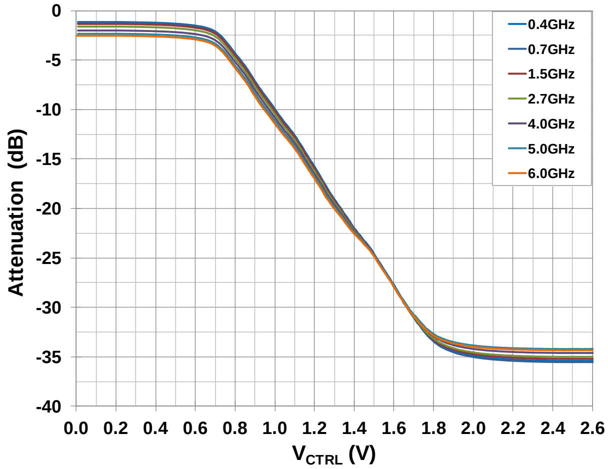



### Attenuation Delta to 25C vs. Frequency

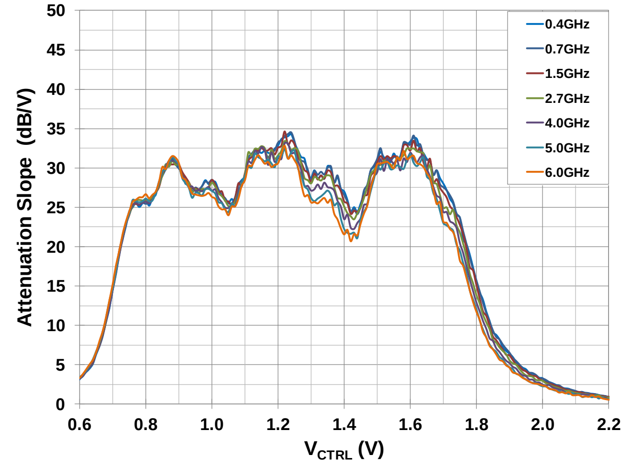


# TYPICAL OPERATING CONDITIONS [S2P VS. $V_{CTRL}$] (- 2 -)

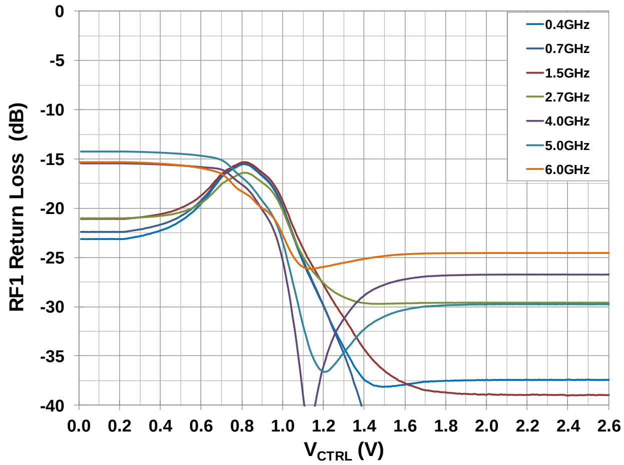
### Attenuation vs. $V_{CTRL}$



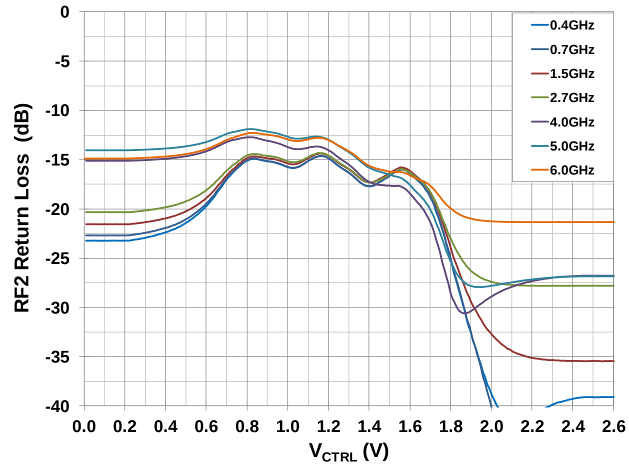

### Attenuation Slope vs. $V_{CTRL}$



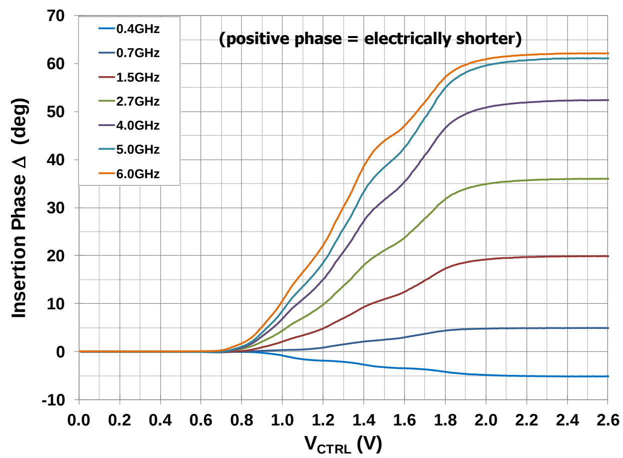

### RF1 Return Loss vs. $V_{CTRL}$



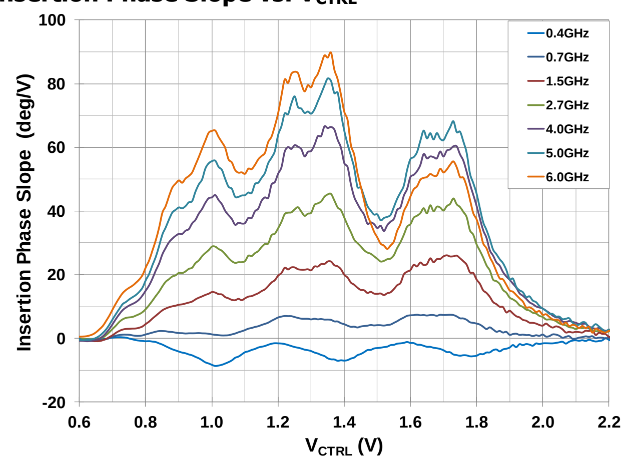

### RF2 Return Loss vs. $V_{CTRL}$




### Insertion Phase Δ vs. $V_{CTRL}$

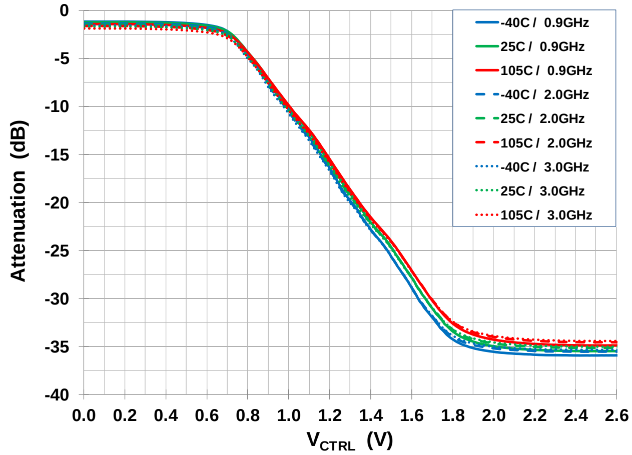



### Insertion Phase Slope vs. $V_{CTRL}$

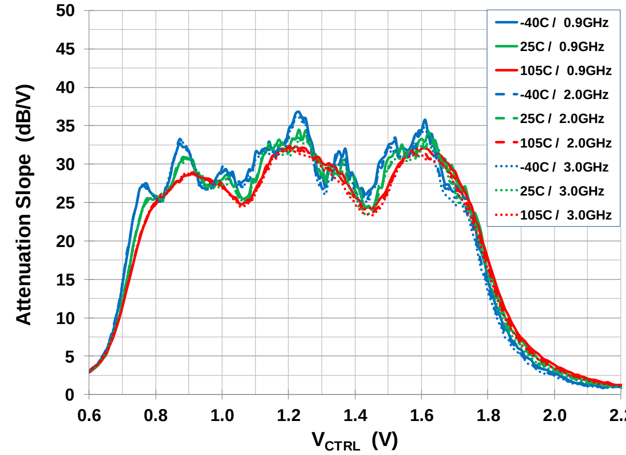


# TYPICAL OPERATING CONDITIONS [S2P VS. $V_{CTRL}$ & TEMPERATURE] (- 3 -)

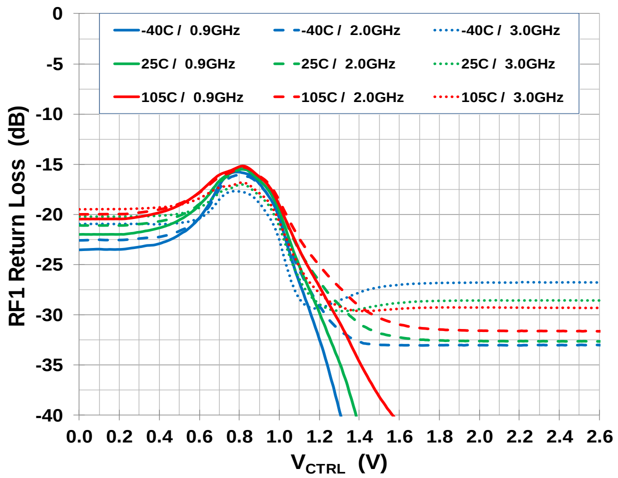
### Attenuation Response vs. $V_{CTRL}$



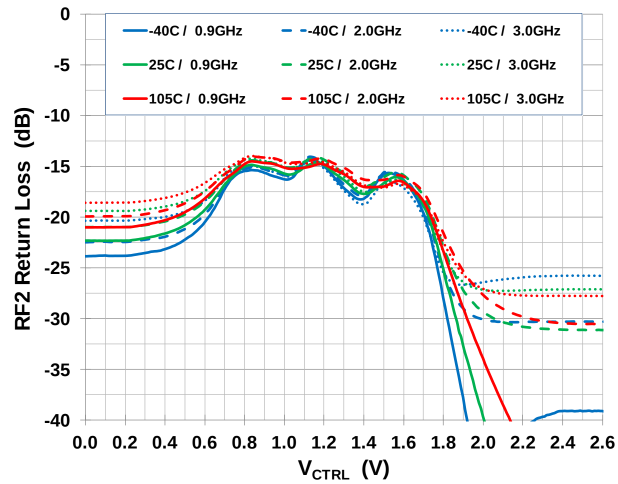

### Attenuation Slope vs. $V_{CTRL}$



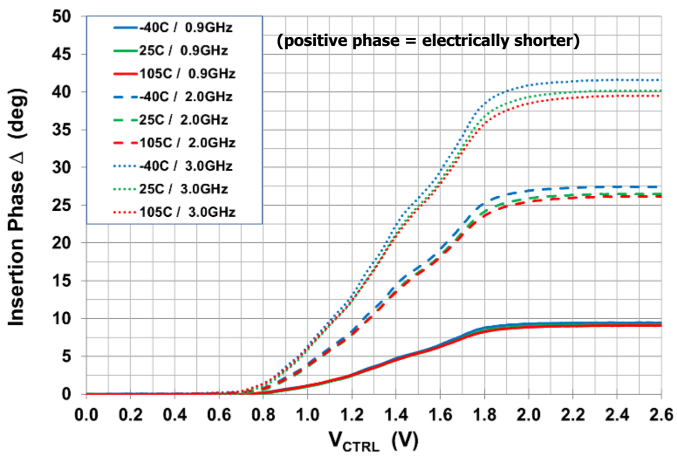

### RF1 Return Loss vs. $V_{CTRL}$



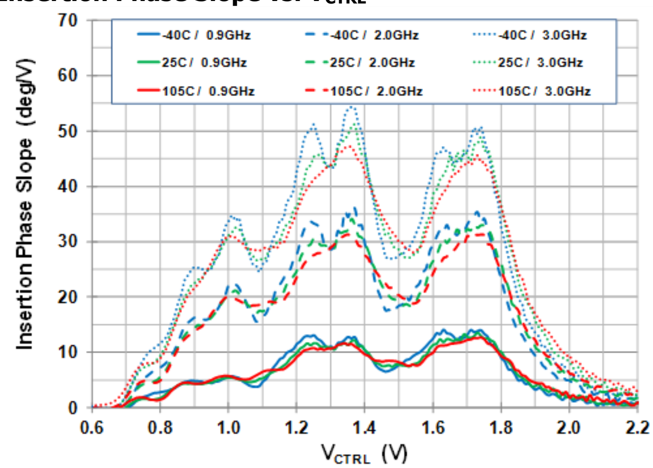

### RF2 Return Loss vs. $V_{CTRL}$




### Insertion Phase Δ vs. $V_{CTRL}$

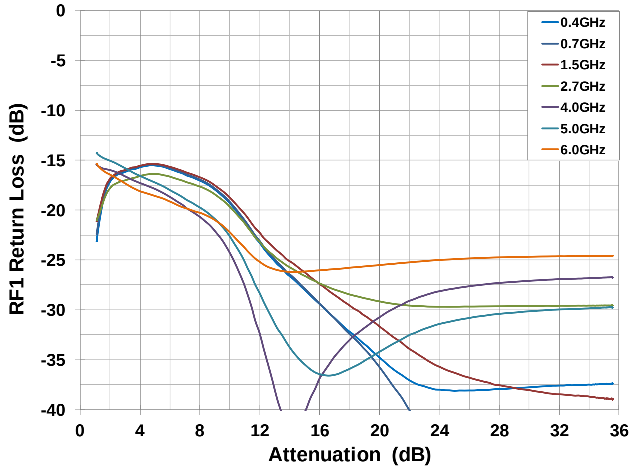



### Insertion Phase Slope vs. $V_{CTRL}$

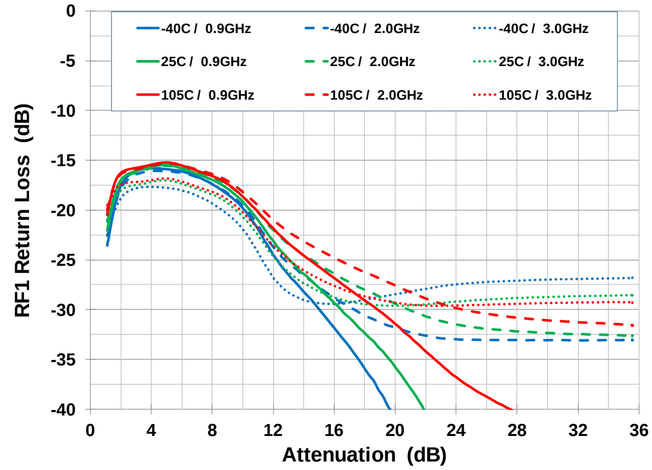


# TYPICAL OPERATING CONDITIONS [S2P VS. ATTENUATION & TEMPERATURE] (- 4 -)

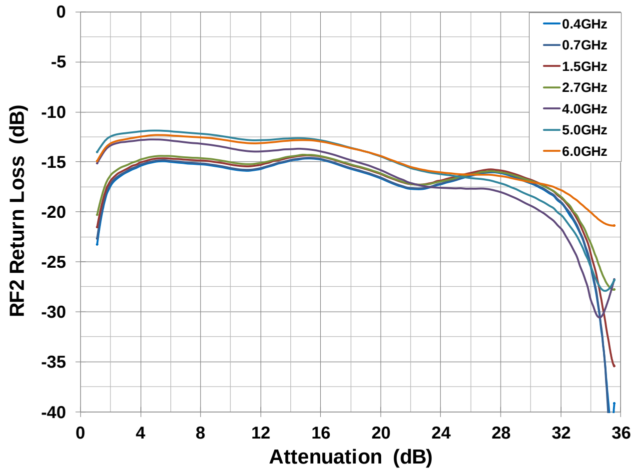
## RF1 Return Loss vs. Attenuation



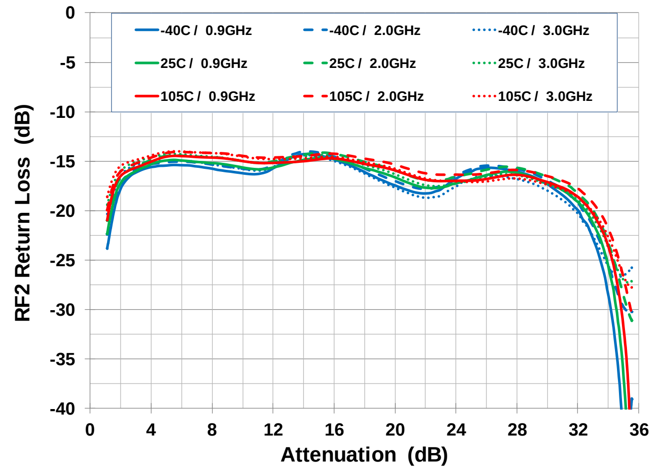

## RF1 Return Loss vs. Attenuation



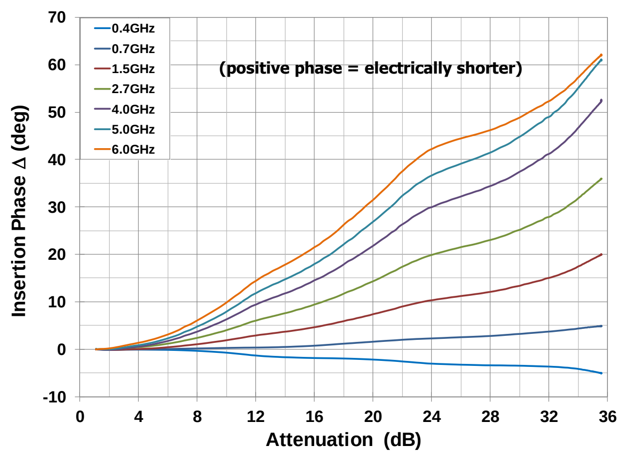

## RF2 Return Loss vs. Attenuation



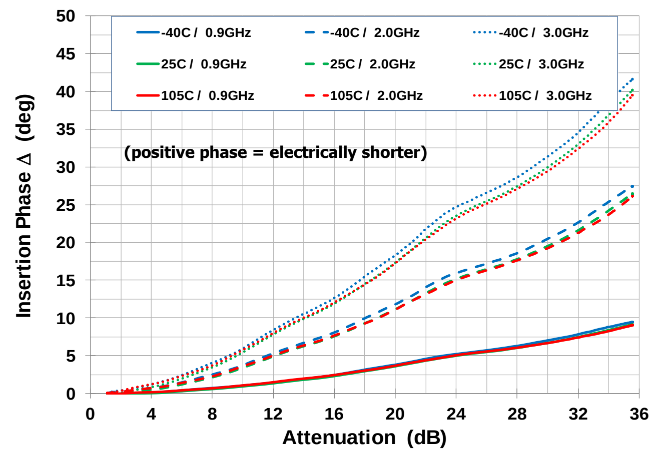

## RF2 Return Loss vs. Attenuation




## Insertion Phase Δ vs. Attenuation

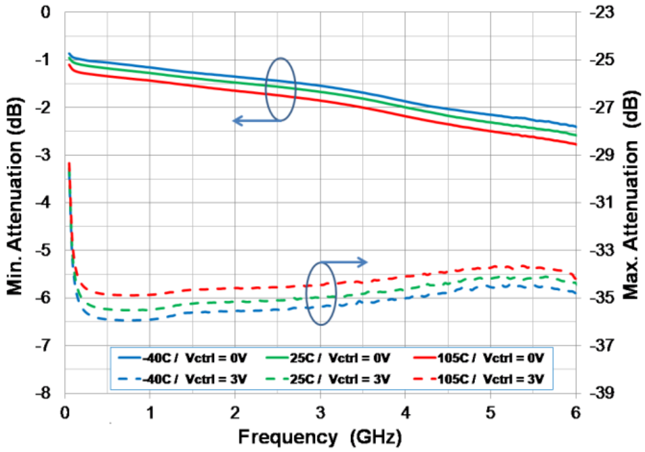



## Insertion Phase Δ vs. Attenuation

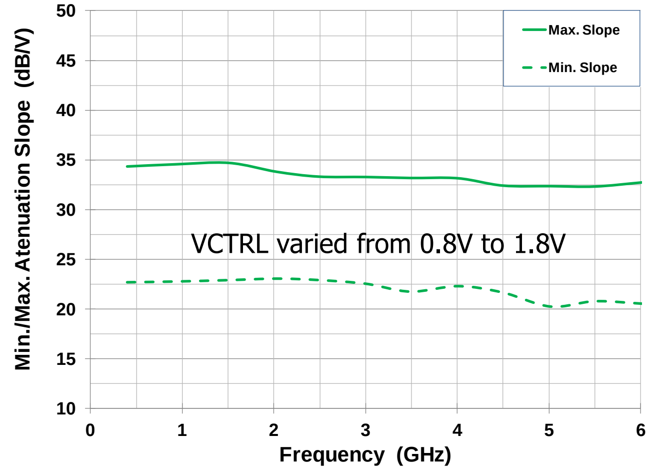


# TYPICAL OPERATING CONDITIONS [S2P VS. FREQUENCY] (- 5 -)

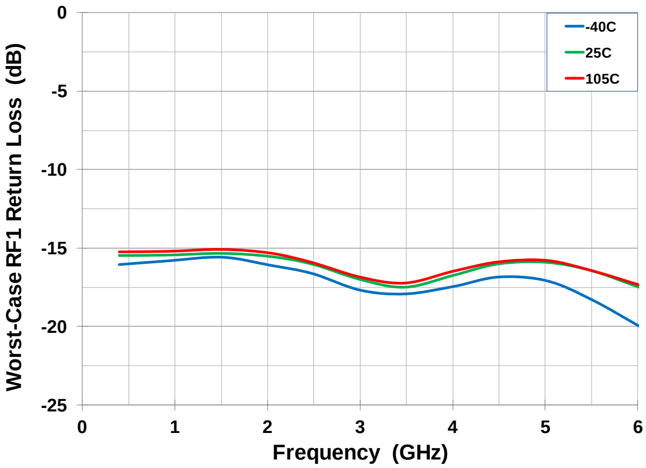
### Min & Max. Attenuation vs. Frequency



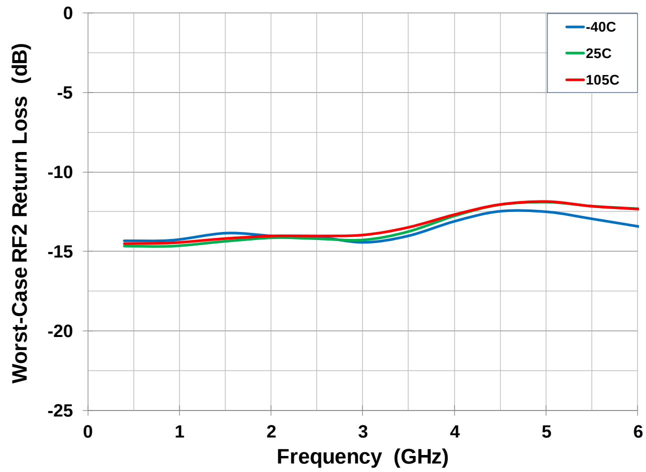

### Min. & Max. Attenuation Slope vs. Frequency



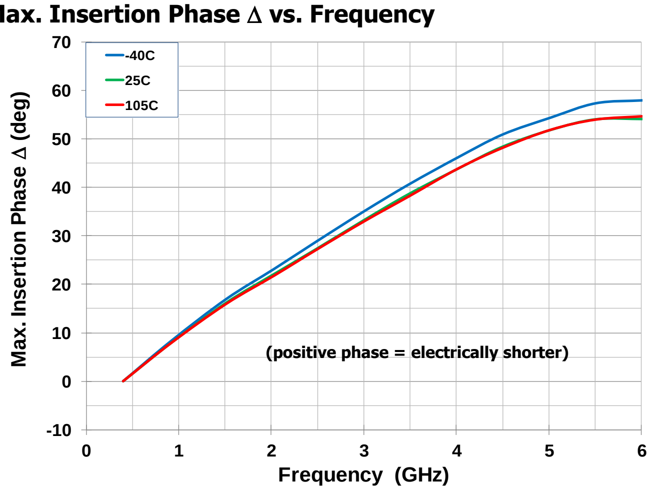

### Worst-Case RF1 Return Loss vs. Frequency



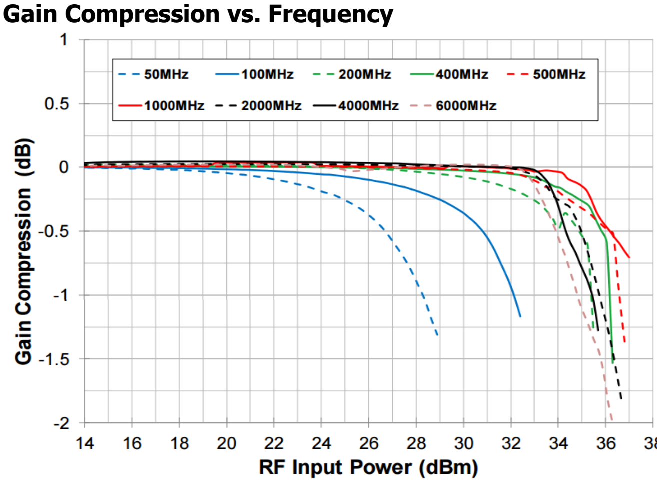

### Worst-Case RF2 Return Loss vs. Frequency




### Max. Insertion Phase Δ vs. Frequency

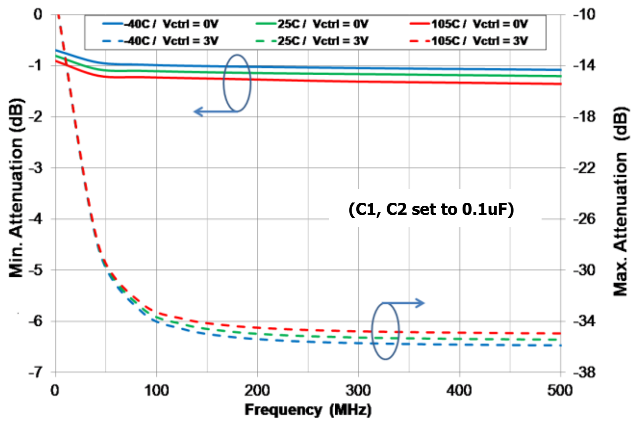



### Gain Compression vs. Frequency

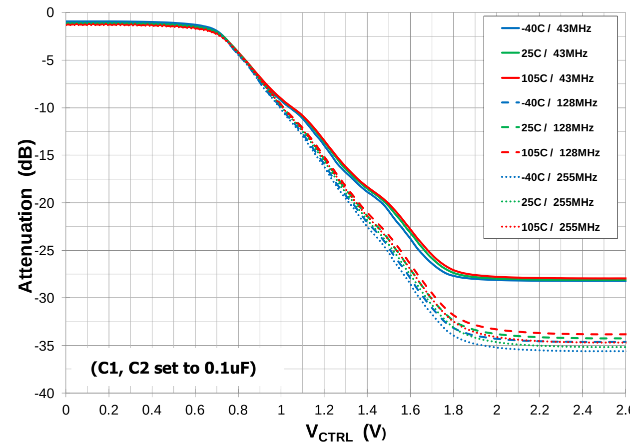


# TYPICAL OPERATING CONDITIONS [S2P @ LOW FREQUENCY, GROUP DELAY] (- 6 -)

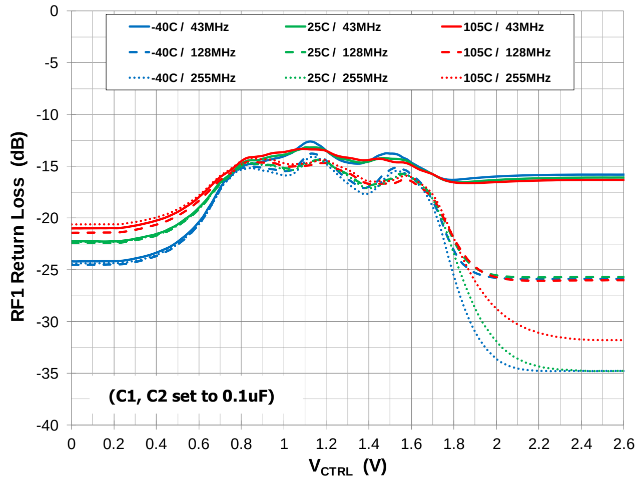
### Min & Max. Attenuation vs. Low Frequency



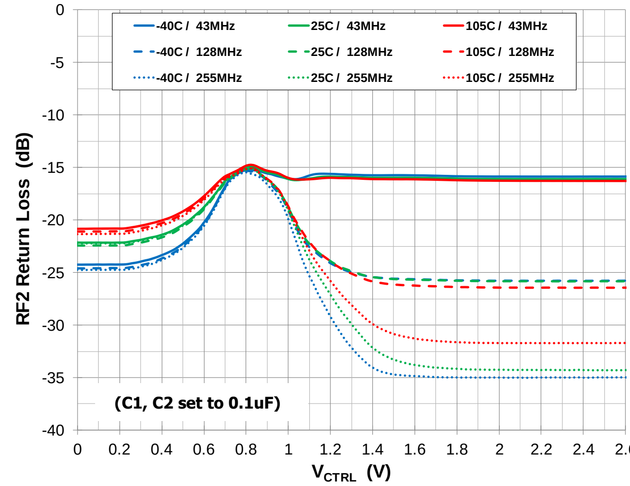

### Low-Frequency Attenuation vs. $V_{CTRL}$



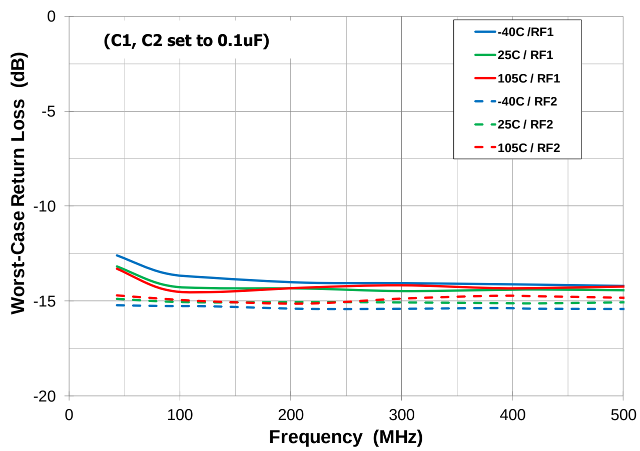

### Low-Frequency RF1 Return Loss vs. $V_{CTRL}$



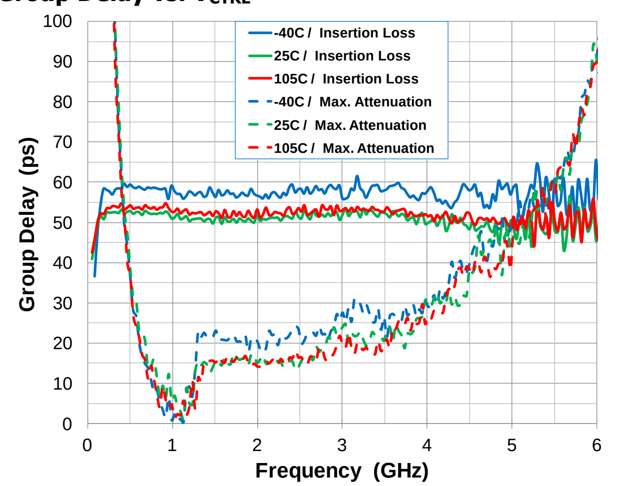

### Low-Frequency RF2 Return Loss vs. $V_{CTRL}$




### Worst-Case Return Loss vs. Low Frequency

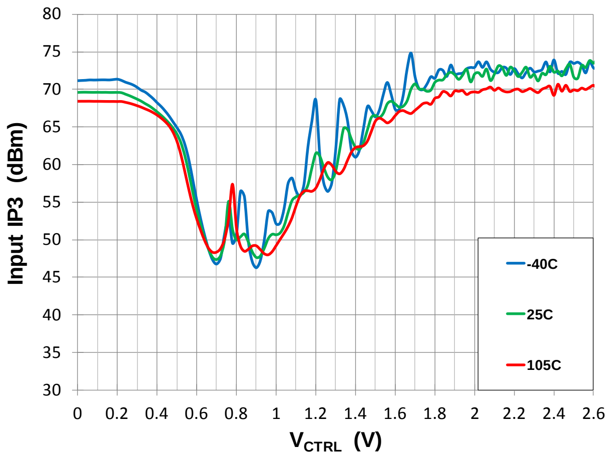



### Group Delay vs. $V_{CTRL}$

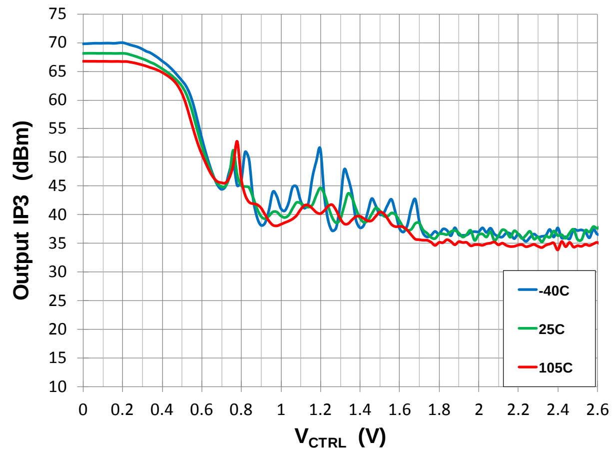


## TYPICAL OPERATING CONDITIONS 2GHz, $V_{DD}$=3.3V [IP3, IP2, IH2, IH3 vs. $V_{CTRL}$] (- 7 -)

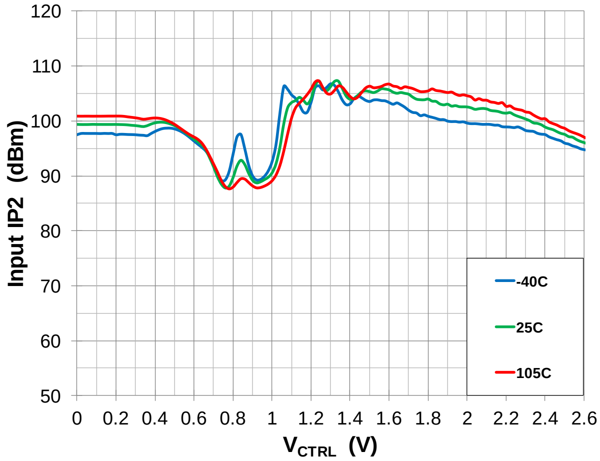
### Input IP3 vs. $V_{CTRL}$



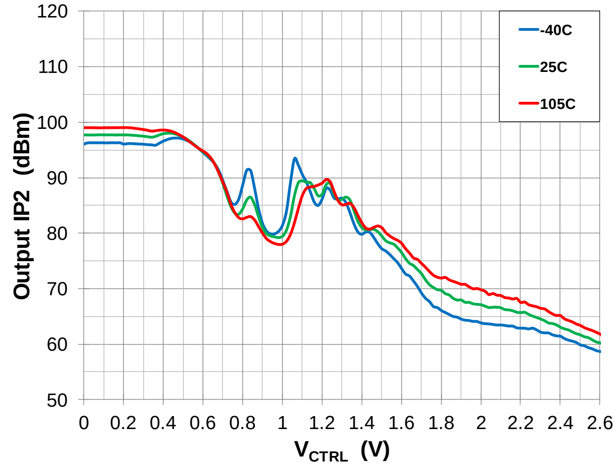

### Output IP3 vs. $V_{CTRL}$



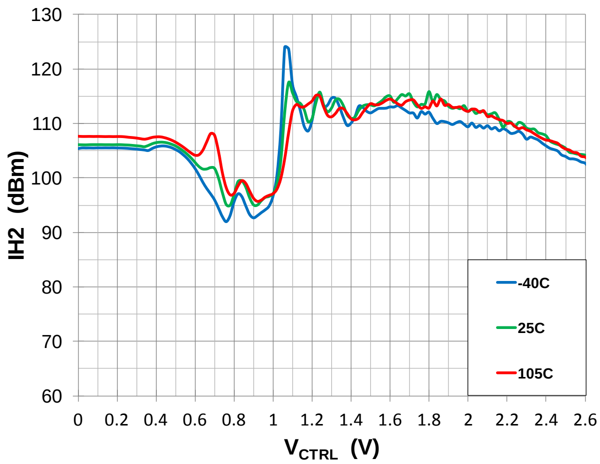

### Input IP2 vs. $V_{CTRL}$



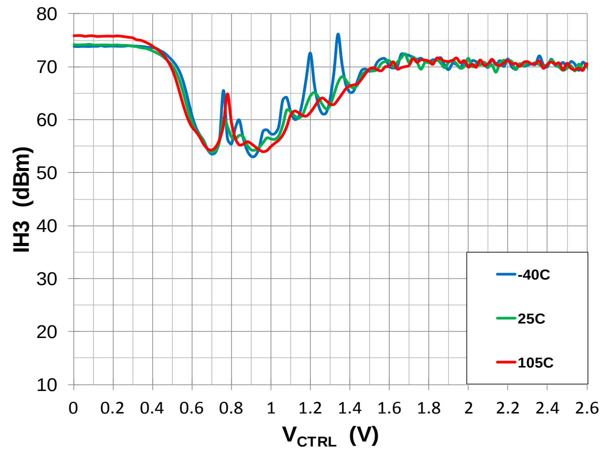

### Output IP2 vs. $V_{CTRL}$




### 2nd Harm Input Intercept Point vs. $V_{CTRL}$

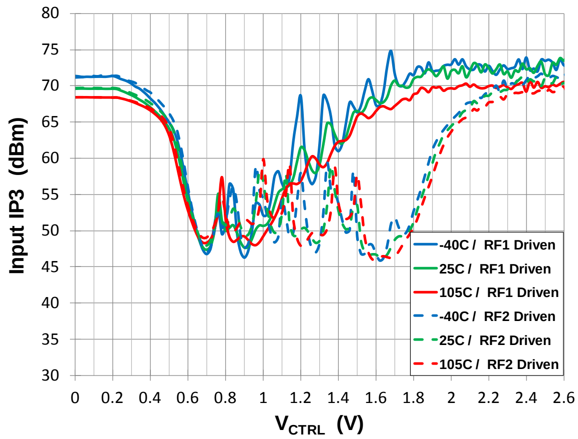



### 3rd Harm Input Intercept Point vs. $V_{CTRL}$

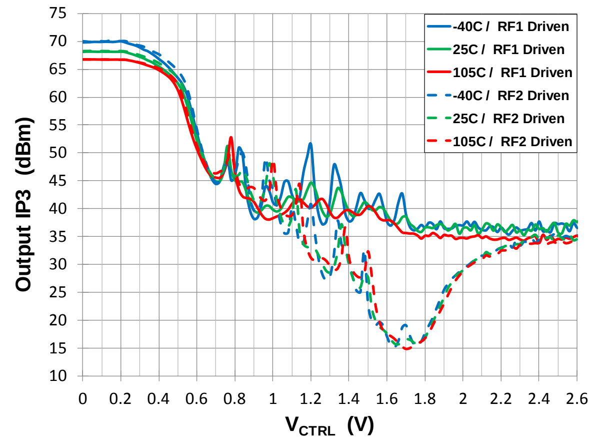


# TYPICAL OPERATING CONDITIONS 2GHz, $V_{DD}$=3.3V [IP3, IP2, IH2, IH3 VS. $V_{CTRL}$, RF1/RF2 DRIVEN] (- 8 -)

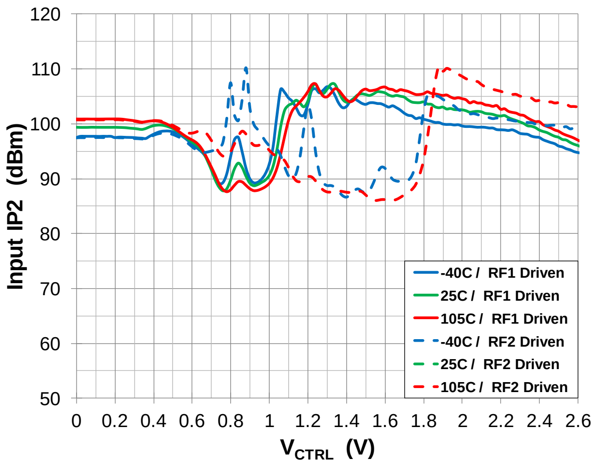
### Input IP3 vs. $V_{CTRL}$



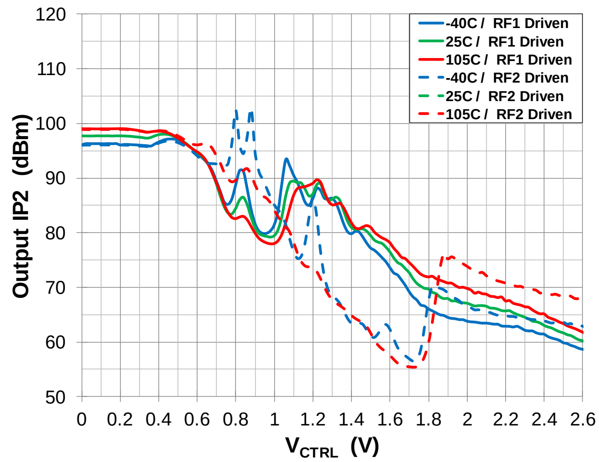

### Output IP3 vs. $V_{CTRL}$



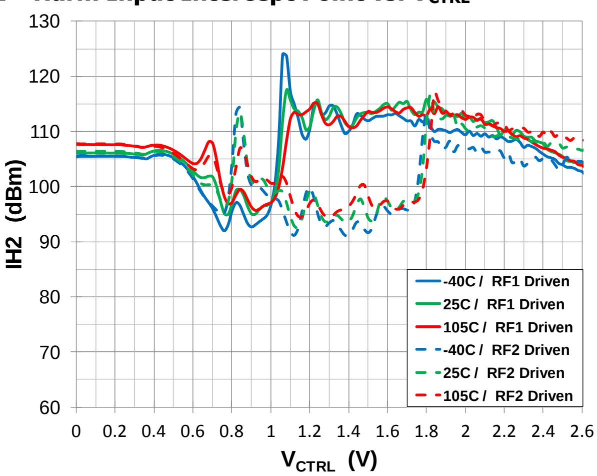

### Input IP2 vs. $V_{CTRL}$



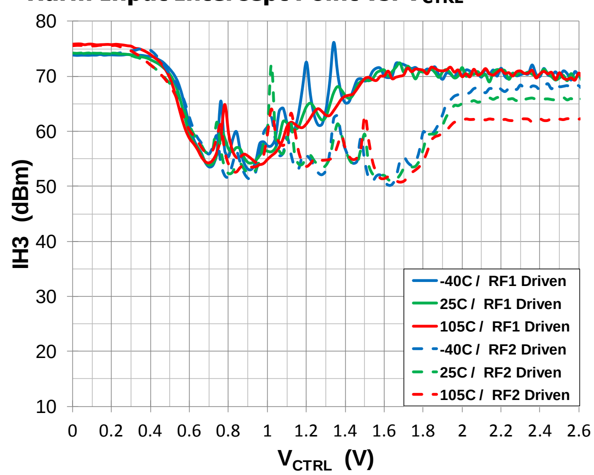

### Output IP2 vs. $V_{CTRL}$




### 2nd Harm Input Intercept Point vs. $V_{CTRL}$

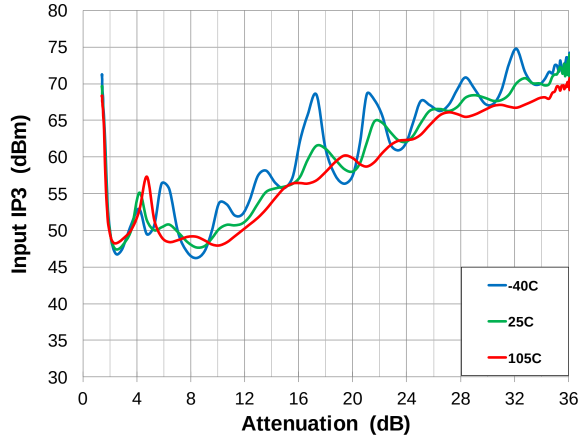



### 3rd Harm Input Intercept Point vs. $V_{CTRL}$

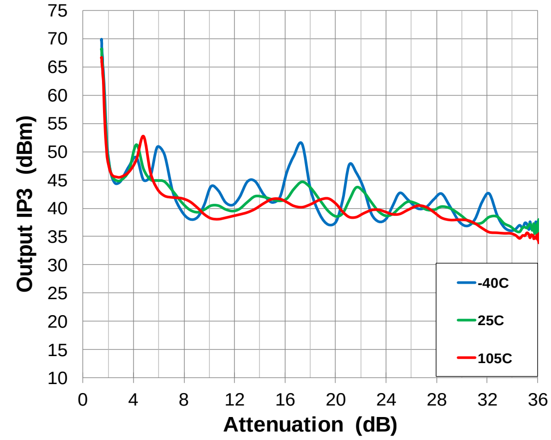


## TYPICAL OPERATING CONDITIONS 2GHZ, $V_{DD}$=3.3V [IP3, IP2, IH2, IH3 VS. ATTENUATION] (- 9 -)

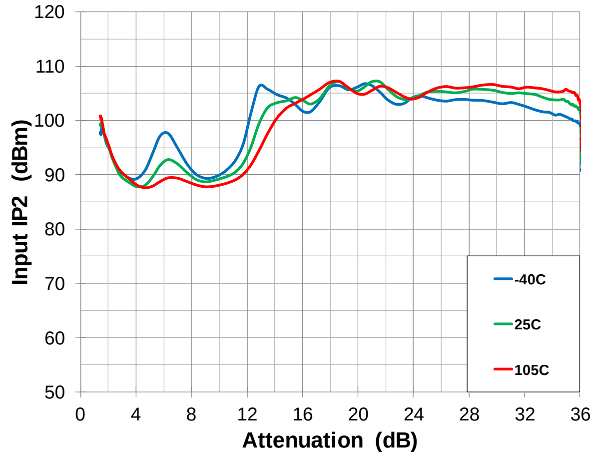
### Input IP3 vs. Attenuation



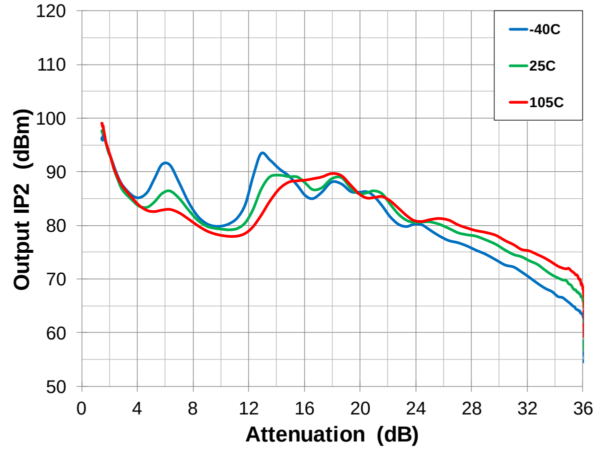

### Output IP3 vs. Attenuation



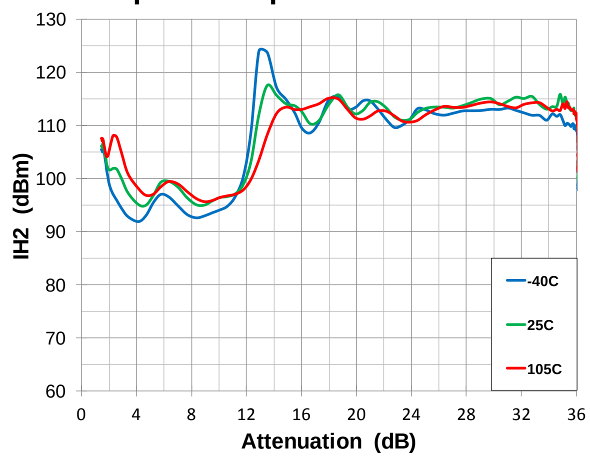

### Input IP2 vs. Attenuation



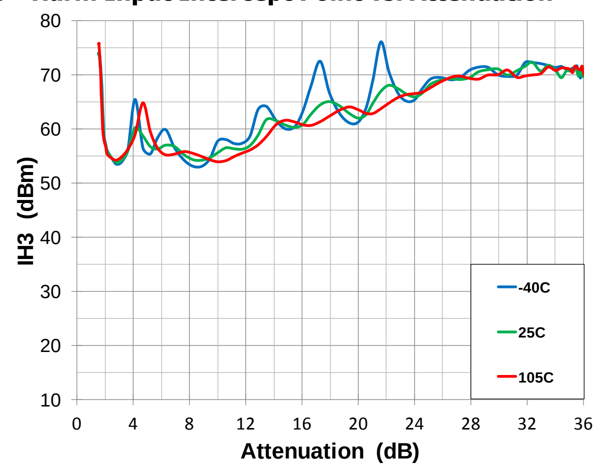

### Output IP2 vs. Attenuation




### 2nd Harm Input Intercept Point vs. Attenuation

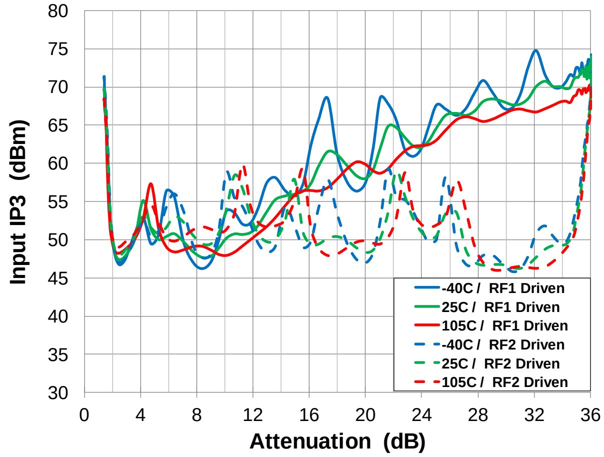



### 3rd Harm Input Intercept Point vs. Attenuation

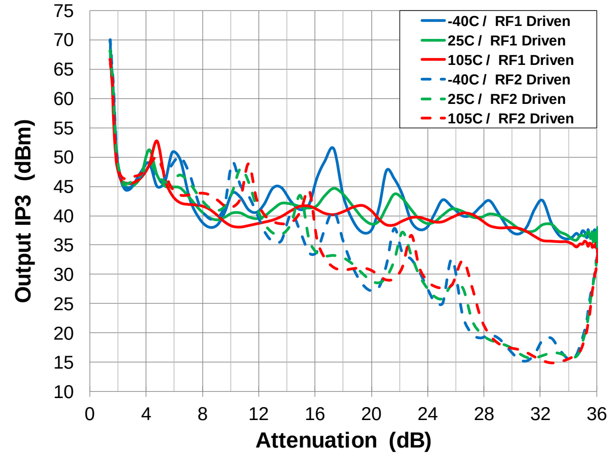


## TYPICAL OPERATING CONDITIONS 2GHz, $V_{DD}$=3.3V [IP3, IP2, IH2, IH3 vs. $V_{CTRL}$, RF1/RF2 DRIVEN] (- 10 -)

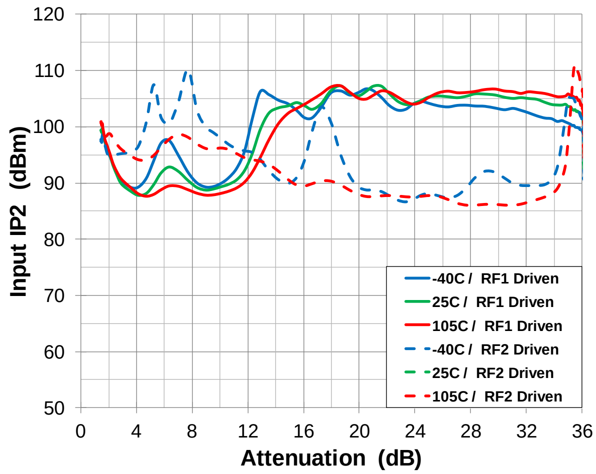
### Input IP3 vs. Attenuation



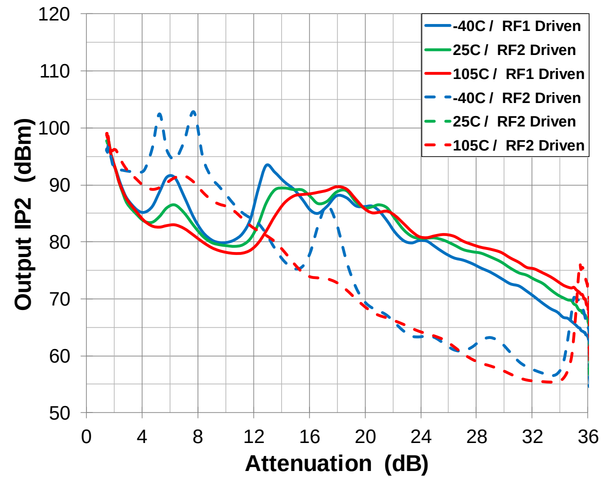

### Output IP3 vs. Attenuation



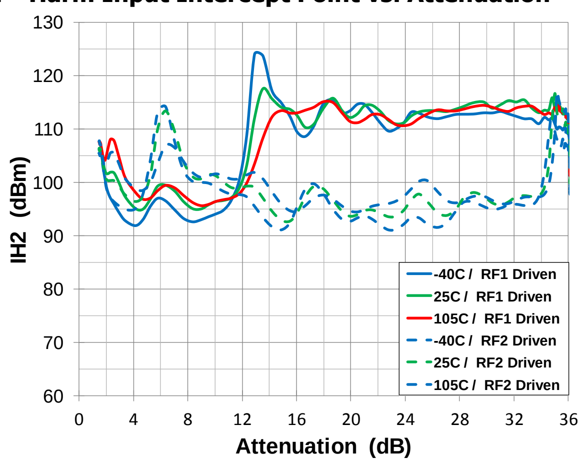

### Input IP2 vs. Attenuation



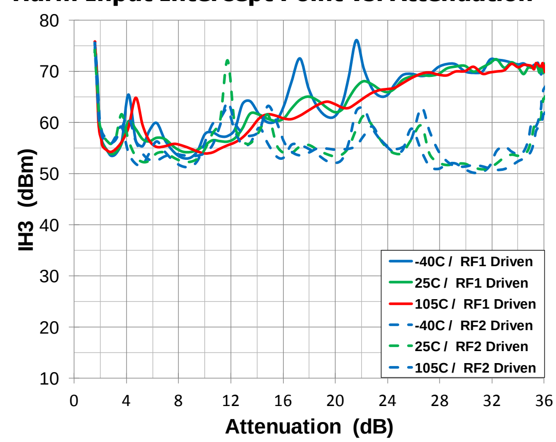

### Output IP2 vs. Attenuation




### 2nd Harm Input Intercept Point vs. Attenuation

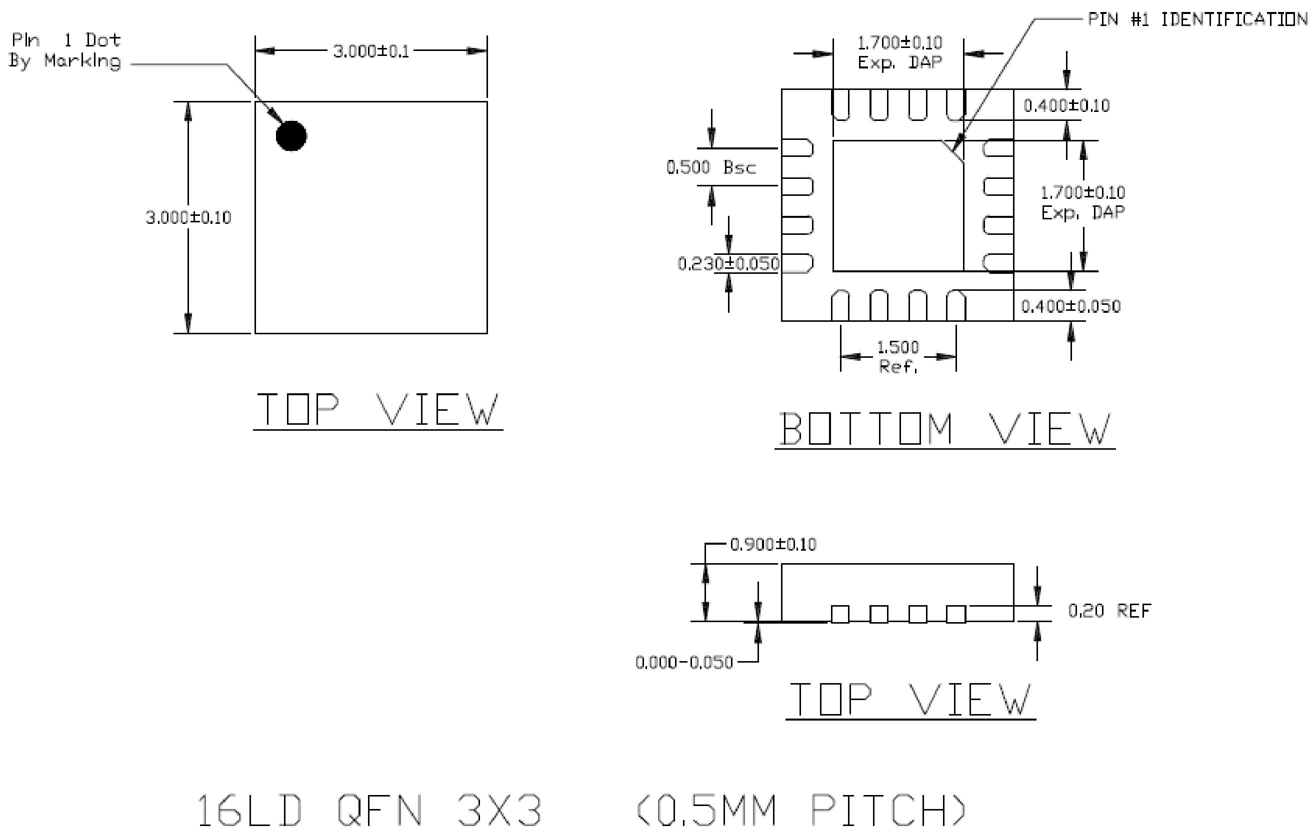



### 3rd Harm Input Intercept Point vs. Attenuation

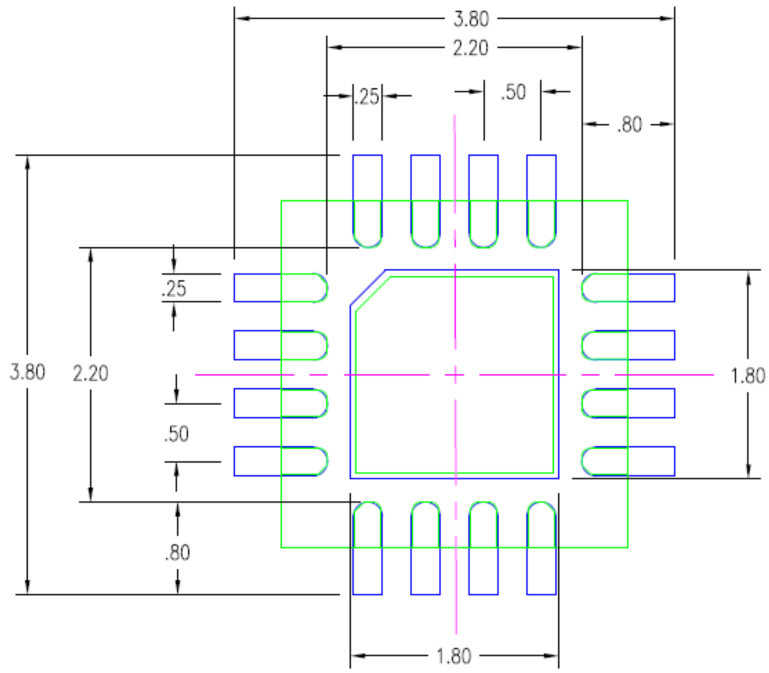


## PACKAGE DRAWING

(3mm x 3mm 16-pin QFN), NLG16

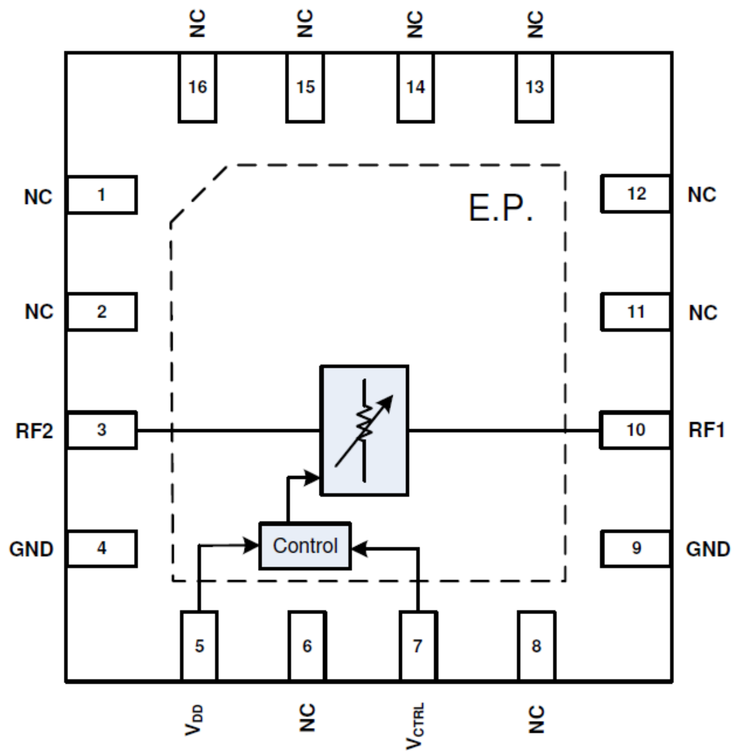


## LAND PATTERN DIMENSION




NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

## PIN DIAGRAM




## PIN DESCRIPTION

| Pin | Name | Function |
|---|---|---|
| 4, 9 | GND | Ground these pins as close to the device as possible. |
| 3 | RF2 | RF Port 2. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest. |
| 5 | $V_{DD}$ | Power supply input. Bypass to GND with capacitors close as possible to pin. |
| 1, 2, 6, 8, 11, 12, 13, 14, 15, 16 | NC | No internal connection. These pins can be left unconnected or connected to ground. |
| 7 | $V_{CTRL}$ | Attenuator control voltage. Apply a voltage in the range as specified in the Operating Conditions Table. See application section for details about $V_{CTRL}$. |
| 10 | RF1 | RF Port 1. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest. |
| | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to achieve the specified RF performance. |

# APPLICATIONS INFORMATION

## Default Start-up

The $V_{CTRL}$ pin has an internal pull-down resistor. If left floating, the part will power up in the minimum attenuation state.

## VCTRL

The $V_{CTRl}$ pin is used to control the attenuation of the F2258. With $V_{DD}$ = 5 V the control range of $V_{CTRl}$ is from 0 V (minimum attenuation) to 3.6 V (maximum attenuation). For other settings of $V_{DD}$ refer to the Operating Conditions Table. Apply $V_{DD}$ before applying voltage to the $V_{CTRl}$ pin to prevent damage to the on-chip pull-up ESD diode. If this sequencing is not possible, then set resistor R2 to 1kΩ to limit the current into the $V_{CTRl}$ pin.

## RF1 and RF2 Ports

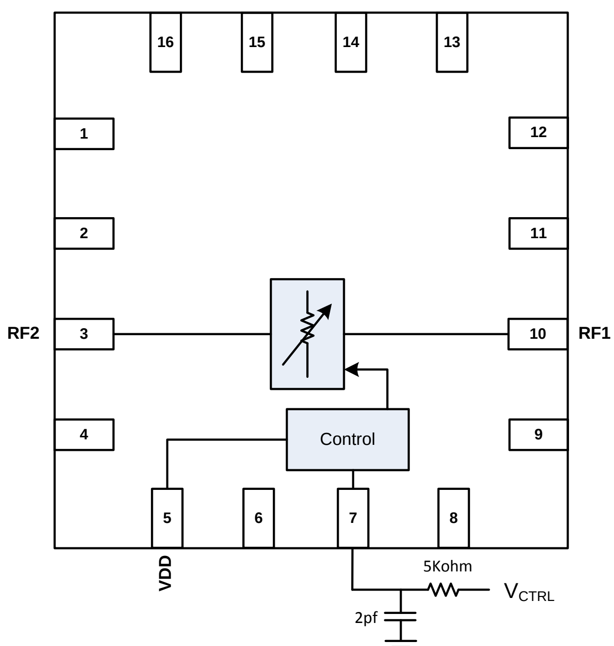
The F2258 is a bi-directional device thus allowing RF1 or RF2 to be used as the RF input. As displayed in the Typical Operating Conditions curves, RF1 shows enhanced linearity. $V_{DD}$ must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

## Power Supplies

The supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

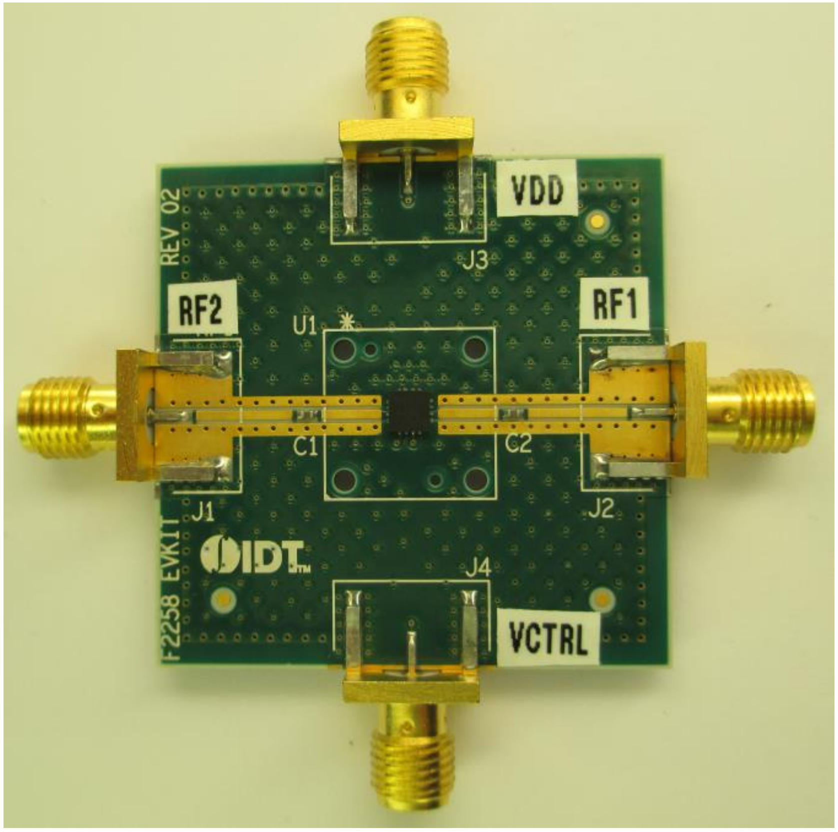
## Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of control pin 7 is recommended as shown below.

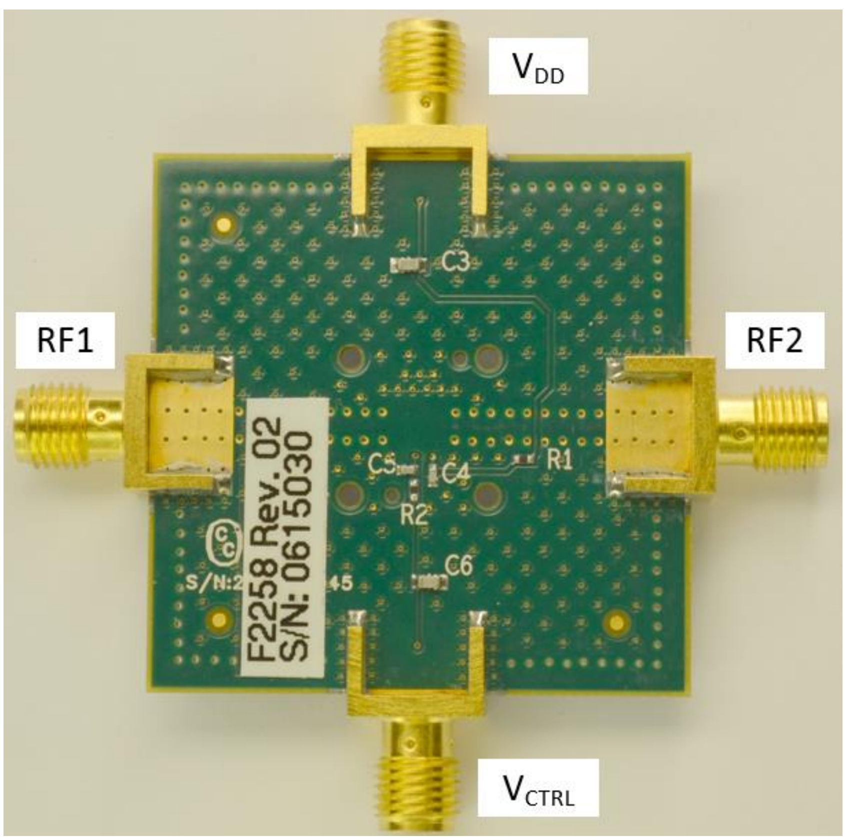


## EVKIT PICTURE

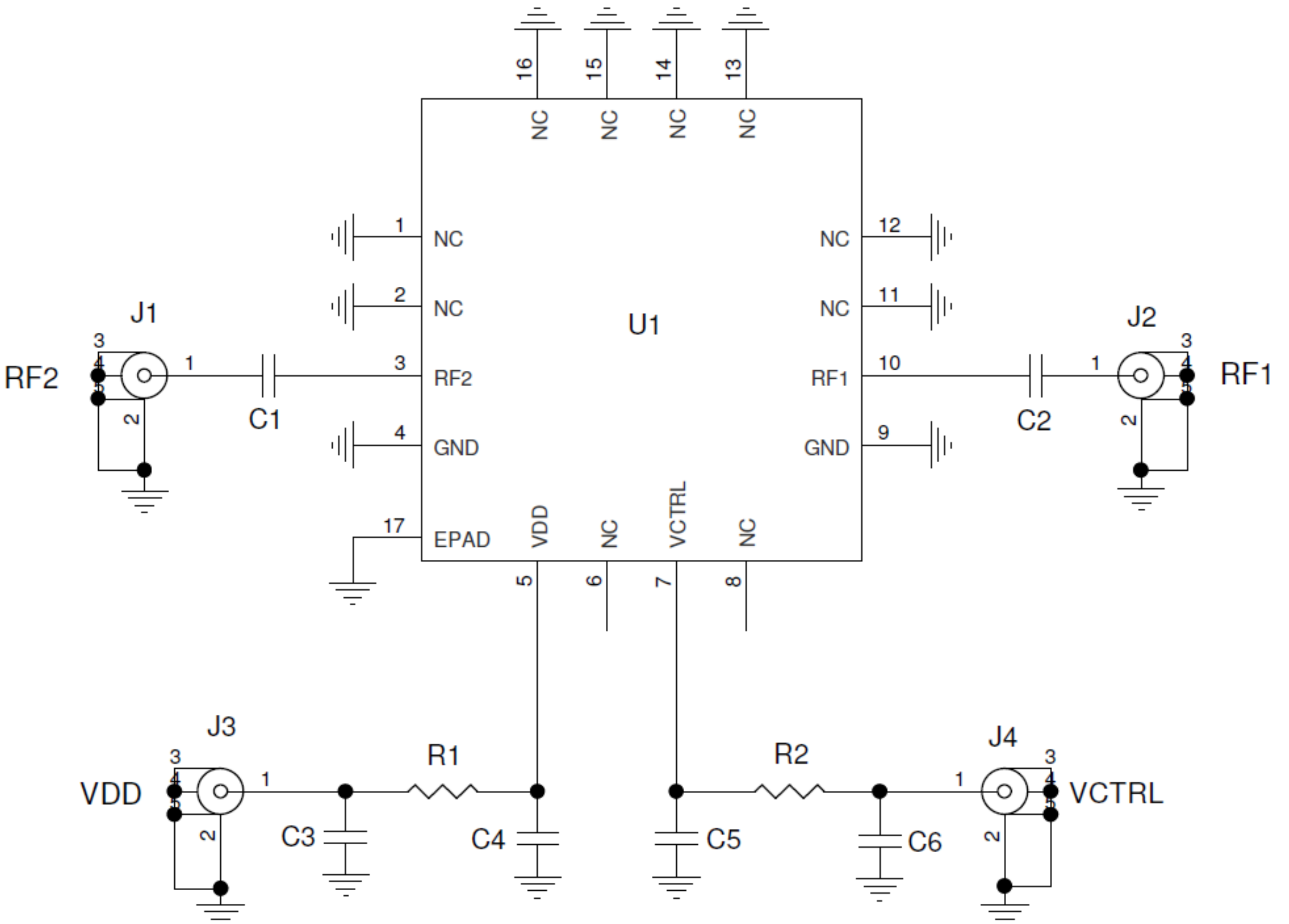
**Top View**




**Bottom View**



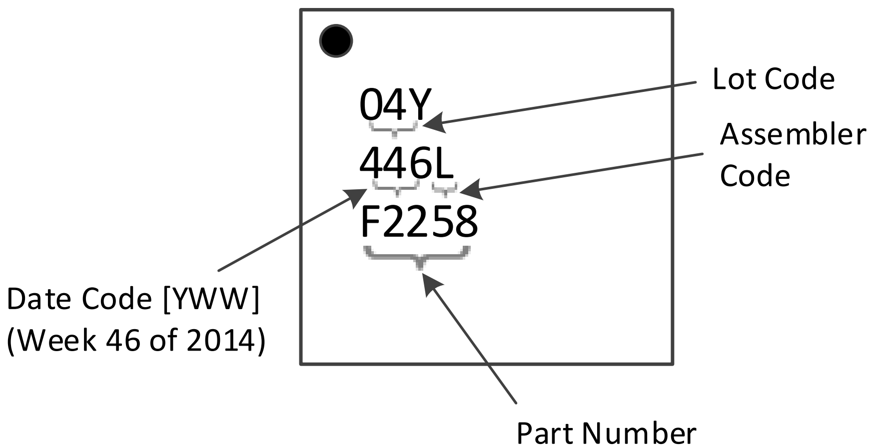
## EVKIT / APPLICATIONS CIRCUIT



## EVKIT BOM (REV 02)

| Item # | Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|---|---|---|---|---|---|
| 1 | C3, C6 | 2 | 10nF ±5%, 50V, X7R Ceramic Capacitor (0603) | GRM188R71H103J | Murata |
| 2 | C4, C5 | 2 | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| 3 | C1, C2 | 2 | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H101J | Murata |
| 4 | R1, R2 | 2 | 0Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| 5 | J1, J2, J3, J4 | 4 | Edge Launch SMA (0.375 inch pitch ground tabs) | 142-0701-851 | Emerson Johnson |
| 6 | U1 | 1 | Voltage Variable Attenuator | F2258NLGK | IDT |
| 7 | | 1 | Printed Circuit Board | F2258 EVKIT REV 02 | IDT |

## TOP MARKINGS



## REVISION HISTORY SHEET

| Rev | Date | Page | Description of Change |
|---|---|---|---|
| O | 2015-Aug-03 | | Initial Release |
| 1 | 2017-Jan-20 | 4 | Increased the Max limits for $I_{DD}$ and $I_{CTRL}$ |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

### Trademarks