

### **Description**

The F2976 is a single-pole double-throw (SP2T) reflective RF switch featuring high linearity and wide bandwidth. This device is optimized from 5MHz to 1.8GHz to support downstream cable modem future migration for DOCSIS 3.1 applications, and operates at up to 10GHz to support a multitude of wireless RF applications. Superb performance is achieved when used in either  $50\Omega$  or  $75\Omega$  terminating impedance applications.

The F2976 uses a single positive supply voltage of either +3.3V or +5.0V and is compatible with either 1.8V or 3.3V control logic.

### **Competitive Advantage**

The F2976 provides extremely low insertion loss across the entire bandwidth while providing superb distortion performance.

- Optimized for DOCSIS 3.1 applications up to 1.8GHz
- Optimized for Wi-Fi applications up to 5.9GHz
- Low insertion loss
- High isolation
- Fast switching
- No external matching required

## **Typical Applications**

- Broadband Cable DOCSIS 3.0 / 3.1
- Set top box
- CATV filter bank switching
- Wi-Fi
- Cellular BTS
- General purpose

#### **General Features**

- Supply voltage: +2.5V to +5.25V
- 1.8V and 3.3V compatible control logic
- 2mm x 2mm, 12-pin TQFN package
- -40°C to +105°C operating temperature range

### Features $(75\Omega)$

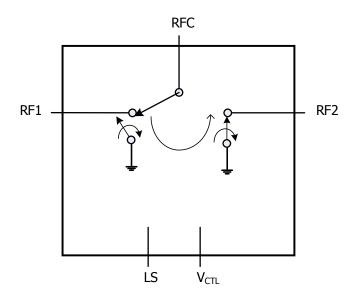
- Low insertion loss:
  - 0.23dB at 204MHz
  - 0.34dB at 1.8GHz
- High Isolation: 40dB at 1.8GHz
- P0.1dB compression of +37dBm at 204MHz
- Second Harmonic: -100dBc at 204MHz
- Third Harmonic: -120dBc at 204MHz
- Composite Second Order Distortion > 100dBc
- Composite Triple Beat Distortion > 100dBc

## Features (50 $\Omega$ )

- Low insertion loss:
  - 0.40dB at 2.4GHz
  - 0.55dB at 8GHz
- High Isolation:
  - 34dB at 2.4GHz
- High Linearity:
  - IIP2 +125dBm at 2.4GHz
  - IIP3 +77dBm at 2.4GHz
- P0.1dB compression of +40dBm at 2.4GHz
- Second Harmonic: -100dBc at 2.4GHz
- Third Harmonic: -110dBc at 2.4GHz

## **Block Diagram**

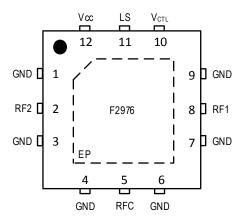
#### Figure 1. Block Diagram





# **Pin Assignments**

Figure 2. Pin Assignments for 2mm x 2mm x 0.5mm 12-pin TQFN, NEG12 – Top View



## **Pin Descriptions**

Table 1. Pin Descriptions

Number	Name	Description
1	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
2	RF2	RF2 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
4	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
5	RFC	RF Common Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
6	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
7	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
8	RF1	RF1 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
9	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
10	$V_{CTL}$	Logic control pin (see Table 9).
11	LS	Truth Table select pin. Defines $V_{CTL}$ logic for RF switching (see Table 9). Pin is internally pulled up to 2.5V through a $500k\Omega$ resistor.
12	Vcc	Power supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.



## **Absolute Maximum Ratings**

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 2. Absolute Maximum Ratings** 

Par	ameter	Symbol	Minimum	Maximum	Units	
V <sub>CC</sub> to GND	V <sub>CC</sub>	-0.3	+5.5	V		
V <sub>CTL</sub> , LS		V <sub>LOGIC</sub>	-0.3	Lower of (V <sub>CC</sub> + 0.3, 3.9)	V	
RF1, RF2, RFC		$V_{RF}$	-0.3	+0.3	V	
	$5MHz \le f_{RF} \le 10MHz$	P <sub>ABSCW1</sub>		30		
Maximum Input CW	$10MHz < f_{RF} \le 25MHz$	P <sub>ABSCW2</sub>		32		
Power, $50\Omega$ , $T_{EP} = 25$ °C, $V_{CC} = 5.25V$ (any port,	$25MHz < f_{RF} \le 200MHz$	P <sub>ABSCW3</sub>		33	dBm	
insertion loss state) [a,b]	$200MHz < f_{RF} \le 6000MHz$	P <sub>ABSCW4</sub>		34		
,	f <sub>RF</sub> > 6000MHz	P <sub>ABSCW5</sub>		33		
	$5MHz \le f_{RF} \le 10MHz$	P <sub>ABSPK1</sub>		35		
Maximum Peak Power,	$10MHz < f_{RF} \le 25MHz$	P <sub>ABSPK2</sub>		37		
$50\Omega$ , $T_{EP} = 25^{\circ}C$ , $Vcc = 5.25V$ (any port,	$25MHz < f_{RF} \le 200MHz$	P <sub>ABSPK3</sub>		38	dBm	
insertion loss state) [a, b, c]	$200MHz < f_{RF} \le 6000MHz$	P <sub>ABSPK4</sub>		39		
,	f <sub>RF</sub> > 6000MHz	P <sub>ABSPK5</sub>		38		
Maximum Junction Temper	rature	T <sub>JMAX</sub>		+140	°C	
Storage Temperature Rang	T <sub>ST</sub>	-65	+150	°C		
Lead Temperature (solderi	T <sub>LEAD</sub>		+260	°C		
Electrostatic Discharge – F (JEDEC/ESDA JS-001-201	V <sub>ESDHBM</sub>		2500 (Class 2)	V		
Electrostatic Discharge – C (JEDEC 22-C101F)	CDM	V <sub>ESDCDM</sub>		1000 (Class C3)	V	

a. In a  $50\Omega$  system, dBmV = dBm  $[50\Omega]$  + 47. In a  $75\Omega$  system, dBmV = dBm  $[75\Omega]$  + 48.75.

b.  $T_{EP}$  = Temperature of the exposed paddle.

c. 5 % duty cycle of a 4.6ms period.



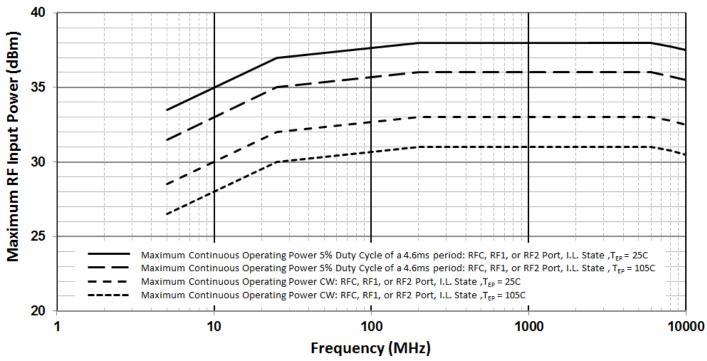
## **Recommended Operating Conditions**

**Table 3. Recommended Operating Conditions** 

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	Vcc		2.5	3.3	5.25	V
Operating Temperature Range	T <sub>EP</sub>	Exposed Paddle	-40		+105	°C
DE Fraguency Dange	ť	75Ω	0.005		1.8	GHz
RF Frequency Range	$f_{RF}$	50Ω	0.005		10	
Maximum Operating Input Power	P <sub>MAX</sub>	Insertion Loss State $Z_S = Z_L = 50\Omega$			See Figure 3 [a]	dBm
Port Impedance (DEC, DE1, DE2)	7	75Ω System		75		0
Port Impedance (RFC, RF1, RF2)	$Z_{RF}$	50Ω System		50		Ω

a. In a  $50\Omega$  system, dBmV = dBm  $[50\Omega]$  + 47. In a  $75\Omega$  system, dBmV = dBm  $[75\Omega]$  + 48.75.

Figure 3. Maximum Operating RF Input Power ( $Z_s = Z_L = 50\Omega$ )





## **General Specifications**

### **Table 4. General Specifications**

See F2976 Typical Application Circuit. Specifications apply when operated with  $V_{CC}$  = +3.3V,  $T_{EP}$  = +25°C, LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V <sub>IH</sub>	V <sub>CTL</sub> , LS pins	1.17 <sup>[b]</sup>		Lower of (V <sub>CC</sub> , 3.6)	V
Logic Input Low Threshold	$V_{IL}$	V <sub>CTL</sub> , LS pins	-0.3		0.6	V
Logic Current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>CTL</sub> , LS pins (each pin)	-10 [a]		+10	μA
DC Current (V <sub>CC</sub> )	I <sub>CC</sub>			80	150	μΑ
Switching Rate	SW <sub>RATE</sub>				25	kHz
$\begin{array}{c} \text{Peak transient duri} \\ \text{Maximum Video Feed-Through,} \\ \text{RFC Port} \end{array}  \begin{array}{c} \text{Peak transient duri} \\ \text{switching. } Z_S = Z_L = \\ \text{Measured with 20n} \\ \text{0V to 3.3V (3.3V to )} \end{array}$		Peak transient during switching. $Z_S = Z_L = 75\Omega$ . Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to $V_{CTL}$ .		5		mVp-p
Switching Time [6]	SW <sub>TIME</sub>	50% V <sub>CTL</sub> to 90% or 10% RF		1.5	3	μs

- a. Items in min/max columns in **bold italics** are guaranteed by test.
- b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
- c. Measured at  $f_{RF} = 1GHz$ .



#### **Electrical Characteristics**

### Table 5. Electrical Characteristics - 75Ω SPECIFICATION

See F2976 75 $\Omega$  Application Circuit. Specifications apply when operated with  $V_{CC}$  = +3.3V,  $T_{EP}$  = +25 $^{\circ}$ C.  $Z_{S}$  =  $Z_{L}$  = 75 $\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units	
		f <sub>RF</sub> = 5MHz		0.20			
	,,	$5MHz < f_{RF} \le 204MHz$		0.23	0.43 [b]	ID	
Insertion Loss (RFC to RF1, RF2)	IL	204MHz < f <sub>RF</sub> ≤ 1.2GHz		0.32	0.52	dB	
		1.2GHz < f <sub>RF</sub> ≤ 1.8GHz		0.34	0.54		
		f <sub>RF</sub> = 5MHz		77			
Isolation (All Paths)	ISO1	$5MHz < f_{RF} \le 204MHz$		60		dB	
ISOIAUOTI (AII PAUTS)	1301	$204MHz < f_{RF} \le 1.2GHz$		44		uь	
		$1.2GHz < f_{RF} \le 1.8GHz$		40			
		$f_{RF} = 5MHz$		35			
Return Loss (RFC, RF1, RF2)	RL	$5MHz < f_{RF} \le 204MHz$		30		dB	
(Insertion Loss States)		$204MHz < f_{RF} \le 1.2GHz$		17		ub -	
		$1.2GHz < f_{RF} \le 1.8GHz$		16			
		f <sub>IN</sub> = 27MHz P <sub>OUT</sub> = 20dBm [c]		-80	-70		
2 <sup>nd</sup> Harmonic	H2	$f_{IN} = 204MHz P_{OUT} = 20dBm$		-100	-90	dBc	
		$f_{IN} = 800MHz P_{OUT} = 20dBm$		-120	-110	] '	
		f <sub>IN</sub> = 17MHz P <sub>OUT</sub> = 20dBm		-95	-80		
3 <sup>rd</sup> Harmonic	Н3	$f_{IN} = 204MHz P_{OUT} = 20dBm$		-120	-105	dBc	
		$f_{IN} = 800MHz P_{OUT} = 20dBm$		-115	-100		
		$f_{RF} = 5MHz$		37			
Input 0.1dB Compression Point [d] (RFC to RF1, RF2)	P0.1dB	f <sub>RF</sub> = 204MHz		37		dBm	
(14 0 to 14 1, 14 2)		f <sub>RF</sub> = 1.8GHz		38			
Composite Second Order	CSO	41dBmV / channel		>100		dBc	
Composite Triple Beat	CTB 137 channels [e]			>100	_	ubc	

- a. Items in min/max columns in **bold italics** are guaranteed by test.
- b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
- c.  $dBmV = dBm [75\Omega] + 48.75$ .
- d. The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum operating RF input power levels.
- e. Total power = -7.75 dBm [75 $\Omega$ ] + 10\*log (137) = +13.62 dBm [75 $\Omega$ ].



## **Electrical Characteristics**

#### Table 6. Electrical Characteristics - 50Ω SPECIFICATION

See F2976  $50\Omega$  Application Circuit. Specifications apply when operated with  $V_{CC}$  = +3.3V,  $T_{EP}$  = +25°C.  $Z_S$  =  $Z_L$  =  $50\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
		f <sub>RF</sub> = 5MHz		0.25	0.45 [b]	
		5MHz < f <sub>RF</sub> ≤ 1GHz		0.33	0.53	
		1GHz < f <sub>RF</sub> ≤ 2GHz [0]		0.36	0.56 <sup>[a]</sup>	
Insertion Loss	п	2GHz < f <sub>RF</sub> ≤ 3GHz		0.40		חר
(RFC to RF1, RF2)	IL	3GHz < f <sub>RF</sub> ≤ 6GHz		0.45		dB
		6GHz < f <sub>RF</sub> ≤ 8GHz		0.55		
		8GHz < f <sub>RF</sub> ≤ 9GHz		0.65		
		9GHz < f <sub>RF</sub> ≤ 10GHz		0.80		
		5MHz < f <sub>RF</sub> ≤ 1GHz	43	48		
		1GHz < f <sub>RF</sub> ≤ 2GHz	36	42		
Isolation	ISO1	2GHz < f <sub>RF</sub> ≤ 3GHz	31	37		- dB
(RFC to RF1, RF2)		3GHz < f <sub>RF</sub> ≤ 6GHz		27		
		6GHz < f <sub>RF</sub> ≤ 8GHz		22		
		8GHz < f <sub>RF</sub> ≤ 10GHz		18		
		5MHz < f <sub>RF</sub> ≤ 1GHz	40	45		
		1GHz < f <sub>RF</sub> ≤ 2GHz	33	38		
Isolation	ISO2	2GHz < f <sub>RF</sub> ≤ 3GHz	29	34		dB
(RF1 to RF2, RF2 to RF1)	1002	$3GHz < f_{RF} \le 6GHz$		26		UB
		6GHz < f <sub>RF</sub> ≤ 8GHz		21		
		8GHz < f <sub>RF</sub> ≤ 10GHz		18		
		5MHz < f <sub>RF</sub> ≤ 1GHz		28		
		1GHz < f <sub>RF</sub> ≤ 2GHz		26		
Deturn Loop (DEC, DE1, DE2)		2GHz < f <sub>RF</sub> ≤ 3GHz		26		
Return Loss (RFC, RF1, RF2) (Insertion loss states)	RL	3GHz < f <sub>RF</sub> ≤ 6GHz		25		dB
		6GHz < f <sub>RF</sub> ≤ 8GHz		23		
		8GHz < f <sub>RF</sub> ≤ 9GHz		18		
		$9GHz < f_{RF} \le 10GHz$		16		

a. Items in min/max columns in **bold italics** are guaranteed by test.

b. Items in min/max columns that are not bold italics are guaranteed by design characterization.

c. Minimum or maximum specification guaranteed by test at 2GHz and by design characterization over the whole frequency range.



## **Electrical Characteristics**

#### Table 7. Electrical Characteristics - 50Ω SPECIFICATION

See F2976  $50\Omega$  Application Circuit. Specifications apply when operated with  $V_{CC}$  = +3.3V,  $T_{EP}$  = +25°C.  $Z_S$  =  $Z_L$  =  $50\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units	
		f <sub>RF</sub> = 2.4GHz		40			
Input 0.1dB Compression [6]	P0.1dB	f <sub>RF</sub> = 6.0GHz		40		dBm	
		f <sub>RF</sub> = 8.0GHz		40			
Input IP3 (RF1, RF2 to RFC)	IIP3	$f_{RF}$ = 2.4GHz IIP3 $P_{IN}$ = +24dBm/tone 100MHz spacing		77		dBm	
Input IP2	IIDO	$f_1$ = 700MHz $f_2$ = 1.7GHz $P_{IN}$ = +24dBm/tone Measure 2.4GHz product		125		dDoo	
(RF1, RF2 to RFC)	IIP2	$\begin{aligned} f_1 &= 2.4 \text{GHz} \\ f_2 &= 3.5 \text{GHz} \\ P_{\text{IN}} &= +24 \text{dBm/tone} \\ \text{Measure 5.9GHz product} \end{aligned}$		120		- dBm	
Second Harmonic	H2	f <sub>IN</sub> = 2.4GHz, P <sub>IN</sub> = +24dBm		-100	-90 [b]	dBc	
(RF1, RF2 to RFC)	ПΖ	f <sub>IN</sub> = 5.9GHz, P <sub>IN</sub> = +24dBm		-90	-80	UDC	
Third Harmonic	Н3	$f_{IN} = 2.4GHz, P_{IN} = +24dBm$		-110	-95	dD.a	
(RF1, RF2 to RFC)	пэ	f <sub>IN</sub> = 5.9GHz, P <sub>IN</sub> = +24dBm		-100	-85	dBc	
Spurious Output (No RF Applied)	P <sub>SPUR1</sub>	f <sub>OUT</sub> ≥ 5MHz All unused ports terminated		-133		dBm	
				-120		UDIII	

- a. Items in min/max columns in **bold italics** are guaranteed by test.
- b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
- c. The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum RF operating input power levels.



### **Thermal Characteristics**

### **Table 8. Package Thermal Characteristics**

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	$ heta_{\sf JA}$	102	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	$ heta_{ extsf{JC\_BOT}}$	56	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

## **Typical Operating Conditions (TOCs)**

Unless otherwise noted:

- V<sub>CC</sub> = +3.3V
- LS = HIGH
- $Z_L = Z_S = 75\Omega$
- $Z_L = Z_S = 50\Omega$
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

## Typical Performance Characteristics - $75\Omega$ Performance

Figure 4. RF1 to RFC Insertion Loss

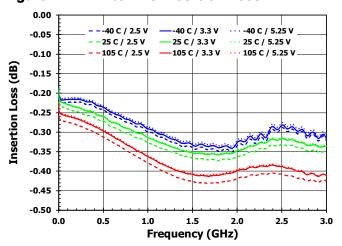


Figure 5. RF2 to RFC Insertion Loss

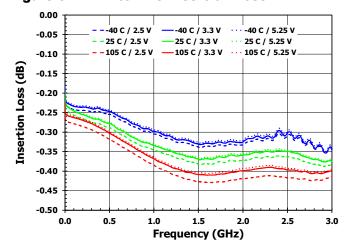


Figure 6. RF1 to RFC Isolation [RF2 On State]

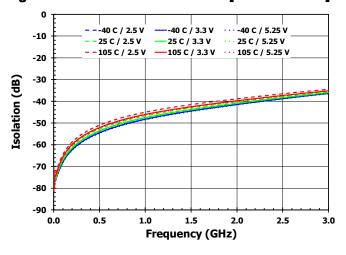


Figure 7. RF2 to RFC Isolation [RF1 On State]

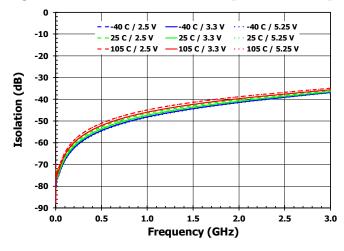


Figure 8. RF1 to RF2 Isolation [RF1 On State]

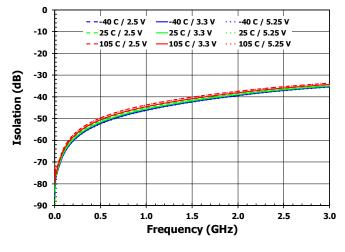
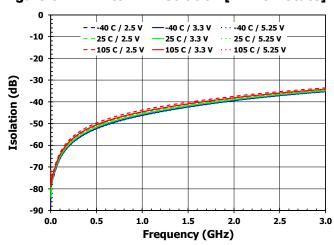


Figure 9. RF1 to RF2 Isolation [RF2 On State]





## Typical Performance Characteristics - $75\Omega$ Performance

Figure 10. RFC Return Loss [RF1 On State]

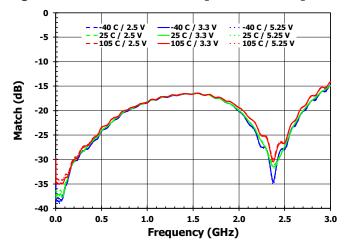


Figure 12. RF1 Return Loss [RF1 On State]

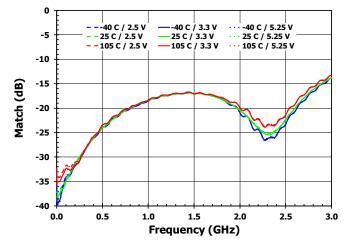


Figure 11. RFC Return Loss [RF2 On State]

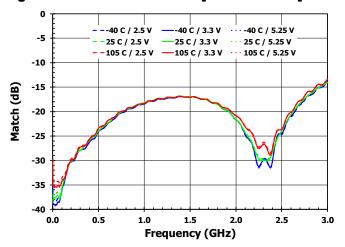
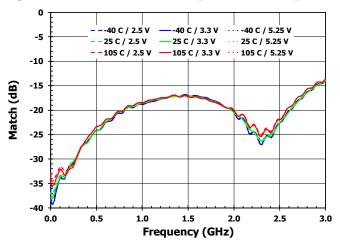


Figure 13. RF2 Return Loss [RF2 On State]



# Typical Performance Characteristics - $\mathbf{50}\Omega$ Performance

Figure 14. RF1 to RFC Insertion Loss

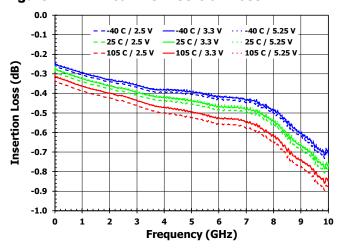


Figure 15. RF2 to RFC Insertion Loss

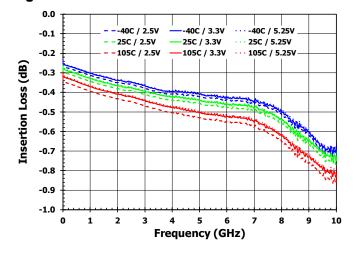


Figure 16. RF1 to RFC Isolation [RF2 On State]

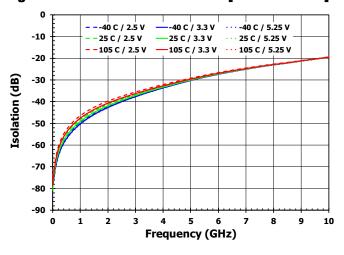


Figure 17. RF2 to RFC Isolation [RF1 On State]

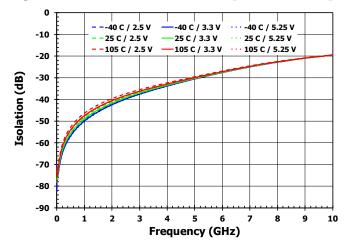


Figure 18. RF1 to RF2 Isolation [RF1 On State]

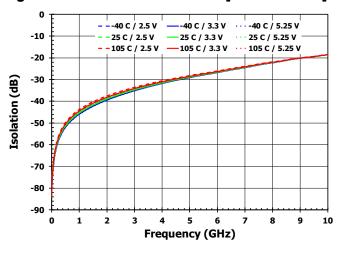
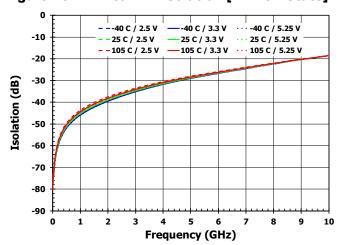


Figure 19. RF1 to RF2 Isolation [RF2 On State]



## Typical Performance Characteristics - $50\Omega$ Performance

Figure 20. RFC Return Loss [RF1 On State]

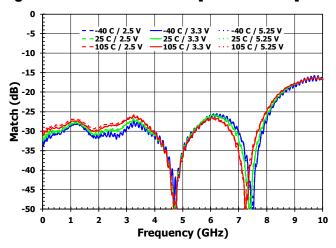


Figure 21. RFC Return Loss [RF2 On State]

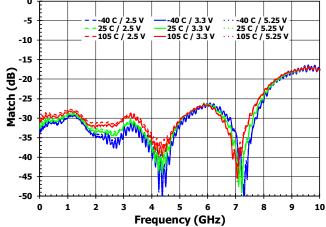


Figure 22. RF1 Return Loss [RF1 On State]

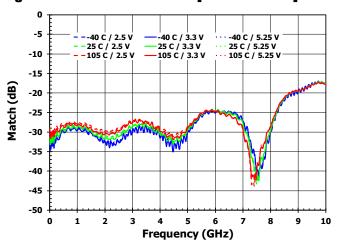


Figure 23. RF2 Return Loss [RF2 On State]

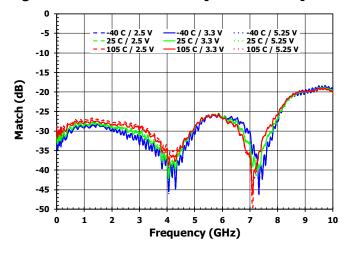


Figure 24. Switching Time [Isolation to Insertion Loss State]

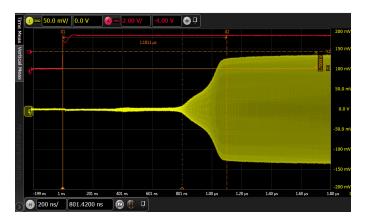
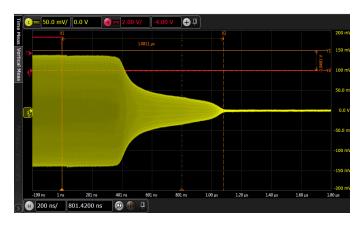


Figure 25. Switching Time [Insertion Loss to Isolation State]





#### **Control Mode**

Table 9. Switch Control Truth Table

V <sub>CTL</sub> (pin 10)	LS (pin 11)	Switch State
HIGH	HIGH	RFC to RF2 Insertion Loss State
LOW	HIGH	RFC to RF1 Insertion Loss State
HIGH	LOW	RFC to RF1 Insertion Loss State
LOW	LOW	RFC to RF2 Insertion Loss State

### **Application Information**

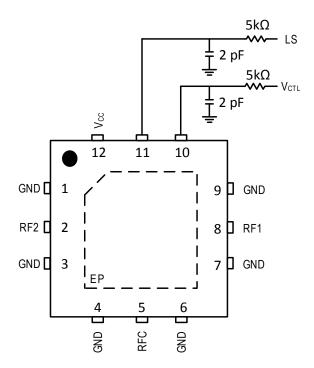
### **Power Supplies**

A common  $V_{CC}$  power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V/20\mu s$ . In addition, all control pins should remain at 0V(+/-0.3V) while the supply voltage ramps up or while it returns to zero.

#### **Control Pin Interface**

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 7 and 8 as shown below.

Figure 26. Control Pin Interface Schematic





## **75** $\Omega$ Evaluation Kit Picture

Figure 27. Top View (75 $\Omega$ )

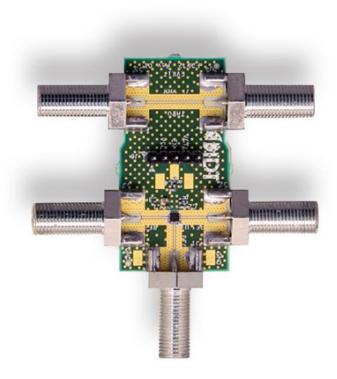
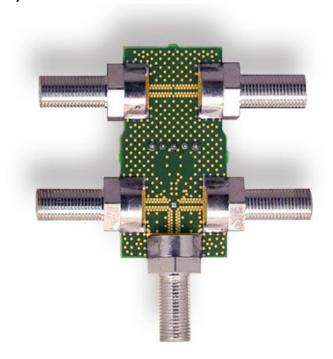


Figure 28. Bottom View (75 $\Omega$ )





## $50\Omega$ Evaluation Kit Picture

Figure 29. Top View (50 $\Omega$ )



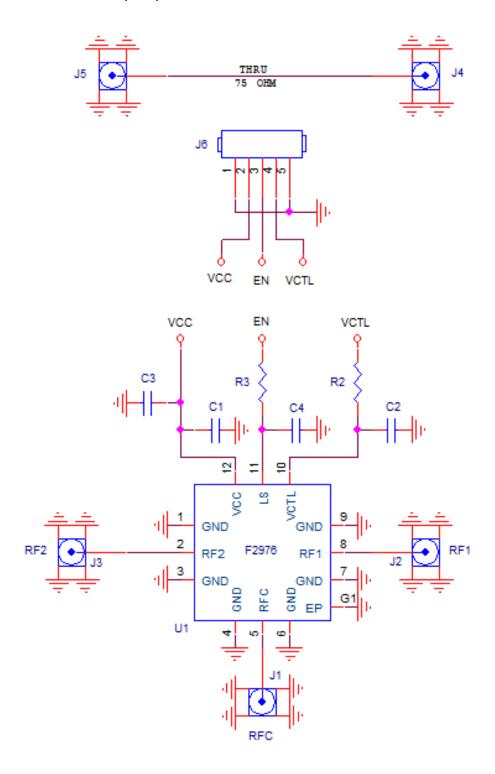
Figure 30. Bottom View (50 $\Omega$ )





# $75\Omega$ Evaluation Kit / Applications Circuit

Figure 31. Electrical Schematic (75 $\Omega$ )

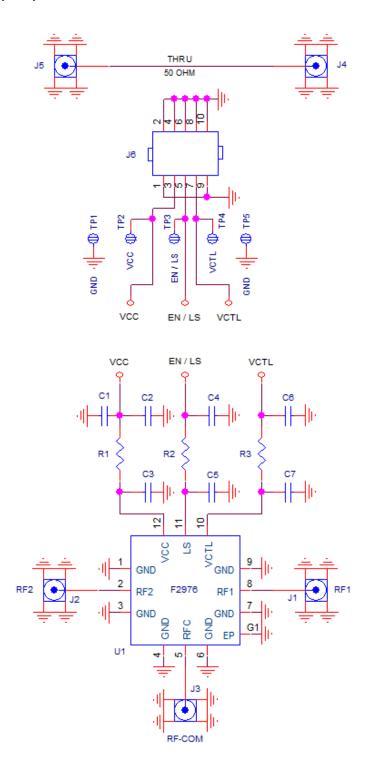


Note: The F2976 75 $\Omega$  EVKit reuses the 75 $\Omega$  PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.



# $50\Omega$ Evaluation Kit / Applications Circuit

Figure 32. Electrical Schematic (50 $\Omega$ )



Note: The F2976  $50\Omega$  EVKit reuses the  $50\Omega$  PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.



Table 10.  $75\Omega$  Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2, C4	2	100pF ±5% 50V, C0G, Ceramic Capacitor (0402)	GRM1555C1H101JA01D	Murata
C3	1	0.01µF ±5% 50V, X7R, Ceramic Capacitor (0603)	GRM188R71H103JA01D	Murata
R2, R3	2	100Ω 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	F-Type Edge Mount	222181	Amphenol RF
J6	1	Conn Header Vert 5x1 Pos Gold	68002-205HLF	Amphenol FCI
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board [a]	F2972 75Ω PCB	IDT

a. The F2976 75 $\Omega$  EVKit reuses the 75 $\Omega$  PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

Table 11.  $50\Omega$  Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C7	0	Not Installed (0402)		
R1– R3	3	0Ω 1/10 W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	Conn Header 10 Pos 0.100" Str 15 Au	68602-210HLF	Amphenol FCI
TP1, TP2, TP3, TP4, TP5	0	Not Installed Test Point Loop		
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board [a]	F2972 50Ω PCB	IDT

a. The F2976  $50\Omega$  EVKit reuses the  $50\Omega$  PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.



## **Evaluation Kit (EVKit) Operation**

### **External Supply Setup**

Set up a V<sub>CC</sub> power supply in the voltage range of 2.5V to 5.25V with the power supply output disabled.

For the 75 $\Omega$  EVKit, connect the disabled Vcc supply connection to J6 pin 2 and GND to J6 pins 1 or 5.

For the 50Ω EVKit, connect the disabled Vcc supply connection to J6 pin 3 and GND to J6 pin 1, 2, 4, 6, 8, 9, or 10.

### **Logic Control Setup**

With the logic control lines disabled set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.

For the 75 $\Omega$  EVKit, connect the disabled logic control lines to J6 EN (pin 3) and V<sub>CTL</sub> (pin 4).

For the  $50\Omega$  EVKit, connect the disabled logic control lines to J6 EN / LS (pin 5) and V<sub>CTL</sub> (pin 7).

See Table 9 for the logic truth table.

#### **Turn On Procedure**

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V<sub>CC</sub> supply.

Enable the logic control signals.

Set the logic settings to achieve the desired Table 9 configuration. Note that external control logic should not be applied without  $V_{CC}$  being present.

#### **Turn Off Procedure**

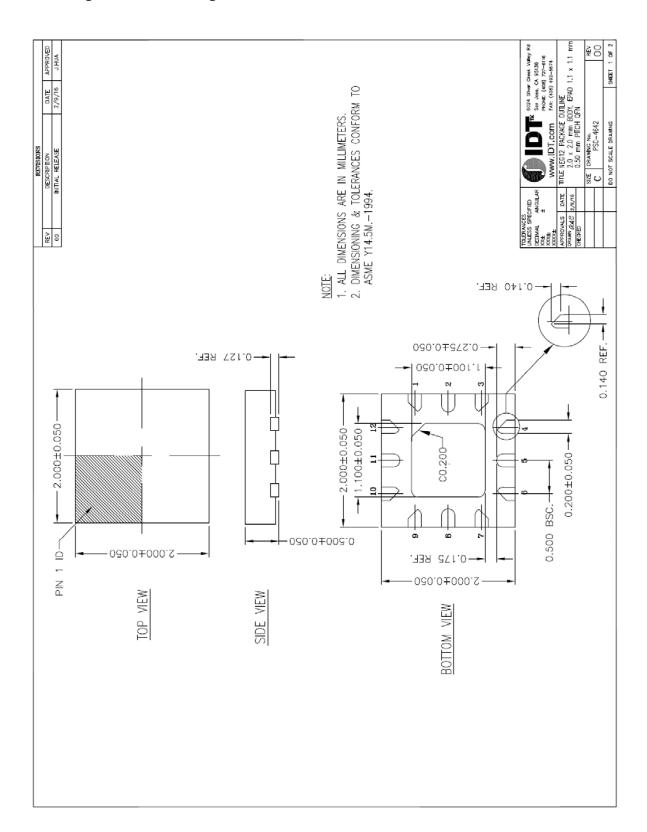
Set the logic control pins to a logic LOW.

Disable the V<sub>CC</sub> supply.



## **Package Drawings**

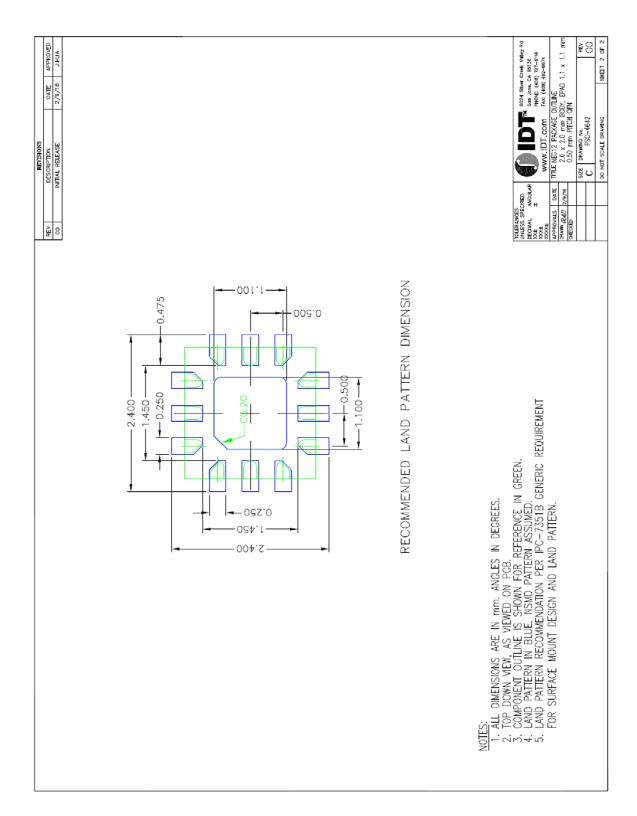
Figure 33. Package Outline Drawing NEG12 PSC-4642





### **Recommended Land Pattern**

Figure 34. Recommended Land Pattern NEG12 PSC-4642





# **Marking Diagram**

2976 YW\*\* Line 1 - 2976 = Abbreviated part number.

Line 2 - Y = Year code.

Line 2 - W = Work week code.

Line 2 - \*\* = Sequential alpha for lot traceability.

# **Ordering Information**

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2976NEGK	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Cut Reel	-40°C to +105°C
F2976NEGK8	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Tape and Reel	-40°C to +105°C
F2976EVBI-75OHM	75Ω Evaluation Board			
F2976EVBI-50OHM	50Ω Evaluation Board			



# **Revision History**

Revision	Revision Date	Description of Change
Rev O	2017-Apr-19	Initial Release

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ADL5725-EVALZ 106815-HMC441LM1 EV1HMC1018ALP4 UXN14M9PE MAX2016EVKIT EV1HMC939ALP4 MAX2410EVKIT
MAX2204EVKIT+ EV1HMC8073LP3D SIMSA868-DKL SIMSA868C-DKL SKY65806-636EK1 SKY68020-11EK1 SKY67159-396EK1
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