intersil

DATASHEET

HA-5147

120MHz, Ultra-Low Noise Precision Operational Amplifiers

FN2910
Rev 1.00
November 6, 2015

The HA-5147 operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Intersil D. I. technology and advanced processing techniques, this unique design unites low noise (3.2nV/√Hz) precision instrumentation performance with high speed (35V/µs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (30mV), wide gain bandwidth (120MHz), high open loop gain (1500V/mV) and high CMRR (120dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten.

Features

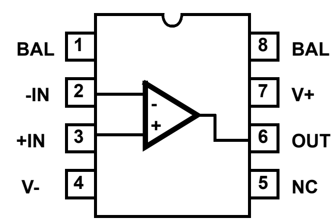
- Slew rate 35V/µs
- Wide gain bandwidth ($A_V \geq 10$) 120MHz
- Low noise . . . . 3.2nV/√Hz at 1kHz
- Low V_{OS} 30µV
- High CMRR 120dB
- High gain 1500V/mV

Applications

- High speed signal conditioners
- Wide bandwidth instrumentation amplifiers
- Low level transducer amplifiers
- Fast, low level voltage comparators
- Highest quality audio preamplifiers
- Pulse/RF amplifiers
- For further design ideas see application note AN553

Pin Configuration

HA-5147 (CERDIP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA7-5147-2	HA7- 5147-2	-55 to +125	8 Ld CerDIP	F8.3A
HA7-5147R5254 (Note 1)	HA7- 5147R5254	-55 to +125	8 Ld CerDIP with Pb-free Hot Solder DIP Lead Finish (SnAgCu)	F8.3A

NOTE:

1. Intersil Pb-free hermetic packaged products employ SnAgCu or Au termination finish, which are RoHS compliant termination finishes and compatible with both SnPb and Pb-free soldering operations. Ceramic dual in-line packaged products (CerDIPs) do contain lead (Pb) in the seal glass and die attach glass materials. However, lead in the glass materials of electronic components are currently exempted per the RoHS directive. Therefore, ceramic dual inline packages with Pb-free termination finish are considered to be RoHS compliant.

Absolute Maximum Ratings T_A = +25°C

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 2) 0.7V
Output Current . . . . Full Short-circuit Protection

Operating Conditions

Temperature Range
HA-5147-2 . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package (Note 3)	135	50

Maximum Junction Temperature (Hermetic Package). . . . .+175°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±15V, $C_L \le$ 50pF, $R_S \le$ 100Ω.

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	30	100	µV
		Full	-	70	300	µV
Average Offset Voltage Drift		Full	-	0.4	1.8	µV/°C
Bias Current		25	-	15	80	nA
		Full	-	35	150	nA
Offset Current		25	-	12	75	nA
		Full	-	30	135	nA
Common Mode Range		Full	±10.3	±11.5	-	V
Differential Input Resistance (Note 4)		25	0.8	4	-	MΩ
Input Noise Voltage (Note 5)	0.1Hz to 10Hz	25	-	0.09	0.25	μV_{P-P}
Input Noise Voltage Density (Note 6)	f = 10Hz	25	-	3.8	8.0	$nV/\sqrt{Hz}$
	f = 100Hz		-	3.3	4.5	$nV/\sqrt{Hz}$
	f = 1000Hz		-	3.2	3.8	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 6)	f = 10Hz	25	-	1.7	-	$pA/\sqrt{Hz}$
	f = 100Hz		-	1.0	-	$pA/\sqrt{Hz}$
	f = 1000Hz		-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Minimum Stable Gain		25	10	-	-	V/V
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	700	1500	-	V/mV
		Full	300	800	-	V/mV
Common Mode Rejection Ratio	V_{CM} = ±10V	Full	100	120	-	dB
Gain-bandwidth Product	f = 10kHz	25	120	140	-	MHz
	f = 1MHz		-	120	-	MHz

Electrical Specifications V_{SUPPLY} = ±15V, $C_L \leq$ 50pF, $R_S \leq$ 100Ω. (Continued)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 600Ω	25	±10.0	±11.5	-	V
	R_L = 2kΩ	Full	±11.4	±13.5	-	V
Full Power Bandwidth (Note 7)		25	445	500	-	kHz
Output Resistance	Open Loop	25	-	70	-	Ω
Output Current		25	16.5	25	-	mA
TRANSIENT RESPONSE (Note 8)						
Rise Time		25	-	22	50	ns
Slew Rate	V_{OUT} = ±3V	25	28	35	-	V/µs
Settling Time	Note 9	25	-	400	-	ns
Overshoot		25	-	20	40	%
POWER SUPPLY CHARACTERISTICS						
Supply Current		25	-	3.5	-	mA
		Full	-	-	4.0	mA
Power Supply Rejection Ratio	V_S = ±4V to ±18V	Full	-	16	51	µV/V

NOTES:

4. This parameter value is based upon design calculations.
5. Refer to Typical Performance section starting on page 6.
6. The limits for this parameter are established based on lab characterization, and reflect lot-to-lot variation.
7. Full power bandwidth established based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
8. Refer to Test Circuits section on page 4.
9. Settling time is specified to 0.1% of final value for a 10V output step and A_V = -10.

Test Circuits and Waveforms

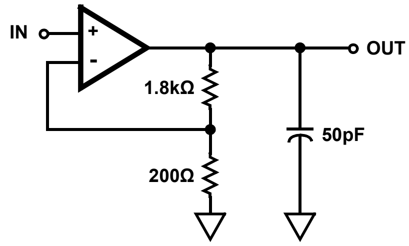
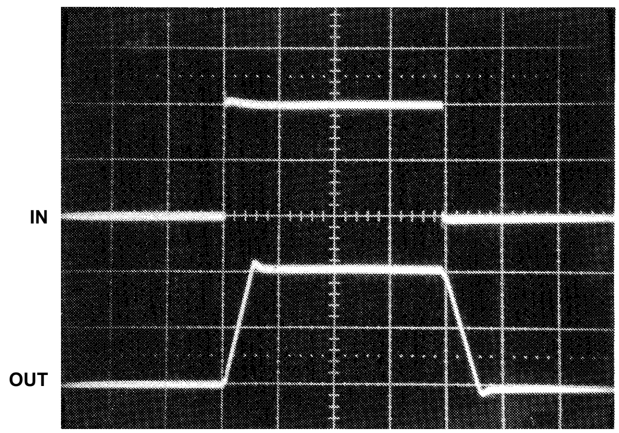
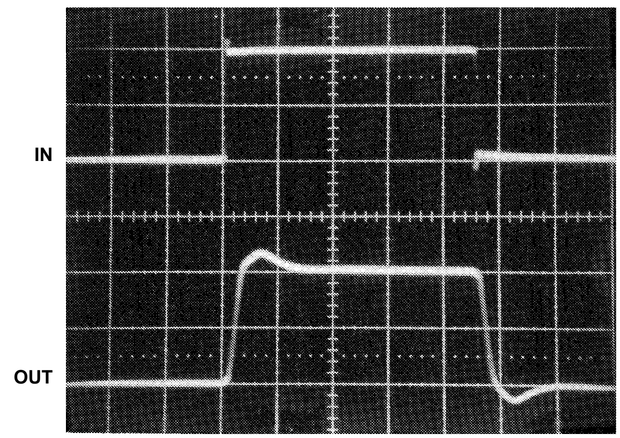


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



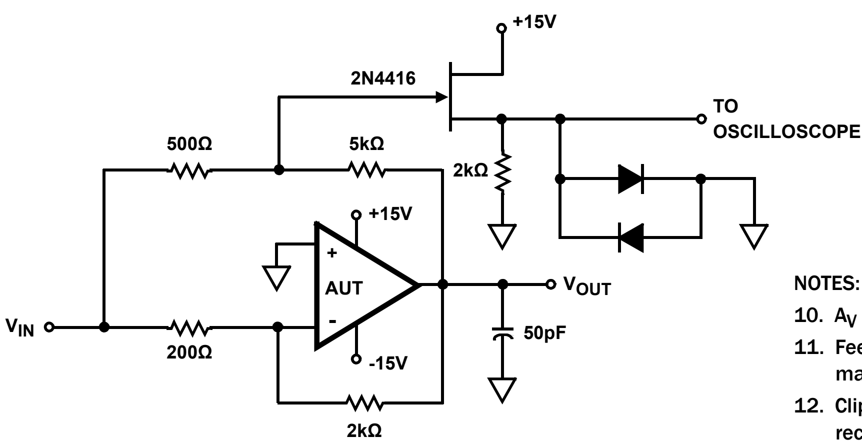
Vertical Scale: Input = 0.5V/DIV
Output = 5V/DIV
Horizontal Scale: 500ns/DIV

FIGURE 2. LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/DIV
Output = 100mV/DIV
Horizontal Scale: 100ns/DIV

FIGURE 3. SMALL SIGNAL RESPONSE

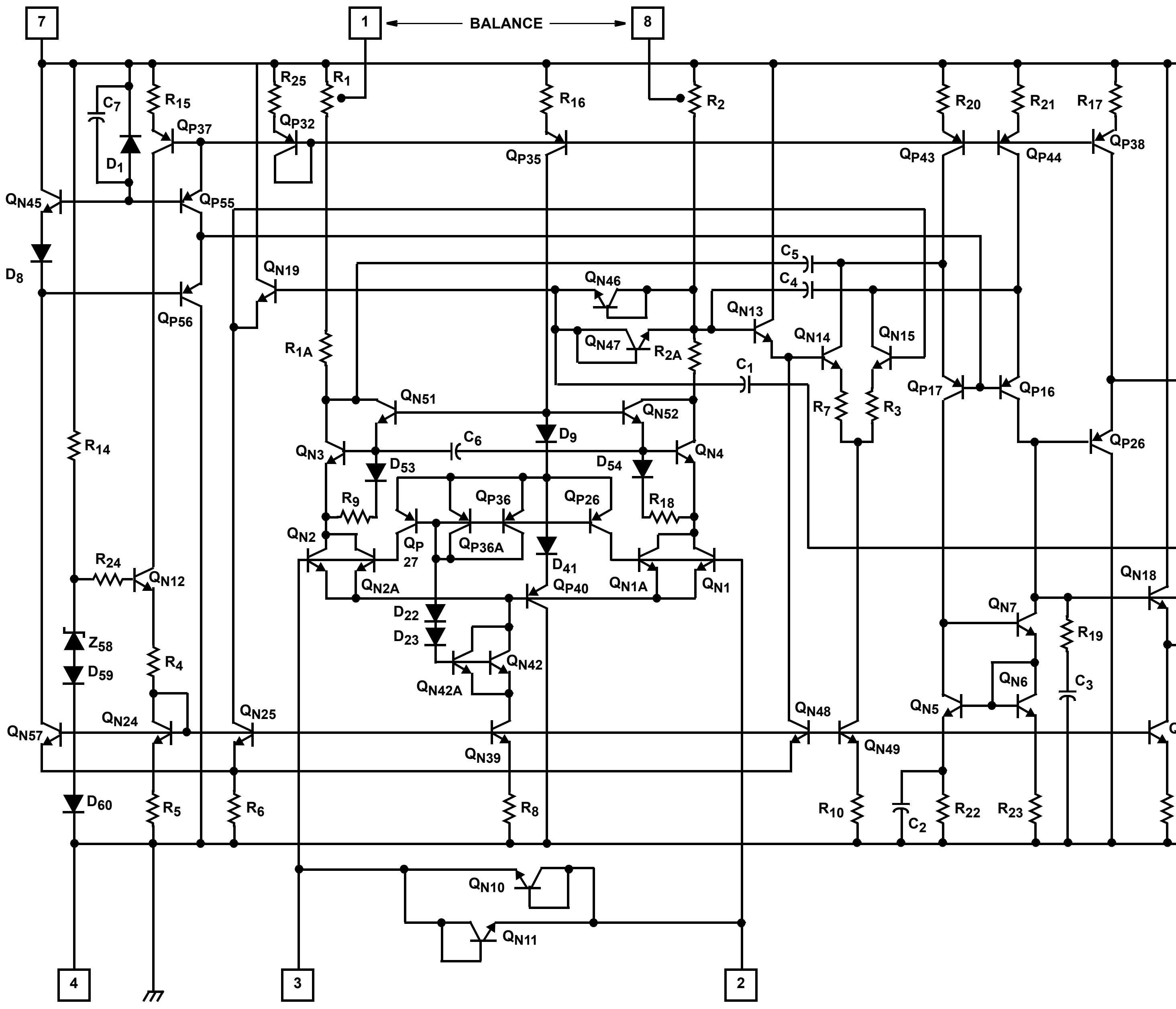


NOTES:

10. $A_V = -10$.
11. Feedback and summing resistors should be 0.1% matched.
12. Clipping diodes are optional. HP5082-2810 recommended.

FIGURE 4. SETTLING TIME TEST CIRCUIT

Schematic Diagram



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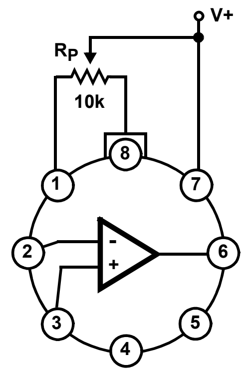
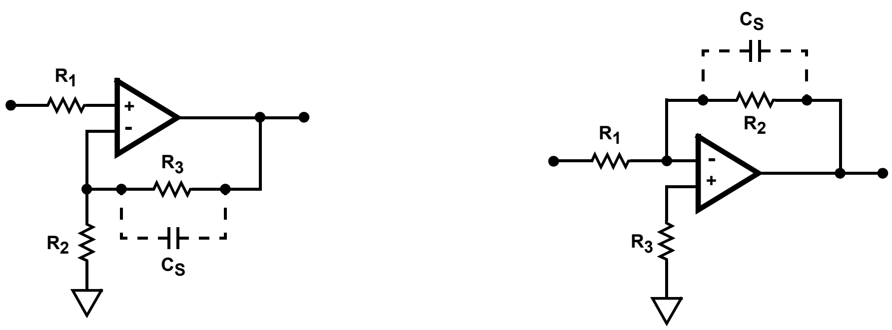
Application Information



NOTE: Tested offset adjustment range is |V_{OS} +1mV| minimum referred to output. Typical range is ±4mV with R_P = 10kΩ.

FIGURE 5. SUGGESTED OFFSET VOLTAGE ADJUSTMENT



NOTE: Low resistances are preferred for low noise applications as a 1kΩ resistor has 4nV/√Hz of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

FIGURE 6. SUGGESTED STABILITY CIRCUITS

Typical Performance Curves

T_A = +25°C, V_{SUPPLY} = ±15V, unless otherwise specified.

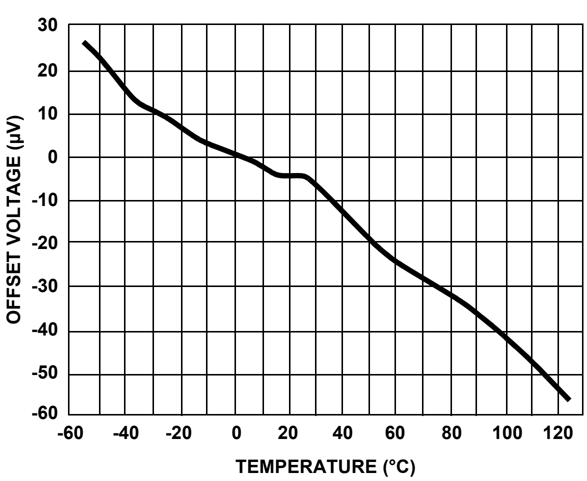


FIGURE 7. TYPICAL OFFSET VOLTAGE vs TEMPERATURE

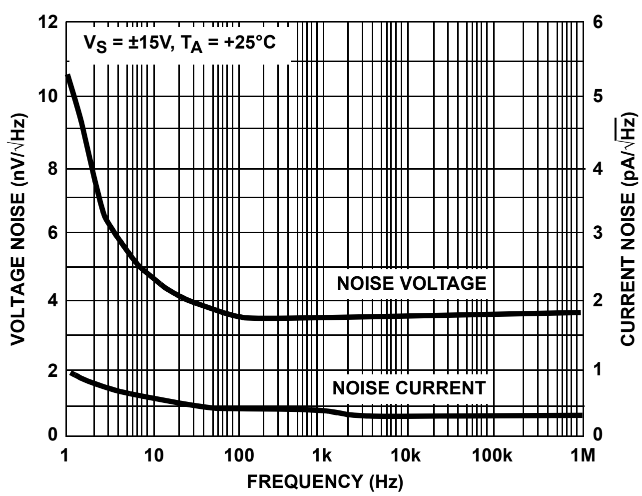


FIGURE 8. NOISE CHARACTERISTICS

Typical Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, unless otherwise specified. (Continued)

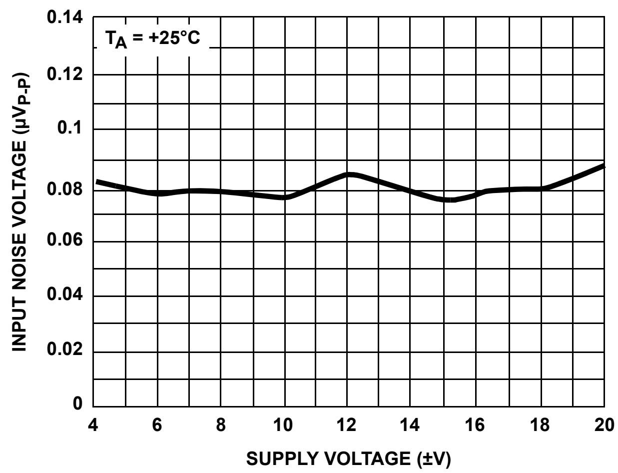


FIGURE 9. NOISE vs SUPPLY VOLTAGE

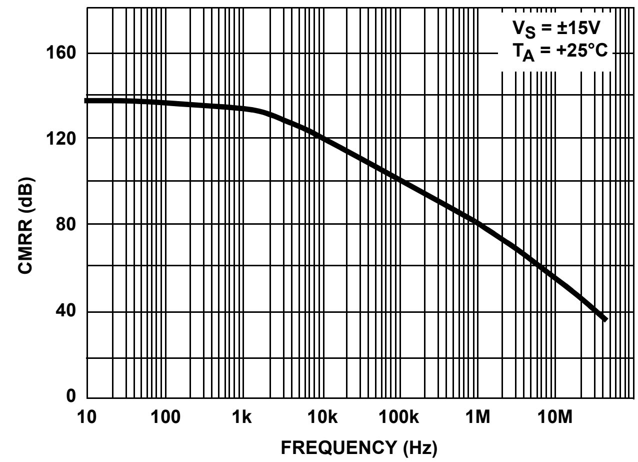


FIGURE 10. CMRR vs FREQUENCY

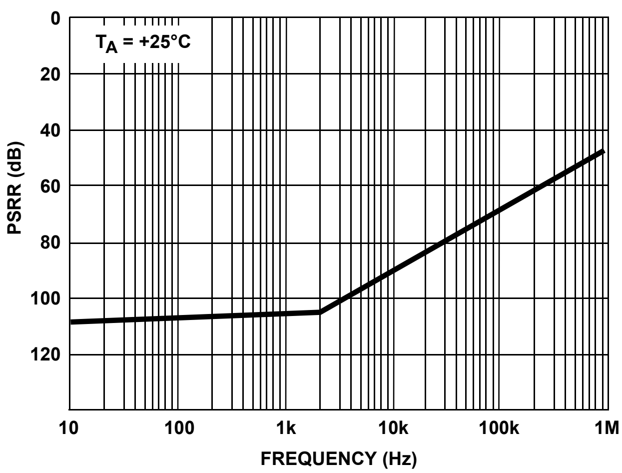


FIGURE 11. PSRR vs FREQUENCY

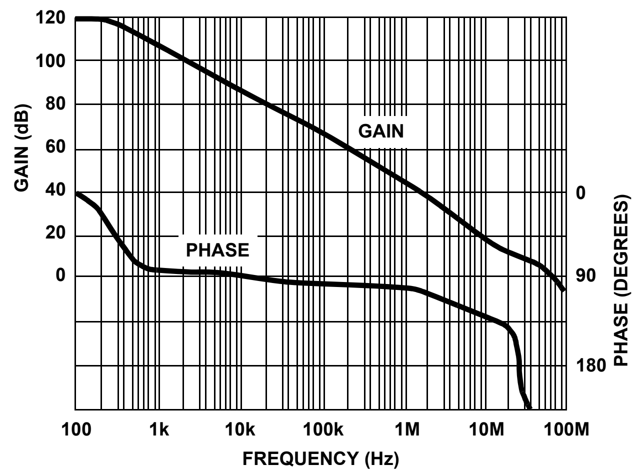


FIGURE 12. OPEN LOOP GAIN AND PHASE vs FREQUENCY

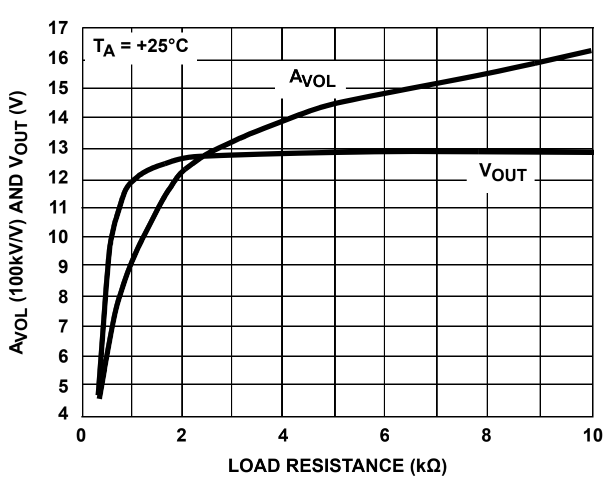


FIGURE 13. A_{VOL} AND V_{OUT} vs LOAD RESISTANCE

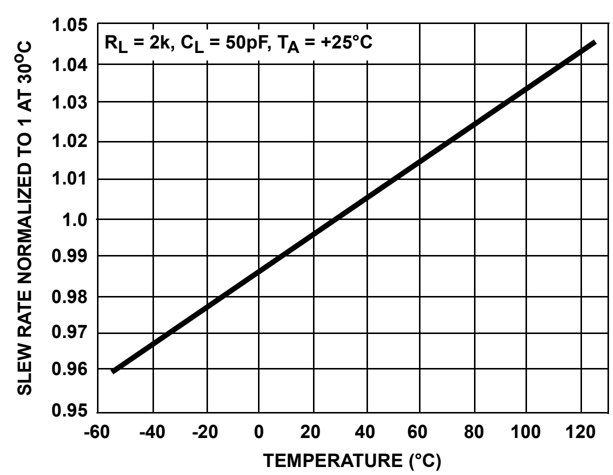


FIGURE 14. NORMALIZED SLEW RATE vs TEMPERATURE

Typical Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, unless otherwise specified. (Continued)

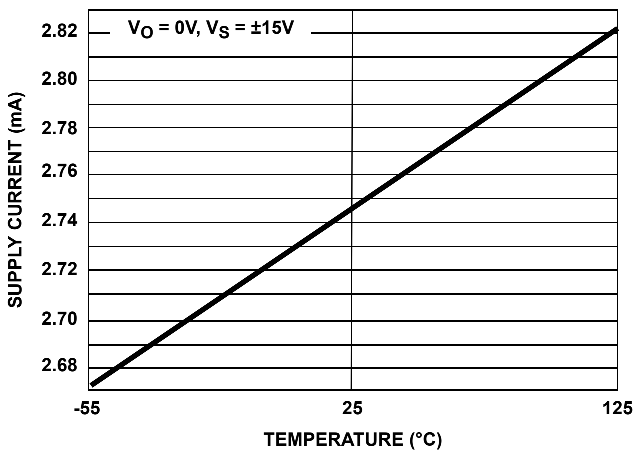


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

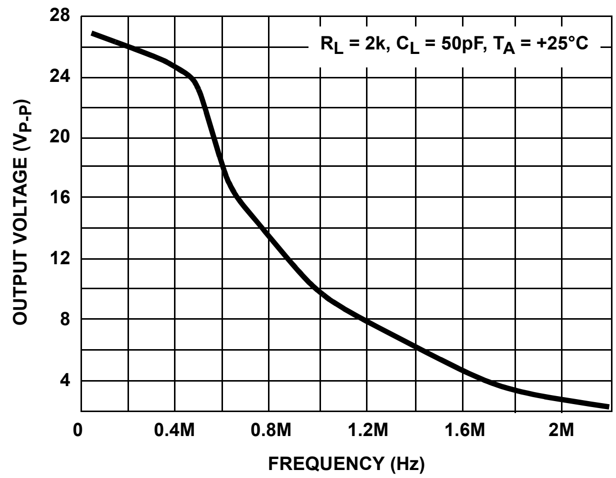


FIGURE 16. V_{OUT} MAX (UNDISTORTED SINEWAVE OUTPUT) vs FREQUENCY

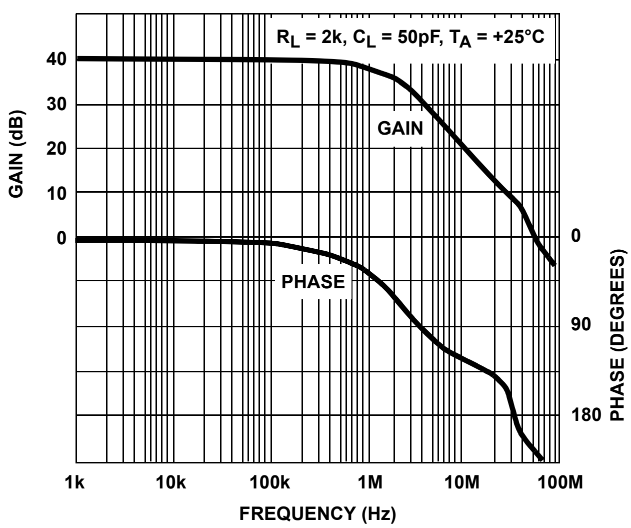
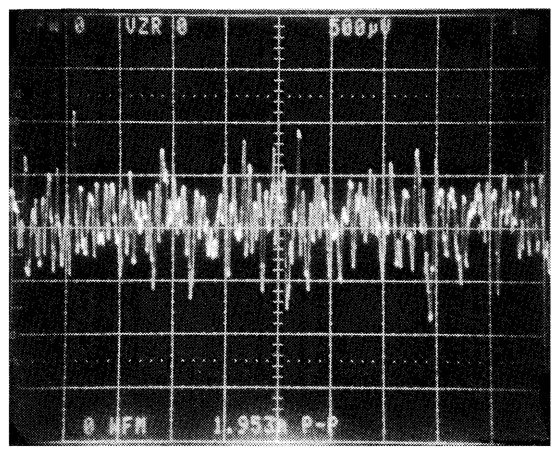


FIGURE 17. CLOSED LOOP GAIN AND PHASE vs FREQUENCY



A_{CL} = 25,000V/V; E_N = 0.08µV_{P-P} RTI
Horizontal Scale = 1s/DIV; Vertical Scale = 0.02µV/DIV

FIGURE 18. PEAK-TO-PEAK NOISE VOLTAGE (0.1Hz TO 10Hz)

Die Characteristics

DIE DIMENSIONS:

104 mils x 65 mils x 19 mils
2650µm x 1650µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (POWERED UP):

V-

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

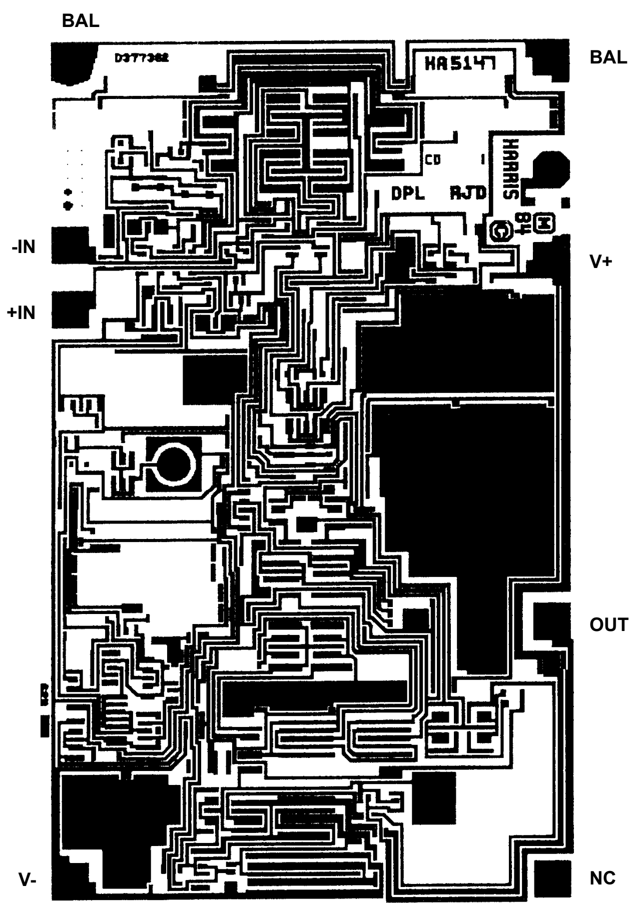
63

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5147



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 6, 2015	FN2910.10	Updated to newest standards and layout. Figure 18 page 8. Changed Vertical Scale = 0.002µV/Div to: Vertical Scale = 0.02µV/DIV Added Revision History and About Intersil sections to page 10

About Intersil

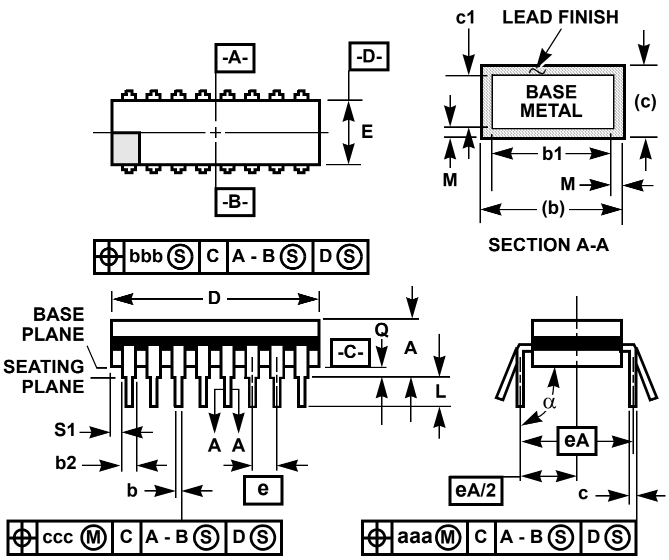
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH