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# **HAF2017(L), HAF2017(S)**

# Silicon N Channel Power MOS FET Power Switching

REJ03G0234-0200Z (Previous ADE-208-1637 (Z)) Rev.2.00 Apr.13.2004

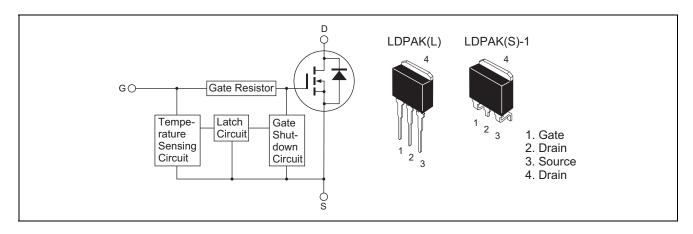
#### **Descriptions**

This FET has the over temperature shutdown capability sensing the junction temperature. This FET has the built-in over temperature shutdown circuit in the gate area. And this circuit operation to shutdown the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

#### **Features**

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shutdown circuit
- Latch type shutdown operation (Need 0 voltage recovery)

#### **Outline**



# HAF2017(L), HAF2017(S)

# **Absolute Maximum Ratings**

 $(Ta = 25^{\circ}C)$ 

Item	Symbol	Rating	Unit	
Drain to source voltage	$V_{DSS}$	60	V	
Gate to source voltage	$V_{GSS}$	16	V	
Gate to source voltage	$V_{GSS}$	-2.5	V	
Drain current	I <sub>D</sub>	20	А	
Drain peak current	I <sub>D</sub> (pulse) Note1	40	А	
Body-drain diode reverse drain current	$I_{DR}$	20	А	
Channel dissipation	Pch <sup>Note2</sup>	50	W	
Channel temperature	Tch	150	°C	
Storage temperature	Tstg	-55 to +150	°C	

Notes: 1. PW  $\leq$  10 $\mu$ s, duty cycle  $\leq$  1%

2. Value at Tch = 25°C

# **Typical Operation Characteristics**

 $(Ta = 25^{\circ}C)$ 

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	3.5	_	_	V	
Input voltage	$V_{IL}$	_	_	1.2	V	
Input current (Gate non shut down)	I <sub>IH1</sub>	_	_	100	μA	Vi = 8V, V <sub>DS</sub> =0
Input current (Gate non shut down)	I <sub>IH2</sub>	_	_	50	μA	Vi = 3.5V, V <sub>DS</sub> =0
Input current (Gate non shut down)	I <sub>IL</sub>	_	_	1	μA	Vi = 1.2V, V <sub>DS</sub> =0
Input current (Gate shut down)	I <sub>IH(sd)1</sub>	_	0.8	_	mA	Vi = 8V, V <sub>DS</sub> =0
Input current (Gate shut down)	I <sub>IH(sd)2</sub>	_	0.35	_	mA	Vi = 3.5V, V <sub>DS</sub> =0
Shutdown temperature	Tsd	_	175	_	°C	Channel temperature
Gate operation voltage	V <sub>OP</sub>	3.5	_	12	V	



#### **Electrical Characteristics**

 $(Ta = 25^{\circ}C)$ 

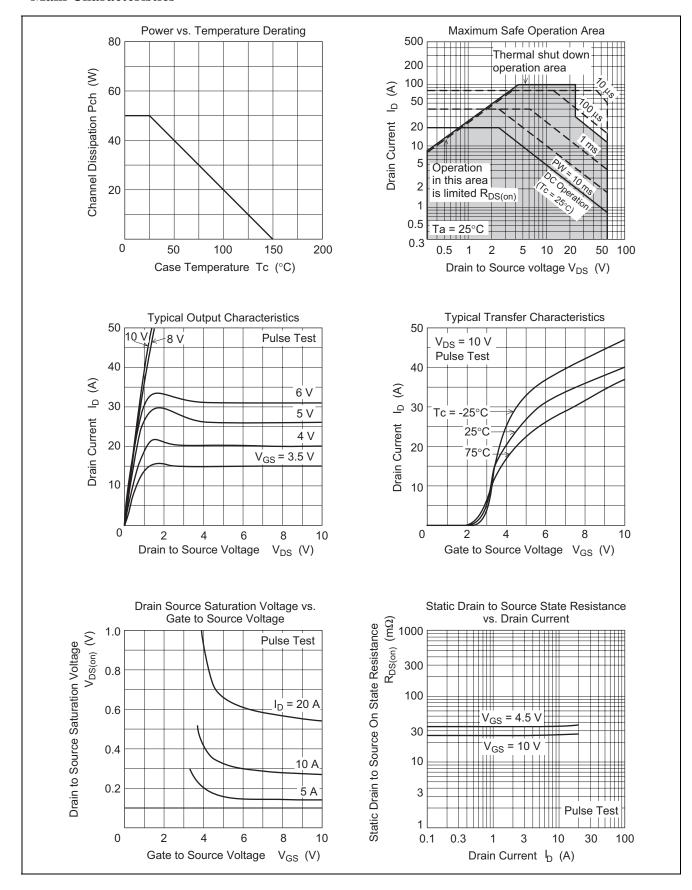
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Darin current	I <sub>D1</sub>	1	_	_	Α	$V_{GS} = 3.5 \text{ V}, V_{DS} = 2 \text{ V}$
Darin current	I <sub>D2</sub>	_	_	10	mA	V <sub>GS</sub> = 1.2 V, V <sub>DS</sub> = 2 V
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown	$V_{(BR)GSS}$	16	_	_	V	$I_G = 800 \ \mu A, \ V_{DS} = 0$
voltage	V <sub>(BR)GSS</sub>	-2.5	_	_	V	$I_G = -100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I <sub>GSS1</sub>	_	_	100	μΑ	V <sub>GS</sub> = 8 V, V <sub>DS</sub> =0
	I <sub>GSS2</sub>	_	_	50	μΑ	$V_{GS} = 3.5 \text{ V}, V_{DS} = 0$
	I <sub>GSS3</sub>	_	_	1	μΑ	V <sub>GS</sub> = 1.2 V, V <sub>DS</sub> =0
	I <sub>GSS4</sub>	_	_	-100	μΑ	$V_{GS} = -2.4 \text{ V}, V_{DS} = 0$
Input current (shut down)	I <sub>GS(OP)1</sub>	_	0.8	_	mA	V <sub>GS</sub> = 8 V, V <sub>DS</sub> =0
	I <sub>GS(OP)2</sub>	_	0.35	_	mA	V <sub>GS</sub> = 3.5 V, V <sub>DS</sub> =0
Zero gate voltage drain current	I <sub>DSS</sub>	_	_	10	μΑ	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	1.4	_	2.6	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward transfer admittance	y <sub>fs</sub>	6	21	_	S	I <sub>D</sub> =10 A, V <sub>DS</sub> =10 V <sup>Note3</sup>
Static drain to source on state	R <sub>DS(on)</sub>	_	35	53	mΩ	$I_D = 10 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note3}}$
resistance	R <sub>DS(on)</sub>	_	27	43	mΩ	$I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note3}}$
Output capacitance	Coss	_	460	_	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$
Turn-on delay time	td(on)	_	8.7	_	μs	$V_{GS}$ = 5 V, $I_{D}$ = 10 A, $R_{L}$ = 3 $\Omega$
Rise time	tr	_	44.6	_	μs	
Turn-off delay time	td(off)	_	2	_	μs	
Fall time	tf	_	2.6	_	μs	
Body-drain diode forward voltage	$V_{DF}$	_	0.9	_	V	$I_F = 20A, V_{GS} = 0$
Body-drain diode reverse recovery	trr	_	120	_	ns	$I_F = 20 \text{ A}, V_{GS} = 0,$
time						$diF/dt = 50 A/\mu s$
Over load shut down operation	t <sub>os1</sub>	_	0.97	_	ms	$V_{GS} = 5 \text{ V}, V_{DD} = 16 \text{ V}$
time <sup>Note4</sup>	t <sub>os2</sub>		0.57		ms	$V_{GS} = 5 \text{ V}, V_{DD} = 24 \text{ V}$

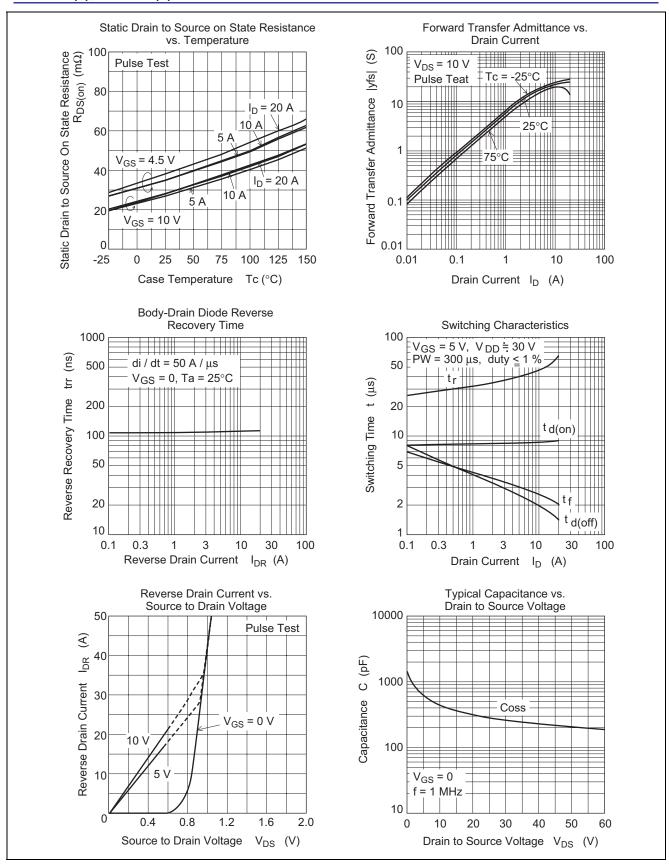
Notes: 3. Pulse test

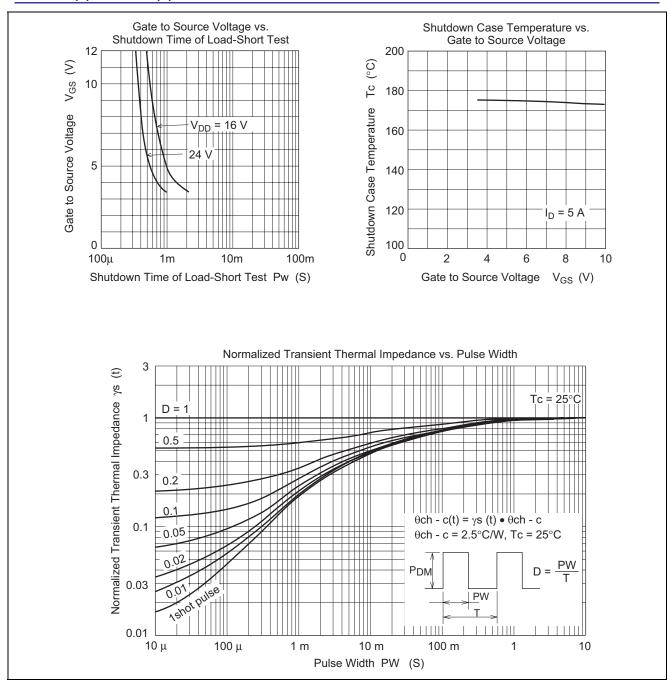


<sup>4.</sup> Include the time shift based on increasing of channel temperature when operate under over load condition.

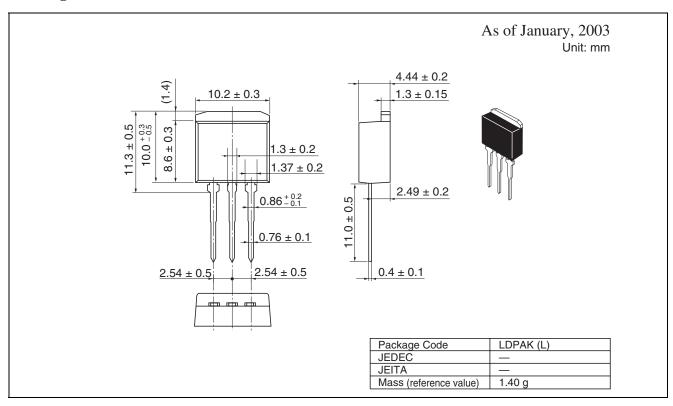
#### **Main Characteristics**

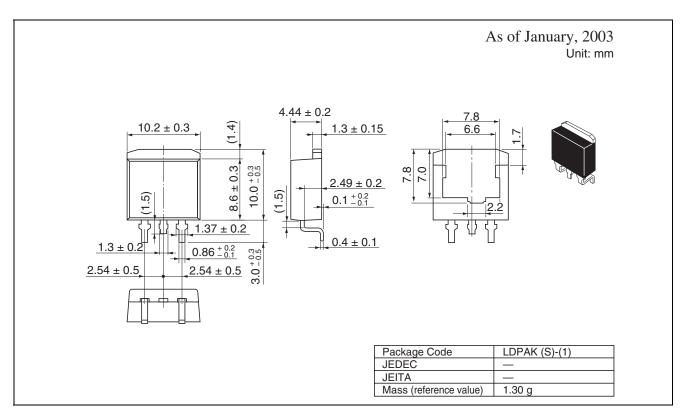






#### **Package Dimensions**





# HAF2017(L), HAF2017(S)

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