NEC

MOS INTEGRATED CIRCUIT
μPD78F0034

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F0034 is a product of the μPD780034 Subseries in the 78K/0 Series and equivalent to the μPD780034 with a flash memory in place of internal ROM.

Because this device can be programmed without being removed from the substrate, it is suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD780024, 780024Y, 780034, 780034Y Subseries User's Manual: to be published soon
78K/0 Series User's Manual Instruction: IEU-1372

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory : 32 Kbytes
- Internal high-speed RAM : 1024 bytes[Note]
- Operable with the same power supply voltage as that of mask ROM version (V_{DD} = 1.8 to 5.5 V)

Note The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0034 AND MASK ROM VERSIONS.**

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0034CW	64-pin plastic shrink DIP (750 mil)	Flash memory
μPD78F0034GC-AB8	64-pin plastic QFP (14 × 14 mm)	Flash memory
μPD78F0034GK-8A8[Note]	64-pin plastic LQFP (12 × 12 mm)	Flash memory

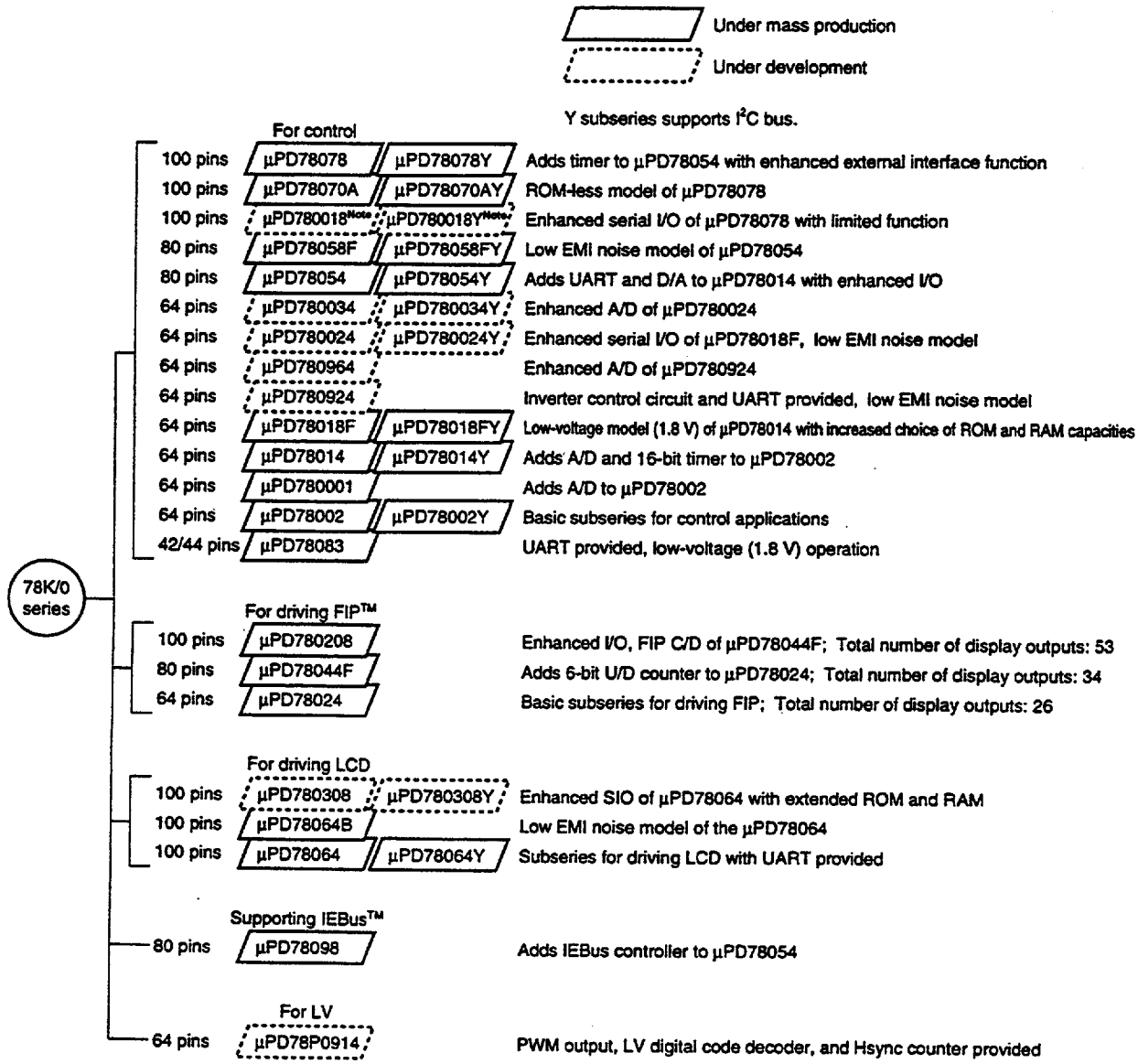
Note Under planning

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Document No. U11993EJ1V0PM00 (1st edition)
Date Published January 1997 N
Printed in Japan

78K/0 SERIES DEVELOPMENT

The products in the 78K/0 series are listed below. The names enclosed in boxes are subseries names.



Note Under planning

The following lists the main functional differences.

Subseries \ Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	VDD MIN. Value	External Expansion
For control	μPD78078	32 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78070A	—									61	2.7 V	
	μPD780018	48 K to 60 K							—	2 ch (Time division 3-wire: 1 ch)	88		
	μPD780034	8 K to 32 K	2 ch				—	8 ch		3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD780964		3 ch	Note	—		—	8ch		2 ch (UART: 2 ch)	47	2.7 V	
	μPD780924						8 ch	—					
	μPD78058F	48 K to 60 K	2 ch						2 ch	3 ch (UART: 1 ch)	69		
	μPD78054	16 K to 60 K										2.0 V	
	μPD78018F	8 K to 60 K							—	2 ch	53	1.8 V	
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		—	—					1 ch	39		—
	μPD78002	8 K to 16 K			1 ch		—				53		√
	μPD78083				—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
For FIP driving	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD78044F	16 K to 40 K									68		
	μPD78024	24 K to 32 K									54		
For LCD driving	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	1.8 V	—
	μPD78064B	32 K								2 ch (UART: 1 ch)		2.0 V	
	μPD78064	16 K to 32 K											
For IEBus	μPD78098	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	√
For LV	μPD78P0914	32 K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	√

Note 10-bit timer: 1 channel

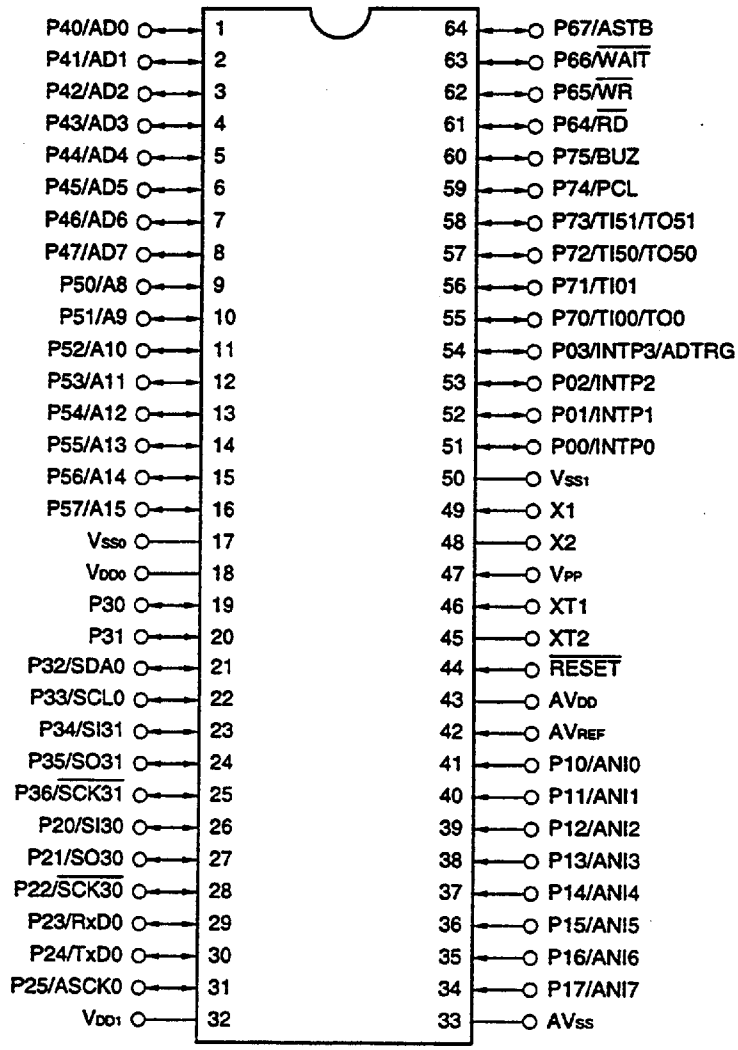
OVERVIEW OF FUNCTION

Item		Function
Internal memory	Flash memory	32 Kbytes[Note]
	High-speed RAM	1024 bytes[Note]
Memory space		64 Kbytes
General-purpose registers		8 bits x 32 registers (8 bits x 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time cycle modification function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)
	When subsystem clock selected	122 μs (at 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiplication/division (8 bits x 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports		Total : 51 • CMOS input : 8 • CMOS I/O : 39 • N-ch open drain I/O (5-V resistance) : 4
A/D converter		• 10-bit resolution x 8 channels • Operable over a wide power supply voltage range: AV_{DD} = 1.8 to 5.5 V
Serial interface		• UART mode : 1 channel • 3-wire serial I/O mode : 2 channels
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (8-bit PWM output capable: 2)
Clock output		131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (main system clock: at 8.38-MHz operation) 32.768 kHz (subsystem clock: at 32.768-kHz operation)
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (main system clock: at 8.38-MHz operation)
Vectored-interrupt source	Maskable	Internal : 14 External : 4
	Non-maskable	Internal : 1
	Software	1
Test input		Internal : 1 External : 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 x 14 mm) • 64-pin plastic LQFP (12 x 12 mm, Under planning)

Note The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

PIN CONFIGURATION (TOP VIEW)

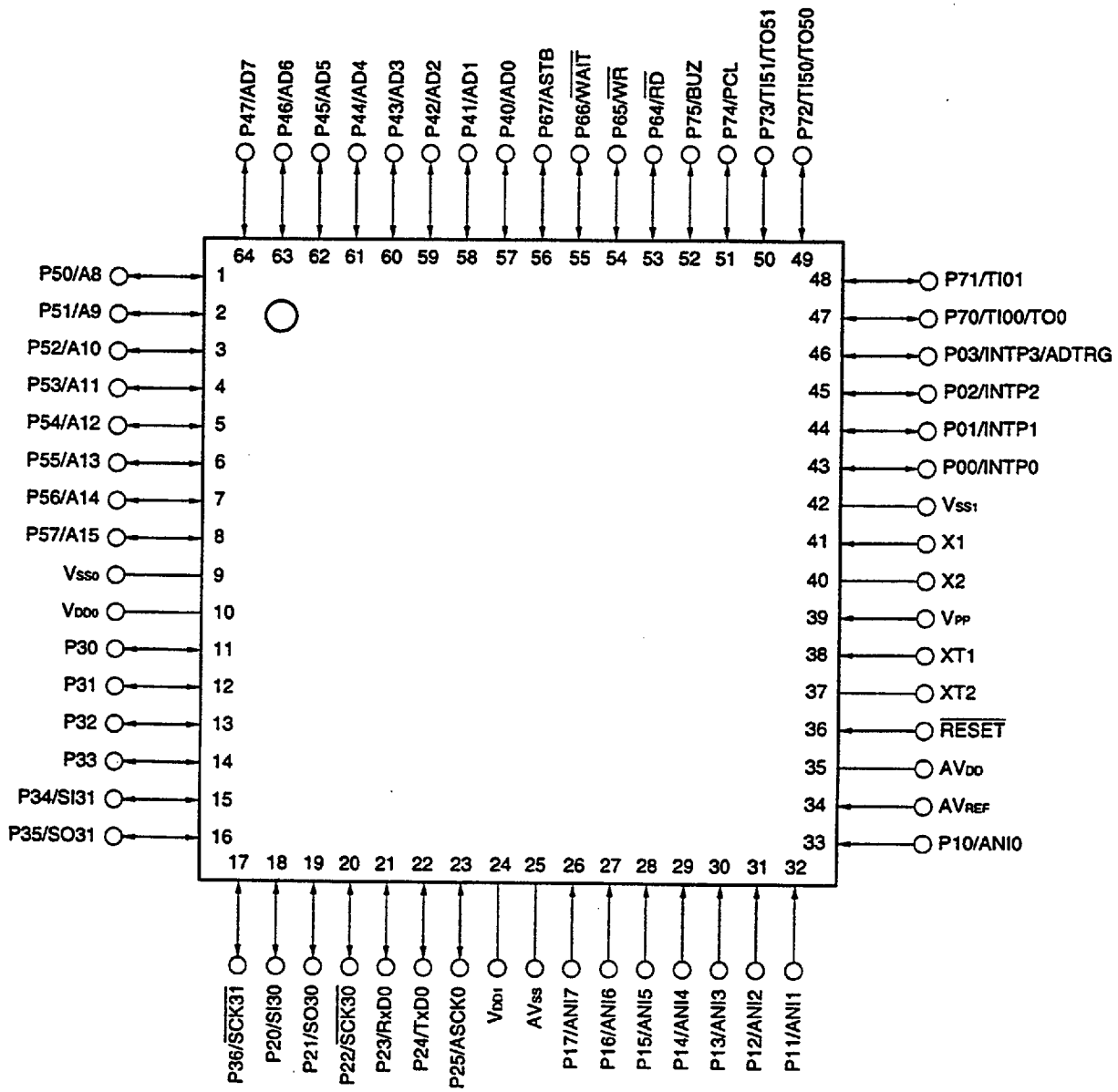
- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD78F0034CW



Cautions
1. **Connect the V_{PP} pin directly to V_{SS0} in normal operation mode.**
2. **Connect the AVss pin to V_{SS0}.**

Remark When the μPD78F0034 is used in application fields that require reduction of the niose generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-Pin Plastic QFP (14 × 14 mm)**
  μPD78F0034GC-AB8
- **64-Pin Plastic LQFP (12 × 12 mm)**
  μPD78F0034GK-8A8[Note]



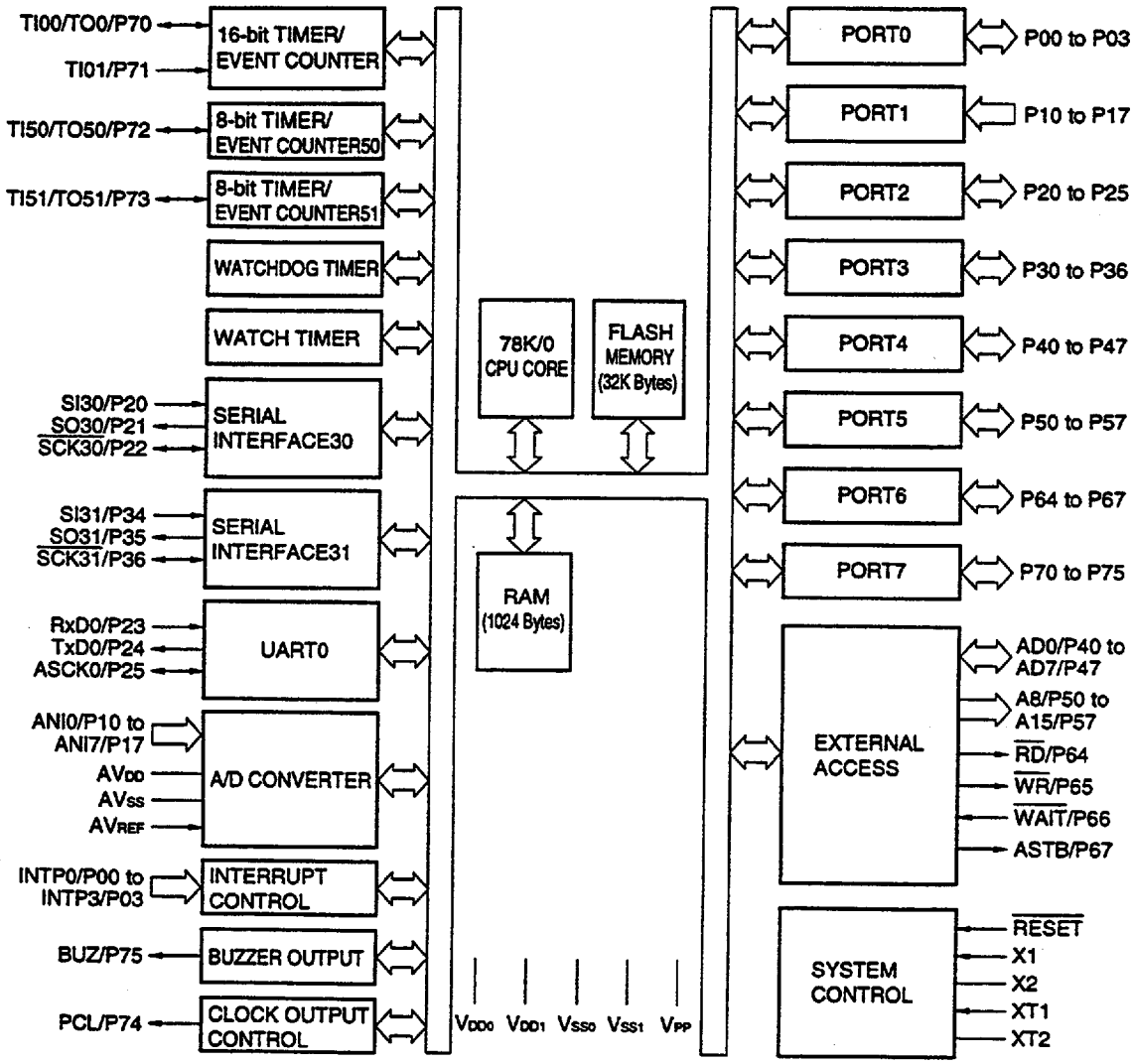
Note Under planning

Cautions 1. **Connect the V_{PP} pin directly to V_{SS0} in normal operation mode.**
2. **Connect the AVss pin to V_{SS0}.**

Remark When the μPD78F0034 is used in application fields that require reduction of the niose generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	P70 to P75	: Port 7
AD0 to AD7	: Address/Data Bus	PCL	: Programmable Clock
ADTRG	: AD Trigger Input	$\overline{RD}$	: Read Strobe
ANI0 to ANI7	: Analog Input	$\overline{RESET}$	: Reset
ASCK0	: Asynchronous Serial Clock	RxD0	: Receive Data
ASTB	: Address Strobe	$\overline{SCK30}$, $\overline{SCK31}$	: Serial Clock
AV_{DD}	: Analog Power Supply	SI30, SI31	: Serial Input
AV_{REF}	: Analog Reference Voltage	SO30, SO31	: Serial Output
AV_{SS}	: Analog Ground	TI00, TI01, TI50, TI51	: Timer Input
BUZ	: Buzzer Clock	TO0, TO50, TO51	: Timer Output
INTP1 to INTP3	: Interrupt from Peripherals	TxD0	: Transmit Data
P00 to P03	: Port 0	V_{DD0}, V_{DD1}	: Power Supply
P10 to P17	: Port 1	V_{PP}	: Programming Power Supply
P20 to P25	: Port 2	V_{SS0}, V_{SS1}	: Ground
P30 to P36	: Port 3	$\overline{WAIT}$	: Wait
P40 to P47	: Port 4	$\overline{WR}$	: Write Strobe
P50 to P57	: Port 5	X1, X2	: Crystal (Main System Clock)
P64 to P67	: Port 6	XT1, XT2	: Crystal (Subsystem Clock)

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0034 AND MASK ROM VERSIONS

The μPD78F0034 is a product provided with a flash memory which enables on-board reading, erasing, and rewriting of programs with device mounted on target system.

The functions of the μPD78F0034 (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0034) and the mask ROM versions (μPD780031, 780032, 780033, and 780034).

Table 1-1. Differences between μPD78F0034 and Mask ROM Versions

Item	μPD78F0034	Mask ROM Versions
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	32 Kbytes	μPD780031 : 8 Kbytes μPD780032 : 16 Kbytes μPD780033 : 24 Kbytes μPD780034 : 32 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD780031 : 512 bytes μPD780032 : 512 bytes μPD780033 : 1024 bytes μPD780034 : 1024 bytes
Internal ROM and internal high-speed RAM capacity changeable/not changeable with memory size switching register	Changeable[Note]	Not changeable
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Electrical specifications	Refer to the data sheet of individual products.	

Note Flash memory is set to 32 Kbytes and internal high-speed RAM is set to 1024 bytes by $\overline{\text{RESET}}$ input.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	INTP0
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.	Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	SI30
P21				SO30
P22				$\overline{\text{SCK30}}$
P23				RxD0
P24				TxD0
P25				ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open drain input/output port. LED can be driven directly.	Input	—
P31					
P32					
P33					
P34			When used as an input port, an internal pull-up resistor can be connected by software.		SI31
P35					SO31
P36					$\overline{\text{SCK31}}$
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by the falling edge detection.	Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	$\overline{\text{RD}}$
P65				$\overline{\text{WR}}$
P66				$\overline{\text{WAIT}}$
P67				ASTB

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SI31				P34
SO30	Output	Serial interface serial data output.	Input	P21
SO31				P35
$\overline{SCK30}$	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{SCK31}$				P36
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P70/TO0
TI01				P71
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/TI00
TO50		8-bit timer (TM50) output (shared with 8-bit PWM output).	Input	P72/TI50
TO51		8-bit timer (TM51) output (shared with 8-bit PWM output).		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation of external memory.		P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Voltage equal to V_{DD0} or V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential. Voltage equal to V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply voltage for ports.	—	—
V_{SS0}	—	Ground potential of ports.	—	—
V_{DD1}	—	Positive power supply (except ports).	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
V_{PP}	—	Applying high-voltage for program write/verify. Connected directly to V_{SS0} in normal operation mode.	—	—

2.3 Recommended Connection of Unused Pins

Table 2-1 shows the recommended connection of unused pins.

Table 2-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection when Not Used
P00/INTP0	I/O	Independently connected to V_{SS0} through a resistor.
P01/INTP1		
P02/INTP2		
P03/INTP3/ADTRG		
P10/ANI0 to P17/ANI7	Input	Independently connected to V_{DD0} or V_{SS0} through a resistor.
P20/SI30	I/O	
P21/SO30		
P22/$\overline{SCK30}$		
P23/RxD0		
P24/TxD0		
P25/ASCK0		
P30 to P33		
P34/SI31		
P35/SO31		
P36/$\overline{SCK31}$		
P40/AD0 to P47/AD7		Independently connected to V_{DD0} through a resistor.
P50/A8 to P57/A15		Independently connected to V_{DD0} or V_{SS0} through a resistor.
P64/$\overline{RD}$		
P65/$\overline{WR}$		
P66/$\overline{WAIT}$		
P67/ASTB		
P70/TI00/TO0		
P71/TI01		
P72/TI50/TO50		
P73/TI51/TO51		
P74/PCL		
P75/BUZ		
$\overline{RESET}$	Input	—
XT1		Connected to V_{DD0}.
XT2	—	Left open.
AV_{REF}		Connected to V_{SS0}.
AV_{DD}		Connected to V_{DD0}.
AV_{SS}		Connected to V_{SS0}.
V_{PP}		Connected directly to V_{SS0}.

3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory unused by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM and RAM).

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to C8H.

Figure 3-1. Format of Memory Size Switching Register

	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
Others				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Others			Setting prohibited

Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780031	42H
μPD780032	44H
μPD780033	C6H
μPD780034	C8H

4. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system. Writing is performed connecting the dedicated flash programmer (Flashpro) to the host machine and the target system.

Remark Flashpro is a product of Naitou Densei Machidaseisakusho Co., Ltd.

4.1 Selection of Transmission Method

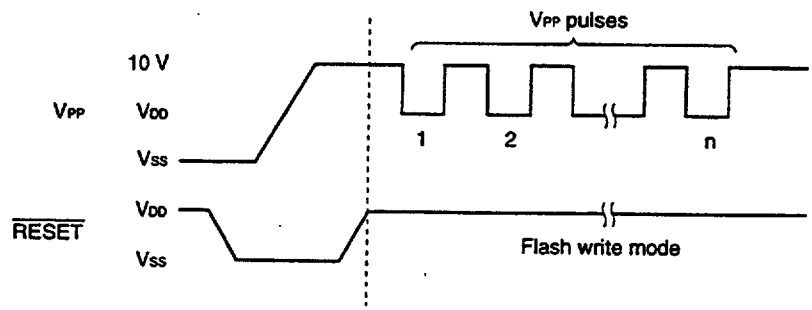
Writing to a flash memory is performed using the Flashpro with a serial transmission mode. One of the transmission method is selected from those in Table 4-1. The selection of the transmission method is made by using the format shown in Figure 4-1. Each transmission method is selected by the number of V_{PP} pulses shown in Table 4-1.

Table 4-1. List of Transmission Method

Transmission Method	Channels	Pin	V_{PP} Pulses
3-wire serial I/O	2	SI30/P20 SO30/P21 $\overline{SCK30}$/P22	0
		SI31/P34 SO31/P35 $\overline{SCK31}$/P36	1
UART	1	RxD0/P23 TxD0/P24 ASCK0/P25	8
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

Caution Select a communication system always using the number of V_{PP} pulses shown in Table 4-1.

Figure 4-1. Format of Transmission Method Selection



4.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 4-2 shows major functions of flash memory programming.

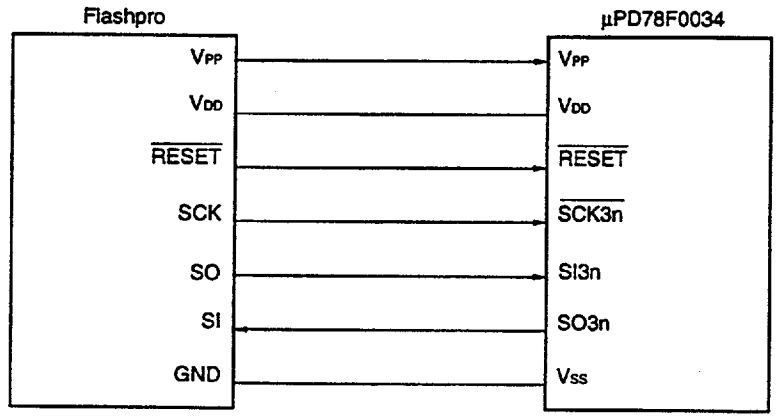
Table 4-2. Major Functions of Flash Memory Programming

Functions	Descriptions
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

4.3 Connection of Flashpro

The connection of the Flashpro and the μPD78F0034 differs according to the transmission method (3-wire serial I/O, UART pseudo 3-wire serial I/O). The connection for each transmission method is shown in Figures 4-2 and 4-3, respectively.

Figure 4-2. Connection of Flashpro for 3-wire Serial I/O System



n = 0, 1

Figure 4-3. Connection of the Flashpro for UART System

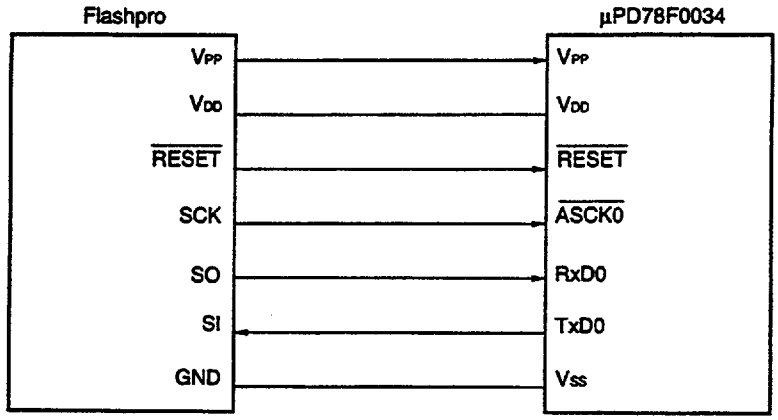
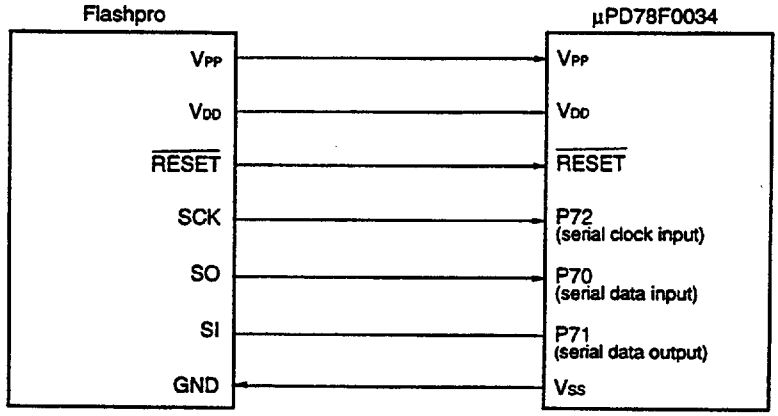
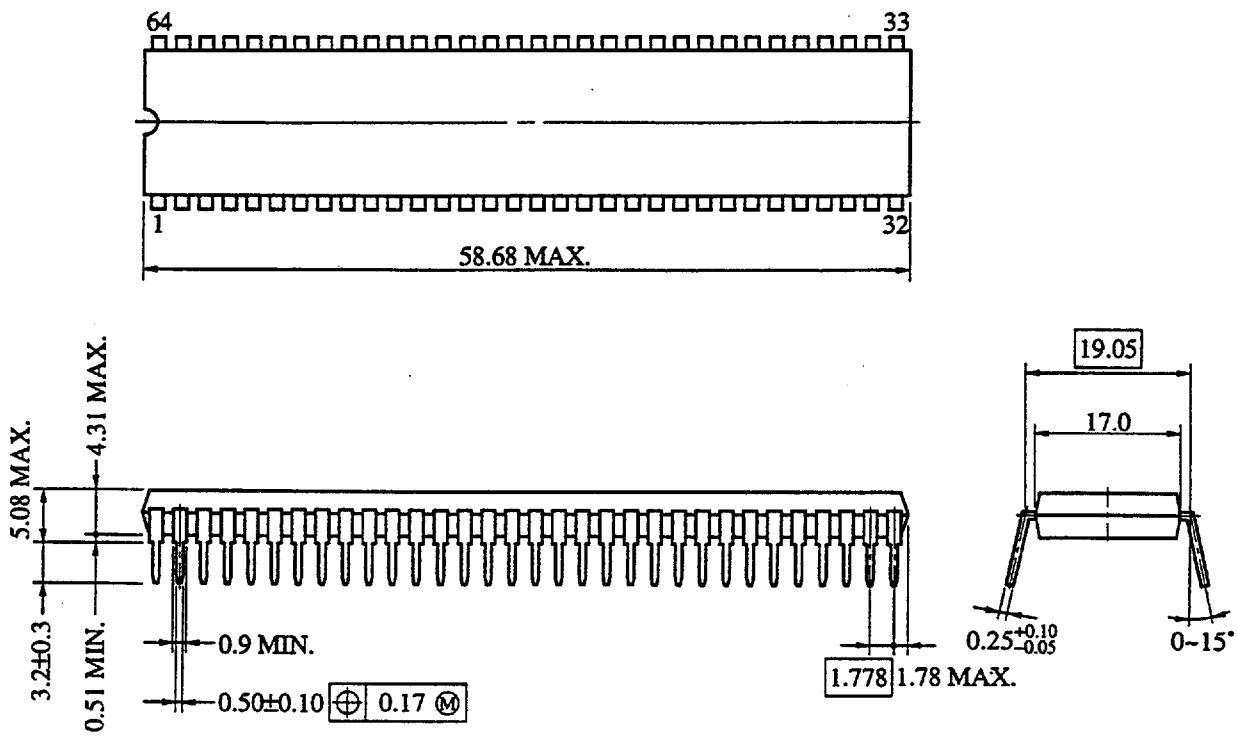


Figure 4-4. Connection of Flashpro Using Pseudo 3-Wire Serial I/O Method



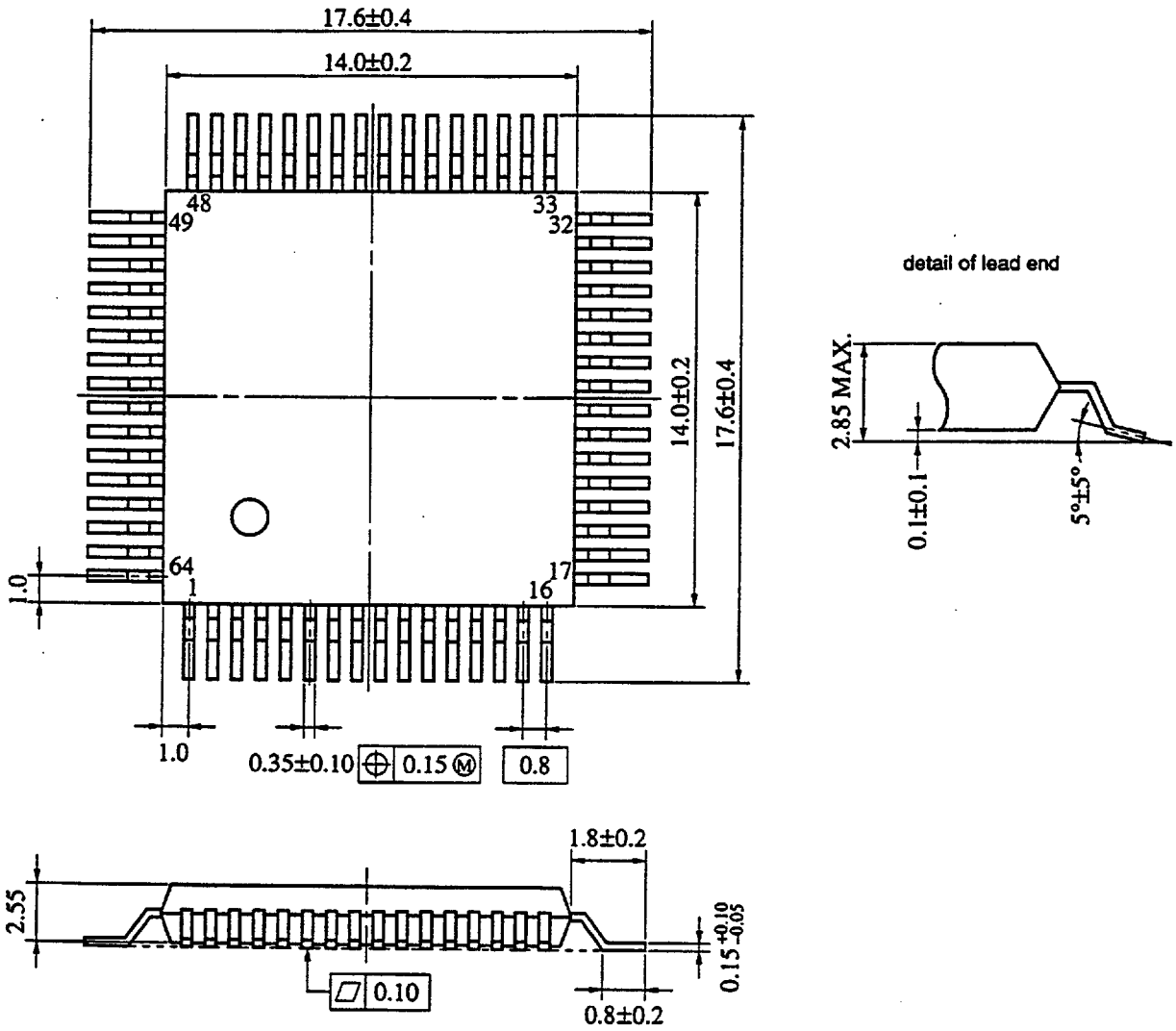
5. PACKAGE DRAWINGS

64-PIN PLASTIC SHRINK DIP (750 mil) (Unit: mm)



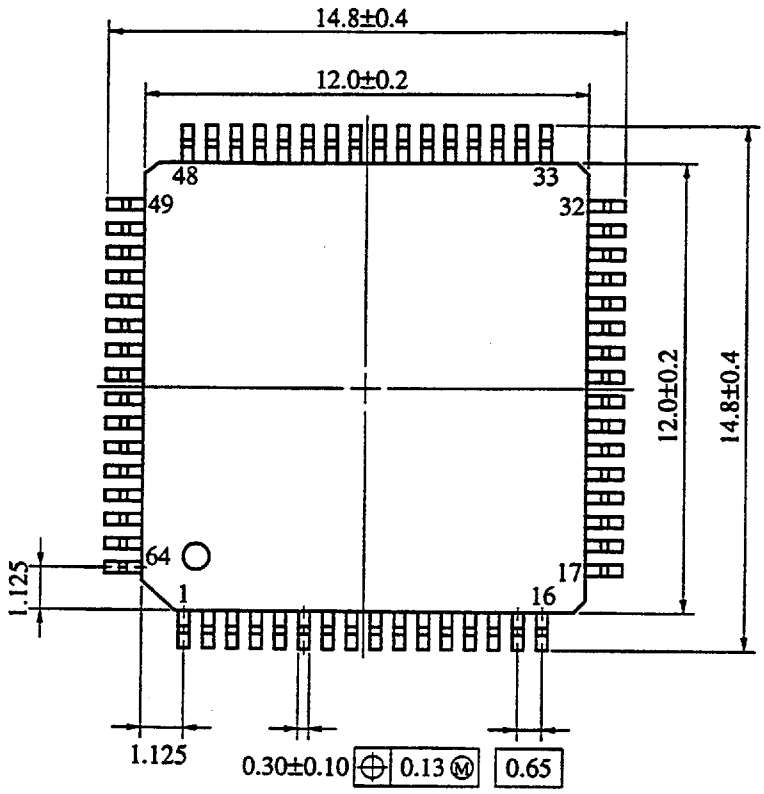
P64C-70-750A,C-1

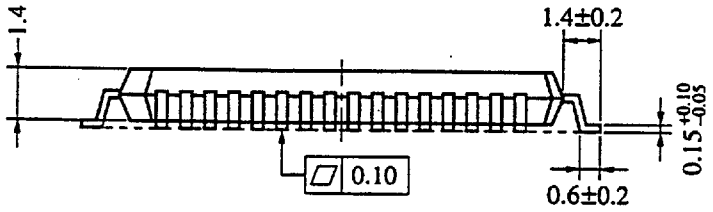
64-PIN PLASTIC QFP (14 x 14) (Unit: mm)

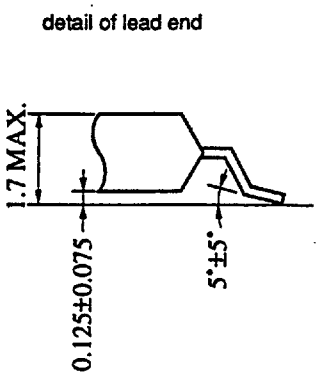


P64GC-80-AB8-3

64-PIN PLASTIC LQFP (12 x 12) (Unit: mm)







P64GK-65-8A8-1

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0034.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF780034 Notes 1, 2, 3, 4, 8	Device file for μPD780034 subseries
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

Flash Memory Writing Tools

Flashpro	Dedicated flash writer Product of Naitou Densei Machidaseisakusho Co., Ltd.
PA-FLASH64CW (Tentative name) Note 8 PA-FLASH64GC (Tentative name) Note 8 PA-FLASH64GK (Tentative name) Note 8	Adapter for flash writing Product of Naitou Densei Machidaseisakusho Co., Ltd.

Debugging Tool

IE-780000-SL Note 8	75XL, 78K/0S, 78K/0, and 78K/IV Series common in-circuit emulator
IE-78K0-SL-EM Note 8	78K/0 Series common CPU core board
IE-78K0-SL-P01 Note 8	78K/0 Series common emulation board
IE-780034-SL-EM4 Note 8	Probe board for μPD780034 Subseries emulation
EP-64CW-SL Note 8	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-64GC-SL Note 8	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on a target system board made for the 64-pin plastic QFP (GC-AB8 type)
EP-64GK-SL Note 8	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Adapter to be mounted on a target system board made for the 64-pin plastic LQFP (GK-8A8 type) Product of Tokyo Eletech Corporation
SM78K0 Notes 5, 6, 7	78K/0 Series common system simulator
ID78K0 Notes 4, 5, 6, 7	78K/0 Series common integrated debugger
DF780034 Notes 1, 2, 5, 6, 7, 8	Device file for μPD780034 Subseries

Real-time OS

RX78K/0[Notes 1, 2, 3, 4]	78K/0 series real-time OS
MX78K0[Notes 1, 2, 3, 4]	78K/0 series OS

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 8]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes
1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™ (HP-UX™) based
4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Remarks
1. For third party development tools, refer to the **78K/0 Series Selection Guide (U11126E)**
2. The RA78K/0, CC78K/0, SM78K0, ID78K0, and RX78K/0 are used in combination with the DF780034.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024, 780024Y, 780034, 780034Y Subseries User's Manual	Planned	Planned
μPD78F0034 Preliminary Product Information	This manual	U11860J
78K/0 Series User's Manual Instruction	IEU-1372	IEU-849
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD780034 Subseries Special Function Register Table	—	Planned

Development Tools Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K/0 C Compiler	Operation	—	U11517J
	Language	—	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEU-618
CC78K Series Library Source File		—	EEU-777
IE-780000-SL		Planned	Planned
IE-78K0-SL-P01		Planned	Planned
IE-780034-SL-EM4		Planned	Planned
EP-64CW-SL		Planned	Planned
EP-64GC-SL		Planned	Planned
EP-64GK-SL		Planned	Planned
SM78K0 System Simulator (Windows Based)	Reference	U10181E	U10181J
SM78K Series System Simulator	External Parts User Open Interface Specification	U10092E	U10092J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger Windows based	Guide	—	U11649J
ID78K0 Integrated Debugger PC based	Reference	—	U11539J

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real Time OS	Basic	—	U11537J
	Installation	—	U11536J
	Technical	—	U11538J
OS for 78K/0 Series MX78K0	Basic	—	EEU-5010
Fuzzy Knowledge Data Creation Tool		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-1458	EEU-921

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grade on NEC Semiconductor Devices	IEI-1209	C11531J
Reliable Quality Maintenance on NEC Semiconductor Devices	C10983E	C10983J
Electrostatic Discharge (ESD) Test	—	MEM539
Semiconductor Devices Quality Guarantee Guide	MEI-1202	MEI-603
Microcomputer Product Series Guide	—	U11416J

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Renesas ***manufacturer:***

Other Similar products are found below :

EL4511CUZ-T7 PYB15-Q24-S5-H-U PQA30-D24-S24-DH PQA30-D48-S12-TH PYB30-Q24-T312-H-U PYB15-Q24-S5-H-T PYB15-Q24-S12-H-T V7815-500-SMT PYB20-Q48-S12-H-T PQZ6-Q24-S15-D PYB20-Q48-S5-H-T PYB20-Q24-S12-H-T VLED15-120-350 VGS-75-12 PYB15-Q24-S12-H-U R5F100GFAFB#V0 VGS-50-15 VGS-50-24 VGS-25-24 VGS-50-5 VGS-100-12 M30620FCAFP#U3 PDQ2-D24-S12-S PDS1-S12-D12-M PDS1-S12-D15-M PYB15-Q24-S12-T PYB20-Q48-S12 R0K33062PS000BE R0K505220S000BE R0K561664S000BE R0K570865S000BE HC55185AIMZ R7S721001VCBGAC0 EMMA050200-P5P-IC EPSA050250UB-P5P-EJ HS0005PUU01H IS82C55A-5 ISL55110IVZ ISL6730AEVAL1Z ISL68200DEMO1Z ISL78235EVAL2Z ISL78268EVAL1Z ISL91107IRA-EVZ ISL9220IRTZEVAL1Z ISLUSBI2CKIT1Z RTK5RX2310P00000ZR SDI120-12-U-P51 PEM1-S24-D12-S PQA30-D24-S24-T PQA30-D48-S24-T