# HS-26CLV31RH, HS-26CLV31EH

Radiation Hardened 3.3V Quad Differential Line Drivers

FN4898
Rev 5.00
Oct 26, 2018

The HS-26CLV31RH and HS-26CLV31EH are radiation hardened 3.3V quad differential line drivers designed for digital data transmission over balanced lines, in low voltage RS-422 protocol applications. CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV31RH and HS-26CLV31EH accept CMOS level inputs and converts them to differential outputs. Enable pins allow several devices to be connected to the same data source and addressed independently. These devices have unique outputs that become high impedance when the driver is disabled or powered-down, maintaining signal integrity in multi-driver applications.

## Related Literature

For a full list of related documents, visit our website:

- HS-26CLV31RH, HS-26CLV31EH product pages

## Features

- Electrically screened to SMD # 5962-96663
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
  - Total dose . . . . . 300krad (Si) (maximum)
  - Single event upset LET . . . . . 100MeV/mg/cm$^2$
  - Single event latch-up immune
- Extremely low stand-by current . . . . . 100µA (maximum)
- Operating supply range . . . . . 3.0V to 3.6V
- CMOS level inputs . . . . . $V_{IH}$ > (0.7) ($V_{DD}$); $V_{IL}$ < (0.3) ($V_{DD}$)
- Differential outputs . . . . . $V_{OH}$ > 1.8V; $V_{OL}$ < 0.5V
- High impedance outputs when disabled or powered down
- Low output impedance . . . . . 10Ω or less
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

## Applications

- Line transmitter for MIL-STD-1553 serial data bus

# Ordering Information

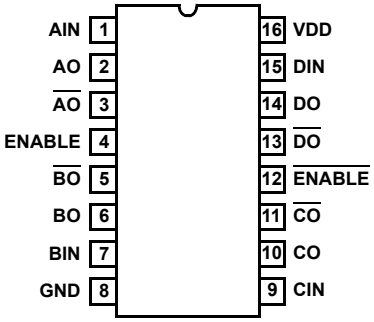
| ORDERING SMD NUMBER (Note 1) | PART NUMBER (Note 2) | TEMP. RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| 5962F9666302QEC | HS1-26CLV31RH-8 | -55 to +125 | 16 Ld SBDIP | D16.3 |
| 5962F9666302QXC | HS9-26CLV31RH-8 | -55 to +125 | 16 Ld FLATPACK | K16.A |
| 5962F9666302VEC | HS1-26CLV31RH-Q | -55 to +125 | 16 Ld SBDIP | D16.3 |
| 5962F9666302VXC | HS9-26CLV31RH-Q | -55 to +125 | 16 Ld FLATPACK | K16.A |
| 5962F9666302V9A | HS0-26CLV31RH-Q | -55 to +125 | Die | |
| N/A | HS1-26CLV31RH/PROTO (Note 4) | -55 to +125 | 16 Ld SBDIP | D16.3 |
| N/A | HS9-26CLV31RH/PROTO (Note 4) | -55 to +125 | 16 Ld FLATPACK | K16.A |
| 5962F9666304VEC | HS1-26CLV31EH-Q | -55 to +125 | 16 Ld SBDIP | D16.3 |
| 5962F9666304VXC | HS9-26CLV31EH-Q | -55 to +125 | 16 Ld FLATPACK | K16.A |
| 5962F9666304V9A | HS0-26CLV31EH-Q | -55 to +125 | Die | |
| N/A | HS0-26CLV31RH/SAMPLE (Note 4) | -55 to +125 | Die | |
| 5962F9666302VYC | HS9G-26CLV31RH-Q (Notes 3, 4) | -55 to +125 | 16 Ld FLATPACK | K16.A |
| 5962F9666304VYC | HS9G-26CLV31EH-Q (Note 3) | -55 to +125 | 16 Ld FLATPACK | K16.A |
| N/A | HS9G-26CLV31RH/PROTO (Notes 3, 4) | -55 to +125 | 16 Ld FLATPACK | K16.A |

NOTES:

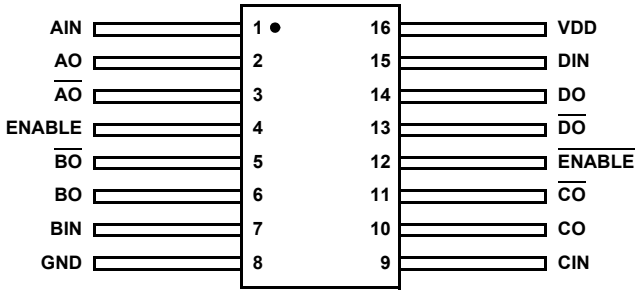
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The lid of these packages are connected to the ground pin of the device.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

# Pin Configurations

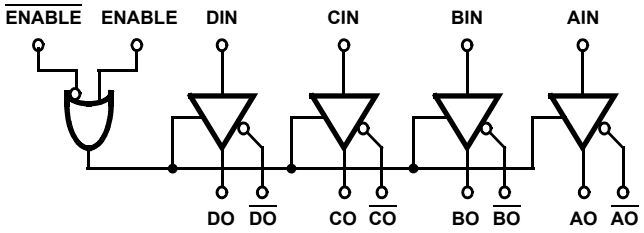
HS1-26CLV31RH, HS1-26CLV31EH
(16 LD SBDIP)
CDIP2-T16
TOP VIEW




HS9-26CLV31RH, HS9-26CLV31EH
(16 LD FLATPACK)
CDFP4-F16
TOP VIEW




# Logic Diagram



# Die Characteristics

**DIE DIMENSIONS:**

96.5 mils x 195 mils x 21 mils
(2450 x 4950)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8kÅ ±1kÅ

**Metallization:**

Bottom: Mo/TiW
Thickness: 5800Å ±1kÅ
Top: AlSiCu (Top)
Thickness: 10kÅ ±1kÅ

**Substrate:**

AVLSI1RA

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential (Powered Up):**

$V_{DD}$

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

$<2.0 \times 10^5 A/cm^2$

**Bond Pad Size:**

110µm x 100µm

# Metallization Mask Layout

**HS-26CLV31RH, HS-26CLV31EH**

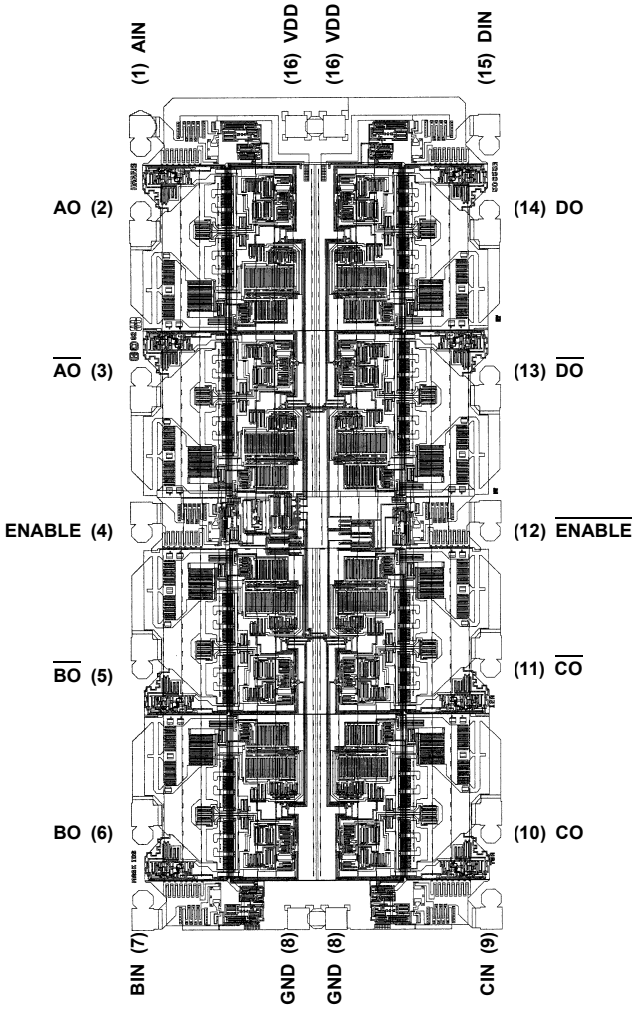



**TABLE 1. HS-26CLV31RH, HS-26CLV31EH PAD COORDINATES**

| | | RELATIVE TO PIN 1 | |
|---|---|---|---|
| PIN NUMBER | PAD NAME | X COORDINATES | Y COORDINATES |
| 1 | AIN | 0 | 0 |
| 2 | A0 | 0 | -570.7 |
| 3 | $\overline{A0}$ | 0 | -1483.5 |
| 4 | ENABLE | 0 | -2124.8 |
| 5 | $\overline{B0}$ | 0 | -2873.5 |
| 6 | B0 | 0 | -3786.3 |
| 7 | BIN | 0 | -4357 |
| 8 | GND | 852.4 | -4357 |
| 8 | GND | 1062.4 | -4357 |
| 9 | CIN | 1912.8 | -4357 |
| 10 | $\overline{C0}$ | 1912.8 | -3786.3 |
| 11 | C0 | 1912.8 | -2873.5 |
| 12 | $\overline{ENABLE}$ | 1912.8 | -2124.8 |
| 13 | $\overline{D0}$ | 1912.8 | -1483.5 |
| 14 | D0 | 1912.8 | -570.7 |
| 15 | DIN | 1912.8 | 0 |
| 16 | VIN | 1062.4 | 0 |
| 16 | VIN | 852.4 | 0 |

NOTE: Dimensions in microns.

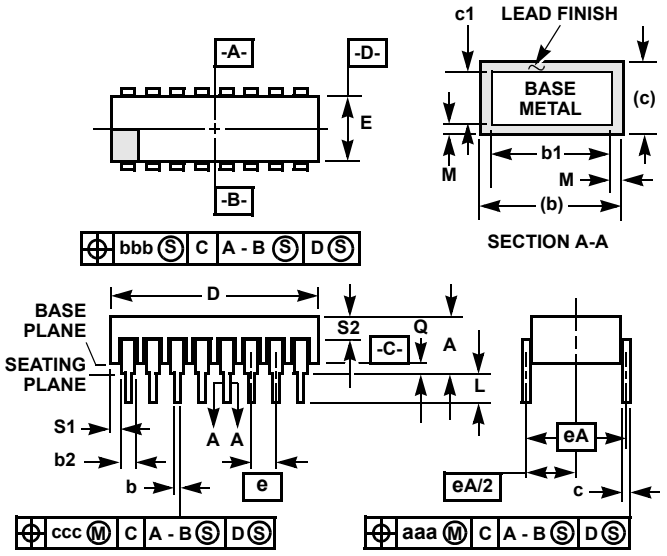
## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Oct 26, 2018 | FN4898.5 | Added Related Literature section.<br>Updated Ordering Information table - added HS9G-26CLV31EH-Q part and added Notes 1 and 4. Removed part Marking column.<br>Added Revision History.<br>Added PODs D16.3 and K16.A<br>Updated Disclaimer. |

## Package Outline Drawings

For the most recent package outline drawing, see D16.3.




NOTES:

5. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
6. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
7. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
8. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
9. Dimension Q shall be measured from the seating plane to the base plane.
10. Measure dimension S1 at all four corners.
11. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
12. N is the maximum number of terminal positions.
13. Braze fillets shall be concave.
14. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
15. Controlling dimension: INCH.

**D16.3** MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

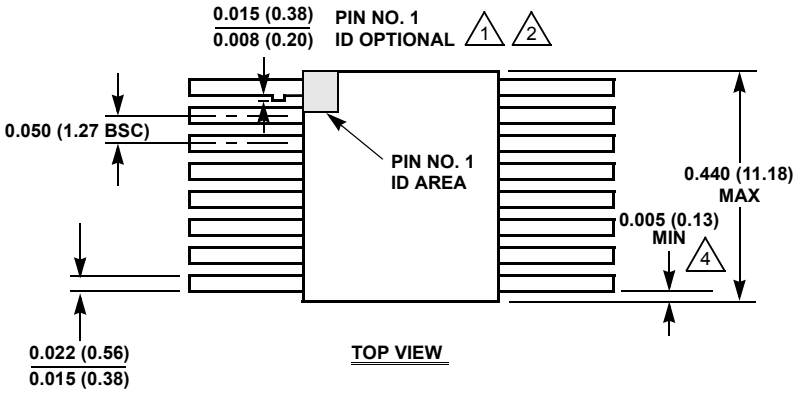
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.840 | - | 21.34 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| $\alpha$ | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 16 | | 16 | | 8 |

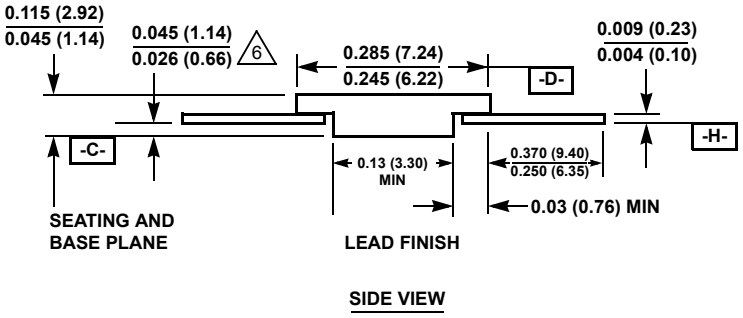
Rev. 0 4/94

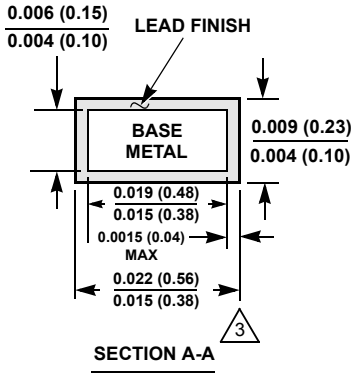
## K16.A

**16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE**
**Rev 2, 1/10**

For the most recent package outline drawing, see K16.A.




**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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