ISL1904

Dimmable AC Mains LED Driver with PFC and Primary Side Regulation

FN8286
Rev 1.00
September 20, 2012

The ISL1904 is a high-performance, critical conduction mode (CrCM), flyback controller used for single-stage conversion of the AC mains to a constant current source with power factor correction (PFC). The controller regulates the output current by monitoring the primary side switching current so the feedback signal does not cross the isolation barrier. Operation in CrCM allows near zero-voltage quasi-resonant switching (ZVS) for improved efficiency while maximizing magnetic core utilization. The ISL1904 LED driver provides all of the features required for high-performance dimmable LED ballast designs and supports AC or DC input, isolated or non-isolated flyback and boost topologies. This advanced BiCMOS controller features all of the functions required to design low cost low parts count LED driver.

Features

- Excellent LED current regulation over line, load, and temperature
- 0 - 100% dimming with leading-edge (triac) and trailing-edge dimmers
- Power factor correction for up to 0.995 power factor and less than 20% harmonic content
- Critical conduction mode (CrCM) operation for quasi-resonant high efficiency performance
- Supports universal AC mains input
- Configurable for PWM or DC current dimming control of LEDs
- Monitors FET switching current for load regulation
- Supports isolated and non-isolated boost and flyback topologies
- Closed loop soft-start for no overshoot
- OFFREF feature to set dimming off-point to improve fixture performance matching
- -40°C to +125°C operation
- Pb-free (RoHS compliant)

Applications

- Industrial and commercial LED lighting
- Retrofit LED lamps with triac dimming
- Universal AC mains input LED retrofit lamps
- AC or DC Input LED ballasts

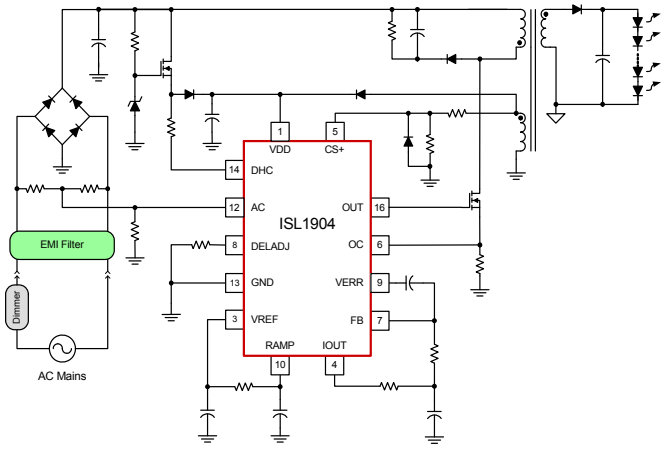


FIGURE 1A. TYPICAL APPLICATION

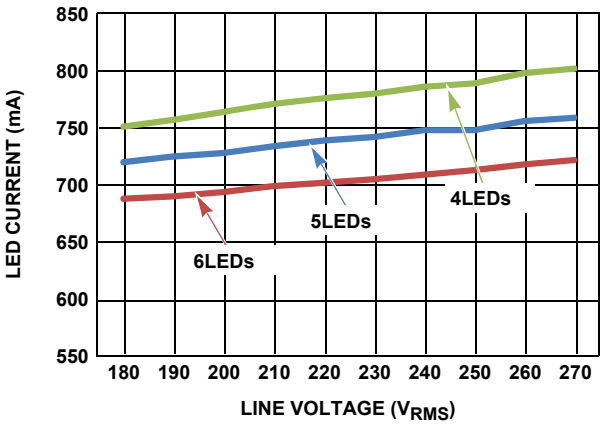
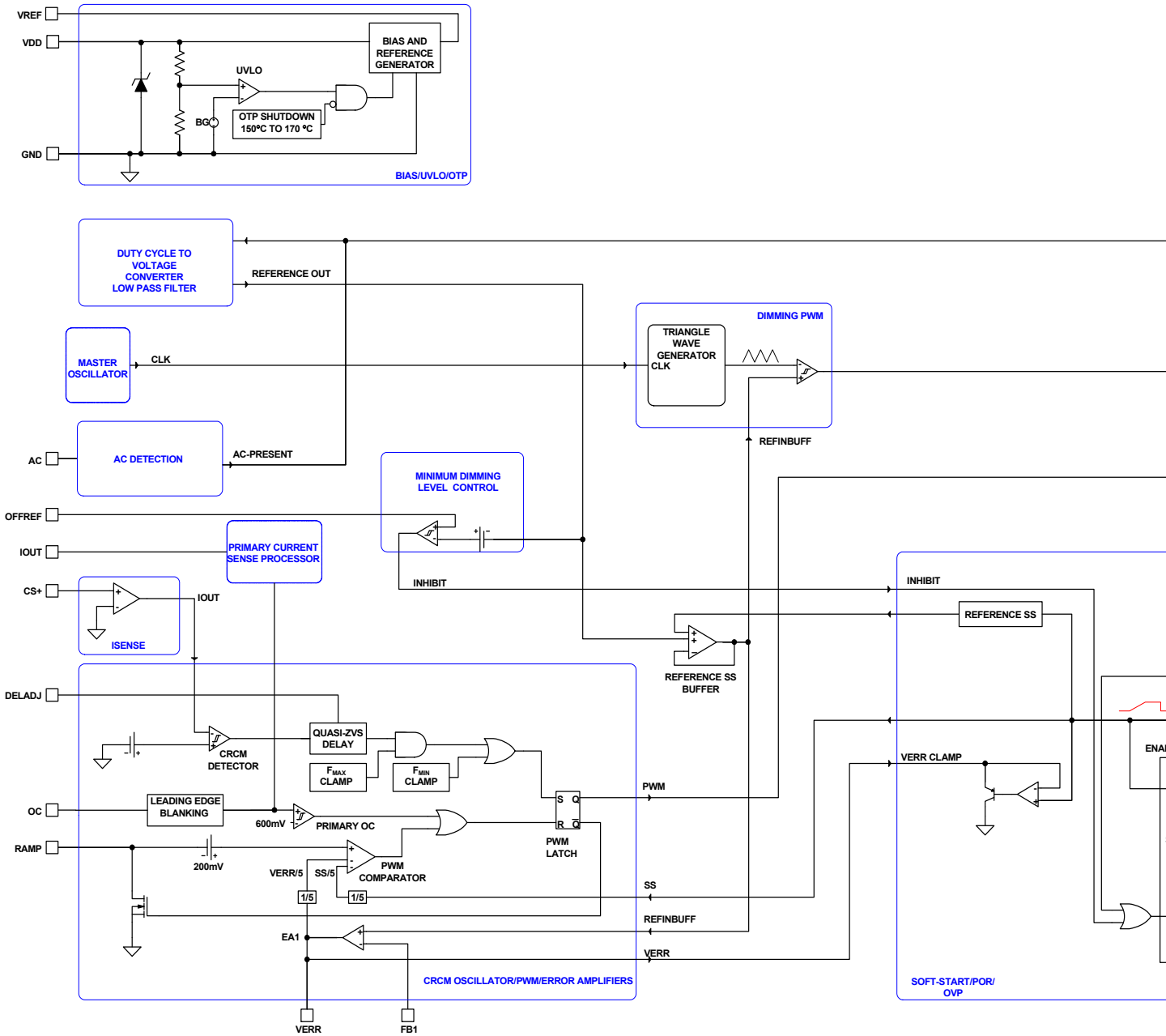


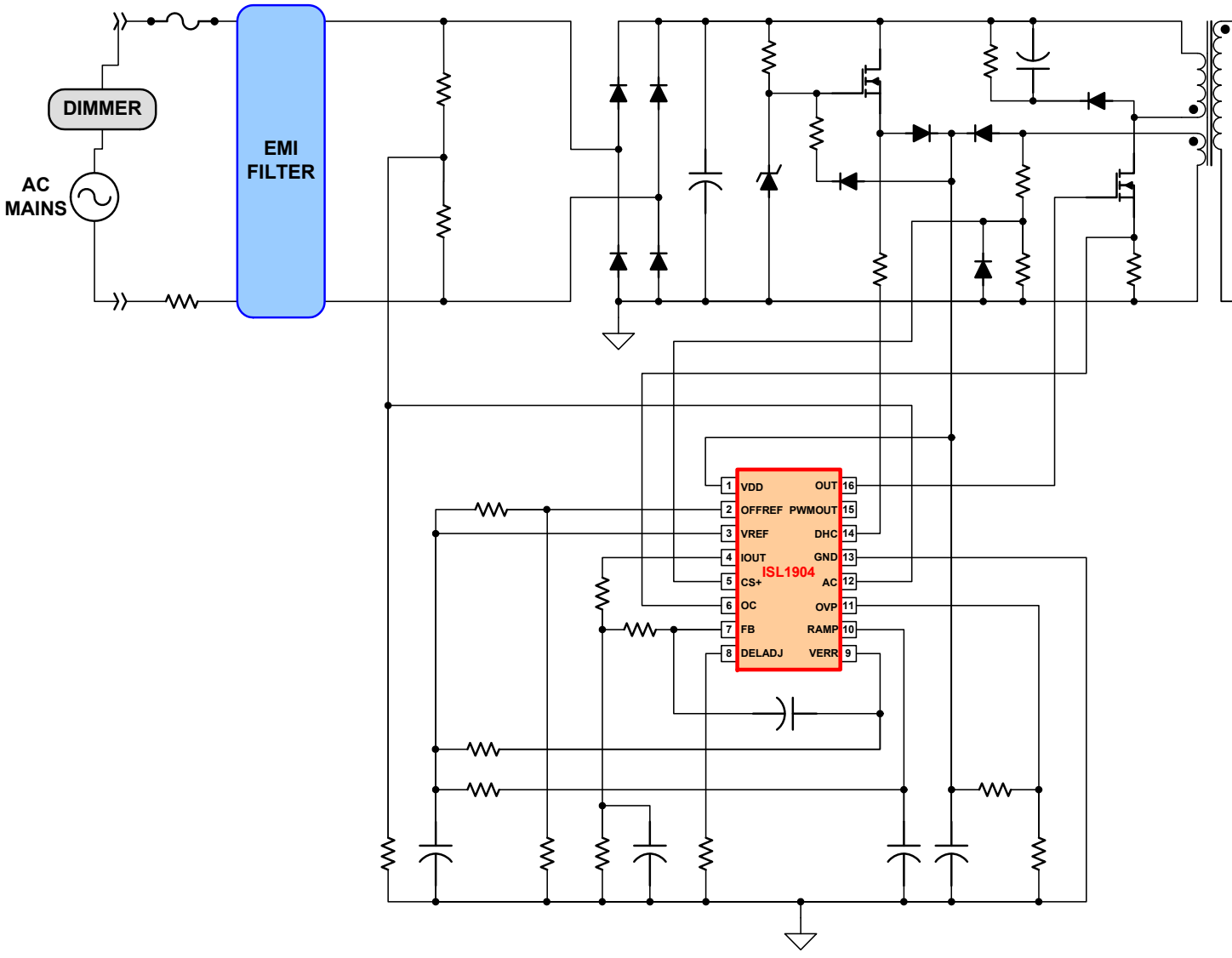
FIGURE 1B. LED CURRENT vs LINE VOLTAGE

FIGURE 1. TYPICAL APPLICATION PERFORMANCE

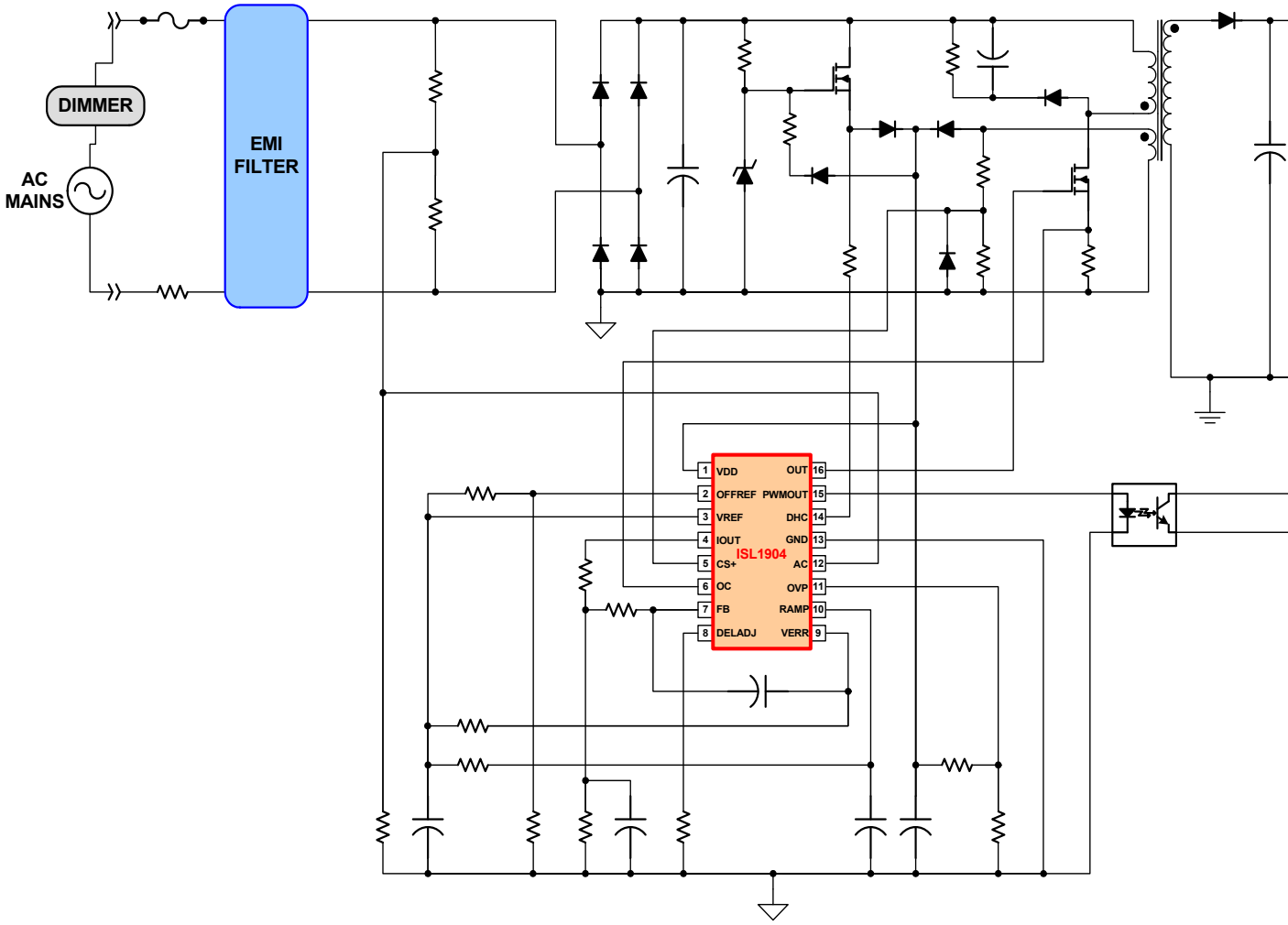
Functional Block Diagram - ISL1904



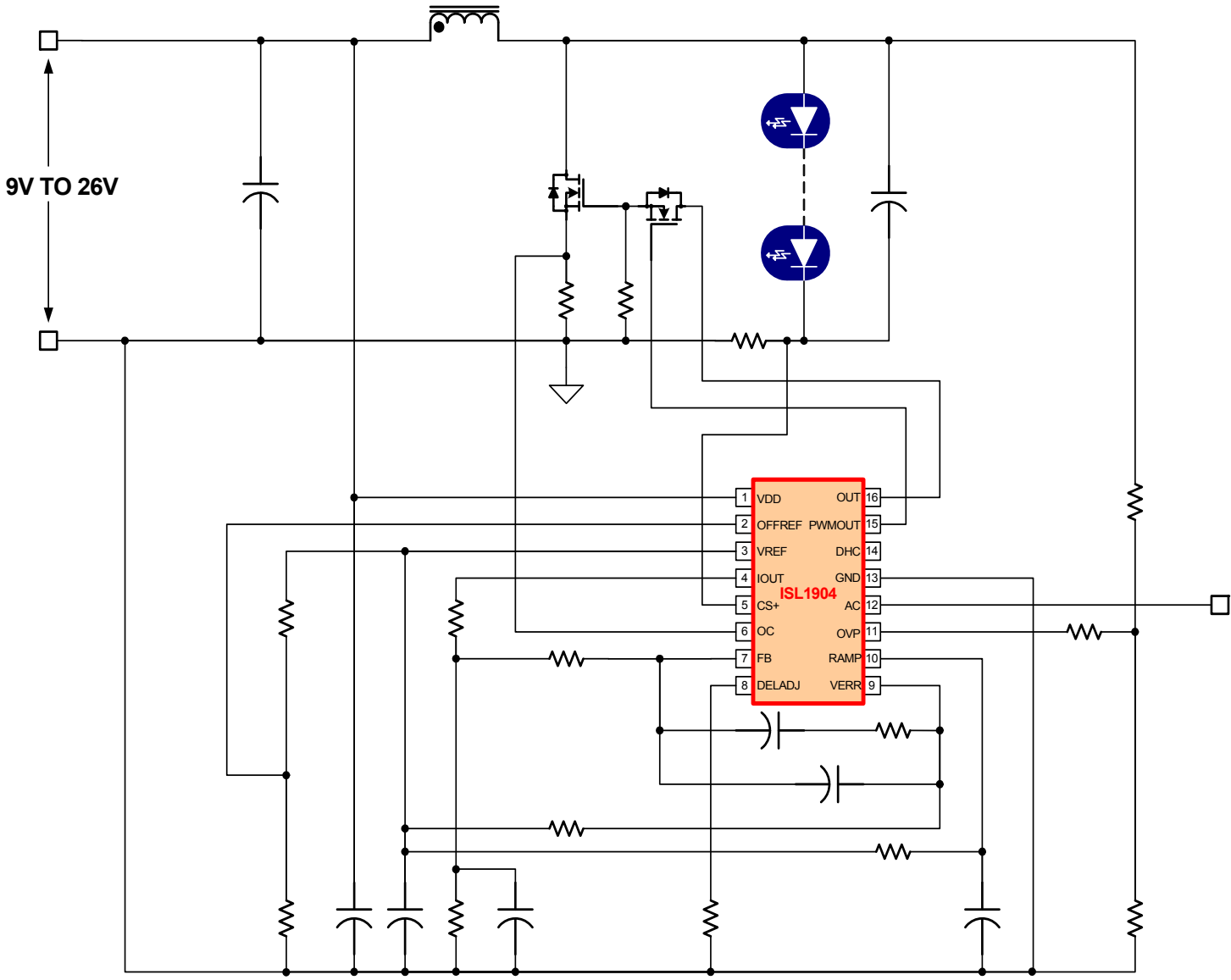
Typical Application - Dimmable Isolated Flyback



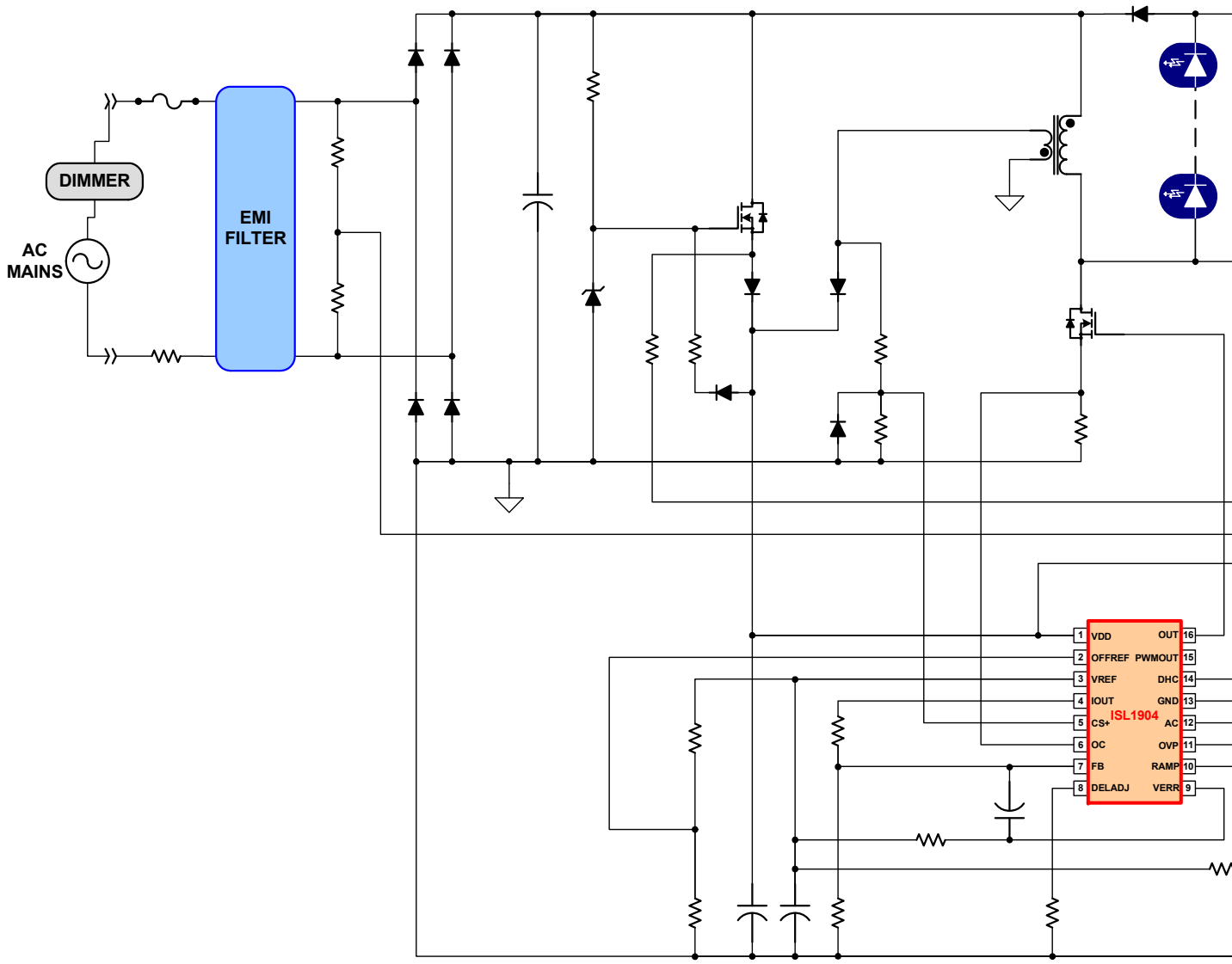
Typical Application - Isolated Flyback with PWM Dimming



Typical Application - Dimmable DC Input Boost Converter

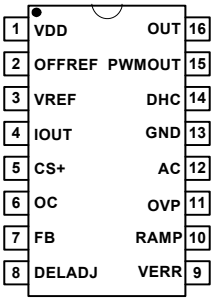


Typical Application - Dimmable Inverting Boost-Buck (Single Winding Flyba



Pin Configuration

ISL1904
(16 LD QSOP)
TOP VIEW



Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	VDD	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.
2	OFFREF	Sets the reference level to disable the driver at light loading. The turn-off reference can be set at any level between 0 and 0.6V, corresponding to 0 to 100% of output loading. This feature is normally used in triac-based wall dimmer applications to disable the output before the dimmer becomes unstable due to insufficient holding current.
3	VREF	The 5.40V reference voltage output having ±100 mV tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF low ESR capacitor.
4	IOUT	A PWM voltage signal with amplitude and duty cycle proportional to the peak switching current used to determine the output current.
5	CS+	The input for the CrCM current sense circuit. This input monitors the winding current to determine the critical conduction operating point.
6	OC	The input to the load current sensing circuitry and the peak overcurrent comparator. The signal is sampled at the peak current level for each switching cycle, amplified, and output on IOUT as a PWM signal. It must be scaled, filtered and averaged prior to being applied to the FB pin of the EA. The overcurrent comparator threshold is set at 600mV nominal. Peak OCP performs cycle-by-cycle over current protection. OCP includes leading-edge-blanking (LEB), which blocks the signal at the beginning of the OUT pulse for the duration of the blanking period and when the OUT pulse is low.
7	FB	FB is the inverting input to the error amplifier (EA). The feedback signal from IOUT, after being scaled and filtered, is applied to the error amplifier.
8	DELADJ	Sets delay before a new switching cycles starts. This adjustment allows the user to delay the next switching cycle until the switching FET drain-source voltage reaches a minimum value to allow quasi-ZVS (Zero Voltage Switching) operation. A resistor to ground programs the delay. Pulling DELADJ to VREF disables the CrCM oscillator.
9	VERR	Output of the error amplifiers and the control voltage input to the inverting input of the PWM comparator. VERR cannot source current and requires an external pull-up resistor to VREF.
10	RAMP	This is the input for the sawtooth waveform for the PWM comparator. Using an RC from VREF, a sawtooth waveform is created for use by the PWM. It is compared to the error amplifier output, Verr, to create the PWM control signal. The RAMP pin is shorted to GND at the termination of the PWM signal.
11	OVP	Input to detect an overvoltage (OV) condition on the output. Since the control variable is output current, a fault that results in an open circuit will cause excessive output voltage. The circuit hysteresis is a switched current source that is active when the OV threshold is exceeded.
12	AC	Input to sense AC voltage presence and amplitude. A resistor divider from line and neutral/line and circuit ground is used to detect the AC voltage.
13	GND	Signal and power ground connections for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
14	DHC	An open drain FET used to load the input voltage to pre-load a triac-based dimmer so that adequate holding current is maintained.

Pin Descriptions (Continued)

PIN #	SYMBOL	DESCRIPTION
15	PWMOUT	The PWM gate drive output for LED dimming. The output level is clamped to ~12V for VDD greater than 12V. PWMOUT has pull-down capability when UVLO is active or when the IC is not biased. This output is used to drive the dimming FET in series with the LED string. The PWM operates at ~ 320Hz.
16	OUT	The gate drive output for the external power FET. OUT is capable of sourcing and sinking 1A @ VDD = 8V. The output level is clamped to ~12V for VDD greater than 12V. OUT has pull-down capability when UVLO is active or when the IC is not biased.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL1904FAZ	1904 FAZ	-40 to +125	16 Ld QSOP	M16.15A
ISL1904EVAL2Z	Evaluation Board			

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1904. For more information on MSL please see tech brief TB363.

Related Products

PART NUMBER	KEY DIFFERENTIATORS
ISL1901	Isolated and non-isolated single-stage flyback regulator.
ISL1902	Isolated and non-isolated single-stage flyback regulator with inrush control and interface features for temperature and ambient light sensors.
ISL1903	Non-isolated single-stage buck regulator using switch current for regulation.
ISL1904	Isolated single-stage flyback regulator with primary side current sense regulation.
ISL1907	Non-isolated two-stage cascaded boost PFC + buck regulator eliminates dependency on electrolytic capacitors.
ISL1908	Isolated two-stage cascaded boost PFC + flyback regulator eliminates dependency on electrolytic capacitors.

Absolute Maximum Ratings (Note 4)

Supply Voltage, VDD . . . . . GND - 0.3V to +28.0V
OUT, PWMOUT, DHC . . . . . GND - 0.3V to VDD
Signal Pins. . . . . GND - 0.3V to V_{REF} + 0.3V
VREF . . . . . GND - 0.3V to 6.0V
Peak OUT Current 2.0A
Peak PWMOUT Current 1.0A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7). 2500V
Machine Model (Per EIAJ ED-4701 Method C-111) 200V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93). 1000V
Latch up (Per JESD-78B; Class 1, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QSOP Package (Notes 5, 6)	85	44

Maximum Junction Temperature . . . . . -55°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +125°C
Supply Voltage Range (Typical). . . . . 9 TO 20 VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. All voltages are with respect to GND.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram - ISL1904" on page 2 and "Typical Application schematics" beginning on page 3. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C; **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY VOLTAGE					
Supply Voltage		-	-	**26**	V
Start-Up Current, IDD	VDD = 5.0V	-	100	**200**	µA
Operating Current, IDD	R_{LOAD}, C_{OUT} = 0	-	6.0	**7.8**	mA
UVLO START Threshold		**8.15**	8.55	**8.95**	V
UVLO STOP Threshold		**6.80**	7.10	**7.50**	V
Hysteresis		-	1.45	-	V
REFERENCE VOLTAGE VREF					
Overall Accuracy	I_{VREF} = 0 - -10mA, 8V < V_{DD}< 26V	**5.30**	5.40	**5.50**	V
Long Term Stability	T_A = 125°C, 1000 hours (Note 8)	-	10	25	mV
Operational Current (Source)	8V < V_{DD}< 26V	**-**	-	**-10**	mA
Current Limit	VREF = 5.00V, 8V < V_{DD}< 26V	**-100**	-	**-15**	mA
Load Capacitance	(Note 8)	**0.1**	-	**3.3**	µF
PEAK CURRENT SENSE (OC)					
Current Limit Threshold	VERR = VREF, RAMP = 0V	**570**	595	**616**	mV
IOUT Amplifier Gain	V_{OC} = 0.4V, 8V < V_{DD}< 17V	**3.83**	4.00	**4.18**	V/V
IOUT High Level Output Voltage (VOH)	V_{IOUT} @ 0µA - V_{IOUT} @ -100µA, 8V < V_{DD}< 26V	-	-	**0.1**	V
IOUT Low Level Output Voltage (VOL)	V_{IOUT} @ 100µA, 8V < V_{DD}< 26V	-	-	**0.1**	V
Leading Edge Blanking (LEB) Duration		**70**	120	**146**	ns
OC to OUT Delay + LEB	T_A = 25°C	110	170	200	ns
Input Bias Current	V_{OC} = 0.3V	**-1.0**	-	**1.0**	µA

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PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
RAMP					
RAMP Sink Current Device Impedance	I_{RAMP} = 10 mA	-	-	**20**	Ω
RAMP to PWM Comparator Offset	T_A = +25°C	181	235	287	mV
Input Bias Current	V_{RAMP} = 0.3V	**-1.0**	-	**1.0**	µA
PULSE WIDTH MODULATOR					
PWM Restart Delay Range	8V < V_{DD}< 26V	**0.2**	-	**2.0**	µs
PWM Restart Cycle Delay	RDELADJ = 20.0k, 8V < V_{DD}< 26V	**240**	280	**320**	ns
	RDELADJ = 210k, 8V < V_{DD}< 26V	**2.00**	2.20	**2.40**	µs
Maximum Frequency Clamp	8V < V_{DD}< 26V, RAMP = 2V, R_{RAMP} = 100Ω	**0.8**	1.0	**1.2**	MHz
Minimum Frequency Clamp	8V < V_{DD}< 26V, R_{RAMP} = 23kΩ	**20**	25	**31**	kHz
Minimum On Time	8V < V_{DD}< 26V, FB = 1V, AC = 2V, RAMP = 0V	**173**	-	**246**	ns
VERR to PWM Gain	8V < V_{DD}< 26V	**-**	0.200	**-**	V/V
SS to PWM Gain	8V < V_{DD}< 26V	**-**	0.222	**-**	V/V
ERROR AMPLIFIER					
Input Common Mode (CM) Range	(Note 8)	**0**	-	**3.4**	V
GBWP	(Note 8)	**1.9**	-	-	MHz
VERR VOL	I_{VERR} = 6mA, 8V < V_{DD}< 26V	-	-	**0.950**	V
VERR VOH	I_{VERR} = 1mA (Ext. pull-up) SS complete	**3.90**	4.00	**4.20**	V
Open Loop Gain	(Note 8)	**70**	-	-	dB
Offset Voltage (VOS)	8V < V_{DD}< 26V	**-7.5**	-	**7.5**	mV
Input Bias Current	8V < V_{DD}< 26V	**-1.0**	-	**1.0**	µA
CURRENT SENSE (CS+)					
Zero Current (CrCM) Detection Threshold, Falling	8V < V_{DD}< 26V	**6**	-	**30**	mV
Input Bias Current	8V < V_{DD}< 26V	**-1.0**	-	**1.0**	µA
AC DETECTOR					
Input Bias Current	8V < V_{DD}< 26V	**-50**	-	**50**	nA
Detection Threshold, Falling	8V < V_{DD}< 26V, AC_{PEAK} = 100mV	**18**	32	**51**	mV
Detection Threshold Hysteresis	8V < V_{DD}< 26V	**-**	23	**-**	mV
Input Operating Range	8V < V_{DD}< 26V	**0**	-	**4.00**	V
Clamp Voltage	$I_{ACDETECT}$ = 1.0mA	**6.8**	7.2	**7.6**	V
EA Reference Input Range	8V < V_{DD}< 26V	**0**	-	**0.538**	V

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PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
EA Reference vs AC Conduction Angle	I_{LPOUT} = 0µA, f = 120Hz (rectified), 8V < V_{DD}< 26V				
	Duty Cycle (α) = 98%	**523**	548	**574**	mV
	Duty Cycle (α) = 75%	**286**	318	**340**	mV
	Duty Cycle (α) = 50%	**117**	139	**156**	mV
	Duty Cycle (α) = 25%	**16**	32	**44**	mV
	Duty Cycle (α) = 10%	**0**	3	**11**	mV
DHC					
Low Level Output Voltage (VOL)	V_{DHC} = 10mA, VDD = 8V operating	-	-	**600**	mV
Turn-off Delay after AC Returns		-	4.0	-	µs
SOFT-START					
Duration		**289**	389	**483**	ms
Reference Soft-Start Initial Step		**11**	27	**43**	mV
OFFREF					
Input Bias Current		**-1.0**	-	**1.0**	µA
Operating Range (Excluding Offset)		**0**	-	**0.5**	V
Threshold Hysteresis		**33**	52	**70**	mV
Threshold Offset		**78**	104	**129**	mV
AC Dropout Disable Delay		-	32	-	ms
OUT					
High Level Output Voltage (VOH)	V_{OUT} @ 0mA - V_{OUT} @ -100mA, VDD = 8V operating, RAMP = 0V	-	0.35	**1.2**	V
Low Level Output Voltage (VOL)	V_{OUT} @ 100mA, VDD = 8V operating	-	0.7	**1.2**	V
Rise Time	C_{LOAD} = 2.2nF, VDD = 8V, $t_{90\%}$ - $t_{10\%}$	-	35	**55**	ns
Fall Time	C_{LOAD} = 2.2nF, VDD = 8V, $t_{10\%}$ - $t_{90\%}$	-	25	**40**	ns
Output Clamp Voltage	VDD = 20V, I_{LOAD} = -10µA	**10.5**	12.0	**13.4**	V
Unbiased Output Voltage Clamp	VDD = 6V, I_{LOAD} = 5mA	-	-	**1.9**	V
PWMOUT					
High Level Output Voltage (VOH)	V_{OUT} @ 0mA - V_{OUT} @ -10mA, VDD = 8V operating	-	0.8	**1.2**	V
Low Level Output Voltage (VOL)	V_{OUT} @ 10mA, VDD = 8V operating	-	0.8	**1.2**	V
Rise Time	C_{LOAD} = 1nF, VDD = 8V operating, $t_{90\%}$ - $t_{10\%}$	-	160	**240**	ns
Fall Time	C_{LOAD} = 1nF, VDD = 8V operating, $t_{10\%}$ - $t_{90\%}$	-	160	**240**	ns
Output Voltage Clamp	VDD = 20V, I_{LOAD} = -10µA	**10.5**	12.0	**13.4**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram - ISL1904" on page 2 and "Typical Application schematics" beginning on page 3. V_{DD} = 17V, R_{RAMP} = 54kΩ, C_{RAMP} = 470pF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C; **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Unbiased Output Voltage Clamp	VDD = 6V, I_{LOAD} = 3mA	-	-	**1.9**	V
Frequency		**291**	320	**349**	Hz
Maximum Duty Cycle	REFIN = 0.5V	-	-	**100**	%
Minimum On-Time	REFIN = 0V	-	-	**0.5**	µs
OVP					
OVP Threshold		**1.46**	1.50	**1.54**	V
OVP Hysteresis		**10**	20	**27**	µA
Input Bias Current		**-1.0**	-	**1.0**	µA
OVP Clamp Voltage	I_{OVP} = 1mA	**5.4**	-	**7.0**	V
THERMAL PROTECTION					
Thermal Shutdown	(Note 8)	**150**	160	**170**	°C
Hysteresis	(Note 8)	-	25	-	°C

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Limits established by characterization and are not production tested.

Test Waveforms and Circuits

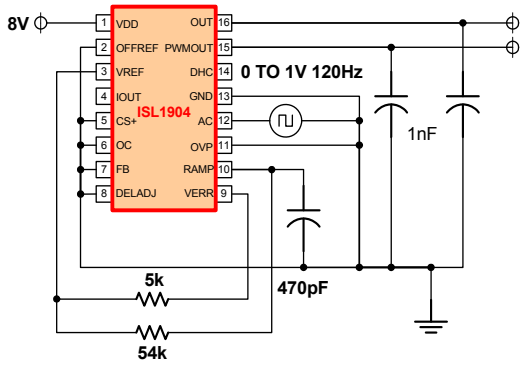


FIGURE 2. RISE/FALL TIME TEST CIRCUIT

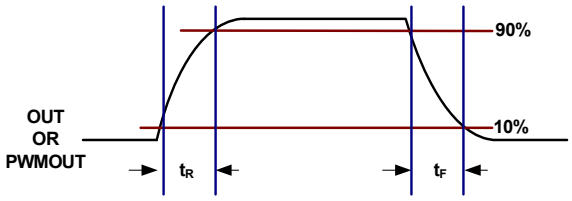


FIGURE 3. RISE/FALL TIMES

Test Waveforms and Circuits (Continued)

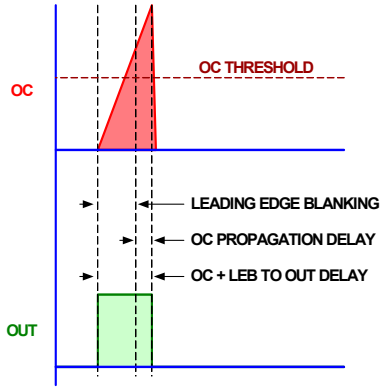


FIGURE 4. OC +LEB TO OUT DELAY

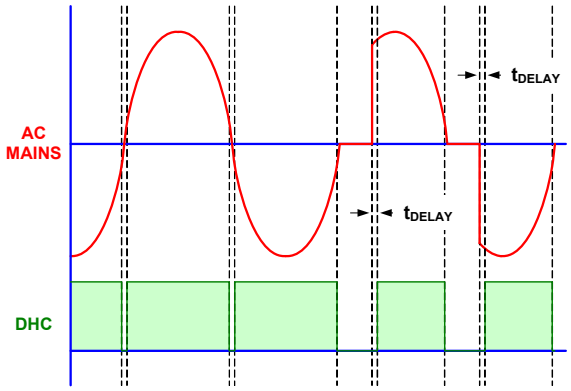


FIGURE 5. AC MAINS TO DHC TIMING

Typical Performance Curves

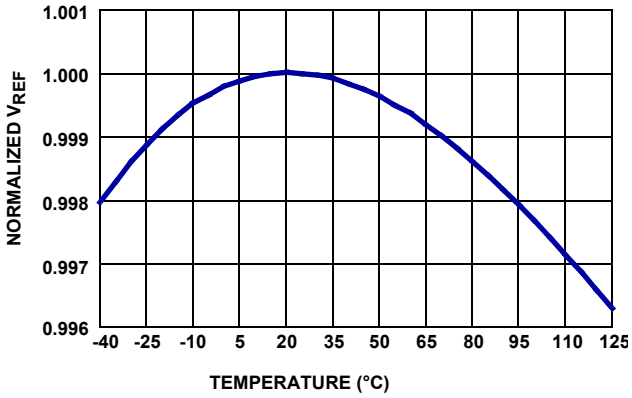


FIGURE 6. REFERENCE VOLTAGE vs TEMPERATURE

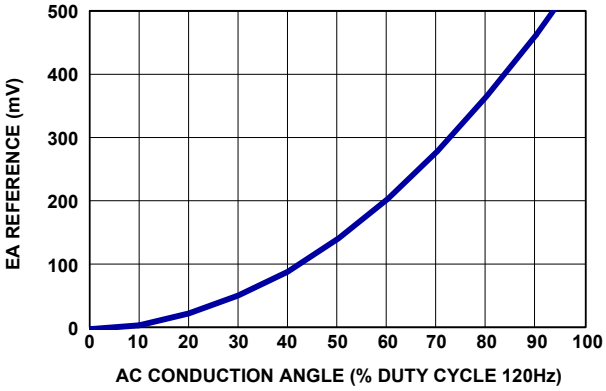


FIGURE 7. EA REFERENCE vs AC SIGNAL DUTY CYCLE

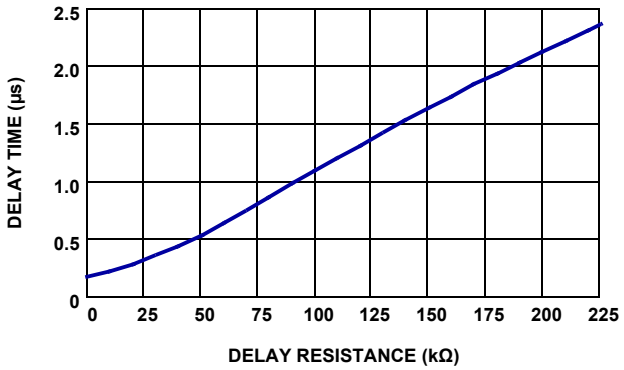


FIGURE 8. DELAY vs DELADJ RESISTANCE

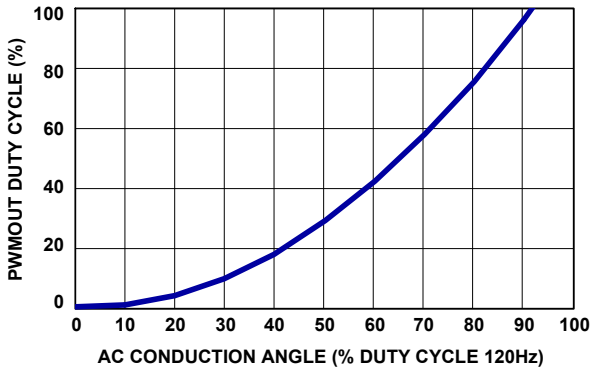


FIGURE 9. PWMOUT DUTY CYCLE vs AC SIGNAL DUTY CYCLE

Functional Description

Features

The ISL1904 LED driver is an excellent choice for low cost. AC mains powered single conversion LED lighting applications. It provides active power factor correction (PFC) to achieve high power factor using critical conduction mode operation, and incorporates additional features for compatibility with triac-based dimmers. Furthermore, it uses primary side current sensing to regulate the output current, eliminating the need to cross the isolation boundary to close the feedback control loop. The ISL1904 includes support for both PWM and DC current dimming of the output.

Oscillator

The ISL1904 uses a critical conduction mode (CrCM) algorithm to control the switching behavior of the converter. The ON-time of the primary power switch is held virtually constant by the low bandwidth control loop (in PFC applications). The OFF-time duration is determined by the time it takes the current or voltage to decay during the flyback period. When the *mmf* (magneto motive force) of the transformer decays to zero, the winding currents are zero and the winding voltages collapse. Either may be monitored and used to initiate the next switching cycle. The ISL1904 monitors the CrCM condition using the CS+ signal. It can be used to monitor either current or voltage.

Additionally, there is a user adjustable threshold, DELADJ, to delay the initiation of the next switching cycle to allow the drain-source voltage of the primary switch to ring to a minimal. This allows quasi-ZVS operation to reduce capacitive switching losses and improve efficiency. See “Quasi-Resonant Switching” on page 18.

By its nature the converter operation is variable frequency. There are both minimum and maximum frequency clamps that limit the range of operation. The minimum frequency clamp prevents the converter from operating in the audible frequency range. The maximum frequency clamps prevents operating at very high frequencies that may result in excessive losses.

An individual switching period is the sum of the ON-time, the OFF-time, and the restart delay duration. The ON-time is determined by the control loop error voltage, VERR, and the RAMP signal. As its name implies, the RAMP signal is a linearly increasing signal that starts at 0V and ramps to a maximum of VERR/5 to 235mV. RAMP requires an external resistor and capacitor connected to VREF to form an RC charging network. If VERR is at its maximum level of VREF, the time required to charge RAMP to ~850mV determines the maximum ON-time of the converter. RAMP is discharged every switching cycle when the ON-time terminates.

The OFF-time duration is determined by the design of the transformer, which depends on the required energy storage/transfer and the inductance of the windings. The transformer design also determines the maximum ON-time that can be supported without saturation, so, in reality, the transformer design is critical to every aspect of determining the switching frequency range. The design methodology is similar to designing a discontinuous mode (DCM) flyback transformer except with the constraint that it must operate at the DCM/CCM boundary at maximum load and minimum input voltage. The difference is that the converter will always operate at the DCM/CCM boundary, whereas a DCM converter will be more discontinuous as the input voltage increases or the load decreases. In PFC applications, the design is further complicated by the input voltage waveform, a rectified sinewave.

Once the output power, Po, the output current, Io, the output voltage, Vo, and the minimum input AC voltage are known, the transformer design can be started. From the minimum AC input voltage, the minimum DC equivalent (RMS) input voltage must be determined. In PFC applications, the converter behaves as if the input voltage is an equivalent DC value due to the low control loop bandwidth. Po determines the amount of energy that must be stored in the transformer on each switching cycle, but must be corrected for efficiency. This includes leakage inductance losses, winding losses, and all secondary side losses. This can be estimated as a portion of the total losses, or as is typically done, may be assigned all of the losses.

A typical minimum operating frequency and maximum duty cycle must be selected. These are somewhat arbitrary in their selection, but do ultimately determine core size. The typical frequency is what occurs when the instantaneous rectified input AC voltage is exactly at the equivalent DC value. The frequency will be higher when the instantaneous input voltage is lower, and lower when the instantaneous input voltage is higher. However, the duty cycle at the equivalent DC input voltage determines the ON-time for the entire AC half-cycle (PFC applications). The ON-time is constant due to the low bandwidth control loop, but the OFF-time and duty cycle vary with the instantaneous input voltage since the peak switch current follows V = Ldi/dt.

The typical frequency may require adjustment once the initial calculations are complete to see if the operating frequency at the peak of the minimum AC input voltage is acceptable. A rule of thumb is to select the typical frequency 25% higher than the absolute lowest desired frequency that occurs when operating at the peak of the minimum input AC voltage.

$$P_{IN} = \frac{P_o}{\eta} \quad W \qquad \text{(EQ. 1)}$$

TABLE 1. OSCILLATOR DEFINITIONS

V_{mINrms} =	Minimum RMS input voltage
$V_{maxINrms}$ =	Maximum RMS input voltage
η =	Efficiency
$f_{min(avg)}$ =	Typical frequency when V_{IN} (instantaneous) = minimum $V_{IN(rms)}$
D_{max} =	Maximum typical duty cycle desired
Dmin =	Minimum typical duty cycle
$t_{ON(MAX)}$ =	$f_{typ(avg)}$ x D_{max}
t_{ON}	ON-time of the power FET controlled by OUT
t_{OFF}	OFF-time duration required for CrCM operation
Ls =	Secondary inductance
Lp =	Primary inductance
Nsp =	Transformer turns ratio, Ns/Np
Ip(peak) =	Peak primary current within a switching cycle
t_{delay} =	User adjustable delay before the next switching cycle begins

The first calculation required is to determine the required secondary inductance shown by Equation 2.

$$L_s = \frac{V_o \cdot (1 - D_{max})^2}{f_{typ(avg)} \cdot 2 \cdot I_o} \quad H \qquad \text{(EQ. 2)}$$

The turns ratio N_{sp} is calculated next in Equation 3.

$$N_{sp} = \frac{V_o \cdot (1 - D_{max})}{\eta \cdot V_{mINrms} \cdot D_{max}} \qquad \text{(EQ. 3)}$$

Knowing the secondary inductance and the turns ratio, the primary inductance can be calculated by using Equation 4.

$$L_p = \frac{L_s}{N_{sp}^2} \quad H \qquad \text{(EQ. 4)}$$

With this information, the lowest switching frequency, which occurs at maximum load and at the peak instantaneous input voltage at the minimum RMS voltage, can be determined. By selecting the maximum duty cycle and a typical average frequency, the ON-time is already determined by Equation 5.

$$t_{ON} = \frac{D_{max}}{f_{min(avg)}} \quad s \qquad \text{(EQ. 5)}$$

The primary peak current at the end of the ON-time is shown in Equation 6:

$$I_{p(peak)} = \frac{V_{rms} \cdot \sqrt{2} \cdot t_{ON}}{L_p} \quad A \qquad \text{(EQ. 6)}$$

The peak secondary current is the peak primary current divided by the transformer turns ratio shown in Equation 7.

$$I_{s(peak)} = \frac{I_{p(peak)}}{N_{sp}} \quad A \qquad \text{(EQ. 7)}$$

And the OFF-time is shown in Equation 8:

$$t_{OFF} = \frac{L_s \cdot I_{s(peak)}}{V_o} \quad s \qquad \text{(EQ. 8)}$$

The lowest switching frequency is the reciprocal of the sum of the ON-time, the OFF-time, and the delay time is shown in Equation 9.

$$f_{min} = \frac{1}{t_{ON} + t_{OFF} + t_{delay}} \quad Hz \qquad \text{(EQ. 9)}$$

The delay time can be approximated if the equivalent drain-source capacitance (C_{oss}) of the primary switch is known. This value should also include any parasitic capacitance on the drain node. These parameters may not be known during the early stages of the design, but are typically on the order of 300ns to 500ns.

$$t_{delay} \approx \frac{\pi \cdot \sqrt{L_p \cdot (C_{oss} + C_{other})}}{2} \quad s \qquad \text{(EQ. 10)}$$

If the lowest frequency does not meet the requirements, then iterative calculations may be required.

The highest frequency is determined by the shortest ON-time summed with t_{delay}. The shortest ON-time occurs at high line and minimum load, and occurs at or near the AC zero crossing when the primary (and secondary) current is zero. The minimum non-zero ON-time the ISL1904 can produce is ~100ns, suggesting an operating frequency above 1MHz. In any event the maximum frequency clamp would limit the frequency to about 1MHz. Once the primary and secondary inductances are known, the general formulae to calculate the ON-time and OFF-time at an equivalent DC input voltage are shown by Equations 11 and 12:

$$t_{OFF} = \frac{2 \cdot L_s \cdot I_o}{V_o} \cdot \left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{INrms}}\right) \quad s \qquad \text{(EQ. 11)}$$

$$t_{ON} = \frac{2 \cdot L_p \cdot N_{sp} \cdot I_o}{V_{INrms}} \cdot \left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{INrms}}\right) \quad s \qquad \text{(EQ. 12)}$$

It is clear from the equations there is a linear relationship between load current and frequency. At some light load the frequency will be limited by the maximum frequency clamp. There is an inverse relationship between the input voltage and frequency and its effect is restricted by the typical input voltage range.

It should be noted, however, that the above equations assume full conduction angle of the AC mains. When conduction angle modulating dimmers are used to block a portion of each AC half-cycle, the switching currents remain essentially unchanged during the conduction portion of the AC half-cycle as the conduction angle is reduced. The conduction angle is reduced, not the amplitude of the waveform envelope. The result being the steady state frequency behavior will not vary much as the conduction angle is reduced.

Soft-Start Operation

Soft-start is not user adjustable and is fixed at ~ 350ms. Both the duty cycle and control loop reference have soft-start. This ensures a well behaved closed loop soft-start that results in virtually no overshoot.

AC Detection and Reference Generation

The ISL1904 creates a 0 to 0.5V reference for the LED current control loop by directly measuring the conduction angle of the AC input voltage. The reference changes only with conduction angle and is virtually unaffected by variation in either voltage amplitude or frequency.

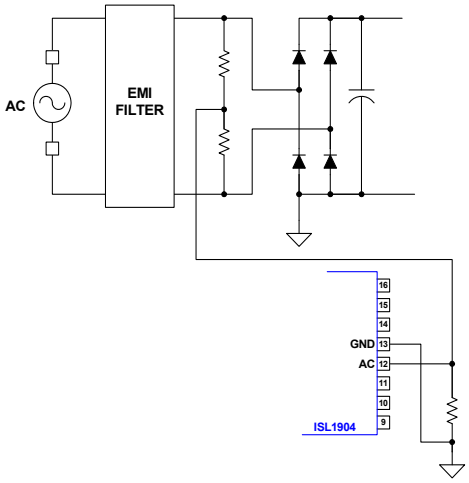


FIGURE 10. AC DETECTION

The ISL1904 detects the conduction angle using a divider network across the AC line and connected to the AC pin, although it can also be located after the AC bridge rectifier. The advantage to sensing the AC voltage directly, rather than the rectified voltage, is that there is no error in detecting the AC zero crossing. If monitored after the AC rectifier bridge, the AC signal tracks the filter capacitor voltage, which may not discharge in phase with the AC voltage. This can lead to incorrect detection of the AC zero crossing. At light load, the filter capacitor may not fully discharge before the AC voltage begins to increase again, resulting in no detection of the AC zero crossing at all.

The AC pin and has an input range of 0 to 4V. The peak of the input signal should range between 1 and 4 volts for uncompromised accuracy. The AC detection circuit measures both the duration of the AC conduction angle and the half-cycle duration. By comparing the two every half-cycle, the detection circuit creates a frequency independent reference that is updated each AC half-cycle.

In the event of an AC outage, the AC mains frequency reference is lost. The ISL1904 will force the reference to zero volts and reset the soft-start circuit approximately 35ms after the last AC zero crossing is detected. If AC is held above it detection threshold, the internal reference is forced to its maximum of 0.5V.

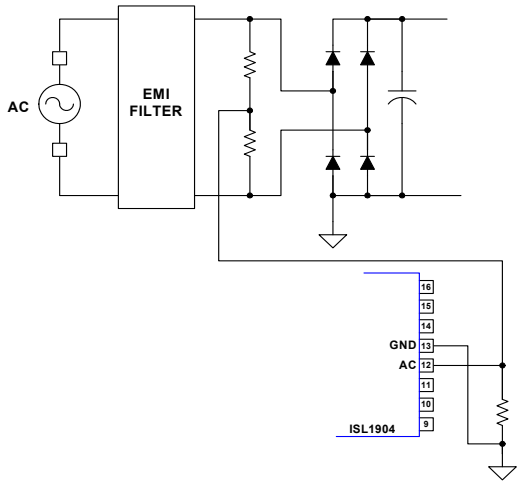


FIGURE 11. AC DETECTION

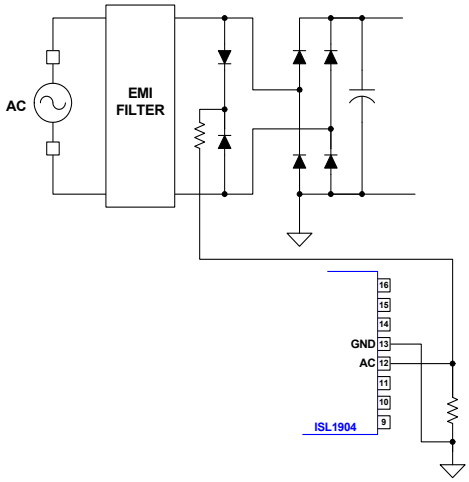


FIGURE 12. ALTERNATE AC DETECTION

AC may be directly coupled to a 90Hz to 130Hz PWM signal to generate a reference if dimming is desired without using an AC dimmer.

Primary Current Sensing

The ISL1904 is configured to regulate the output current by monitoring the primary switch current at the OC pin. The peak primary switch current is captured, processed, and output on IOUT as a PWM voltage signal modulated in proportion to the output current. The IOUT PWM frequency is the same as the converter switching frequency and its amplitude is equivalent to 4x the peak switch current during the previous ON-time. It must be scaled and filtered before being input to the control loop at the FB pin. The required filter time constant depends on the compensated error amplifier bandwidth. The filter bandwidth must be greater than the control loop bandwidth, typically an order of magnitude greater, but it is generally not necessary to filter the IOUT PWM signal to a low ripple DC level. The compensated error amplifier, with its limited bandwidth, performs that function.

The OC pin also provides cycle-by-cycle overcurrent protection. The ON-time is terminated if OC exceeds 0.6V nominal. There is ~120ns of leading edge blanking (LEB) on OC to minimize or eliminate external filtering.

Dimming

The ISL1904 supports both PWM and DC current modulation dimming. In either case, the control loop determines the average current delivered to the load.

The usual method of dimming an LED string is to modulate the DC current through the string. DC current dimming is the lower cost method, but results in a non-linear dimming characteristic due to the increasing efficacy of the LEDs as current is reduced. PWM dimming results in linear dimming behavior.

For PWM dimming, an external FET, controlled by PWMOUT, is required to gate the drive signal to the switching FET. See "Typical Application - Dimmable DC Input Boost Converter" on page 5 for an example. When PWMOUT is high, the main switching FET operates normally. When PWMOUT is low, the main switching FET gate signal is blocked and the converter is effectively off. This method is typically used when the LED string is not ground referenced.

Another method uses an external FET to interrupt the LED load current as shown in "Typical Application - Isolated Flyback with PWM Dimming" on page 4.

Regardless of the dimming method used, the control loop determines the average current delivered to the load. It does not matter if the load current is DC or pulsed as long as the control loop bandwidth is sufficiently lower than the pulsed current frequency. The converter control loop and output capacitance operate to filter and average the converter output current independently of the actual load current waveform.

The dimming PWM and control loop are linked together such that the PWM duty cycle tracks the main control loop reference setpoint. If the control loop is set for 50% load, for example, the dimming PWM duty cycle is set for 50%. The LED current will be at 100% load for 50% of the time and 0% load for 50% of the time, which averages to the 50% average load setpoint. See Figures 7 and 9 for a graphical representation of the relationship between the control loop reference and PWMOUT duty cycle. It should be noted that the PWMOUT duty cycle is not allowed to go to zero.

Control Loop

The control loop configuration is user adjustable with the selection of the external compensation components. For applications requiring power factor correction (PFC), a very low bandwidth integrator is used, typically 20Hz or less. In other applications, the control loop bandwidth can be increased as required like any other externally compensated voltage mode PWM controller.

Referring to Figure 13, the FET switching current flowing through Rs, is applied to the OC pin of the ISL1904. The peak signal is sampled, buffered, and output on IOUT as a PWM signal with a gain of four and a duty equal to the complement of the converter duty cycle (OUT). The voltage on IOUT, when averaged, is a scaled representation of the maximum steady state output current, Io.

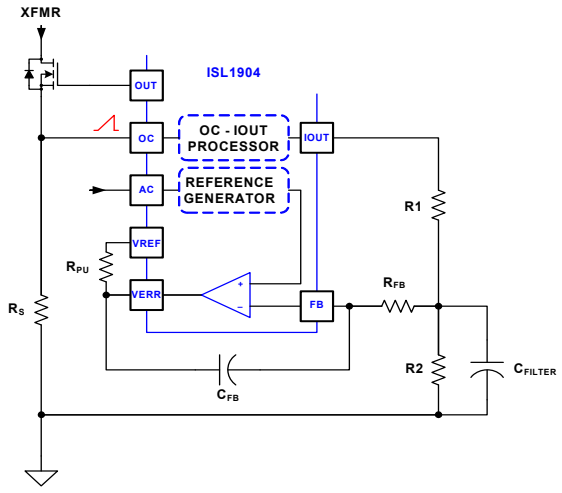


FIGURE 13. CONTROL LOOP CONFIGURATION

$$\overline{IOUT} = \frac{8 \cdot Rs}{N_{sp}} \cdot I_o \quad V \qquad \text{(EQ. 13)}$$

where $\overline{IOUT}$ is the average value of IOUT. $\overline{IOUT}$ must be scaled such that at maximum output current Io is equal to the maximum reference level (nominally 0.530V), while also limiting the maximum peak primary OC signal to less than the overcurrent threshold of 0.6V.

$$R_s = \frac{V_{OC}}{2 \cdot \sqrt{2} \cdot N_{sp} \cdot I_{oCL}\left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{mINrms}}\right)} \quad \Omega \qquad \text{(EQ. 14)}$$

where I_{oCL} is the output current limit threshold, V_{OC} is the current limit threshold, and Rs is the current sensing resistor. Once the value of Rs is determined, Equation 14 can be used to solve for the level of OC at any steady state current and input voltage when Io is substituted for Io_{CL}.

$$V_{OC(SS)} = R_s \cdot 2 \cdot \sqrt{2} \cdot N_{sp} \cdot I_o\left(1 + \frac{L_p \cdot N_{sp} \cdot V_o}{L_s \cdot V_{INrms}}\right) \quad V \qquad \text{(EQ. 15)}$$

where $V_{OC(SS)}$ is the peak steady state value of OC corresponding for the specific operating conditions.

As indicated previously, $\overline{IOUT}$ must be scaled properly prior to connection to the FB input. Using Equation 13, and the value of Rs obtained from Equation 14, the divider network to scale $\overline{IOUT}$ can be determined.

The EA compensation depends on the bandwidth required for the application. For PFC applications the BW is necessarily limited to 20Hz or less. For other applications, the BW may be increased as required up to about 1/5 of the lowest switching frequency allowed as described in "Oscillator" on page 14. For the low BW applications a Type I compensation configuration is adequate. For higher BW applications, a Type II configuration may be required. Figure 13 shows the Type I configuration. Figures 13 and 14 show the Type I and Type II configurations, respectively.

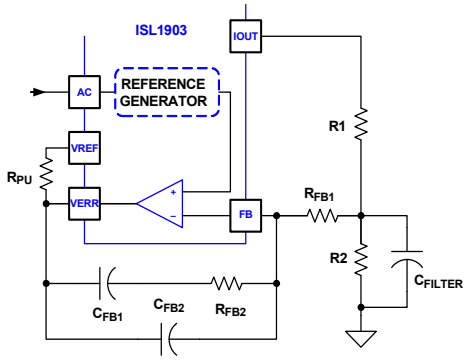


FIGURE 14. TYPE II EA CONFIGURATION

OVP

The ISL1904 has independent overvoltage protection accessed through the OV pin. There is a nominal 20µA switched current source used to create hysteresis. The current source is active only during an OV fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis voltage is a

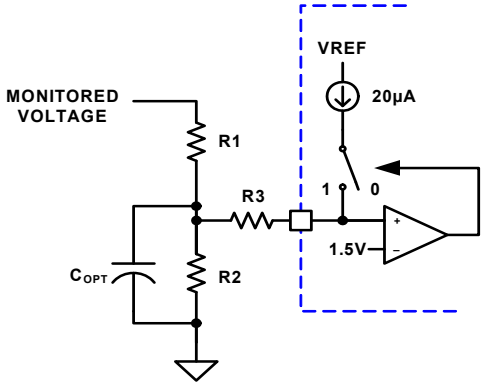


FIGURE 15. OV HYSTERESIS

function of the external resistor divider impedance.

$$V_{ov(rising)} = 1.5 \cdot \frac{(R1 + R2)}{R2} \quad V \qquad \text{(EQ. 16)}$$

If the divider formed by R1 and R2 is sufficiently high impedance, R3 is not required, and the hysteresis is:

$$\Delta V = 20 \cdot 10^{-6} \cdot R1 \quad V \qquad \text{(EQ. 17)}$$

If that does not result in the desired hysteresis then R3 is needed, and the hysteresis is:

$$\Delta V = 20 \cdot 10^{-6} \cdot \left(R1 + R3 \cdot \frac{(R1 + R2)}{R2}\right) \quad V \qquad \text{(EQ. 18)}$$

If the OV signal requires filtering, the filter capacitor, Copt, should be placed as shown in Figure 11. The current hysteresis provides great flexibility in setting the magnitude of the hysteresis voltage, but it is susceptible to noise due to its high impedance. If the hysteresis was implemented as a fixed voltage instead, the signal could be filtered with a small capacitor placed between the OV pin and signal ground. This technique does not work well when the hysteresis is a current source because a current source takes time to charge the filter capacitor. There is no instantaneous change in the threshold level rendering the current hysteresis ineffective. To remedy the situation, the filter capacitor must be separated from the OV pin by R3. The capacitor and R3 must be physically close to the OV pin.

OFFREF Control

The ISL1904 provides the ability to disable the output based on the level of the control loop reference, set by the AC conduction angle on the AC pin. Setting OFFREF to a voltage between 0 and 0.6V determines the threshold voltage that disables the output.

$$REFIN(off) = OFFREF - 0.100 \quad V \qquad \text{(EQ. 19)}$$

OFFREF allows the designer to disable the output at a pre-determined load current to prevent undesirable behavior such as at light loading conditions when there may be insufficient current to maintain the holding current in a triac-based dimmer. Setting OFFREF to less than 100mV disables this feature. OFFREF has a nominal hysteresis of 50mV.

$$REFIN(on) = OFFREF - 0.050 \quad V \qquad \text{(EQ. 20)}$$

Quasi-Resonant Switching

The ISL1904 uses critical conduction mode PWM control algorithm. Near zero voltage switching (ZVS) or quasi-resonant valley switching, as it is sometimes referred to, can be achieved in the flyback topology by delaying the next switching cycle after the transformer current decays to zero (critical conduction mode). The delay allows the primary inductance and capacitance to oscillate, causing the switching FET drain-source voltage to ring down to a minimal. If the FET is turned on at this minimal, the capacitive switching loss ($1/2\ CV^2$) is greatly reduced.

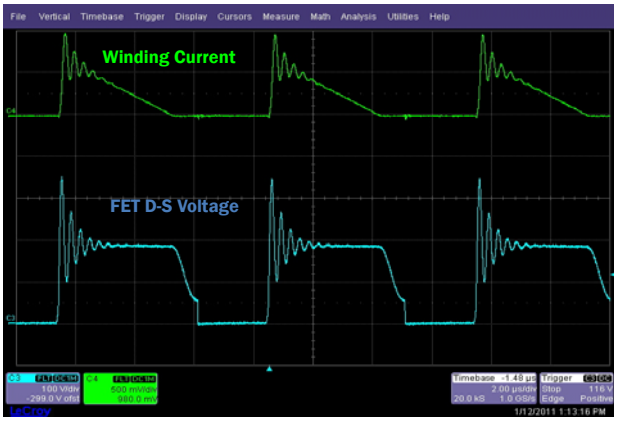


FIGURE 16. QUASI-RESONANT NEAR-ZVS SWITCHING

The delay duration is set with a resistor from DELADJ to ground. Figure 8 on page 13 shows the graphical relationship between the delay duration and the value of the DELADJ resistance. The

relationship is linear for resistance values greater than ~ 20 kΩ and can be estimated using Equation 21.

$$t_{delay} \approx 73.33 + 10.2 \cdot R_{DELADJ}(k\Omega) \quad ns \qquad \text{(EQ. 21)}$$

DHC (Dimmer Holding Current)

The DHC pin provides a method to pre-load a triac-based dimmer during the period of time when the AC is blocked, with overlap at each edge of the AC conduction period to ensure adequate holding current. DHC is an open drain FET used to control an external resistor to act as the load.

DHC controls a resistor on the external high voltage start-up bias regulator. See “Typical Application - Dimmable Isolated Flyback” on page 3 for an example of its usage. Note the series resistor and diode connecting VDD to the gate of the start-up bias FET. It is required to keep the device on when the AC voltage is near the zero-crossing.

Gate Drive

The ISL1904 output is capable of sourcing and sinking up to 1A. The OUT high level is limited to the OUT clamp voltage or VDD, whichever is lower.

Thermal Protection

Internal die over-temperature protection is provided. An integrated temperature sensor protects the device should the junction temperature exceed +160°C. There is approximately +10°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. VDD and VREF should be bypassed directly to GND with good high frequency capacitance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 27, 2012	FN8286.1	Page 15: Changed Equation 6, from H to A. Equation 7, from H to A. Equation 8 Page 17: Changed Equation 14 from V to ohms
August 10, 2012	FN8286.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL1904

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

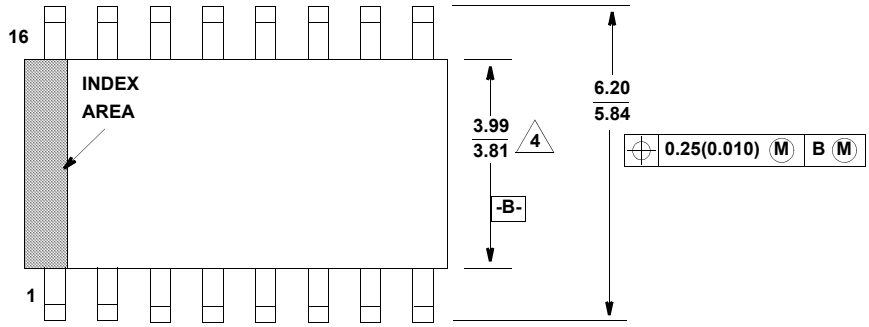
Package Outline Drawing

M16.15A

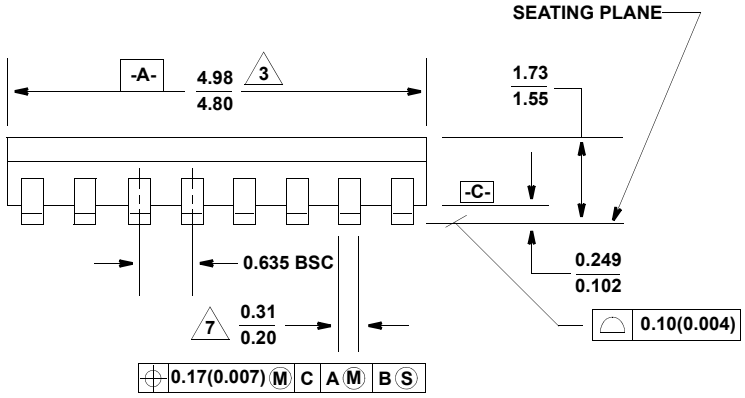
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (QSOP/SSOP)

0.150" WIDE BODY

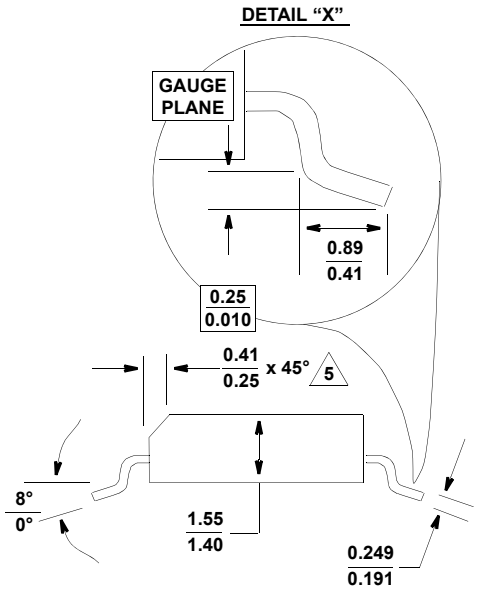
Rev 3, 8/12



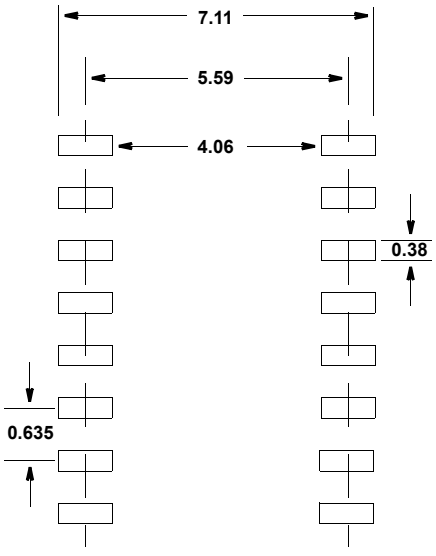
TOP VIEW



SIDE VIEW 1



SIDE VIEW 2



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Terminal numbers are shown for reference only.
7. Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
8. Controlling dimension: MILLIMETER.

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