ISL22313

Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power, I^2C Bus, 256 Taps

FN6421
Rev 1.00
August 18, 2016

The ISL22313 integrates a single digitally controlled potentiometer (DCP), control logic and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR control the position of the wiper. At power up the device recalls the contents of the DCP's IVR to the WR.

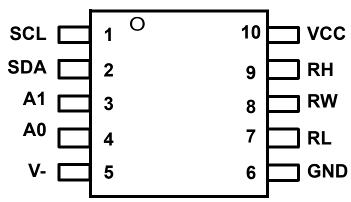
The ISL22313 also has 14 general purpose non-volatile registers that can be used as storage of lookup table for multiple wiper position or any other valuable information.

The ISL22313 features a dual supply, that is beneficial for applications requiring a bipolar range for DCP terminals between V- and VCC.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Pinout

ISL22313
(10 LD MSOP)
TOP VIEW



Features

- 256 resistor taps
- I^2C serial interface
  - Two address pins, up to four devices per bus
- Non-volatile EEPROM storage of wiper position
- 14 General Purpose non-volatile registers
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T≤+55°C
- Wiper resistance: 70Ω typical @ 1mA
- Standby current <2.5µA max
- Shutdown current <2.5µA max
- Dual power supply
  - VCC = 2.25V to 5.5V
  - V- = -2.25V to -5.5V
- DCP terminal voltage from V- to VCC
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40 to +125°C
- 10 Lead MSOP
- Pb-free plus anneal product (RoHS compliant)

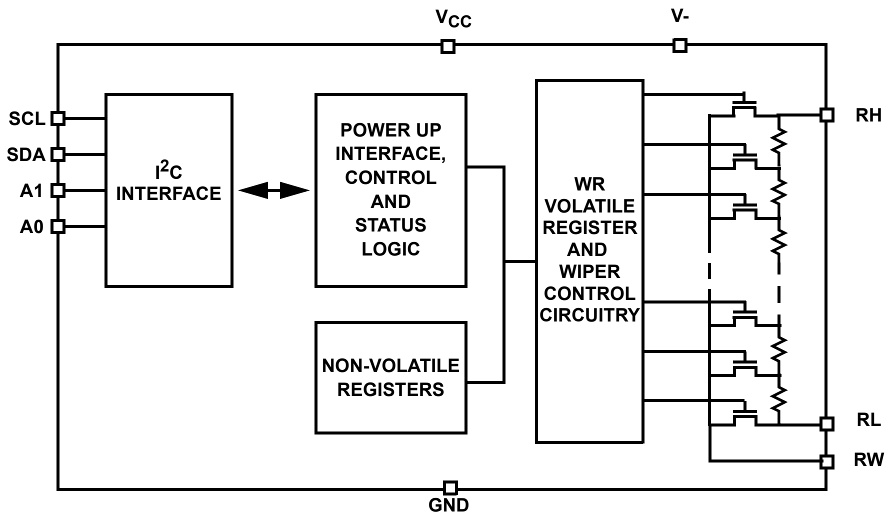
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL22313TFU10Z **(No longer available, recommended replacement: ISL22313UFU10Z)**	313TZ	100	-40 to +125	10 Ld MSOP	M10.118
ISL22313UFU10Z	313UZ	50	-40 to +125	10 Ld MSOP	M10.118
ISL22313WFU10Z	313WZ	10	-40 to +125	10 Ld MSOP	M10.118

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	SCL	Open drain I^2C interface clock input
2	SDA	Open drain Serial data I/O for the I^2C interface
3	A1	Device address input for the I^2C interface
4	A0	Device address input for the I^2C interface
5	V-	Negative supply pin
6	GND	Device ground pin
7	RL	"Low" terminal of DCP
8	RW	"Wiper" terminal of DCP
9	RH	"High" terminal of DCP
10	VCC	Power supply pin

Absolute Maximum Ratings

Storage Temperature . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . -0.3V to +6V
V- . . . . -6V to 0.3V
Voltage at any DCP Pin with
respect to GND. . . . . V- to V_{CC}
I_W (10s) . . . . ±6mA
Latchup . . . . Class II, Level A at +125°C
ESD
Human Body Model 3kV
Machine Model. 400V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
10 Lead MSOP. 120
Maximum Junction Temperature (Plastic Package). . . . . +150°C
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Full Industrial) . . . .-40°C to +125°C
Power Rating 15mW
V_{CC} . . . . 2.25V to 5.5V
V- . . . .-2.25V to -5.5V
Max Wiper Current Iw . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated. Limits are established by characterization.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
R_{TOTAL}	RH to RL resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RH to RL resistance tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±150		ppm/°C
		U, T option		±50		ppm/°C
V_{RH}, V_{RL}	DCP terminal voltage	V_{RH} and V_{RL} to GND	V-		V_{CC}	V
R_W	Wiper resistance	RH - floating, V_{RL} = V-, force I_W current to the wiper, I_W = (V_{CC} - V_{RL})/R_{TOTAL}		70	250	Ω
$C_H/C_L/C_W$ (Note 16)	Potentiometer capacitance	See Macro Model below.		10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins	Voltage at pin from GND to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ RL; V_{CC} @ RH; measured at RW, unloaded)						
INL (Note 9)	Integral non-linearity	W option	-1.5	±0.5	1.5	LSB (Note 5)
		U, T option	-1.0	±0.2	1.0	
DNL (Note 8)	Differential non-linearity	W option	-1.0	±0.4	1.0	LSB (Note 5)
		U, T option	-0.5	±0.15	0.5	
ZSerror (Note 6)	Zero-scale error	W option	0	1	5	LSB (Note 5)
		U, T option	0	0.5	2	
FSerror (Note 7)	Full-scale error	W option	-5	-1	0	LSB (Note 5)
		U, T option	-2	-1	0	
TC_V (Notes 10, 16)	Ratiometric temperature coefficient	DCP register set to 80 hex		±4		ppm/°C

Analog Specifications Over recommended operating conditions unless otherwise stated. Limits are established by characterization. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
f_{cutoff} (Note 16)	-3dB cut off frequency	Wiper at midpoint (80hex) W option (10k)		1000		kHz
		Wiper at midpoint (80hex) U option (50k)		250		kHz
		Wiper at midpoint (80hex) T option (100k)		120		kHz
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)						
RINL (Note 14)	Integral non-linearity	W option	-3	±1.5	3	MI (Note 11)
		U, T option	-1	±0.3	1	MI (Note 11)
RDNL (Note 13)	Differential non-linearity	W option	-1.5	±0.4	1.5	MI (Note 11)
		U, T option	-0.5	±0.15	0.5	MI (Note 11)
Roffset (Note 12)	Offset	W option	0	1	5	MI (Note 11)
		U, T option	0	0.5	2	MI (Note 11)
TC_R (Notes 15, 16)	Resistance temperature coefficient	DCP register set between 32 hex and FF hex		±50		ppm/°C

Operating Specifications Over the recommended operating conditions unless otherwise specified. Limits are established by characterization.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = +5.5V, V- = -5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		0.07	0.15	mA
		V_{CC} = +2.25V, V- = -2.25V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		0.02	0.05	mA
I_{V-1}	V- Supply Current (volatile write/read)	V- = -5.5V, V_{CC} = +5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-1	-0.18		mA
		V- = -2.25V, V_{CC} = +2.25V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-0.4	-0.06		mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = +5.5V, V- = -5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		1	2	mA
		V_{CC} = +2.25V, V- = -2.25V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		0.3	0.7	mA
I_{V-2}	V- Supply Current (non-volatile write/read)	V- = -5.5V, V_{CC} = +5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-2	-1.2		mA
	V- Supply Current (non-volatile write/read)	V- = -2.25V, V_{CC} = +2.25V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-0.7	-0.4		mA

Operating Specifications Over the recommended operating conditions unless otherwise specified. Limits are established by characterization. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, I^2C interface in standby state		0.2	1.5	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, I^2C interface in standby state		1	2.5	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, I^2C interface in standby state		0.1	1	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, I^2C interface in standby state		0.5	2	µA
$I_{V\text{-}SB}$	V- Current (standby)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, I^2C interface in standby state	-2.5	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, I^2C interface in standby state	-4	-3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, I^2C interface in standby state	-1.5	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, I^2C interface in standby state	-3	-1		µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V, V- = -5.5V @ +85°C, I^2C interface in standby state		0.2	1.5	µA
		V_{CC} = +5.5V, V- = -5.5V @ +125°C, I^2C interface in standby state		1	2.5	µA
		V_{CC} = +2.25V, V- = -2.25V @ +85°C, I^2C interface in standby state		0.1	1	µA
		V_{CC} = +2.25V, V- = -2.25V @ +125°C, I^2C interface in standby state		0.5	2	µA
$I_{V\text{-}SB}$	V- Current (standby)	V- = -5.5V, V_{CC} = +5.5V @ +85°C, I^2C interface in standby state	-2.5	-0.7		µA
		V- = -5.5V, V_{CC} = +5.5V @ +125°C, I^2C interface in standby state	-4	-3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +85°C, I^2C interface in standby state	-1.5	-0.3		µA
		V- = -2.25V, V_{CC} = +2.25V @ +125°C, I^2C interface in standby state	-3	-1		µA
I_{LkgDig}	Leakage current, at pins A0, A1, SDA, and SCL	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{DCP} (Note 16)	DCP wiper response time	SCL falling edge of last bit of DCP data byte to wiper new position		1.5		µs
$t_{ShdnRec}$ (Note 16)	DCP recall time from shutdown mode	SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on recall voltage	Minimum V_{CC} at which memory recall occurs	1.9		2.1	V
VCC Ramp	V_{CC} ramp rate		0.2			V/ms
t_D	Power-up delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			5	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
t_{WC} (Note 17)	Non-volatile Write cycle time			12	20	ms

Operating Specifications

Over the recommended operating conditions unless otherwise specified. Limits are established by characterization. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, SDA, and SCL input buffer LOW voltage		-0.3		0.3*V_{CC}	V
V_{IH}	A1, A0, SDA, and SCL input buffer HIGH voltage		0.7*V_{CC}		V_{CC} + 0.3	V
Hysteresis (Note 16)	SDA and SCL input buffer hysteresis		0.05*V_{CC}			V
V_{OL} (Note 16)	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
Cpin (Note 16)	A1, A0, SDA, and SCL pin capacitance				10	pF
f_{SCL}	SCL frequency				400	kHz
t_{sp}	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA} (Note 16)	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF} (Note 16)	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input data hold time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP condition hold time for read, or volatile only write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH} (Note 16)	Output data hold time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R (Note 16)	SDA and SCL rise time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 16)	SDA and SCL fall time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 16)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 16)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ

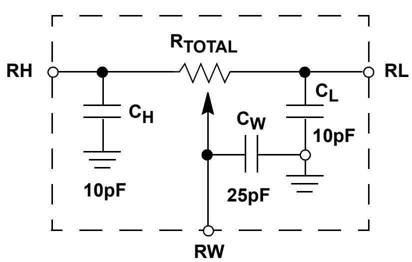
Operating Specifications Over the recommended operating conditions unless otherwise specified. Limits are established by characterization. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
$t_{SU:A}$	A1 and A0 setup time	Before START condition	600			ns
$t_{HD:A}$	A1 and A0 hold time	After STOP condition	600			ns

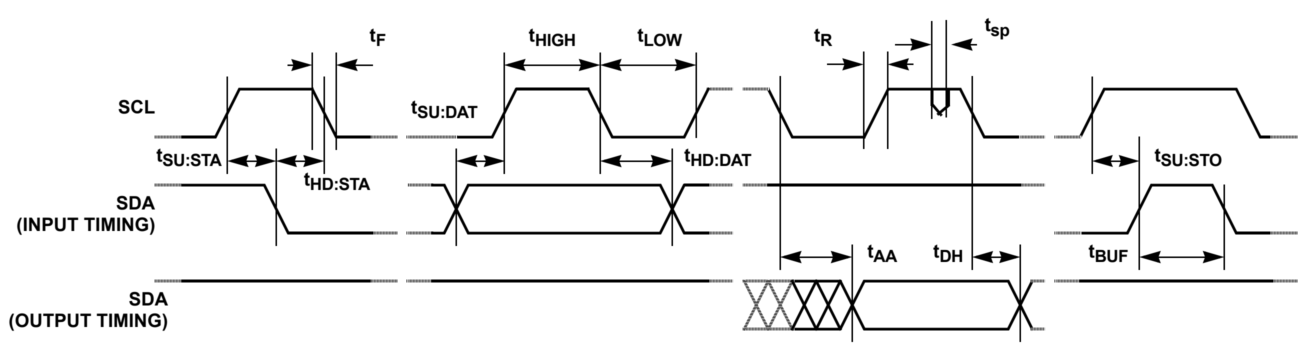
NOTES:

4. Typical values are for T_A = +25°C and 3.3V supply voltage.
5. LSB: $[V(R_W)_{255} - V(R_W)_0]/255$. $V(R_W)_{255}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
6. ZS error = $V(RW)_0/LSB$.
7. FS error = $[V(RW)_{255} - V_{CC}]/LSB$.
8. DNL = $[V(RW)_i - V(RW)_{i-1}]/LSB-1$, for i = 1 to 255. i is the DCP register setting.
9. INL = $[V(RW)_i - i \cdot LSB - V(RW)_0]/LSB$ for i = 1 to 255
10. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 255 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
11. MI = $|RW_{255} - RW_0|/255$. MI is a minimum increment. RW_{255} and RW_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
12. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{255}/MI, when measuring between RW and RH.
13. RDNL = $(RW_i - RW_{i-1})/MI - 1$, for i = 16 to 255.
14. RINL = $[RW_i - (MI \cdot i) - RW_0]/MI$, for i = 16 to 255.
15. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 255, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
16. Limits should be considered typical and are not production tested.
17. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I²C serial interface, to the end of the self-timed internal non-volatile write cycle.
18. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

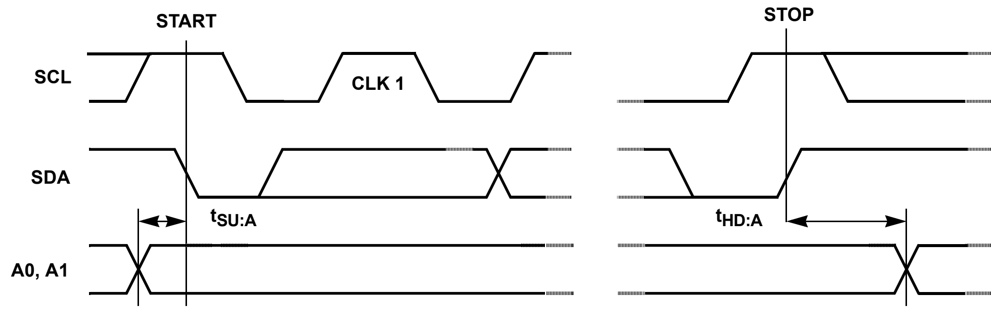
DCP Macro Model



SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

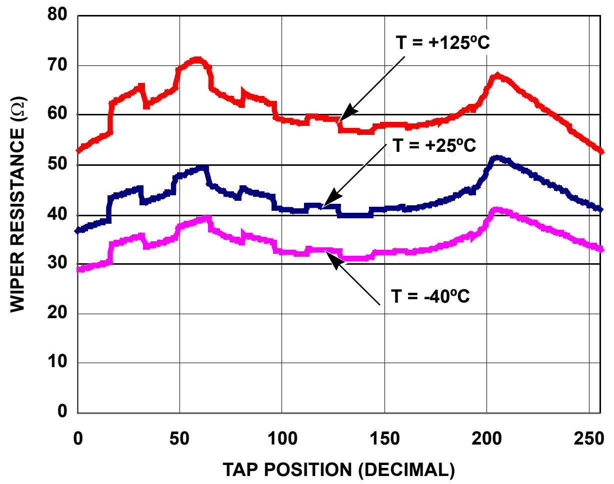


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

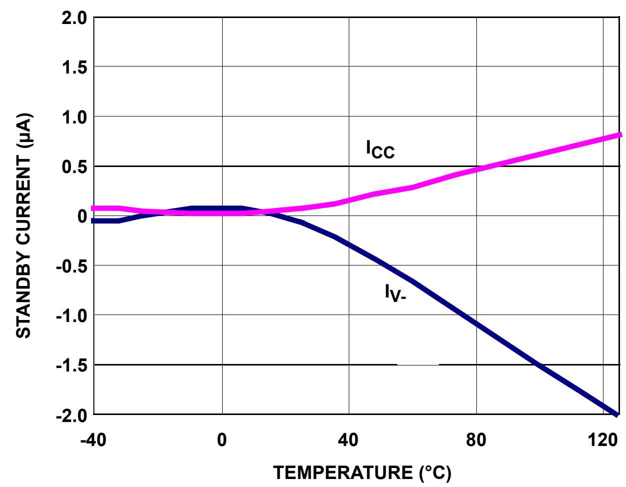


FIGURE 2. STANDBY I_{CC} AND I_{V-} vs TEMPERATURE

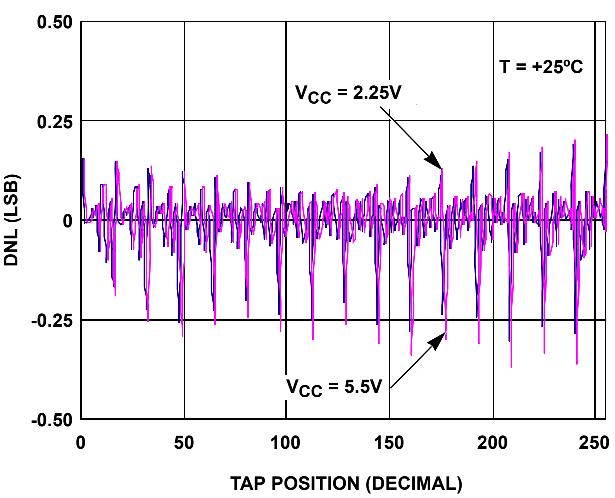


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

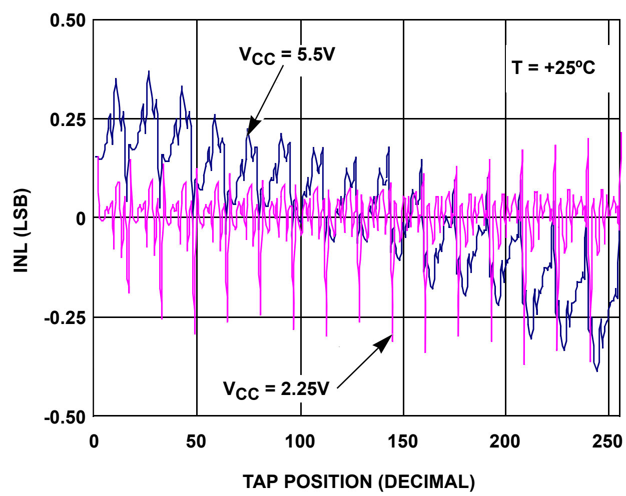


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

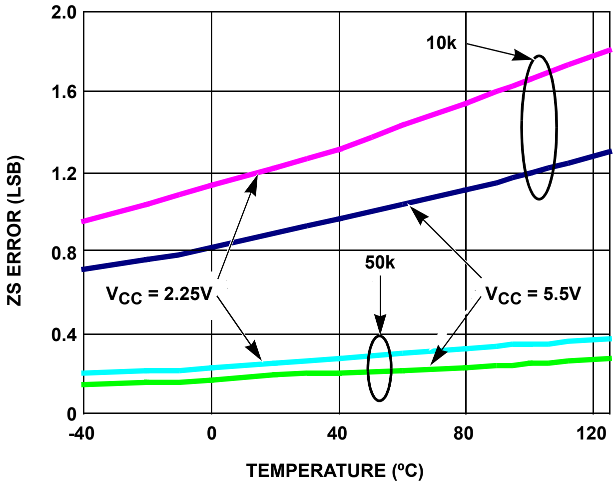


FIGURE 5. ZS ERROR vs TEMPERATURE

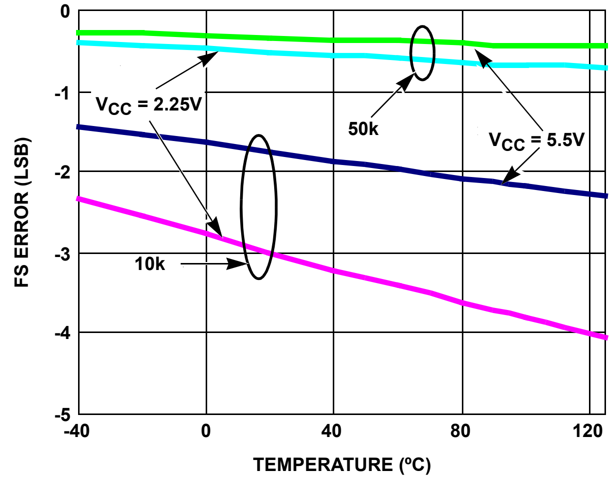


FIGURE 6. FS ERROR vs TEMPERATURE

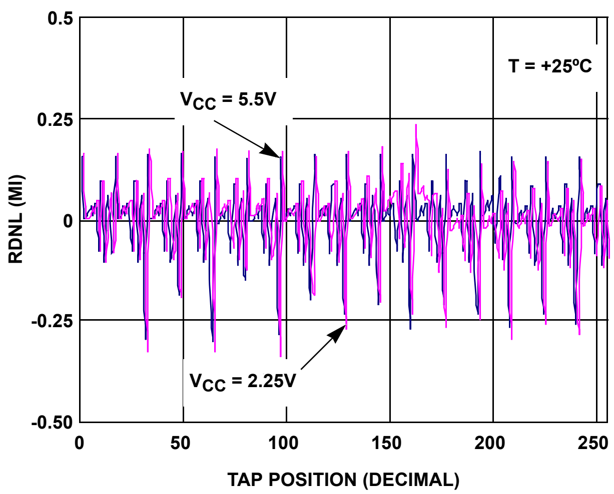


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

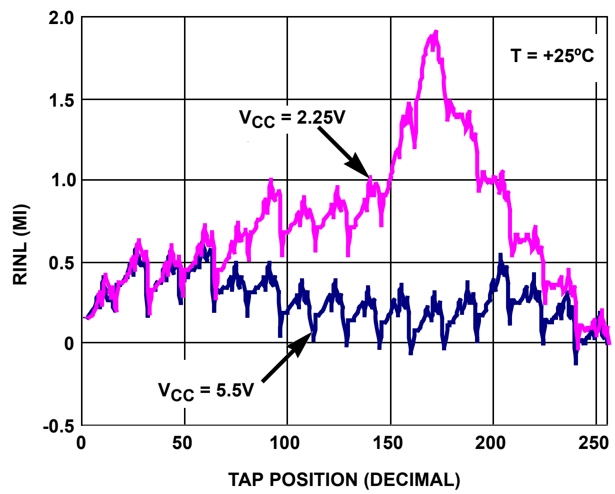


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

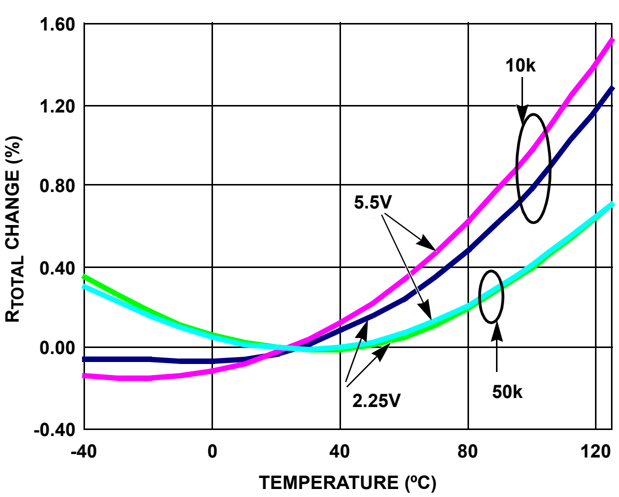


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

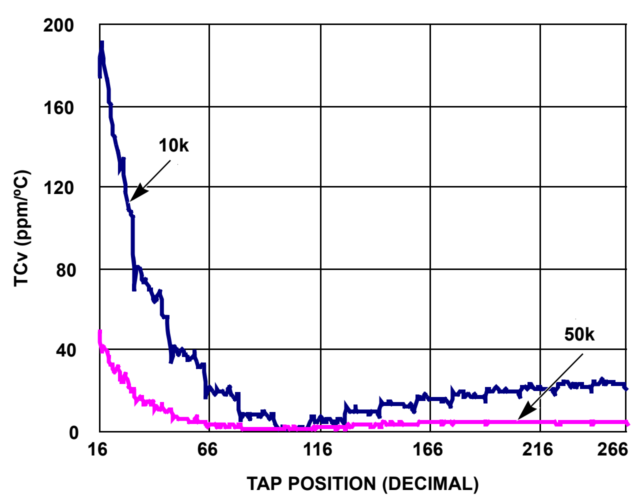


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

Typical Performance Curves (Continued)

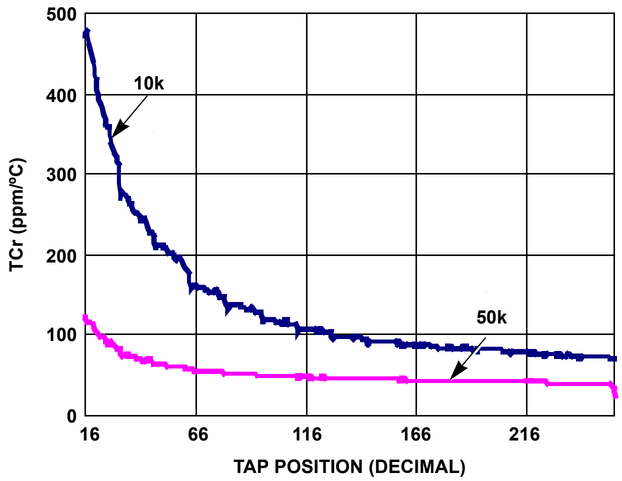


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

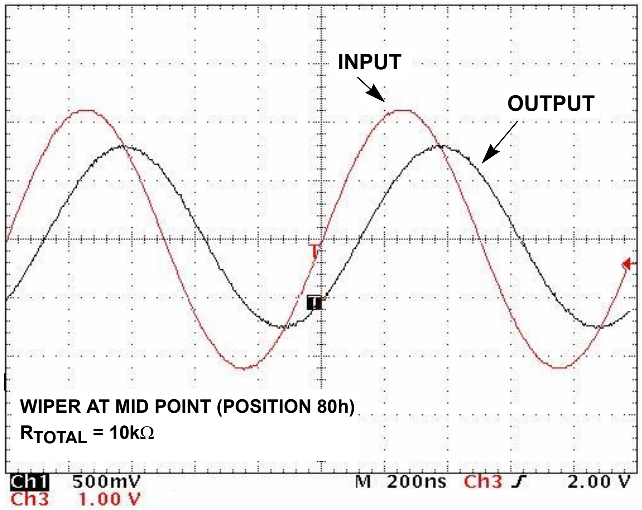


FIGURE 12. FREQUENCY RESPONSE (1MHz)

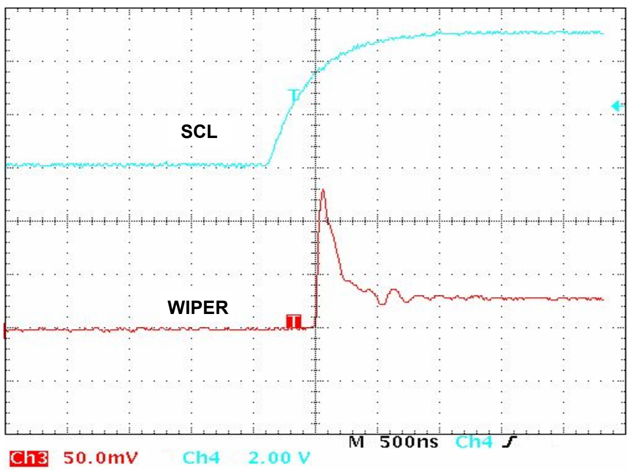


FIGURE 13. MIDSCALE GLITCH, CODE 7Fh TO 80h

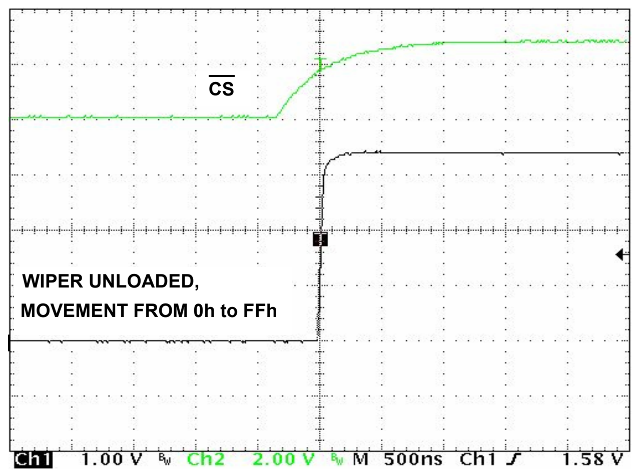


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometers Pins

RH and RL

The high (RH) and low (RL) terminals of the ISL22313 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 255 decimal, the wiper will be closest to RH, and with the WR set to 0, the wiper is closest to RL.

RW

RW is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

Bus Interface Pins

Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

Serial Clock (SCL)

This input is the serial clock of the I^2C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

Device Address (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22313. A maximum of four ISL22313 devices may occupy the I^2C serial bus (see Table 3).

Principles of Operation

The ISL22313 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR are recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[7:0]= 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR[7:0]= FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the position closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22313 is being powered up, the WR is reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reloaded with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL22313 contains one non-volatile 8-bit Initial Value Register (IVR), fourteen General Purpose non-volatile 8-bit registers and two volatile 8-bit registers: Wiper Register (WR) and Access Control Register (ACR). Memory map of ISL22313 is in Table 1. The non-volatile register (IVR) at address 0, contains initial wiper position and volatile register (WR) contains current wiper position.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
10	N/A	ACR
F	Reserved	
E	General Purpose	N/A
D	General Purpose	N/A
C	General Purpose	N/A
B	General Purpose	N/A
A	General Purpose	N/A
9	General Purpose	N/A
8	General Purpose	N/A
7	General Purpose	N/A
6	General Purpose	N/A
5	General Purpose	N/A
4	General Purpose	N/A
3	General Purpose	N/A
2	General Purpose	N/A
1	General Purpose	N/A
0	IVR	WR

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME	VOL	$\overline{SHDN}$	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note: Value is written to IVR register also is written to the WR. The default value of this bit is 0.

The $\overline{SHDN}$ bit (ACR[6]) disables or enables Shutdown mode. When this bit is 0, i.e. DCP is forced to end-to-end open circuit and RW is shorted to RL as shown on Figure 15. Default value of the $\overline{SHDN}$ bit is 1.

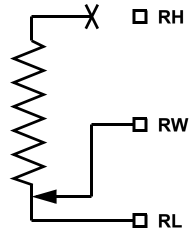


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

The WIP bit (ACR[5]) is a read-only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WR or ACR while WIP bit is 1.

I^2C Serial Interface

The ISL22313 supports an I^2C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22313 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL22313, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22313 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

The ISL22313 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22313 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 10100 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is "1" for a Read operation and "0" for a Write operation (see Table 3).

TABLE 3. IDENTIFICATION BYTE FORMAT

LOGIC VALUES AT PINS A1 AND A0, RESPECTIVELY

1	0	1	0	0	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

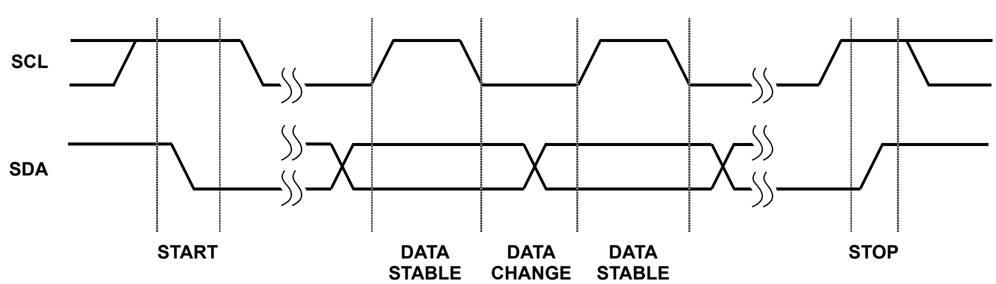


FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS

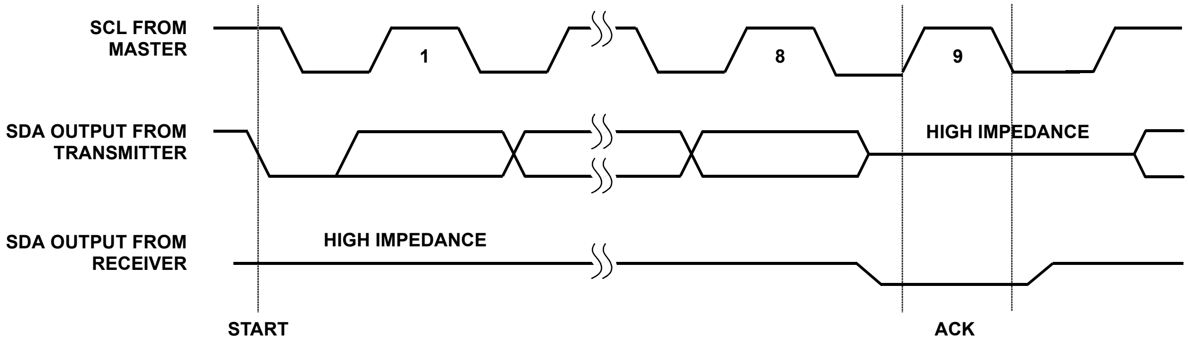


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

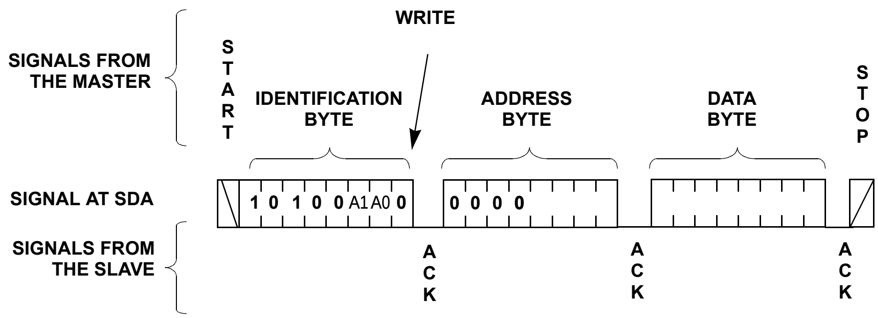


FIGURE 18. BYTE WRITE SEQUENCE

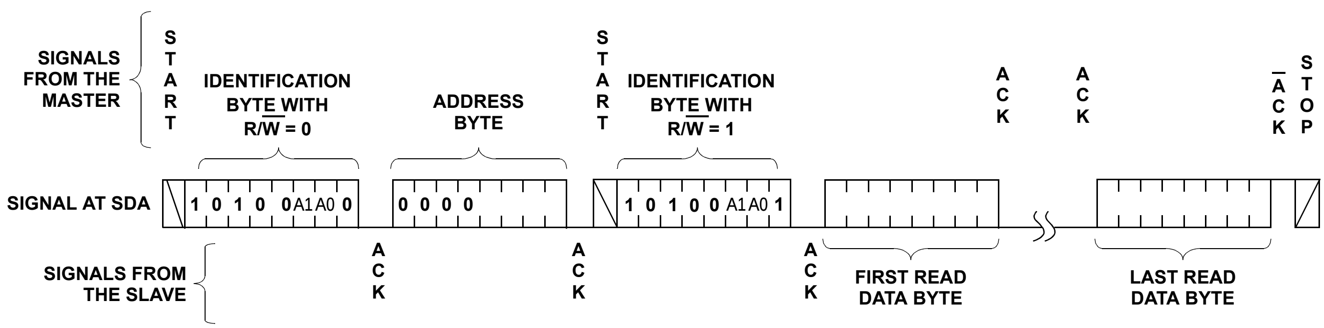


FIGURE 19. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22313 responds with an ACK. At this time, the device enters its standby state (see Figure 18).

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (see Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22313 responds with an ACK. Then the ISL22313 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 0Fh, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.The master terminates the read operation issuing a NACK ($\overline{ACK}$) and a STOP condition following the last bit of the last Data Byte (see Figure 19).

Applications Information

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients (or overshoot/undershoot) resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break within an extremely short period of time (<50ns). Two such code transitions are EFh to F0h, and 0Fh to 10h. Note that all switching transients will settle well within the settling time as stated in the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus this may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 18, 2016	FN6421.1	Updated the Ordering information table on page 2. Added Revision History and About Intersil sections. Updated POD M10.118 to the latest revision. Changes are as follows: Updated to new POD template and added land pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

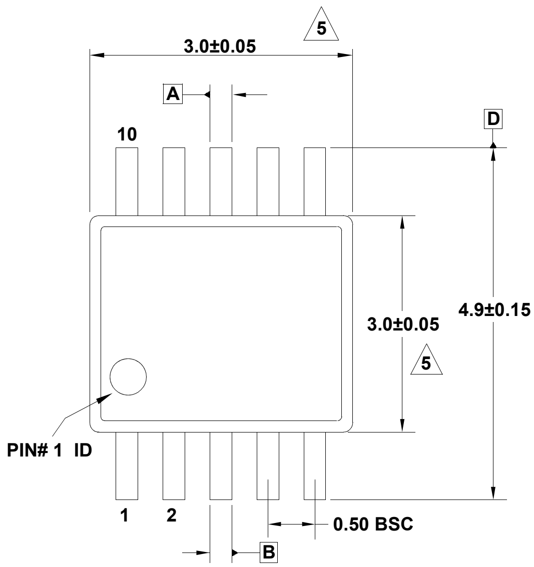
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

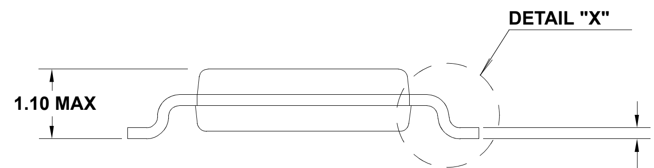
M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

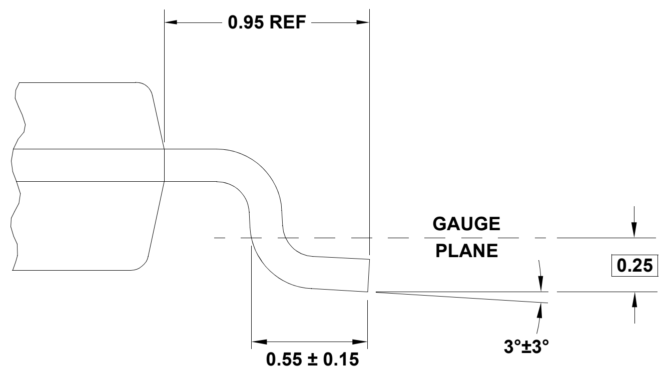
Rev 1, 4/12



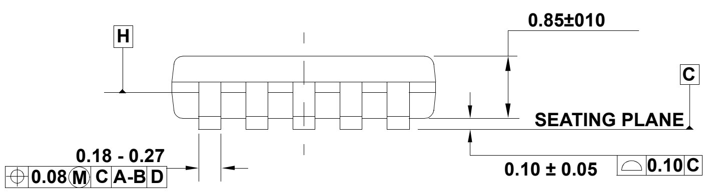
TOP VIEW



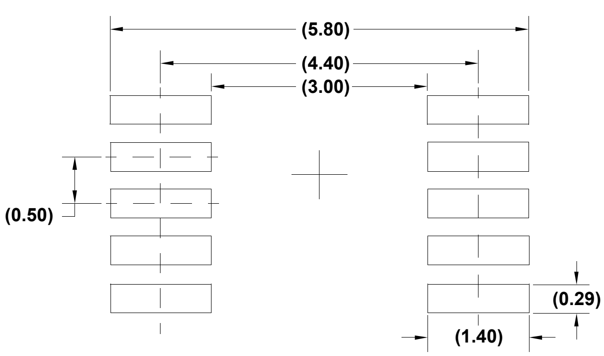
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.