ISL2671286

12-Bit, 20kSPS SAR ADC

FN7863
Rev 0.00
November 1, 2011

The ISL2671286 is a sampling SAR-type ADC which features excellent linearity over supply and temperature variations, and provides a drop-in compatible alternative to all ADS1286 performance grades. The robust high impedance input minimizes errors due to leakage currents, and specified measurement accuracy is maintained with input signals up to the supply rails.

The reference accepts inputs between 1.25V to 5.0V, providing design flexibility in a wide variety of applications. The ISL2671286 also features up to 8kV Human Body Model ESD survivability.

The serial digital interface is SPI compatible and is easily interfaced to all popular FPGAs and microcontrollers. Operating from a 5V supply, power dissipation is 1.4mW at a sampling rate of 20kSPS and just 15µW between conversions utilizing the Auto Power-Down mode. These features make the ISL2671286 an excellent solution for remote industrial sensors and battery-powered instruments.

The ISL2671286 is available in an 8 Ld SOIC package and is specified for operation over the industrial temperature range of –40°C to +85°C.

Features

- Drop-In Compatible with ADS1286 (All Performance Grades)
- Simple SPI-compatible Serial Digital Interface
- Guaranteed No Missing Codes
- 20kHz Sampling Rate
- +4.50V to +5.25V Supply
- Low 280µA Operating Current (20kSPS)
- Power-down Current between Conversions: 3µA
- Excellent Differential Non-Linearity (0.75LSB Max)
- Low THD: -83dB (Typ)
- Pb-Free (RoHS Compliant)
- Available in SOIC Package

Applications

- Remote Data Acquisition
- Battery Operated Systems
- Industrial Process Control
- Energy Measurement
- Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

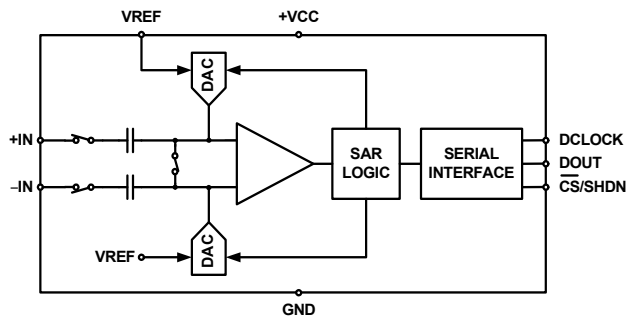


FIGURE 1. BLOCK DIAGRAM

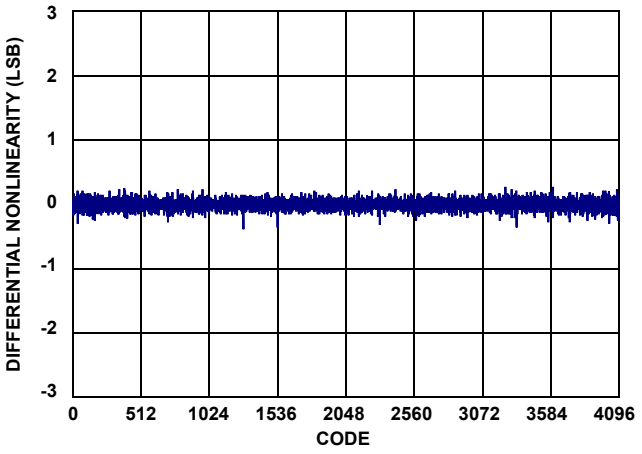
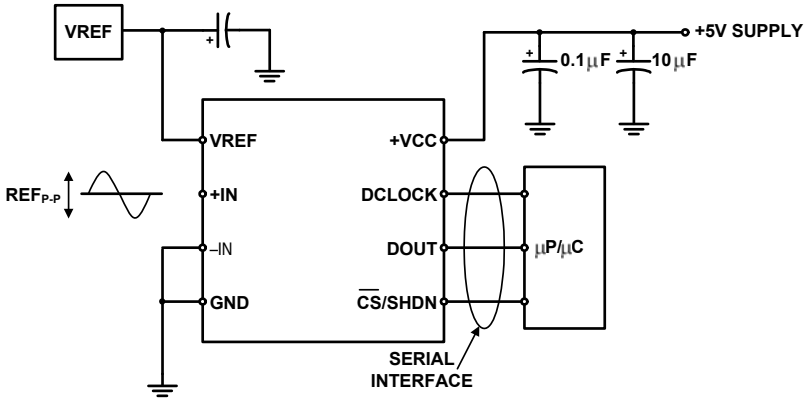


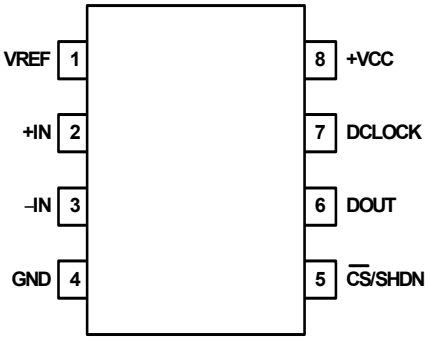
FIGURE 2. DIFFERENTIAL LINEARITY ERROR vs CODE

Typical Connection Diagram



Pin Configuration

ISL2671286
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
VREF	1	Reference input
+IN	2	Non-inverting input
–IN	3	Inverting input. Connect to ground or remote sense point.
GND	4	Ground
$\overline{CS}$/SHDN	5	Chip select when low; shut-down mode when high.
DOUT	6	Serial output data word comprises 12 bits of data. In operation, data is valid on falling edge of DCLOCK. Second clock pulse after falling edge of $\overline{CS}$/SHDN enables serial output. After one null bit, data is valid for next 12 edges.
DCLOCK	7	Data clock synchronizes serial data transfer.
+VCC	8	Power supply

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	+VCC RANGE (V)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL2671286IBZ (Note 3)	2671286 IBZ	4.50 to 5.25	-40°C to +85°C	8 Ld SOIC	M8.15
Coming Soon ISL2671286IPZ	2671286 IPZ	4.50 to 5.25	-40°C to +85°C	8 Ld PDIP	E8.3

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL2671286. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

Any Pin to GND . . . . . -0.3V to +6.0V
Analog Input to GND. . . . . -0.3V to +VCC+0.3V
Digital I/O to GND. . . . . -0.3V to +VCC+0.3V
External Reference Voltage . . . . . +6V
Maximum Current In to Any Pin 10mA
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 8kV
  Machine Model (Tested per JESD22-A115B) 400V
  Charged Device Model (Tested per JESD22-C101E). 1.5kV
Latch Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5).	120	64
8 Ld PDIP Package (Notes 5, 6, 7).	120	66

Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Case Temperature . . . . . +100°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Electrical Specifications

+VCC = +5V, V_{REF} = +5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 • f_{SAMPLE} , unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
ANALOG INPUT (Note 9)						
|AIN|	Full-Scale Input Range	+IN – (–IN)	**0**		**VREF**	V
	Absolute Input Voltage	+IN	**-0.2**		**+VCC +0.2**	V
		–IN	**-0.2**		**+0.2**	V
C_{IN}	Input Capacitance	Track/Hold mode		19/1.8		pF
I_{LEAK}	Input DC Leakage Current (Note 10)		**-1**	0.01	**1**	µA
SYSTEM PERFORMANCE						
N	Resolution			12		Bits
	No Missing Codes	Guaranteed no missed codes	**12**			Bits
INL	Integral Linearity		**-1**	±0.5	**1**	LSB
DNL	Differential Linearity		**-0.75**	±0.4	**0.75**	LSB
OFFSET	Zero-Code Error		**-3**	±0.1	**3**	LSB
GAIN	Gain Error		**-8**	±0.2	**8**	LSB
PSRR	Power Supply Rejection			82		dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion Time				**12**	Clk Cycles
t_{ACQ}	Acquisition Time		**1.5**			Clk Cycles
SSBW	Small Signal Bandwidth			320		kHz
DYNAMIC CHARACTERISTICS						
THD	Total Harmonic Distortion	AIN = $5.0V_{PP}$ at f_{IN} = 1kHz		-82		dB
		AIN = $5.0V_{PP}$ at f_{IN} = 5kHz		-83		dB
SINAD	Signal-to (Noise + Distortion) Ratio	AIN = $5.0V_{P-P}$ at f_{IN} = 1kHz		72		dB
SFDR	Spurious Free Dynamic Range	AIN = $5.0V_{P-P}$ at f_{IN} = 1kHz		83		dB

Electrical Specifications

+VCC = +5V, V_{REF} = +5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 • f_{SAMPLE} , unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
REFERENCE INPUT						
REF	REF Input Range		**1.25**	2.5	**VCC + 0.05**	V
REFLEAK	Current Drain	$\overline{CS}$/SHDN = VCC	**-2.5**	0.01	**2.5**	µA
		t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz		0.06	**20**	µA
		t_{CYC} = 80µs, f_{CLK}= 200kHz		0.5	**20**	µA
DIGITAL INPUT/OUTPUT						
	Logic Family			CMOS		
V_{IH}	Input High Voltage		**3**		**+VCC**	V
V_{IL}	Input Low Voltage		**0.0**		**0.8**	V
V_{OH}	Output High Voltage	I_{OH} = 250µA	**3**		**+VCC**	V
V_{OL}	Output Low Voltage	I_{OL} = 250µA	**0.0**		**0.4**	V
	Data Format			Straight Binary		
I_{LEAK}	Input DC Leakage Current		**-1**	0.01	**1**	µA
C_{IN}	Input Capacitance			9		pF
I_{OZ}	Floating-State Output Leakage Current		**-1**	0.01	**1**	µA
C_{OUT}	Floating-State Output Capacitance			6		pF
POWER SUPPLY REQUIREMENTS						
+VCC	Power Supply Voltage		**4.50**	5	**5.25**	V
V_{ANA}	Quiescent Current	t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz		280	**500**	µA
		t_{CYC} = 90µs, f_{CLK}= 200kHz		360	**600**	µA
	Power Down	$\overline{CS}$/SHDN = VCC		0.5	**3**	µA
TEMPERATURE RANGE						
	Specified Performance		**-40**		**+85**	°C

NOTES:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. The absolute voltage applied to each analog input must be between GND and +VCC to guarantee datasheet performance.
10. Applies only to +IN.

Timing Specifications

At f_{CLK} = 200kHz , unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
t_{SMPL}	Analog Input Sample Time	See operating sequence; Figure 3	**1.5**		**2.0**	CLK Cycles
$t_{SMPL\ (MAX)}$	Maximum Sampling Frequency				**20**	kHz
t_{CONV}	Conversion Time	See operating sequence; Figure 3		12		CLK Cycles
t_{dDO}	Delay Time, DCLOCK↓ to DOUT Data Valid	See test circuits; Figure 4		36	**150**	ns
t_{DIS}	Delay Time, $\overline{CS}$/SHDN↑ to DOUT Hi-Z	See test circuits; Figure 4 (Note 11)			**50**	ns
t_{EN}	Delay Time, DCLOCK↓ to DOUT Enable	See test circuits; Figure 4		21	**100**	ns

Timing Specifications At f_{CLK} = 200kHz , unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
t_{hDO}	Output Data Remains Valid After DCLOCK↓	CLOAD = 100pF	**15**	30		ns
t_f	DOUT Fall Time	See test circuits; Figure 4		1	**100**	ns
t_R	DOUT Rise Time	See test circuits; Figure 4		1	**100**	ns
t_{CSD}	Delay Time, $\overline{CS}$/SHDN↓ to DCLOCK↓	See operating sequence; Figure 3			**0**	ns
t_{SUCS}	Delay Time, $\overline{CS}$/SHDN↓ to DCLOCK↑	See operating sequence; Figure 3	**30**			ns

NOTE:

11. During characterization, t_{DIS} is measured from the release point with a 10pF load (see Figure 4) and the equivalent timing using the ADS1286 loading (3kΩ, 100pF) is calculated.

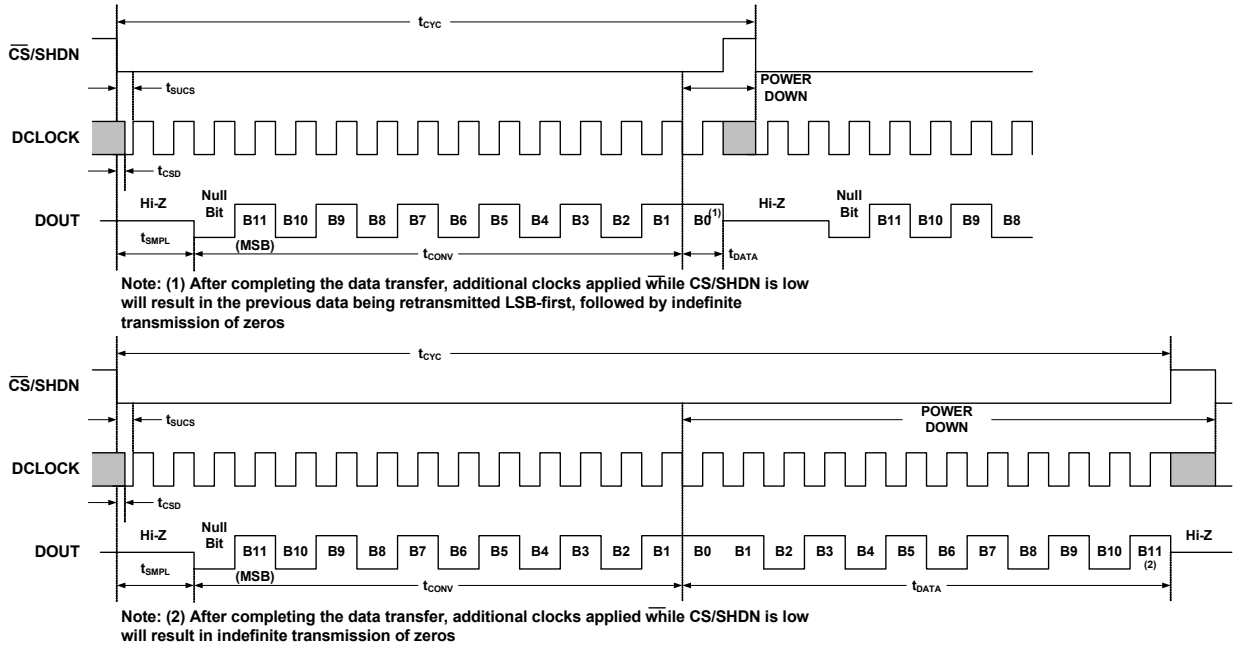


FIGURE 3. SERIAL INTERFACE TIMING DIAGRAM

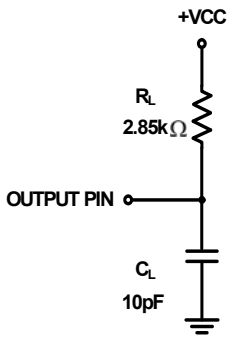


FIGURE 4. EQUIVALENT LOAD CIRCUIT

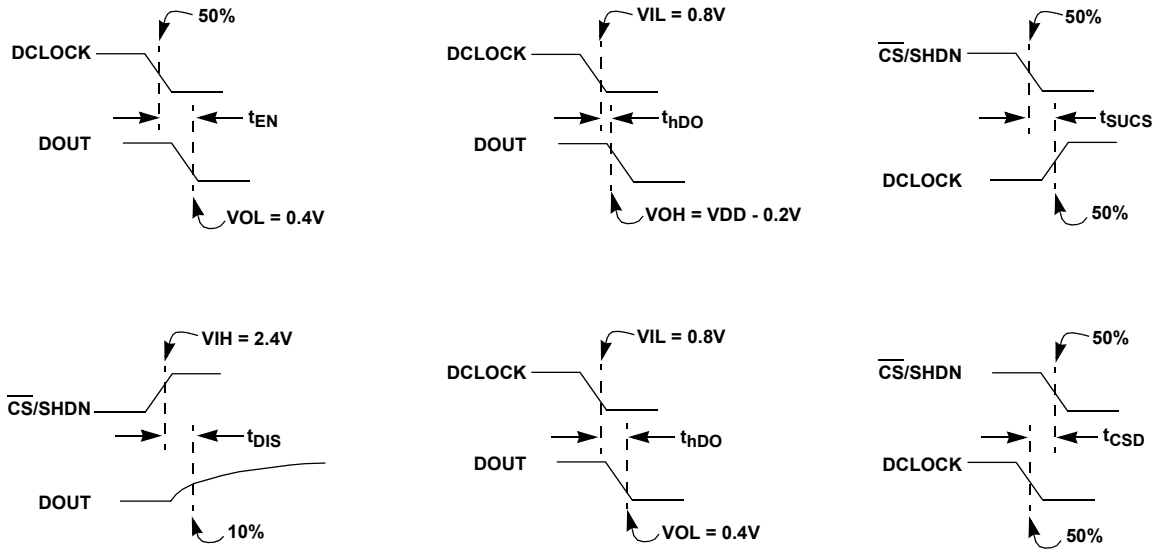


FIGURE 5. TIMING PARAMETER DEFINITIONS

Typical Performance Characteristics

At T_A = +25°C, +VCC = V_{REF} = 5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 * f_{SAMPLE}, unless otherwise specified.

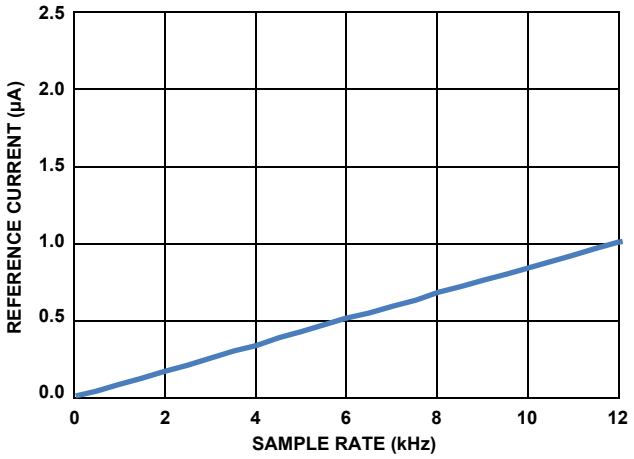


FIGURE 6. REFERENCE CURRENT vs SAMPLE RATE

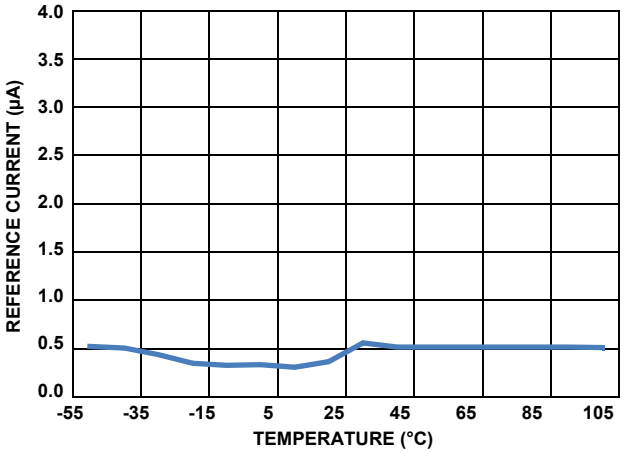


FIGURE 7. REFERENCE CURRENT vs TEMPERATURE

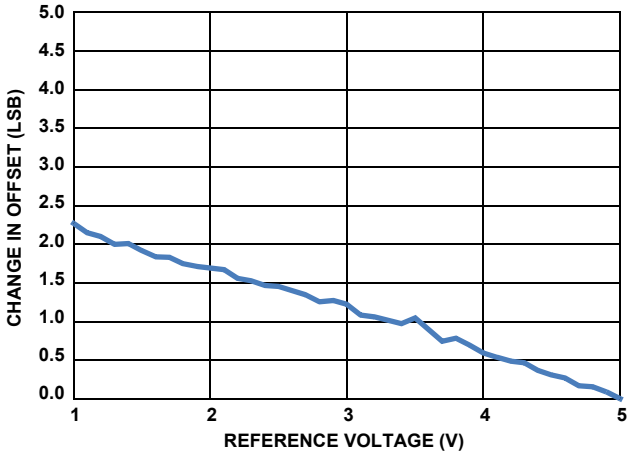


FIGURE 8. CHANGE IN OFFSET vs REFERENCE VOLTAGE

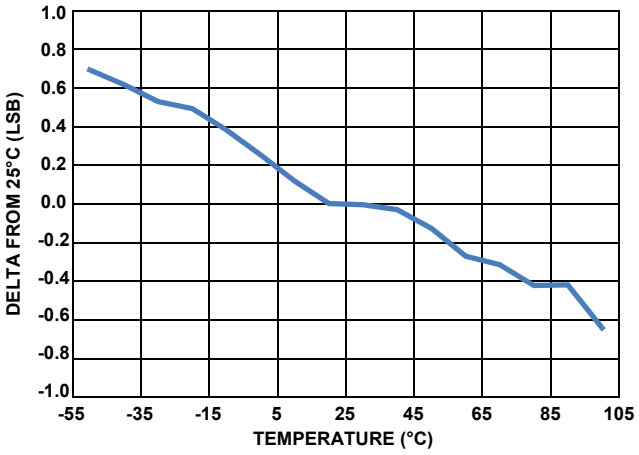


FIGURE 9. CHANGE IN OFFSET vs TEMPERATURE

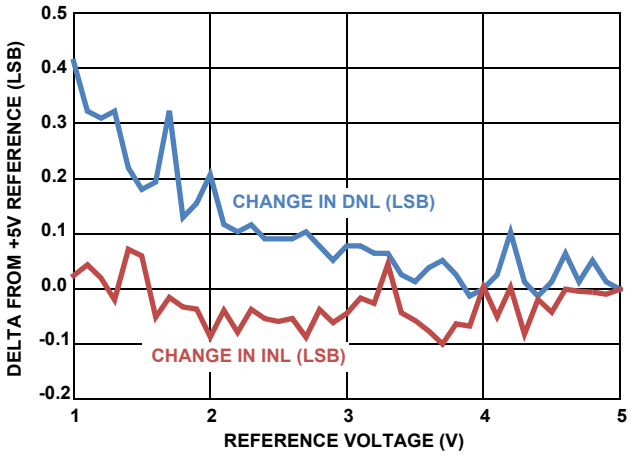


FIGURE 10. CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE

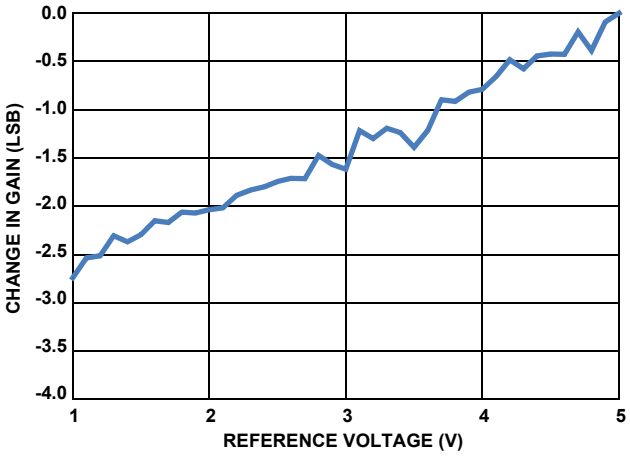


FIGURE 11. CHANGE IN GAIN vs REFERENCE VOLTAGE

Typical Performance Characteristics

At T_A = +25°C, +VCC = V_{REF} = 5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 * f_{SAMPLE}, unless otherwise specified. **(Continued)**

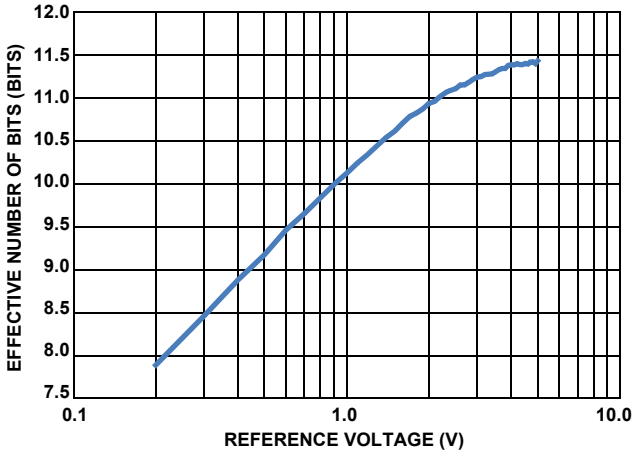


FIGURE 12. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE

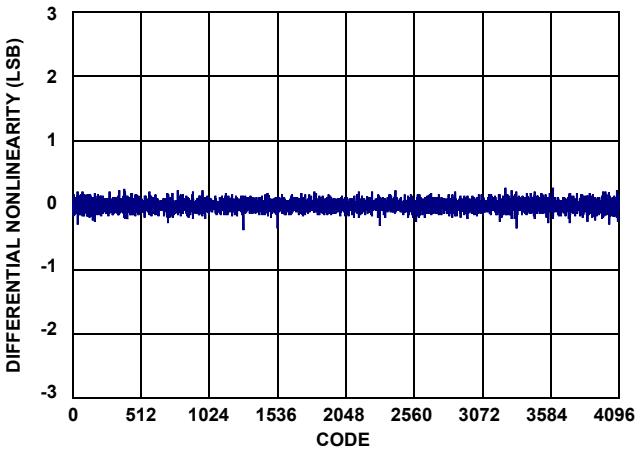


FIGURE 13. DIFFERENTIAL LINEARITY ERROR vs CODE

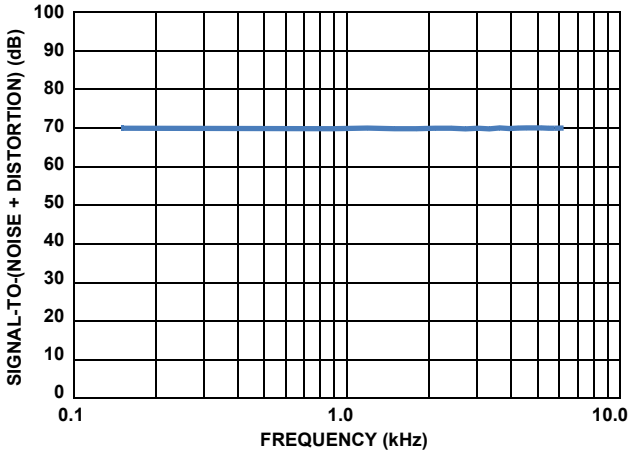


FIGURE 14. SIGNAL-TO-(NOISE + DISTORTION) vs FREQUENCY

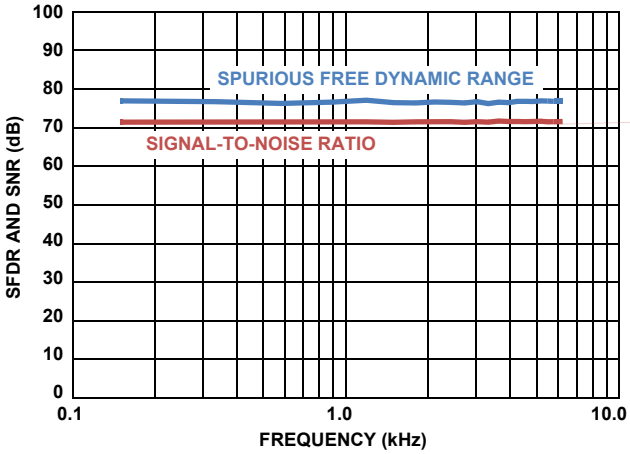


FIGURE 15. SPURIOUS FREE DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO vs FREQUENCY

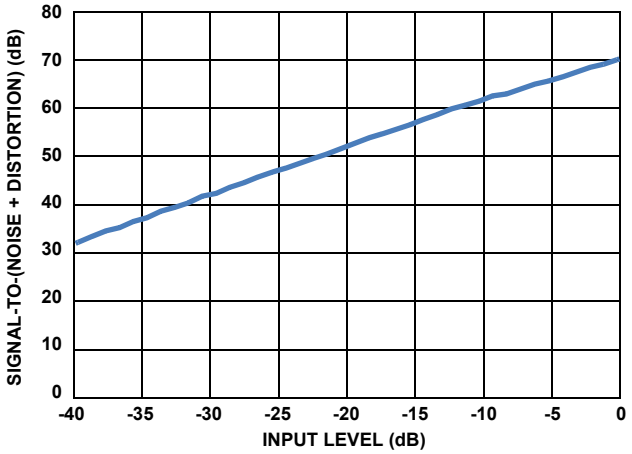


FIGURE 16. SIGNAL-TO-(NOISE + DISTORTION) vs INPUT LEVEL

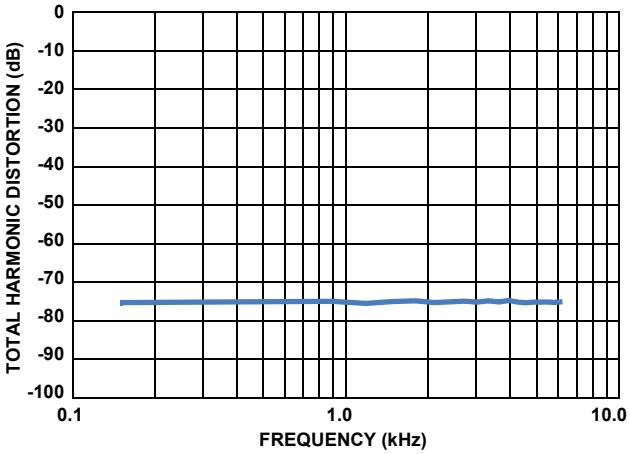


FIGURE 17. TOTAL HARMONIC DISTORTION vs FREQUENCY

Typical Performance Characteristics

At T_A = +25°C, +VCC = V_{REF} = 5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 * f_{SAMPLE}, unless otherwise specified. **(Continued)**

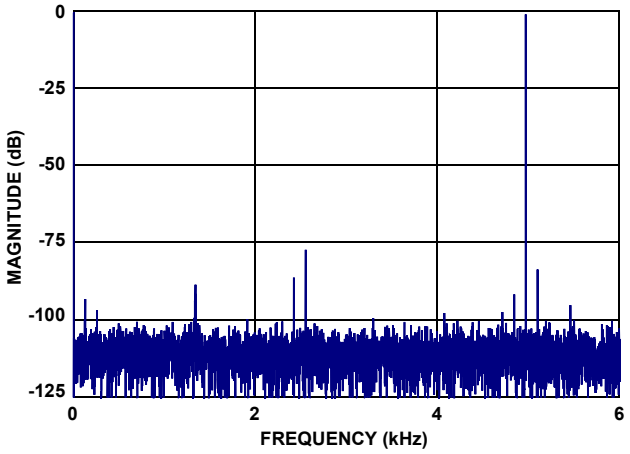


FIGURE 18. 4096 POINT FFT

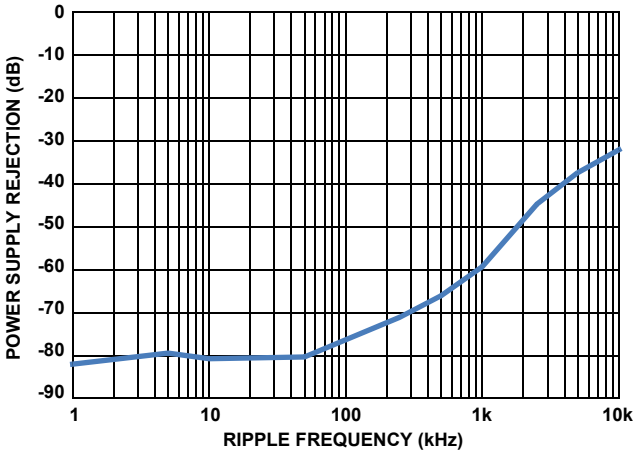


FIGURE 19. POWER SUPPLY REJECTION vs RIPPLE FREQUENCY

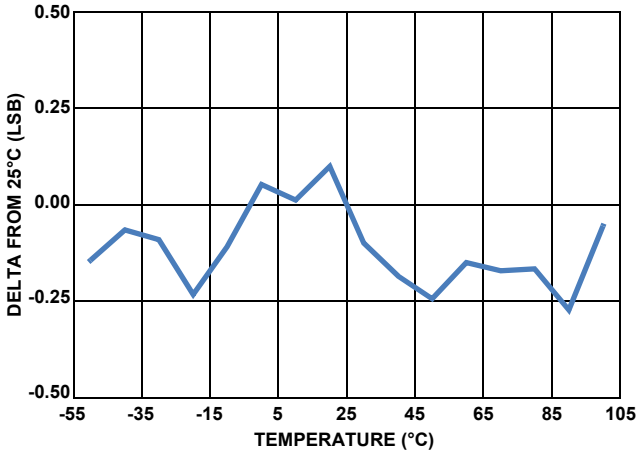


FIGURE 20. CHANGE IN GAIN vs TEMPERATURE

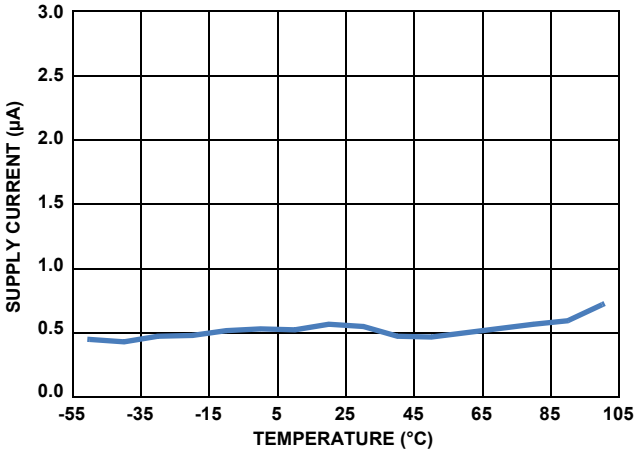


FIGURE 21. POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

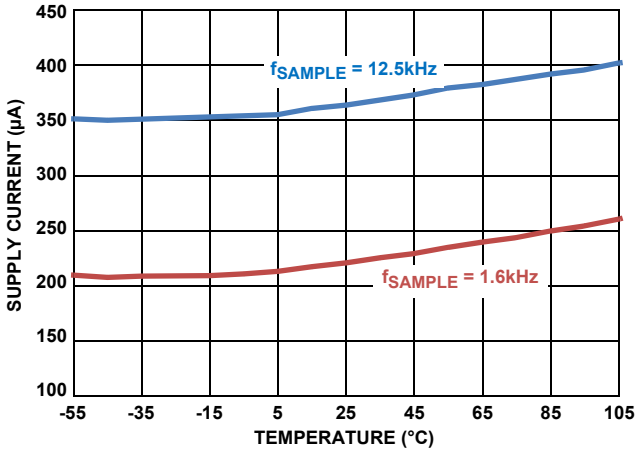


FIGURE 22. SUPPLY CURRENT vs TEMPERATURE

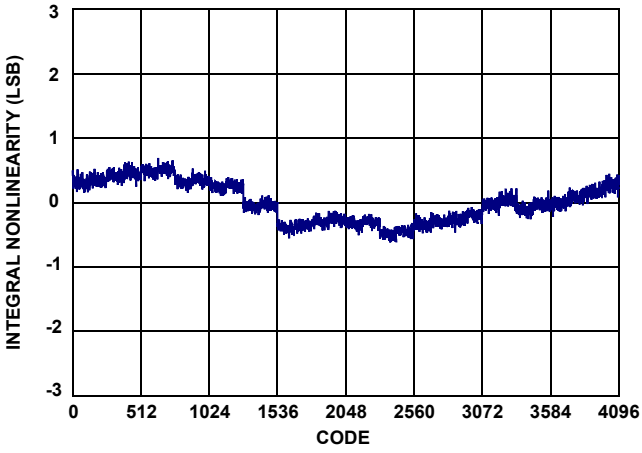


FIGURE 23. INTEGRAL LINEARITY ERROR vs CODE

Typical Performance Characteristics

At T_A = +25°C, +VCC = V_{REF} = 5V, f_{SAMPLE} = 12.5kHz, f_{CLK} = 16 * f_{SAMPLE}, unless otherwise specified. **(Continued)**

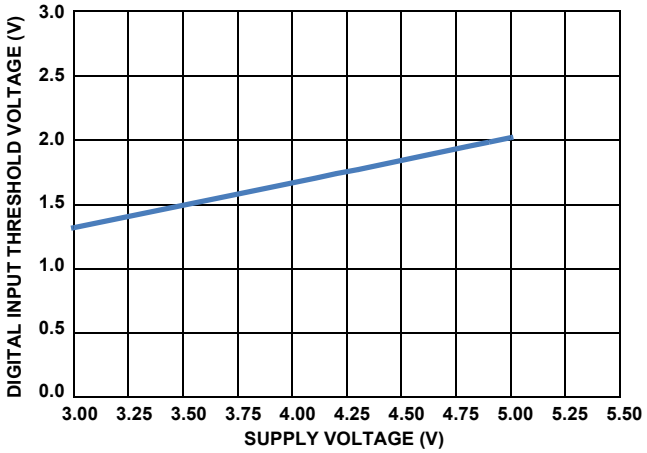


FIGURE 24. DIGITAL INPUT LINE THRESHOLD vs SUPPLY VOLTAGE

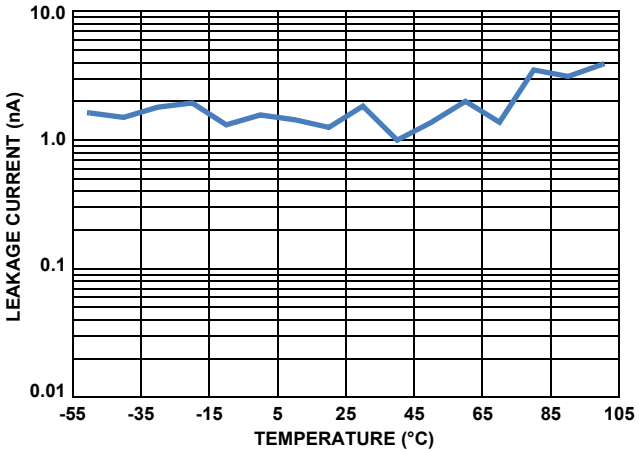


FIGURE 25. INPUT LEAKAGE CURRENT vs TEMPERATURE

Functional Description

The ISL2671286 is based on a successive approximation register (SAR) architecture utilizing capacitive charge redistribution digital-to-analog converters (DACs). Figure 26 shows a simplified representation of the converter. During the acquisition phase (ACQ), the differential input is stored on the sampling capacitors (CS). The comparator is in a balanced state since the switch across its inputs is closed. The signal is fully acquired after t_{ACQ} has elapsed, and the switches then transition to the conversion phase (CONV) so the stored voltage can be converted to digital format. The comparator becomes unbalanced when the differential switch opens and the input switches transition (assuming that the stored voltage is not exactly at mid-scale). The comparator output reflects whether the stored voltage is above or below mid-scale, which sets the value of the MSB. The SAR logic then forces the capacitive DACs to adjust up or down by one-quarter of full-scale by switching in binarily weighted capacitors. Again, the comparator output reflects whether the stored voltage is above or below the new value and sets the value of the next lowest bit. This process repeats until all 12 bits have been resolved.

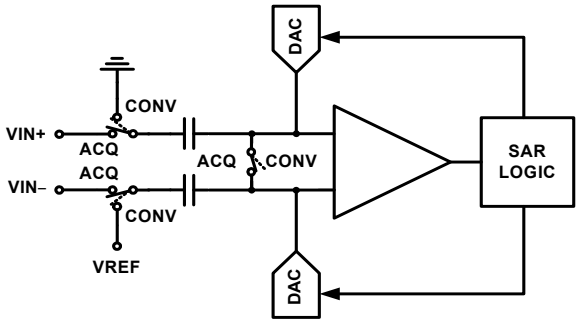


FIGURE 26. SAR ADC ARCHITECTURAL BLOCK DIAGRAM

ADC Transfer Function

The output coding for the ISL2671286 is straight binary. The first code transition occurs at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size is VREF/4096. The ideal transfer characteristic of the ISL2671286 is shown in Figure 27.

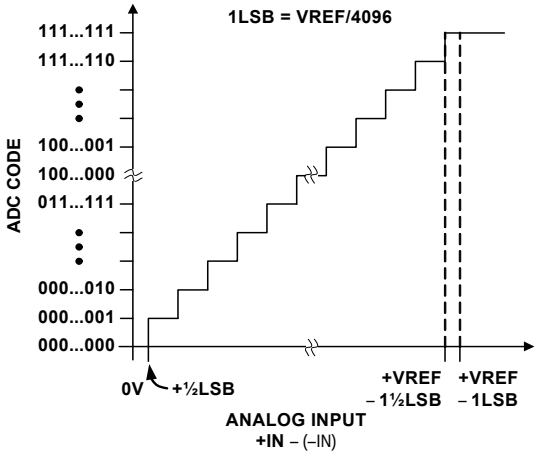


FIGURE 27. IDEAL TRANSFER CHARACTERISTICS

Analog Input

The ISL2671286 features a pseudo-differential input with a nominal full-scale range equal to the applied VREF voltage. The negative input (VIN–) must be biased within 200mV of ground.

Modes of Operation

There are two possible modes of operation, which are controlled by the $\overline{CS}$/SHDN signal. When $\overline{CS}$/SHDN is high (deasserted), the ADC is in static mode. Conversely, when $\overline{CS}$/SHDN is low (asserted), the device is in dynamic mode. There is no minimum or maximum number of SCLK cycles required to enter static mode. This simplifies power management and allows the user to easily optimize power dissipation versus throughput for various application requirements.

DYNAMIC MODE

This mode is entered when a conversion result is desired by asserting $\overline{CS}$/SHDN. Figure 28 shows the general operation in this mode. The conversion is initiated on the falling edge of $\overline{CS}$/SHDN (refer to “Serial Digital Interface” section). When $\overline{CS}$/SHDN is deasserted, the conversion is terminated, and DOUT returns to a high-impedance state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$/SHDN may idle high until the next conversion or idle low until sometime prior to the next conversion. Once a data transfer is complete (DOUT has returned to a high-impedance state), another conversion can be initiated by again asserting $\overline{CS}$/SHDN.

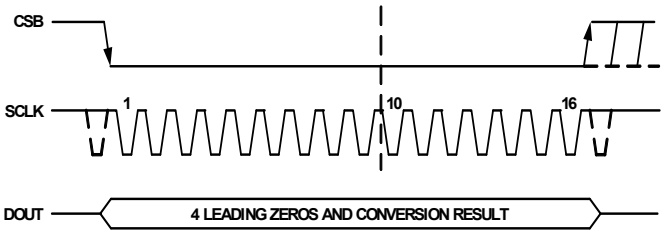


FIGURE 28. NORMAL MODE OPERATION

STANDBY MODE

The ISL2671286 enters the power-saving static mode automatically any time $\overline{CS}$/SHDN is deasserted. The user is not required to force a device into this mode following a conversion in order to optimize power consumption.

SHORT CYCLING

In cases where a lower resolution conversion is acceptable, $\overline{CS}$/SHDN can be pulled high before 12 SCLK falling edges have elapsed. This is referred to as short cycling, and it can be used to further optimize power dissipation. In this mode, a lower resolution result is acquired, but the ADC enters static mode sooner and exhibits a lower average power dissipation than if the complete conversion cycle is carried out. The acquisition time (t_{ACQ}) requirement must be met for the next conversion to be valid.

POWER-ON RESET

The ISL2671286 performs a power-on reset that requires approximately 2.5ms to execute when the supplies are first

activated. After reset is complete, a single dummy cycle lasting one conversion must be executed to initialize the switched capacitor track and hold. Once the dummy cycle is complete, the ADC mode is determined by the state of $\overline{CS}$/SHDN. At this point, switching between dynamic and static modes is controlled by $\overline{CS}$/SHDN, with no delay required between states.

POWER vs THROUGHPUT RATE

The ISL2671286 power consumption is reduced slightly at lower conversion rates. Figure 29 shows the typical power consumption over a wide range of throughput rates.

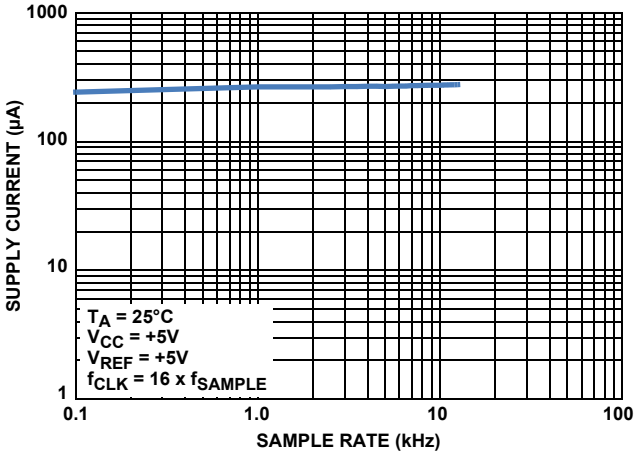


FIGURE 29. SUPPLY CURRENT vs SAMPLE RATE

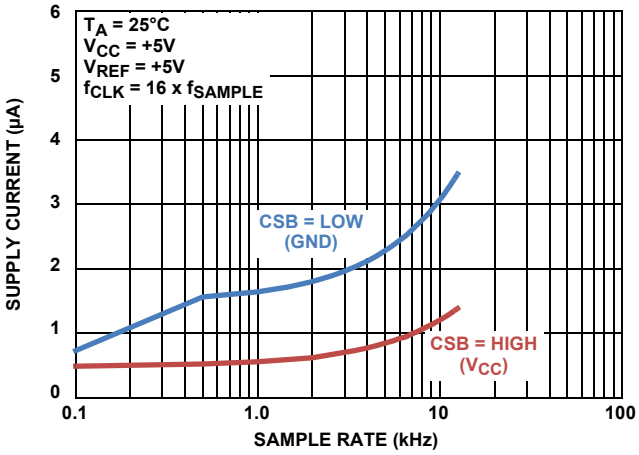


FIGURE 30. SHUTDOWN CURRENT vs SAMPLE RATE

Serial Digital Interface

The ISL2671286 communicates using a 3-wire serial interface. DCLOCK synchronizes the data transfer, with each bit transmitted on the falling DCLOCK edge and captured on the rising DCLOCK edge in the receiving system. A falling $\overline{CS}$/SHDN initiates data transfer, as shown in Figure 3. After $\overline{CS}$/SHDN falls, the second DCLOCK pulse enables DOUT. After one null bit, the A/D conversion result is output on the DOUT line. Bringing $\overline{CS}$/SHDN high resets the ISL2671286 for the next data exchange.

Figure 3 shows a detailed timing diagram for the serial interface. The serial clock provides the conversion clock and controls the transfer of data during conversion. $\overline{CS}$/SHDN initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$/SHDN puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion initiated at this point.

The conversion result from the ISL2671286 is provided on DOUT output as a serial data stream. The bits are clocked out on the falling of the SCLK input. The output coding is two's complement.

Applications Information

Analog Input Filtering

A low-pass, anti-alias filter is recommended to optimize performance, as shown in Figure 31. The capacitive input switching currents are averaged into a net DC current by C_{FILT}. It is recommended that a high-quality capacitor with low voltage and temperature coefficients, such as C0G/NP0, be used. A small series resistance value minimizes voltage drops across the resistor.

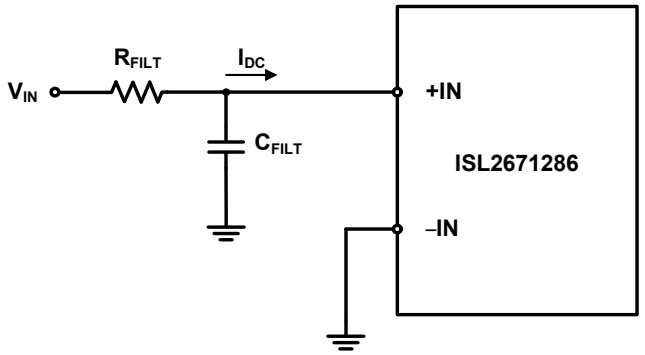


FIGURE 31. INPUT FILTERING

Reduced Reference Operation

The ISL2671286 exhibits good linearity and gain over a wide range of reference voltages (see Figures 10 and 11). When operating at low values of VREF, offset errors and noise must be considered because of the reduced LSB size.

Input errors can have a larger impact on performance when operating the ADC with a reduced reference voltage, since LSB size is proportional to VREF. Figure 8 shows how the offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 100µV is 0.082 LSB with a 5V reference. If VREF is reduced to 1V, the same 100µV offset is 0.41 LSB, and it increases to 2.05 LSB with a 0.2V reference. The offset can be corrected digitally after conversion, or an opposing bias can be applied to the –IN pin (within the allowable range according to the "Electrical Specifications").

Similarly, total input referred noise appears as a larger fraction of an LSB when operating at reduced VREF values. Attention should be paid to the output noise of the driving amplifier, and proper filtering should be applied to limit the noise that aliases in the Nyquist zone. Averaging multiple readings can improve performance if the application conditions allow.

Grounding and Layout

The printed circuit board that houses the ISL2671286 should be designed so that the analog and digital sections are separated

and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the ISL2671286 as possible. Avoid running digital lines under the device, as this couples noise onto the die. The analog ground plane should be allowed to run under the ISL2671286 to avoid noise coupling.

Power supply lines to the device should use as large a trace as possible, to provide low impedance paths and to reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board. Clock signals should never run near analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board.

A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best performance from these decoupling components, they must be placed as close as possible to the device.

Terminology

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the RMS amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding DC. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given in Equation 1:

$$\text{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\text{dB} \quad \text{(EQ. 1)}$$

Thus, for a 12-bit converter, the ratio is 74dB and for a 10-bit converter is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of harmonics to the fundamental. For the ISL2671286, it is defined as shown in Equation 2:

$$THD(dB) = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \quad \text{(EQ. 2)}$$

where V_1 is the RMS amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the RMS amplitudes of the second through the sixth harmonic.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the RMS value of the next largest component in the ADC output spectrum (up to fs/2 and excluding DC) to the RMS value of the fundamental. Also referred to as Spurious Free Dynamic Range (SFDR), the value of this specification normally is determined by the largest harmonic in the spectrum. For ADCs in which the harmonics are buried in the noise floor, however, SFDR is a noise peak.

Small-Signal Bandwidth

Small-signal bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a signal whose peak-to-peak amplitude spans no more than 10% of the full-scale input range.

Integral Nonlinearity (INL)

Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero-Code Error

Zero-code error is the deviation of the first code transition (000...000 to 000...001) from an ideal ½ LSB step.

Gain Error

Gain error is the deviation of the full-scale input (111...111) from the ideal span (i.e., +VREF – 1LSB) after the zero code error has been adjusted out.

Track-and-Hold Acquisition Time

Track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

Power supply rejection ratio is the ratio of the power in the ADC output at full-scale frequency, f, to ADC +VCC supply of frequency f_S (Equation 3). The frequency of this input varies from 1kHz to 1MHz.

$$PSRR(dB) = 10\log(Pf/Pfs) \quad \text{(EQ. 3)}$$

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency f_S in the ADC output.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
11/1/2011	FN7863.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL2671286

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

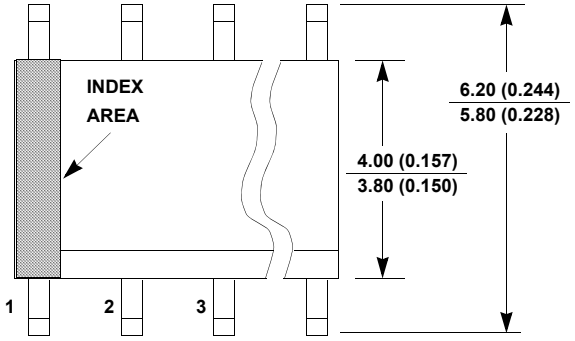
FITs are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

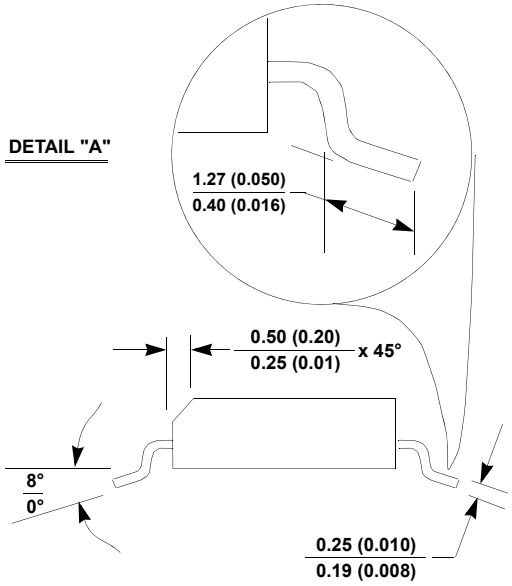
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

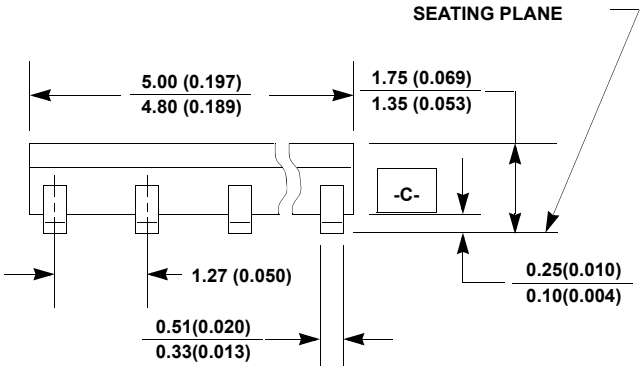
Rev 3, 3/11



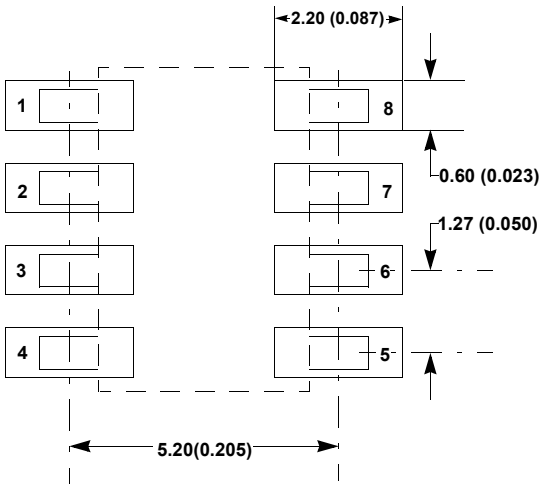
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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