ISL28006

Micropower, Rail to Rail Input Current Sense Amplifier with Voltage Output

FN6548
Rev 6.00
November 22, 2013

The ISL28006 is a micropower, uni-directional high-side and low-side current sense amplifier featuring a proprietary rail-to-rail input current sensing amplifier. The ISL28006 is ideal for high-side current sense applications where the sense voltage is usually much higher than the amplifier supply voltage. The device can be used to sense voltages as high as 28V when operating from a supply voltage as low as 2.7V. The micropower ISL28006 consumes only 50µA of supply current when operating from a 2.7V to 28V supply.

The ISL28006 features a common-mode input voltage range from 0V to 28V. The proprietary architecture extends the input voltage sensing range down to 0V, making it an excellent choice for low-side ground sensing applications. The benefit of this architecture is that a high degree of total output accuracy is maintained over the entire 0V to 28V common mode input voltage range.

The ISL28006 is available in fixed (100V/V, 50V/V, 20V/V and Adjustable) gains in the space saving 5 Ld SOT-23 package and the 6 Ld SOT-23 package for the adjustable gain part. The parts operate over the extended temperature range from -40°C to +125°C.

Features

- Low Power Consumption. . . . . 50µA, Typ
- Supply Range . . . . .2.7V to 28V
- Wide Common Mode Input. 0V to 28V
- Gain Versions
  - ISL28006-100 . . . . 100V/V
  - ISL28006-50 . . . . 50V/V
  - ISL28006-20 . . . . 20V/V
  - ISL28006-ADJ . . . . ADJ (Min Gain = 20V/V)
- Operating Temperature Range . . . .-40°C to +125°C
- Packages. . . . . .5 Ld SOT-23, 6 Ld SOT-23

Applications

- Power Management/Monitors
- Power Distribution and Safety
- DC/DC, AC/DC Converters
- Battery Management/Charging
- Automotive Power Distribution

Related Literature

- See AN1532 for “ISL28006 Evaluation Board User’s Guide”

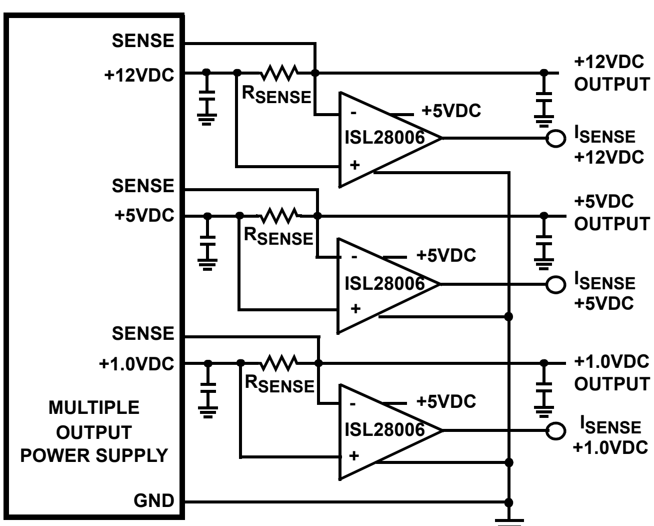


FIGURE 1. TYPICAL APPLICATION

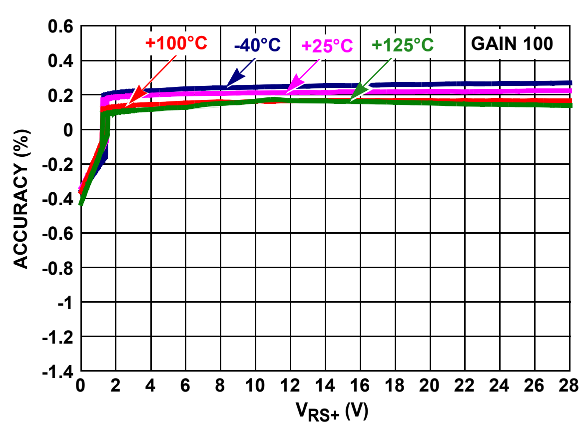
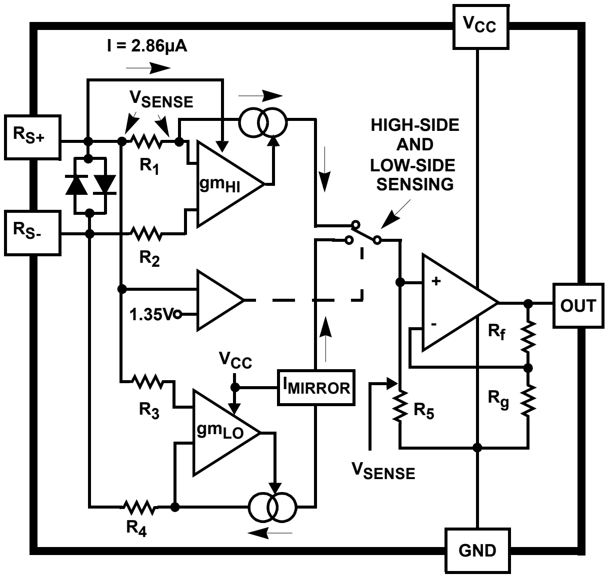
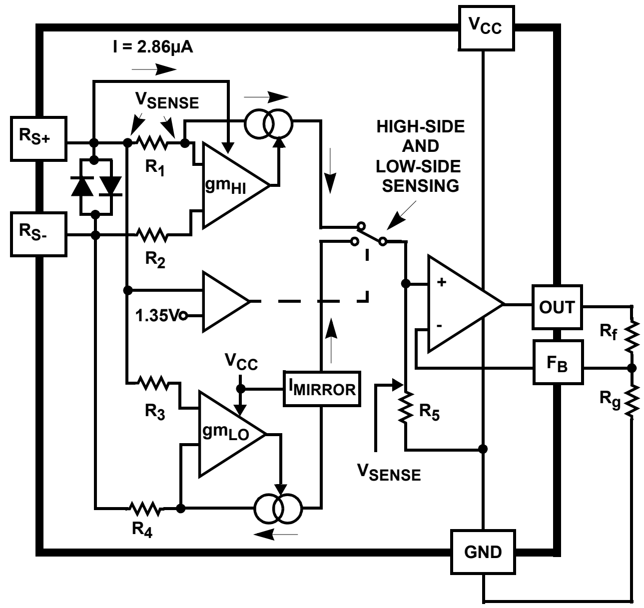


FIGURE 2. GAIN ACCURACY vs V_{RS+} = 0V TO 28V

Block Diagram



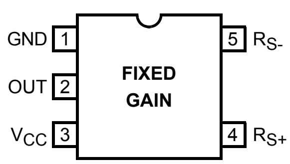
FIXED GAIN PARTS



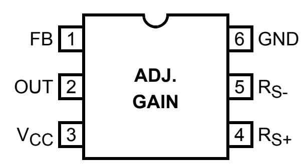
ADJUSTABLE GAIN PART

Pin Configurations

ISL28006-100, 50, 20
(5 LD SOT-23)
TOP VIEW

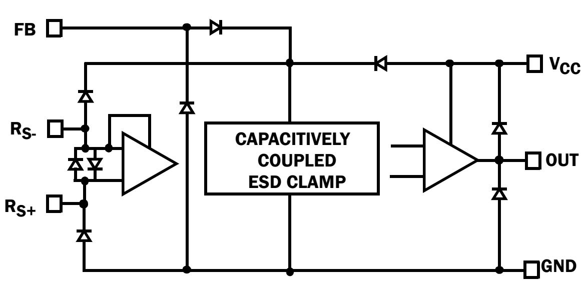


ISL28006-ADJ
(6 LD SOT-23)
TOP VIEW



Pin Descriptions

ISL28006-100, 50, 20 (5 LD SOT-23)	ISL28006-ADJ (6 LD SOT-23)	PIN NAME	DESCRIPTION
1	6	GND	Power Ground
	1	FB	Input Pin for External Resistors
2	2	OUT	Amplifier Output
3	3	V_{CC}	Positive Power Supply
4	4	R_{S+}	Sense Voltage Non-inverting Input
5	5	R_{S-}	Sense Voltage Inverting Input



Ordering Information

PART NUMBER (Notes 1, 2, 3)	GAIN	PART MARKING	PACKAGE Tape & Reel (Pb-Free)	PKG. DWG. #
ISL28006FH100Z-T7	100V/V	BDJA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FH100Z-T7A	100V/V	BDJA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FH50Z-T7	50V/V	BDHA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FH50Z-T7A	50V/V	BDHA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FH20Z-T7	20V/V	BDGA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FH20Z-T7A	20V/V	BDGA (Note 4)	5 Ld SOT-23	P5.064A
ISL28006FHADJZ-T7	ADJ	BDFA (Note 4)	6 Ld SOT-23	P6.064
ISL28006FHADJZ-T7A	ADJ	BDFA (Note 4)	6 Ld SOT-23	P6.064
ISL28006FH-100EVAL1Z	100V/V Evaluation Board			
ISL28006FH-50EVAL1Z	50V/V Evaluation Board			
ISL28006FH-20EVAL1Z	20V/V Evaluation Board			
ISL28006FH-ADJEVAL1Z	Adjustable Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28006. For more information on MSL please see techbrief TB363.
4. The part marking is located on the bottom of the part.

Absolute Maximum Ratings

Max Supply Voltage 28V
Max Differential Input Current 20mA
Max Differential Input Voltage . . . . ±0.5V
Max Input Voltage (R_{S+}, R_{S-}, FB) . . . . GND - 0.5V to 30V
Max Input Current for Input Voltage <GND - 0.5V. . . . . ±20mA
Output Short-Circuit Duration . . . . Indefinite
Di-Electrically Isolated PR40 Process . . . . Latch-up free
ESD Rating
- Human Body Model (Tested per JESD22-A114F). 4kV
- Machine Model (Tested per EIA/JESD22-A115-A) 200V
- Charged Device Model (Tested per JESD22-C101D) 1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 (Notes 5, 6)	190	90
6 Ld SOT-23 (Notes 5, 6)	180	90

Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{OS} (Input Offset Voltage)	Gain = 100 (Notes 8, 9)	V_{CC} = $V_{RS}+$ = 12V, V_{SENSE} = 20mV to 100mV	-250	60	250	µV
			-300		**300**	µV
		V_{CC} = 12V, $V_{RS}+$ = 0.2V, V_{SENSE} = 20mV to 100mV	-2.5	-1.2	2.5	mV
			-2.8		**2.8**	mV
	Gain = 50, Gain = 20 (Notes 8, 9)	V_{CC} = $V_{RS}+$ = 12V, V_{SENSE} = 20mV to 100mV	-300	60	300	µV
			-450		**450**	µV
		V_{CC} = 12V, $V_{RS}+$ = 0.2V, V_{SENSE} = 20mV to 100mV	-2.8	-1.2	2.8	mV
			-3.2		**3.2**	mV
	Adjustable, Gain = 21 R_f = 100kΩ, R_g = 5kΩ (Notes 8, 9)	V_{CC} = $V_{RS}+$ = 12V, V_{SENSE} = 20mV to 100mV	-300	60	300	µV
			-450		**450**	µV
		V_{CC} = 12V, $V_{RS}+$ = 0.2V, V_{SENSE} = 20mV to 100mV	-3.1	-1.2	3.1	mV
			-3.4		**3.4**	mV
$I_{RS}+$, $I_{RS}-$	Leakage Current	V_{CC} = 0V, V_{RS+} = 28V		0.041	1.2	µA
					1.5	µA
$I_{RS}+$ (+ Input Bias Current)	Gain = 100	$V_{RS}+$ = 2V, V_{SENSE} = 5mV		4.7	6	µA
					7	µA
		$V_{RS}+$ = 0V, V_{SENSE} = 5mV	-500	-432		nA
			-600			nA
	Gain = 50, Gain = 20	$V_{RS}+$ = 2V, V_{SENSE} = 5mV		4.7	6	µA
					8	µA
		$V_{RS}+$ = 0V, V_{SENSE} = 5mV	-700	-432		nA
			-840			nA
	ADJ Gain = 101 R_f = 100kΩ, R_g = 1kΩ	$V_{RS}+$ = 2V, V_{SENSE} = 5mV		4.7	6	µA
					7	µA
		$V_{RS}+$ = 0V, V_{SENSE} = 5mV	-500	-432		nA
			-600			nA

Electrical Specifications V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
I_{RS}- (- Input Bias Current)	G = 100, 50, 20, ADJ	V_{RS}+ = 2V, V_{SENSE} = 5mV		5	50	nA
					75	nA
		V_{RS}+ = 0V, V_{SENSE} = 5mV	-125	-45		nA
			-130			nA
CMRR	Common Mode Rejection Ratio	V_{RS}+ = 2V to 28V	**105**	**115**		dB
PSRR	Power Supply Rejection Ratio	V_{CC} = 2.7V to 28V, V_{RS}+ = 2V	**90**	**105**		dB
V_{FS}	Full-scale Sense Voltage	V_{CC} = 28V, V_{RS}+ = 0.2V, 12V	200			mV
G (Gain)	(Note 8)	ISL28006-100		100		V/V
		ISL28006-50		50		V/V
		ISL28006-20		20		V/V
		ISL28006-ADJ	20			V/V
G_A (Gain Accuracy)	Gain = 100 (Note 10)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-0.2		0.7	%
			-1		**1**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV		-0.25		%
	Gain = 50, Gain = 20 (Note 10)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-0.35		0.7	%
			-1		**1**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV	-2.2	-0.33	2.2	%
			-2.3		**2.3**	%
	ADJ Gain = 21 R_f = 100kΩ, R_g = 5kΩ (Note 10)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 20mV to 100mV	-0.65		1	%
			-1		**1.05**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 20mV to 100mV	-2.2	-0.33	2.2	%
			-2.3		**2.3**	
V_{OA} (Total Output Accuracy)	Gain = 100 (Note 11)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-0.7		0.7	%
			-0.9		**0.9**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV		-1.25		%
	Gain = 50, Gain = 20 (Note 11)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-0.7		0.7	%
			-0.9		**0.9**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV	-4.7	-1.41	1.8	%
			-5.2		**2.3**	%
	ADJ Gain = 21 R_f = 100kΩ, R_g = 5kΩ (Note 11)	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV	-0.7		1.05	%
			-0.9		**1.2**	%
		V_{CC} = 12V, V_{RS}+ = 0.1V, V_{SENSE} = 100mV	-4.7	-1.41	1.8	%
			-5.2		**2.3**	%
V_{OH}	Output Voltage Swing, High V_{CC} - V_{OUT}	I_O = -500µA, V_{CC} = 2.7V, V_{SENSE} = 100mV, V_{RS}+ = 2V		39	50	mV
V_{OL}	Output Voltage Swing, Low V_{OUT}	I_O = 500µA, V_{CC} = 2.7V, V_{SENSE} = 0V, V_{RS}+ = 2V		30	50	mV
R_{OUT}	Output Resistance	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV, I_{OUT} = 10µA to 1mA		6.5		Ω
I_{SC+}	Short Circuit Sourcing Current	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		4.8		mA
I_{SC-}	Short Circuit Sinking Current	V_{CC} = V_{RS}+ = 5V, R_L = 10Ω		8.7		mA

Electrical Specifications

V_{CC} = 12V, V_{RS+} = 0V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
I_{CC}	Gain = 100	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	59	µA
					62	µA
	Gain = 50, 20,	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	62	µA
					63	µA
	ADJ Gain = 21 R_f = 100kΩ, R_g = 5kΩ	V_{RS}+ > 2V, V_{SENSE} = 5mV		50	62	µA
					63	µA
V_{CC}	Supply Voltage	Guaranteed by PSRR	**2.7**		**28**	V
Slew Rate	Gain = 100	Pulse on R_{S+} pin, V_{OUT} = 8V_{P-P} (Figure 75)	0.58	0.76		V/µs
	Gain = 50	Pulse on R_{S+} pin, V_{OUT} = 8V_{P-P} (Figure 75)	0.58	0.67		V/µs
	Gain = 20	Pulse on R_{S+} pin, V_{OUT} = 3.5V_{P-P} (Figure 75)	0.50	0.67		V/µs
	ADJ Gain = 21 R_f = 100kΩ, R_g = 5kΩ	Pulse on R_{S+} pin, V_{OUT} = 3.5V_{P-P} (Figure 75)	0.50	0.67		V/µs
BW_{-3dB}	Gain = 100	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		110		kHz
	Gain = 50	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		160		kHz
	Gain = 20	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV		180		kHz
	ADJ, Gain = 101 (Figure 65)	V_{RS}+ = 12V, 0.1V, V_{SENSE} = 100mV, R_f = 100kΩ, R_g = 1kΩ		40		kHz
	ADJ, Gain = 51 (Figure 65)	V_{RS}+ = 12V, V_{SENSE} = 100mV, R_f = 100kΩ, R_g = 2kΩ		78		kHz
		V_{RS}+ = 0.1V, V_{SENSE} = 100mV, R_f = 100kΩ, R_g = 2kΩ		122		kHz
	ADJ, Gain = 21 (Figure 65)	V_{RS}+ = 12V, V_{SENSE} = 100mV, R_f = 100kΩ, R_g = 5kΩ		131		kHz
		V_{RS}+ = 0.1V, V_{SENSE} = 100mV, R_f = 100kΩ, R_g = 5kΩ		237		kHz
t_S	Output Settling Time to 1% of Final Value	V_{CC} = V_{RS}+ = 12V, V_{OUT} = 10V step, V_{SENSE} > 7mV		15		µs
		V_{CC} = V_{RS}+ = 0.2V, V_{OUT} = 10V step, V_{SENSE} > 7mV		20		µs
	Capacitive-Load Stability	No sustained oscillations		300		pF
$t_{S\ Power-up}$	Power-Up Time to 1% of Final Value	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV		15		µs
		V_{CC} = 12V, V_{RS}+ = 0.2V, V_{SENSE} = 100mV		50		µs
	Saturation Recovery Time	V_{CC} = V_{RS}+ = 12V, V_{SENSE} = 100mV, overdrive		10		µs

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. DEFINITION OF TERMS:
   - $V_{SENSE}A = V_{SENSE}$ @ 100mV
   - $V_{SENSE}B = V_{SENSE}$ @ 20mV
   - $V_{OUT}A = V_{OUT}$ @ $V_{SENSE}A$ = 100mV
   - $V_{OUT}B = V_{OUT}$ @ $V_{SENSE}B$ = 20mV
   - $G = GAIN = \left(\frac{V_{OUT}A - V_{OUT}B}{V_{SENSE}A - V_{SENSE}B}\right)$
9. V_{OS} is extrapolated from the gain measurement. $V_{OS} = V_{SENSE}A - \frac{V_{OUT}A}{G}$
10. % Gain Accuracy = $G_A = \left(\frac{G_{MEASURED} - G_{EXPECTED}}{G_{EXPECTED}}\right) \times 100$
11. Output Accuracy % VOA = $\left(\frac{VOUT_{MEASURED} - VOUT_{EXPECTED}}{VOUT_{EXPECTED}}\right) \times 100$, where $V_{OUT} = V_{SENSE}$ X GAIN and V_{SENSE} = 100mV

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified.

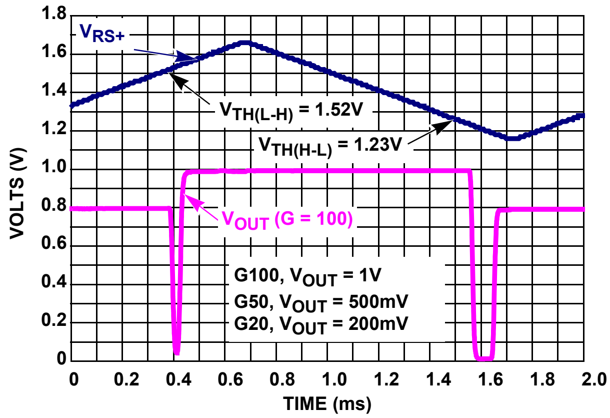


FIGURE 3. HIGH-SIDE and LOW-SIDE THRESHOLD VOLTAGE $V_{RS+(L-H)}$ and $V_{RS+(H-L)}$, V_{SENSE} = 10mV

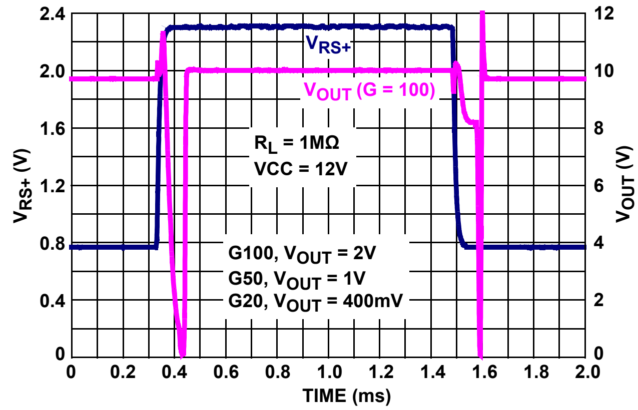


FIGURE 4. V_{OUT} vs V_{RS+}, V_{SENSE} = 20mV TRANSIENT RESPONSE

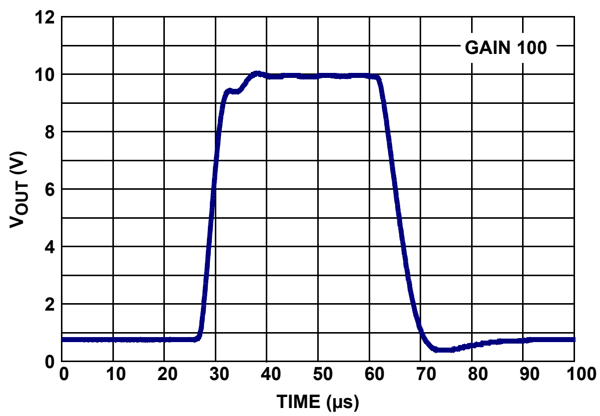


FIGURE 5. LARGE SIGNAL TRANSIENT RESPONSE V_{RS+} = 0.2V, V_{SENSE} = 100mV

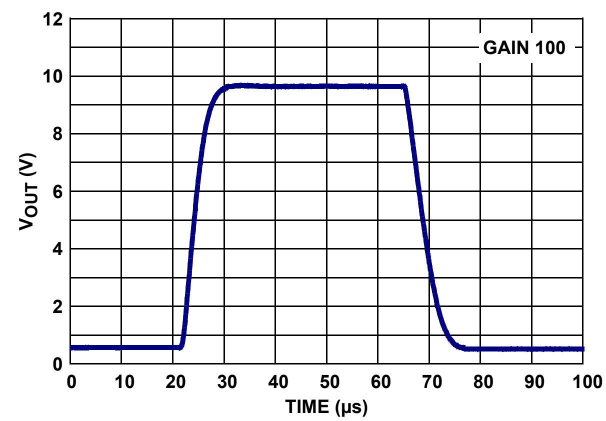


FIGURE 6. LARGE SIGNAL TRANSIENT RESPONSE V_{RS+} = 12V, V_{SENSE} = 100mV

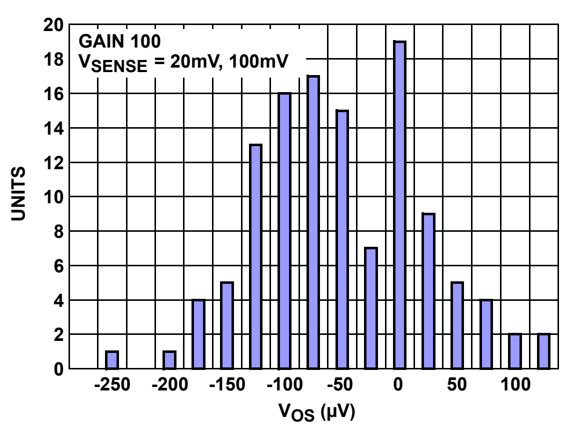


FIGURE 7. V_{OS} (µV) DISTRIBUTION AT +25°C, V_{RS+} = 12V, QUANTITY: 100

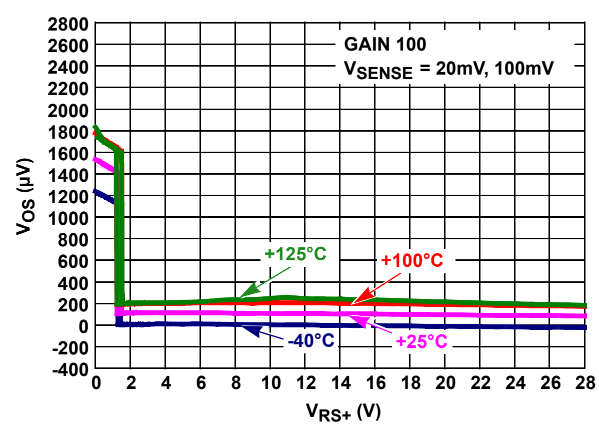


FIGURE 8. V_{OS} vs V_{RS+}

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. (Continued)

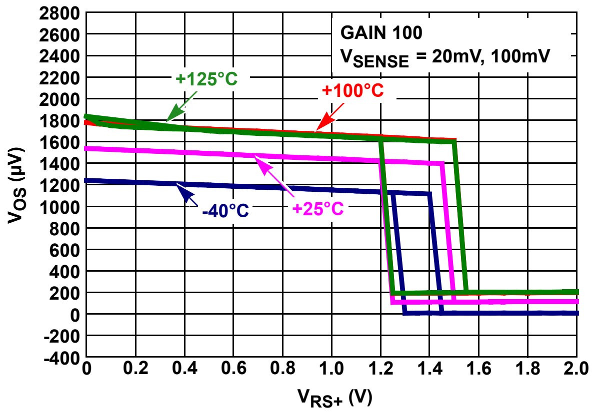


FIGURE 9. V_{OS} vs V_{RS+}

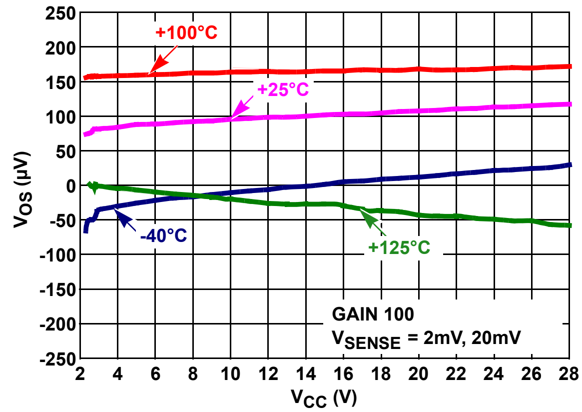


FIGURE 10. V_{OS} vs V_{CC}, V_{RS+}= 12V

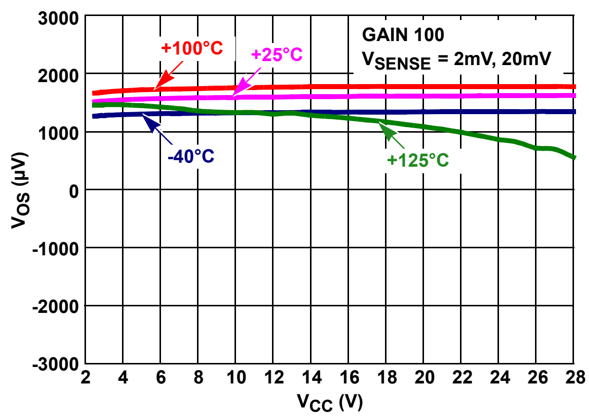


FIGURE 11. V_{OS} vs V_{CC}, V_{RS+} = 0.1V

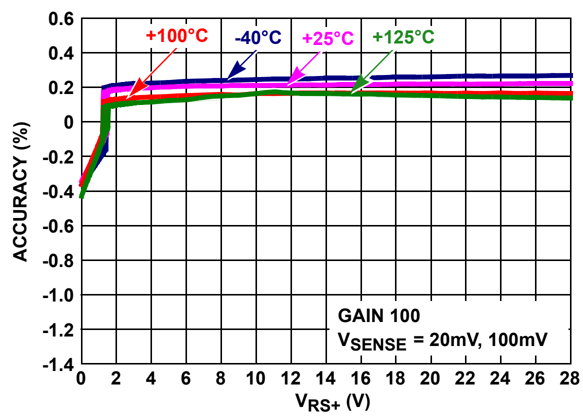


FIGURE 12. GAIN ACCURACY vs V_{RS+} = 0V TO 28V

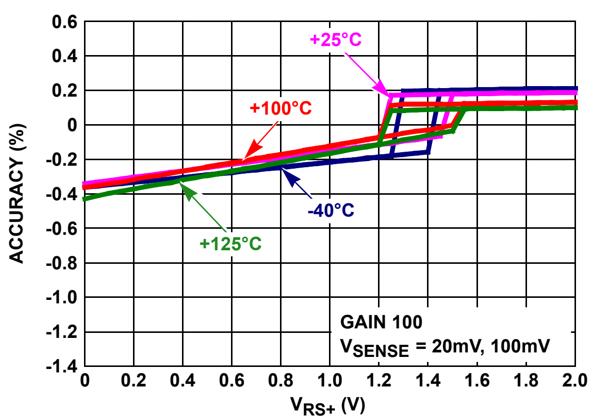


FIGURE 13. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

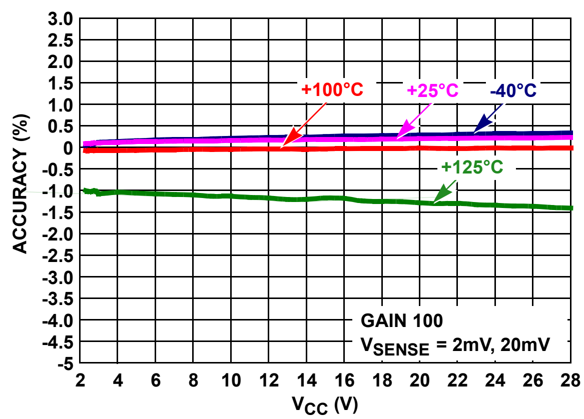


FIGURE 14. GAIN ACCURACY vs V_{CC}, V_{RS+} = 12V

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

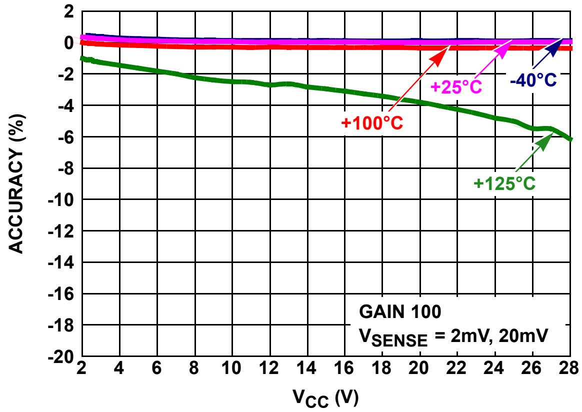


FIGURE 15. GAIN ACCURACY vs V_{CC}, V_{RS+} = 0.1V

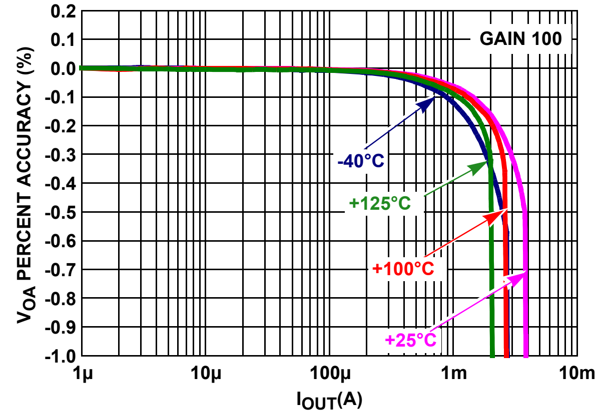


FIGURE 16. NORMALIZED V_{OA} vs I_{OUT}

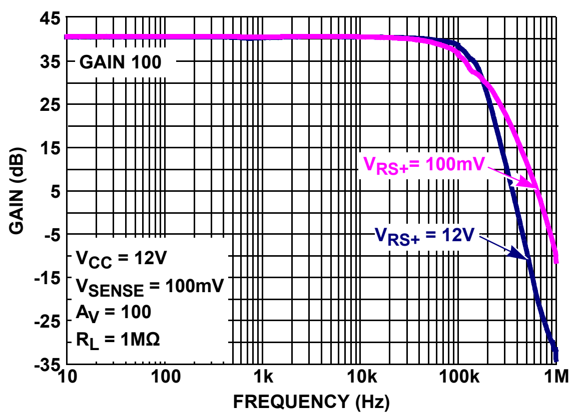


FIGURE 17. GAIN vs FREQUENCY V_{RS+} = 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 50mV$_{P-P}$

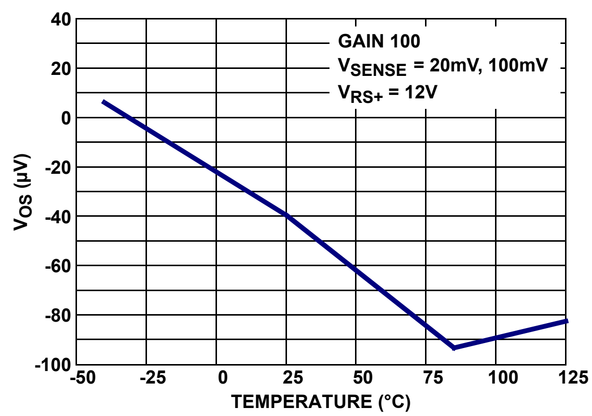


FIGURE 18. V_{OS} (µV) vs TEMPERATURE

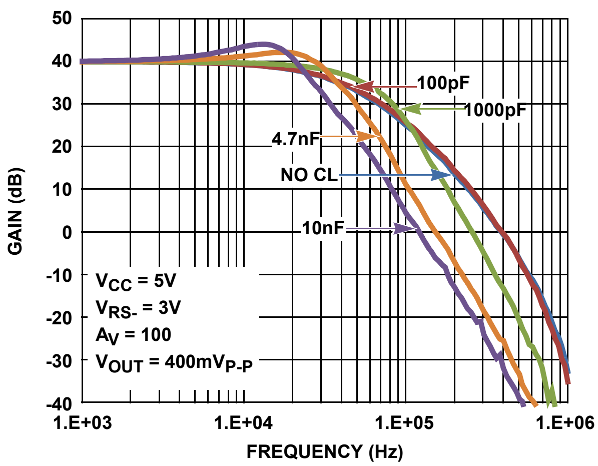


FIGURE 19. CAPACITIVE LOAD DRIVE GAIN vs FREQUENCY

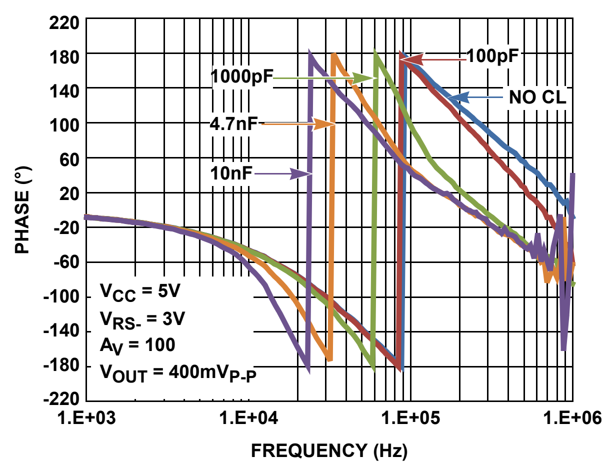


FIGURE 20. CAPACITIVE LOAD DRIVE PHASE vs FREQUENCY

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. (Continued)

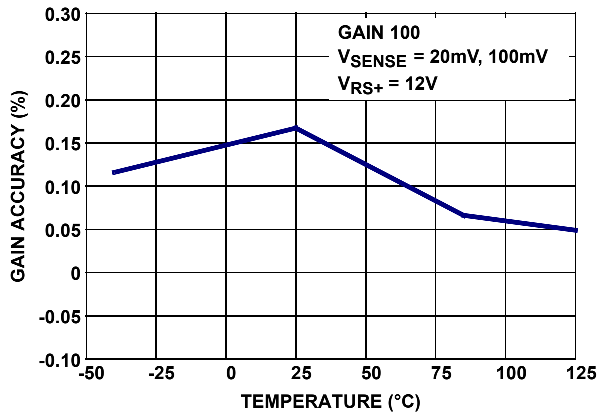


FIGURE 21. GAIN ACCURACY (%) vs TEMPERATURE

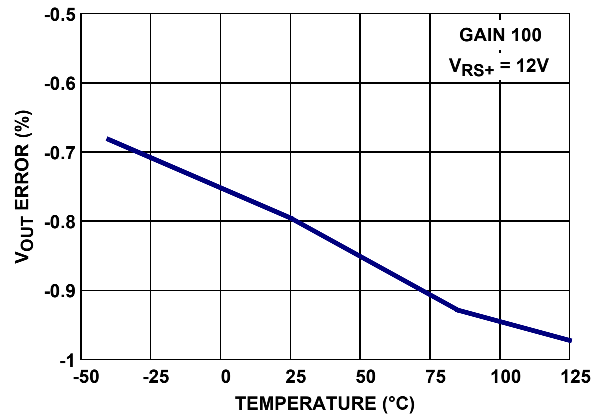


FIGURE 22. V_{OUT} ERROR (%) vs TEMPERATURE

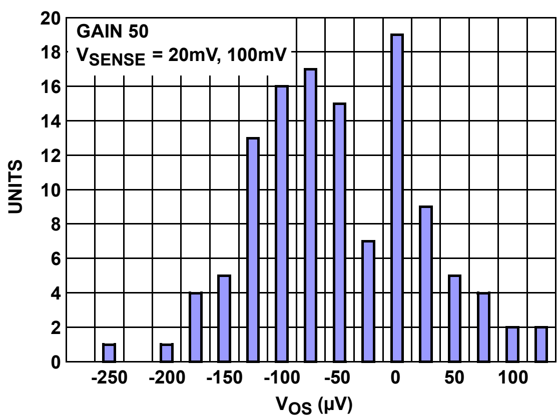


FIGURE 23. V_{OS} (µV) DISTRIBUTION AT +25°C, V_{RS+} = 12V, QUANTITY: 100

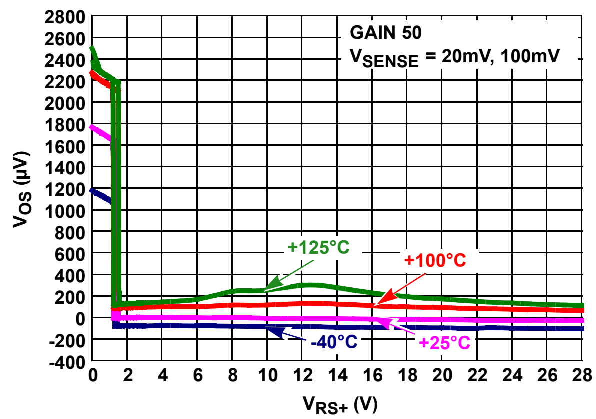


FIGURE 24. V_{OS} vs V_{RS+}

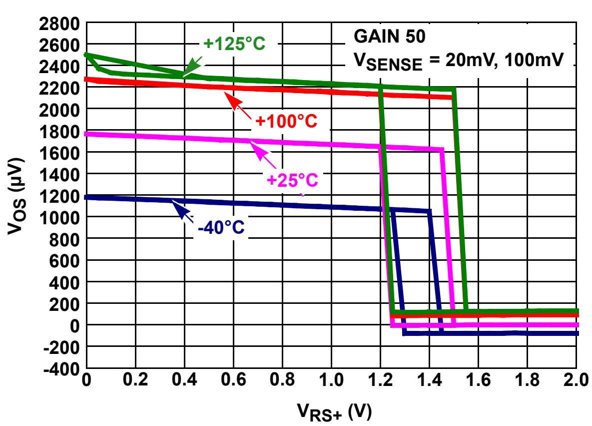


FIGURE 25. V_{OS} vs V_{RS+}

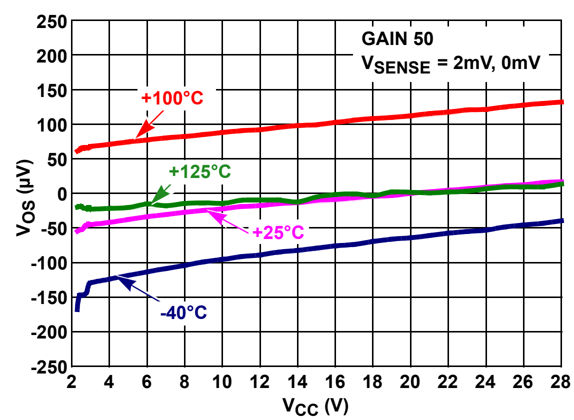


FIGURE 26. V_{OS} vs V_{CC}, V_{RS+} = 12V

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

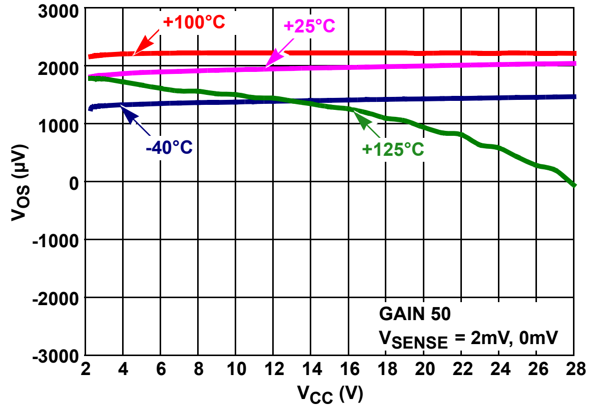


FIGURE 27. V_{OS} vs V_{CC}, V_{RS+} = V_{RS+} = 0.1V

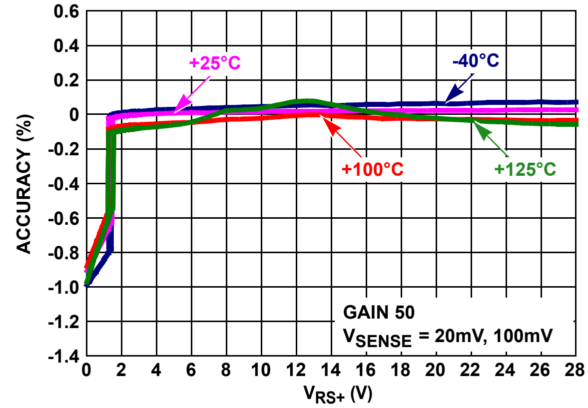


FIGURE 28. GAIN ACCURACY vs V_{RS+} = 0V TO 28V

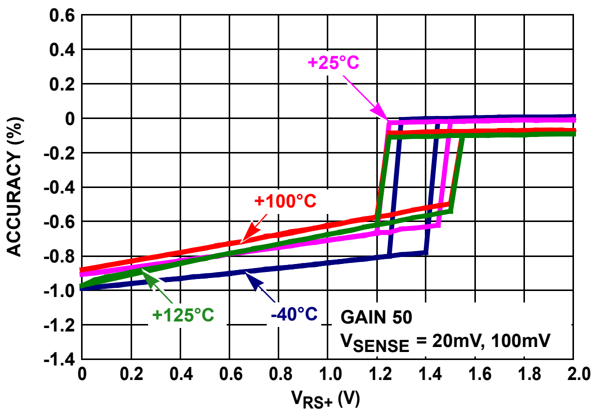


FIGURE 29. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

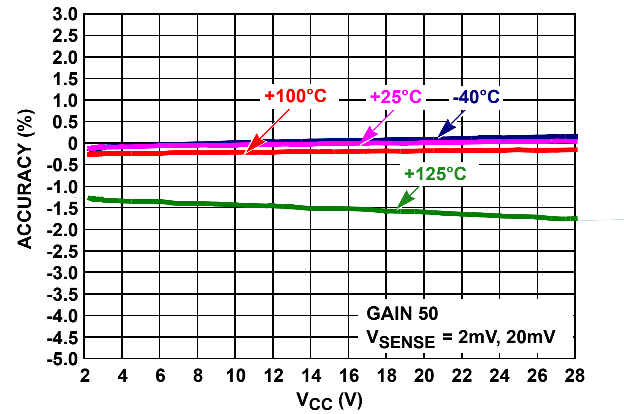


FIGURE 30. GAIN ACCURACY vs V_{CC}, HIGH-SIDE

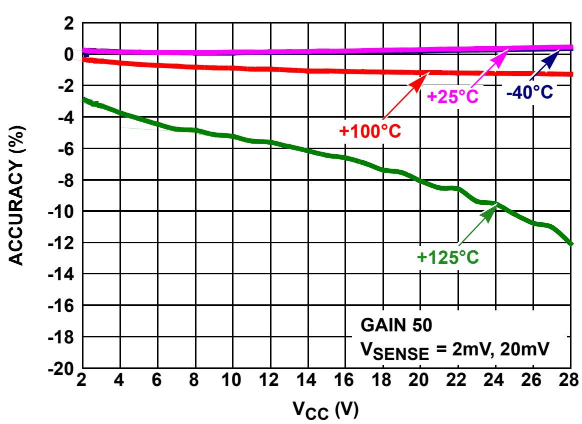


FIGURE 31. GAIN ACCURACY vs V_{CC}, LOW-SIDE

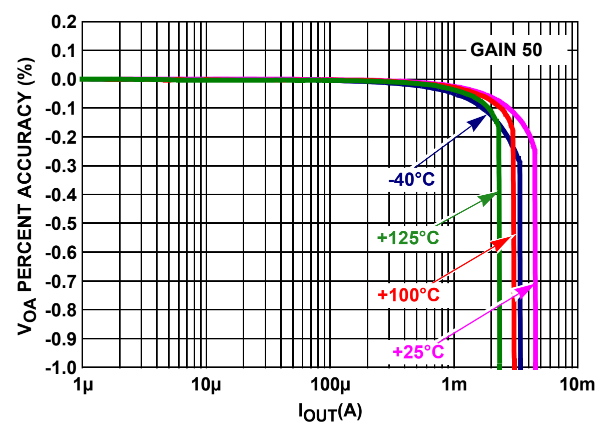


FIGURE 32. NORMALIZED V_{OA} vs I_{OUT}

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

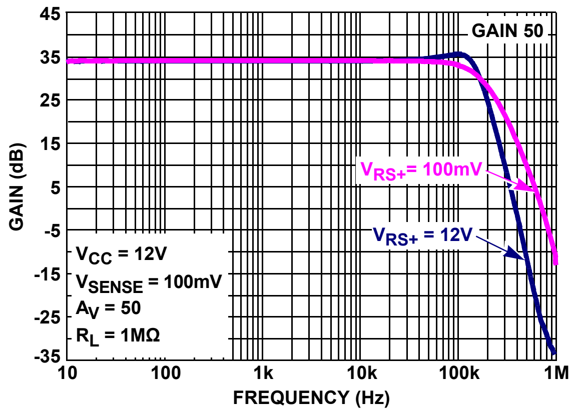


FIGURE 33. GAIN vs FREQUENCY V_{RS+} = 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 50mV_{P-P}

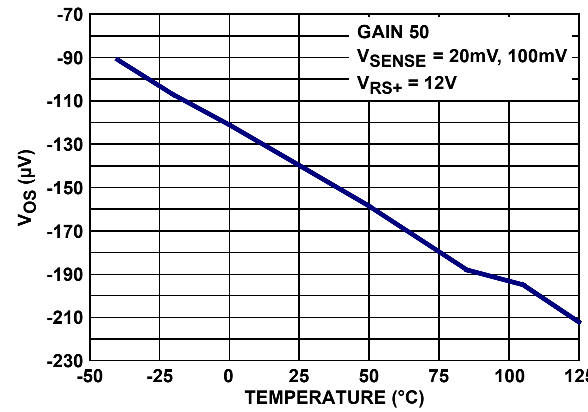


FIGURE 34. V_{OS} (µV) vs TEMPERATURE

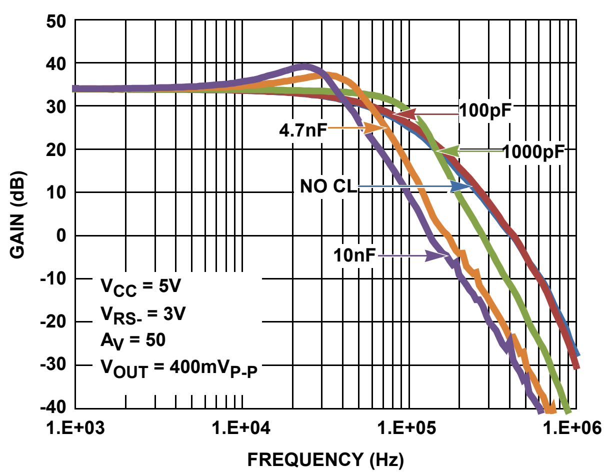


FIGURE 35. CAPACITIVE LOAD DRIVE GAIN vs FREQUENCY

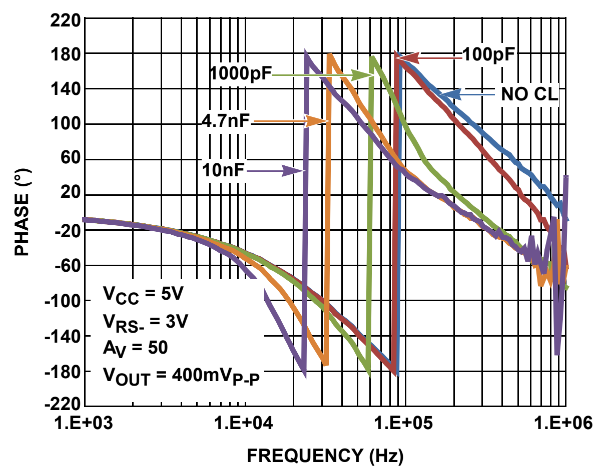


FIGURE 36. CAPACITIVE LOAD DRIVE PHASE vs FREQUENCY

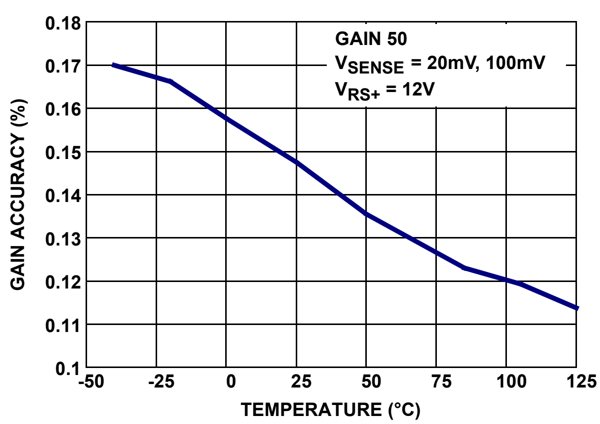


FIGURE 37. GAIN ACCURACY (%) vs TEMPERATURE

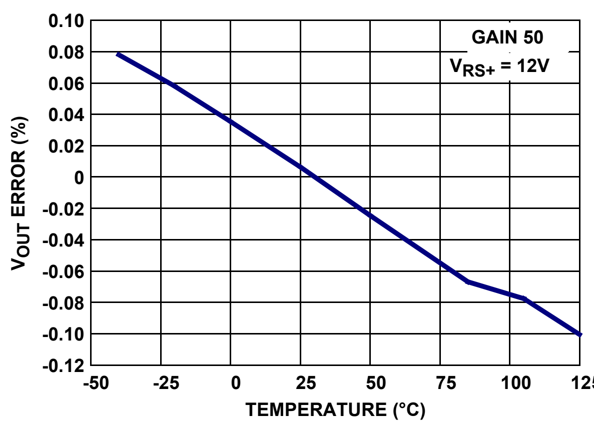


FIGURE 38. V_{OUT} ERROR (%) vs TEMPERATURE

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

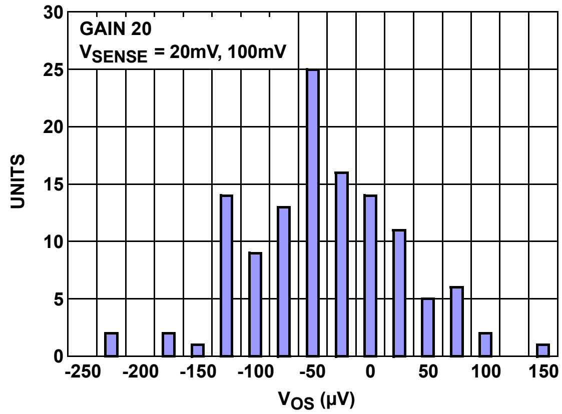


FIGURE 39. V_{OS} (µV) DISTRIBUTION AT +25°C, V_{RS+} = 12V, QUANTITY: 100

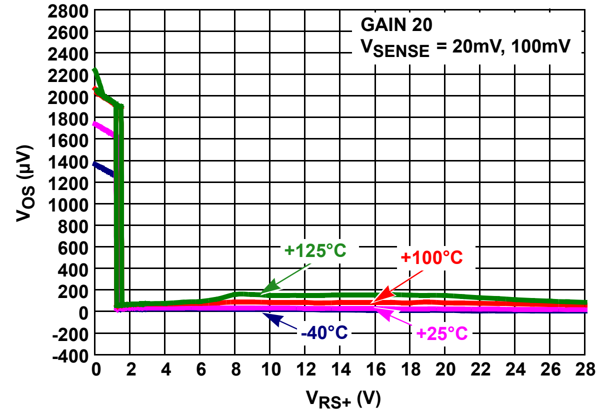


FIGURE 40. V_{OS} vs V_{RS+}

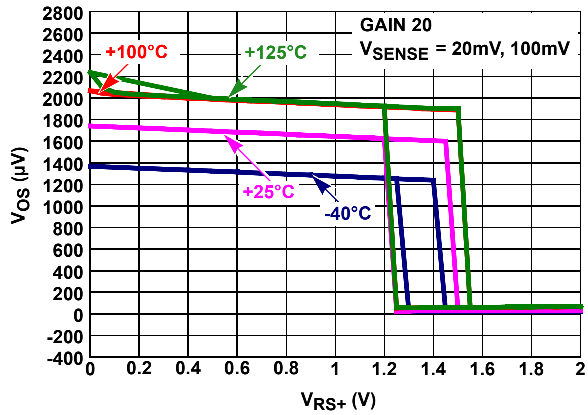


FIGURE 41. V_{OS} vs V_{RS+}

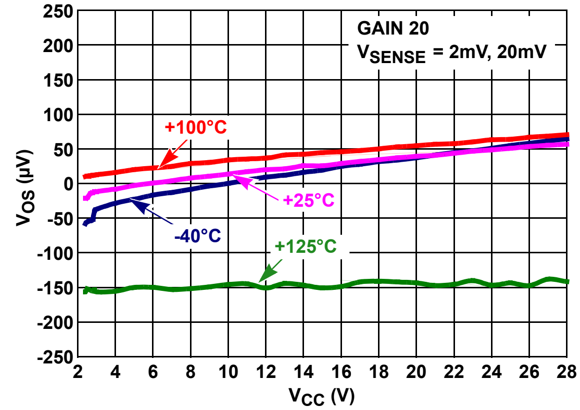


FIGURE 42. V_{OS} vs V_{CC}, V_{RS+} = 12V

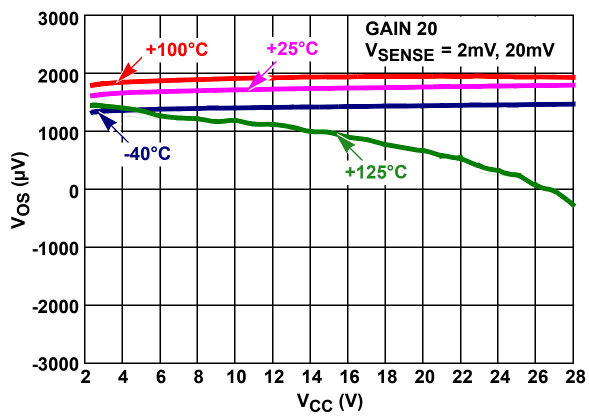


FIGURE 43. V_{OS} vs V_{CC}, V_{RS+} = 0.1V

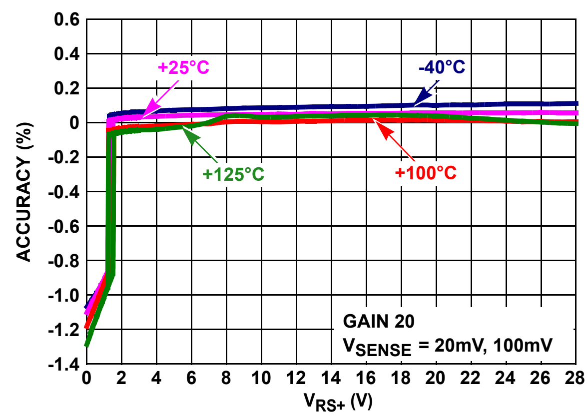


FIGURE 44. GAIN ACCURACY vs V_{RS+} = 0V TO 28V

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

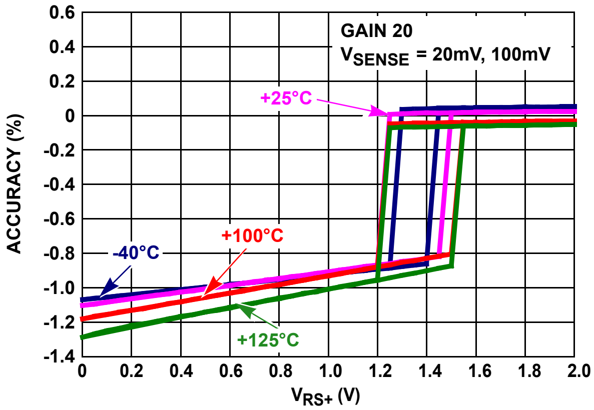


FIGURE 45. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

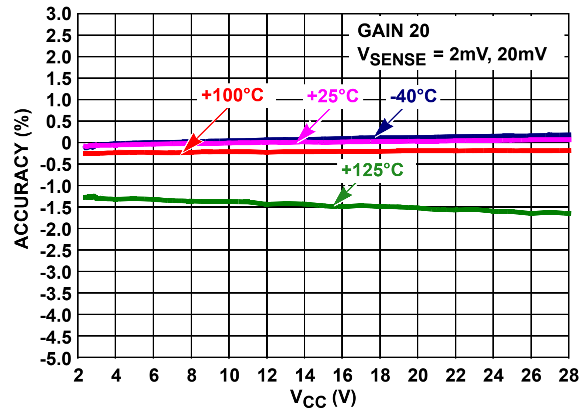


FIGURE 46. GAIN ACCURACY vs V_{CC}, HIGH-SIDE

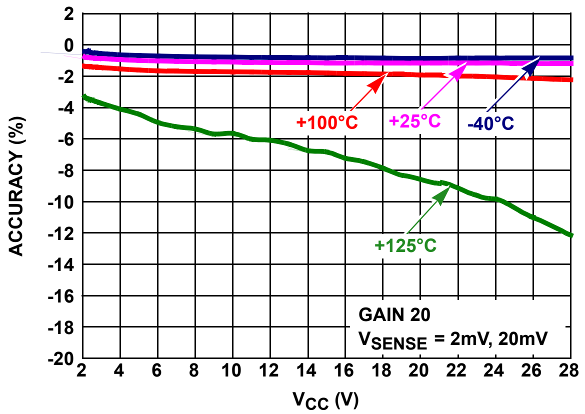


FIGURE 47. GAIN ACCURACY vs V_{CC}, LOW-SIDE

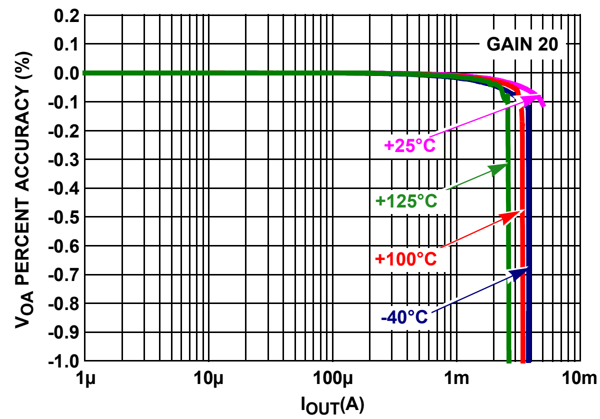


FIGURE 48. NORMALIZED V_{OA} vs I_{OUT}

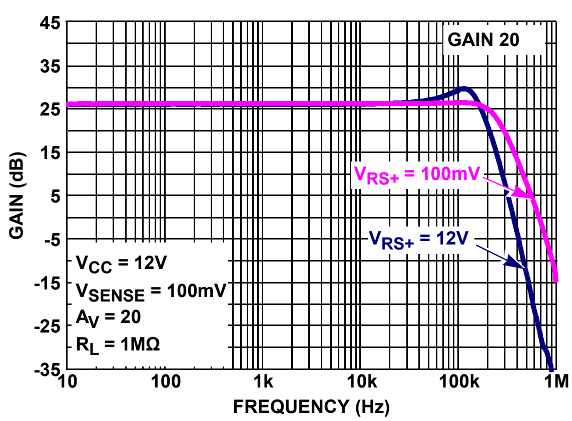


FIGURE 49. GAIN vs FREQUENCY V_{RS+} = 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 50mV$_{P-P}$

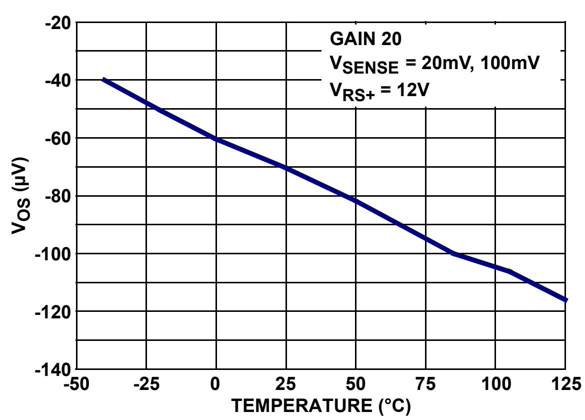


FIGURE 50. V_{OS} (µV) vs TEMPERATURE

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

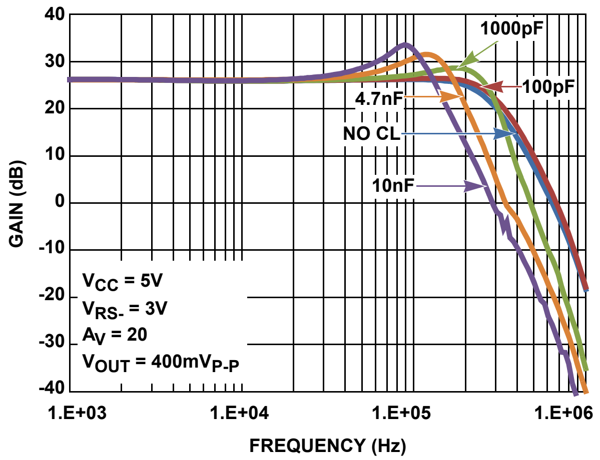


FIGURE 51. CAPACITIVE LOAD DRIVE GAIN VS FREQUENCY

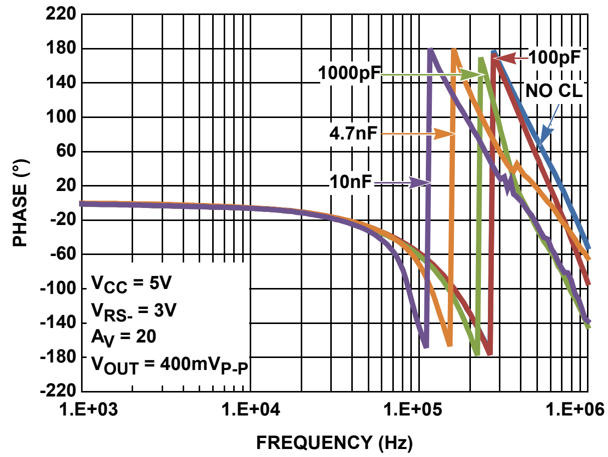


FIGURE 52. CAPACITIVE LOAD DRIVE PHASE VS FREQUENCY

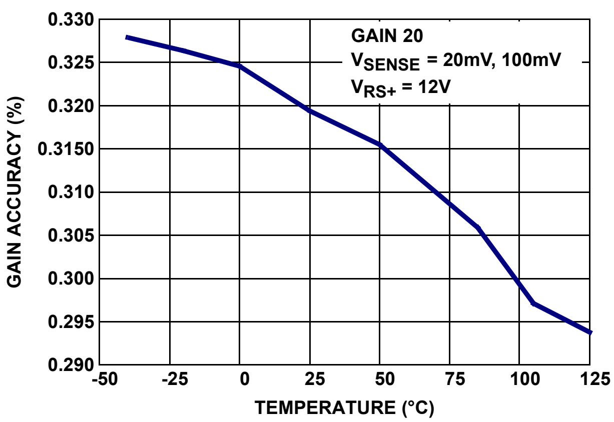


FIGURE 53. GAIN ACCURACY (%) vs TEMPERATURE

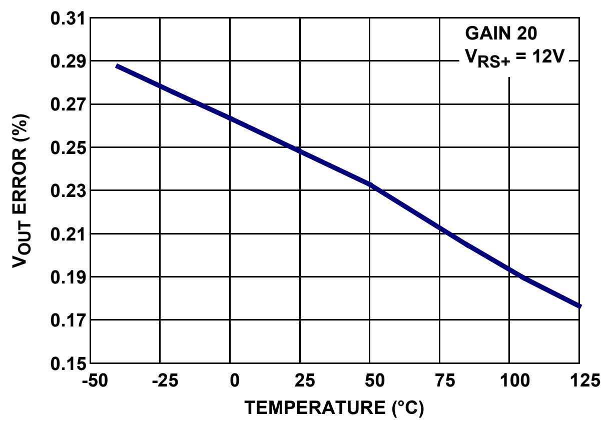


FIGURE 54. V_{OUT} ERROR (%) vs TEMPERATURE

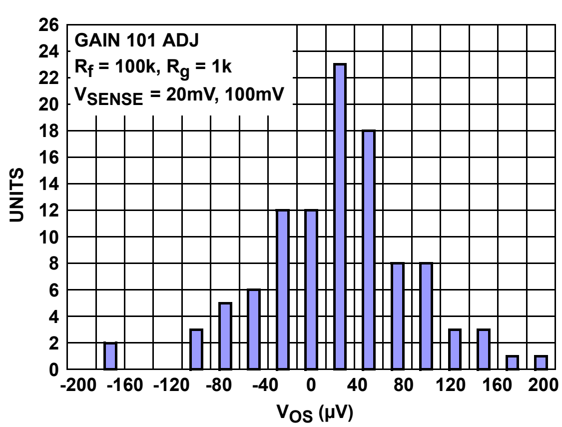


FIGURE 55. V_{OS} (µV) DISTRIBUTION AT +25°C, V_{RS+} = 12V, QUANTITY: 100

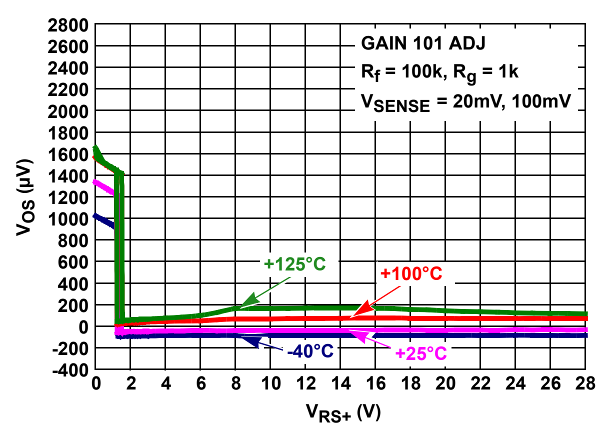


FIGURE 56. V_{OS} vs V_{RS+}

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. **(Continued)**

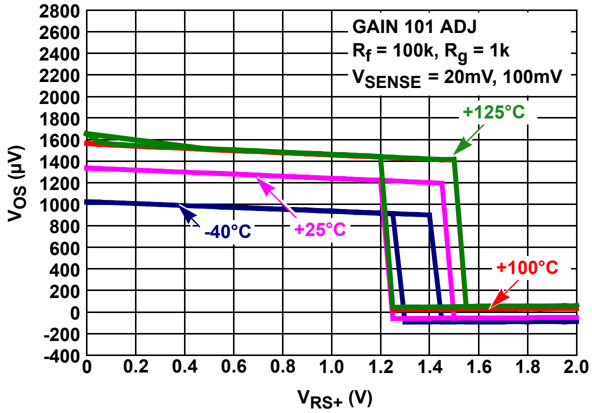


FIGURE 57. V_{OS} vs V_{RS+}

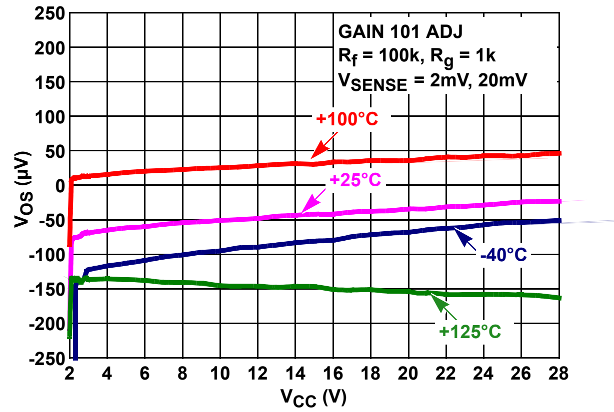


FIGURE 58. V_{OS} vs V_{CC}, HIGH-SIDE

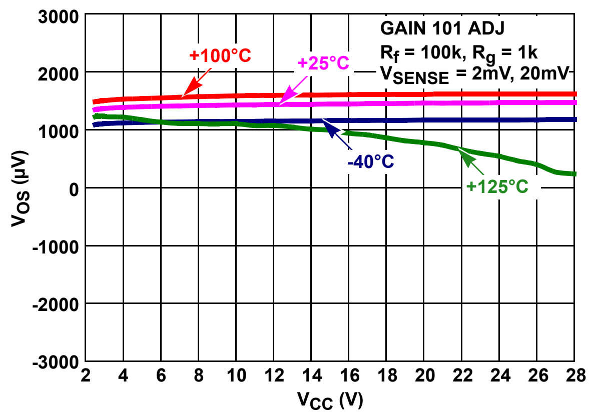


FIGURE 59. V_{OS} vs V_{CC}, LOW-SIDE

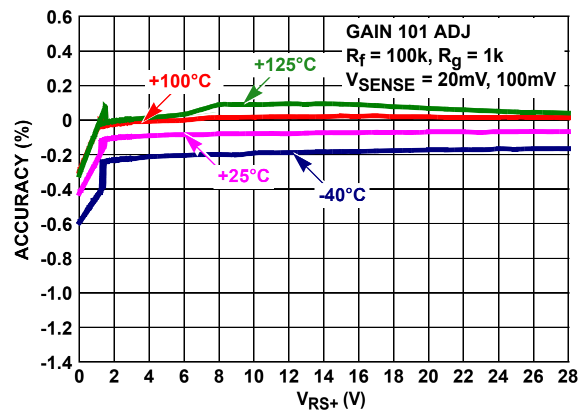


FIGURE 60. GAIN ACCURACY vs V_{RS+} = 0V TO 28V

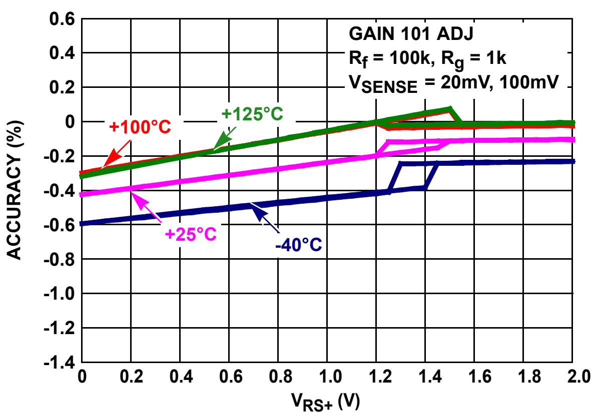


FIGURE 61. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

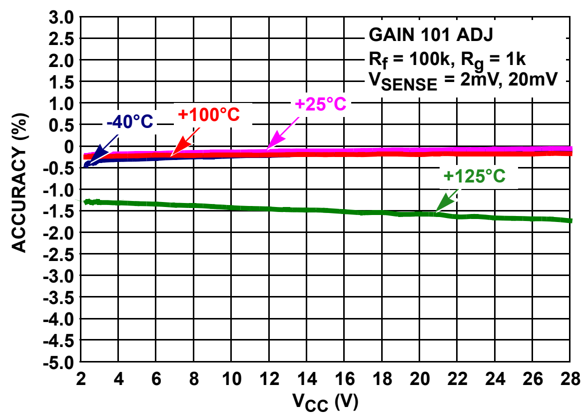


FIGURE 62. GAIN ACCURACY vs V_{CC}, V_{RS+} = 12V

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. (Continued)

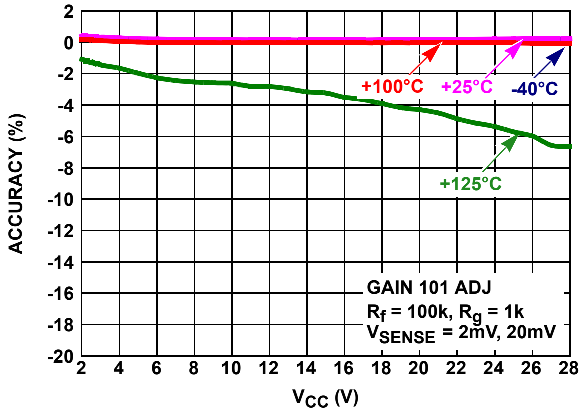


FIGURE 63. GAIN ACCURACY vs V_{CC}, V_{RS+} = 0.1V

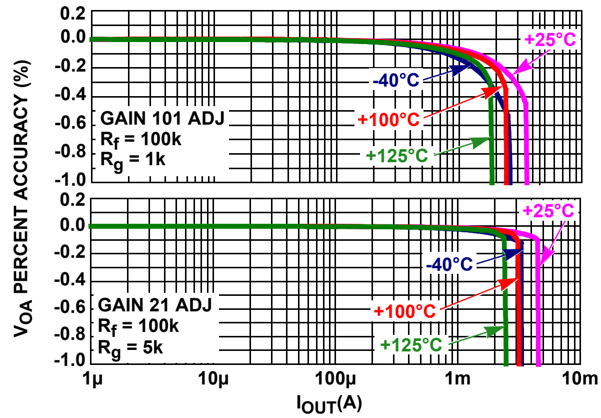


FIGURE 64. NORMALIZED V_{OA} vs I_{OUT}

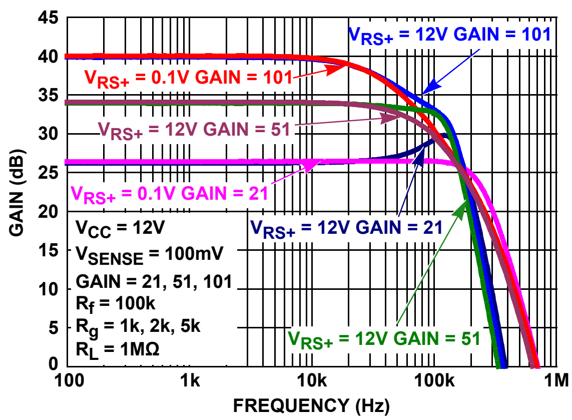


FIGURE 65. GAIN vs FREQUENCY V_{RS+} = 100mV/12V, V_{SENSE} = 100mV, V_{OUT} = 50mV$_{P-P}$

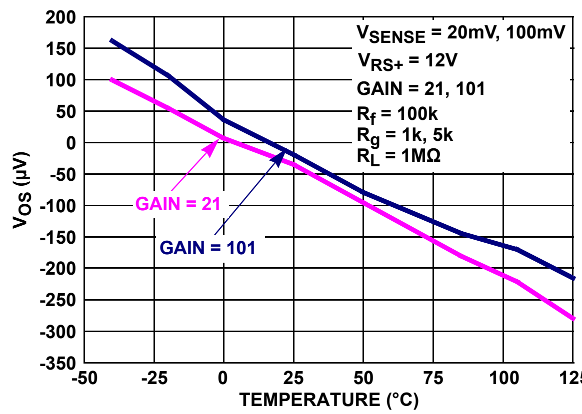


FIGURE 66. V_{OS} (µV) vs TEMPERATURE

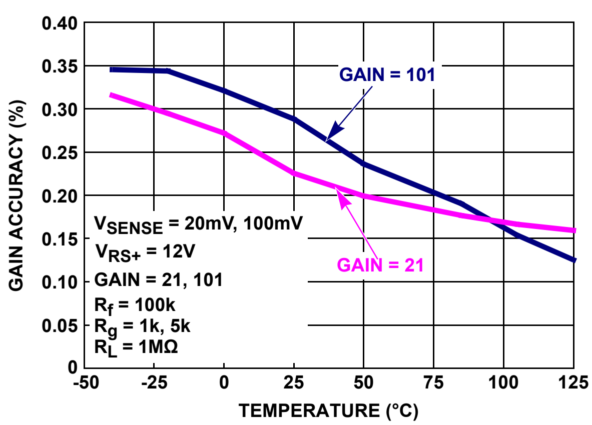


FIGURE 67. GAIN ACCURACY (%) vs TEMPERATURE

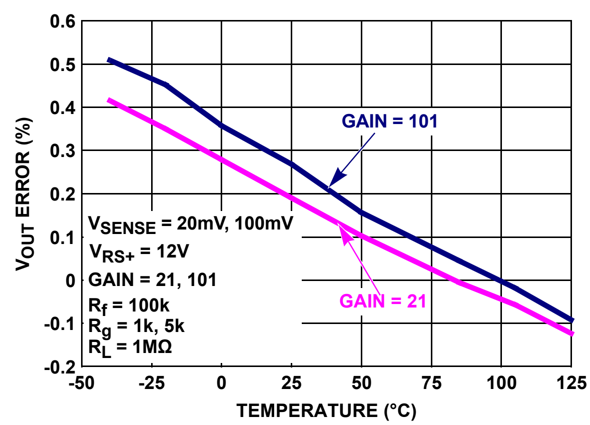


FIGURE 68. V_{OUT} ERROR (%) vs TEMPERATURE

Typical Performance Curves V_{CC} = 12V, R_L = 1MΩ, unless otherwise specified. (Continued)

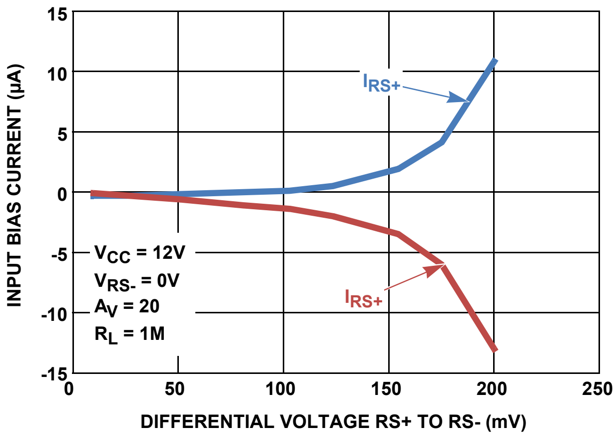


FIGURE 69. LOW SIDE CURRENT SENSING INPUT BIAS CURRENTS

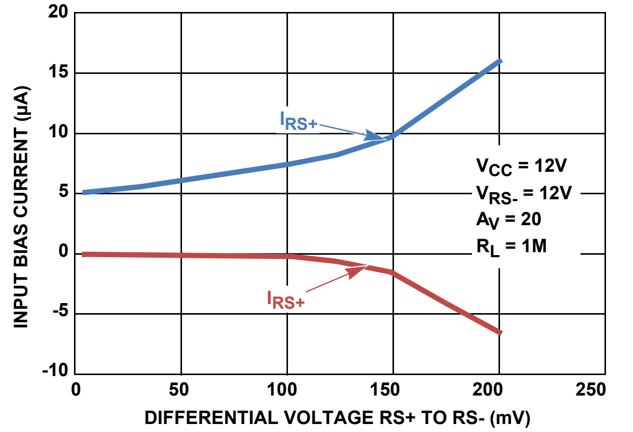


FIGURE 70. HIGH SIDE CURRENT SENSING INPUT BIAS CURRENTS

Test Circuits and Waveforms

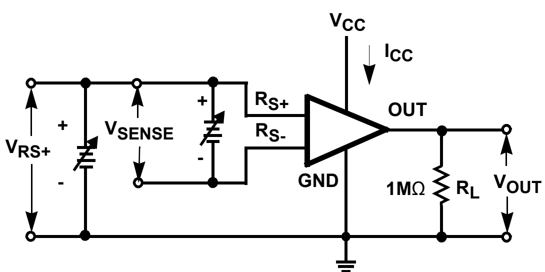


FIGURE 71. I_{CC}, V_{OS}, V_{OA}, CMRR, PSRR, GAIN ACCURACY

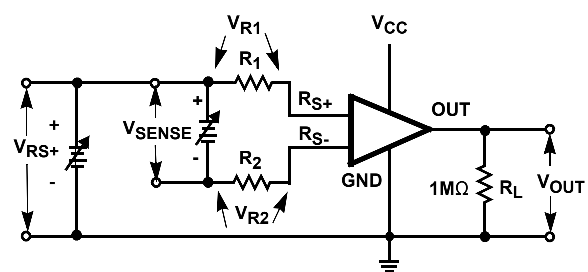


FIGURE 72. INPUT BIAS CURRENT, LEAKAGE CURRENT

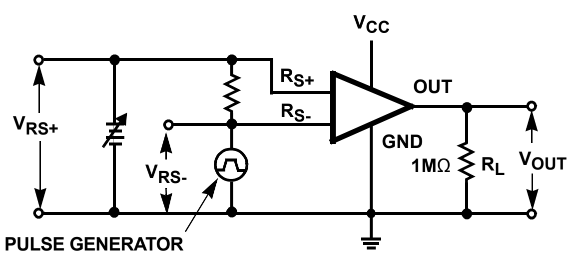


FIGURE 73. t_s, SATURATION RECOVERY TIME

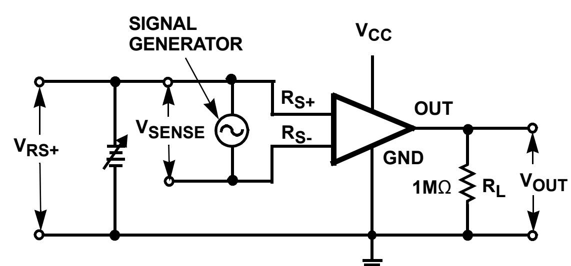


FIGURE 74. GAIN vs FREQUENCY

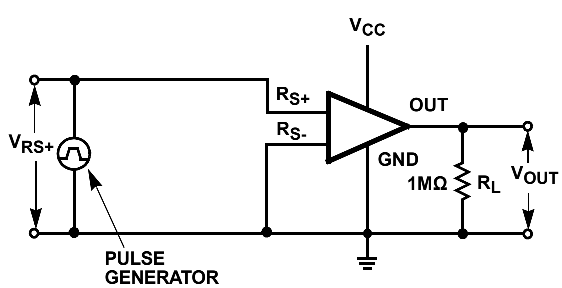


FIGURE 75. SLEW RATE

Applications Information

Functional Description

The ISL28006-20, ISL28006-50 and ISL28006-100 are single supply, uni-directional current sense amplifiers with fixed gains of 20V/V, 50V/V and 100V/V respectively. The ISL28006-ADJ is single supply, uni-directional current sense amplifier with an adjustable gain via external resistors (see Figure 80). The ISL28006-ADJ is stable for gains of 20 and higher.

The ISL28006 is a 2-stage amplifier. Figure 76 shows the active circuitry for high-side current sense applications where the sense voltage is between 1.35V to 28V. Figure 77 shows the active circuitry for ground sense applications where the sense voltage is between 0V to 1.35V.

The first stage is a bi-level trans-conductance amp and level translator. The gm stage converts the low voltage drop (V_{SENSE}) sensed across an external milli-ohm sense resistor, to a current (@ gm = 21.3µA/V). The trans-conductance amplifier forces a current through R_1 resulting to a voltage drop across R_1 that is equal to the sense voltage (V_{SENSE}). The current through R_1 is mirrored across R_5 creating a ground-referenced voltage at the input of the second amplifier equal to V_{SENSE}.

The second stage is responsible for the overall gain and frequency response performance of the device. The fixed gains (20, 50, 100) are set with internal resistors R_f and R_g. The variable gain (ADJ) has an additional FB pin and uses external gain resistors to set the gain of the output. For the fixed gain amps the only external component needed is a current sense resistor (typically 0.001Ω to 0.01Ω, 1W to 2W).

The transfer function for the fixed gain parts is given in Equation 1.

$$V_{OUT} = GAIN \times (I_S R_S + V_{OS}) \quad \text{(EQ. 1)}$$

The transfer function for the adjustable gain part is given in Equation 2.

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right)(I_S R_S + V_{OS}) \quad \text{(EQ. 2)}$$

Where $I_S R_S$ is the product of the load current and the sense resistor and is equal to V_{SENSE}.

When the sensed input voltage is >1.35V, the gm_{HI} amplifier path is selected and the input gm stage derives its ~2.86µA supply current from the input source through the RS+ terminal. When the sense voltage at R_S+ drops below the 1.35V threshold, the gm_{LO} amplifier is enabled for Low Side current sensing. The gm_{LO} input bias current reverses, flowing out of the RS- pin. Since the gm_{LO} amplifier is sensing voltage around ground, it cannot source current to R5. A current mirror referenced off Vcc supplies the current to the second stage for generating a ground referenced output voltage. See Figures 69 and 70 for typical input bias currents for High and Low side current sensing.

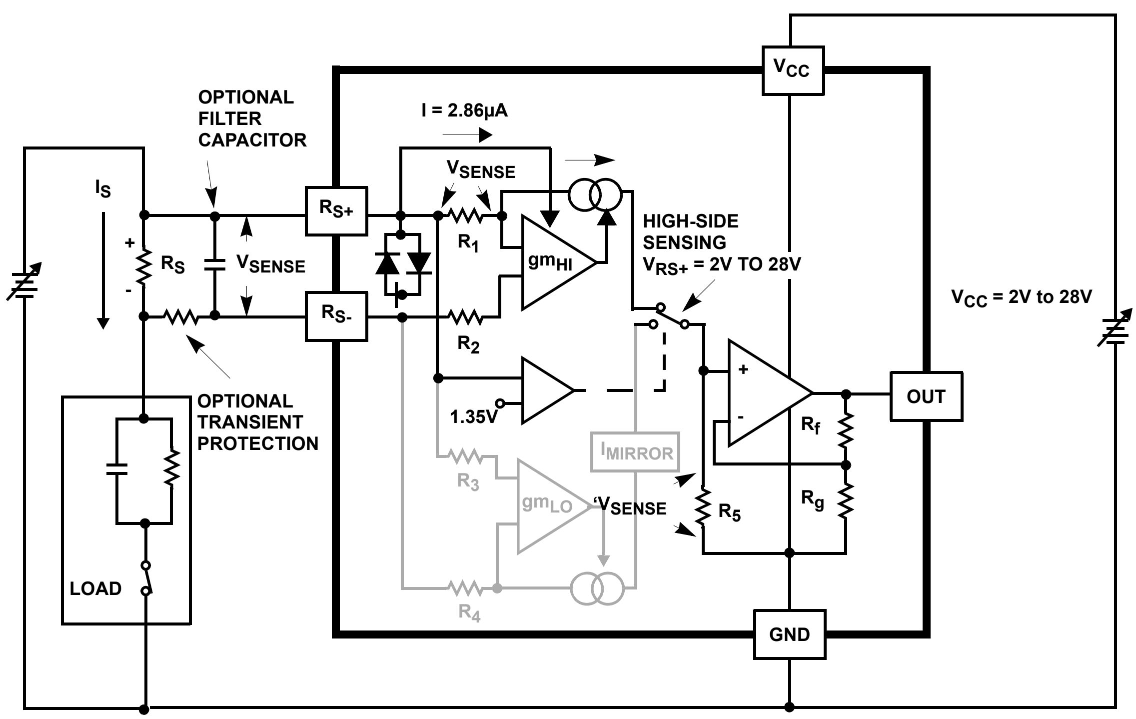


FIGURE 76. HIGH-SIDE CURRENT DETECTION

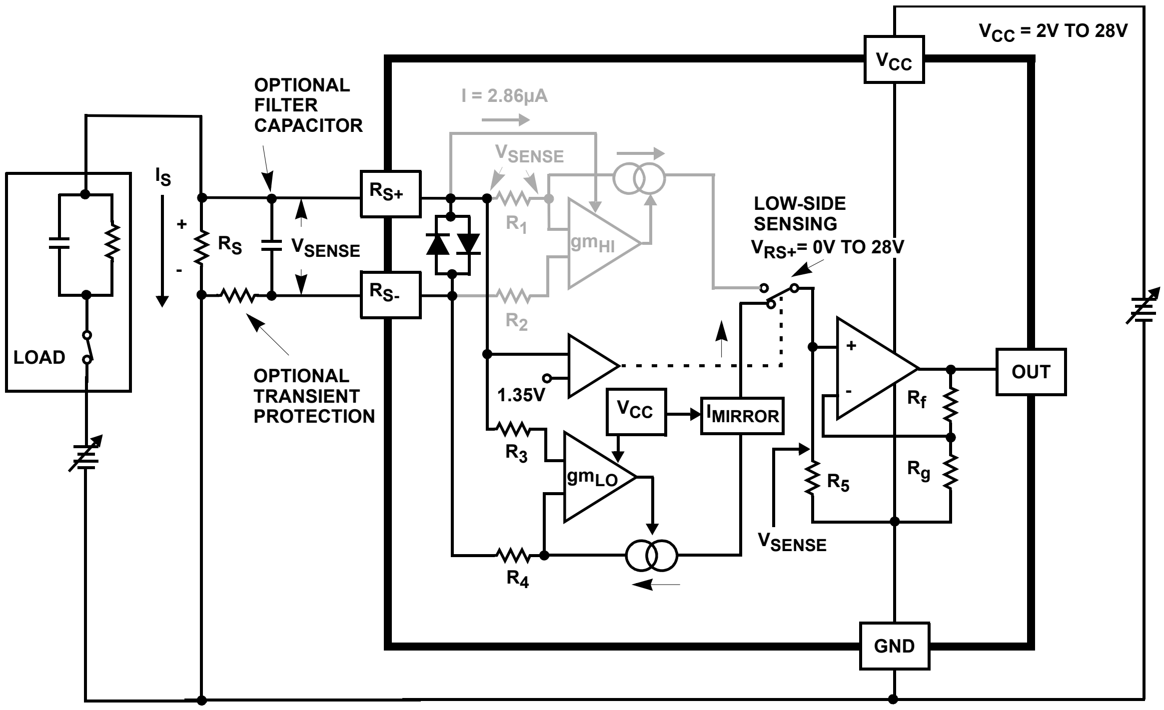


FIGURE 77. LOW-SIDE CURRENT DETECTION

Hysteretic Comparator

The input trans-conductance amps are under control of a hysteretic comparator operating from the incoming source voltage on the R_{S+} pin (Figure 78). The comparator monitors the voltage on R_{S+} and switches the sense amplifier from the low-side gm amp to the high-side gm amplifier whenever the input voltage at R_{S+} increases above the 1.35V threshold. Conversely, a decreasing voltage on the R_{S+} pin, causes the hysteric comparator to switch from the high-side gm amp to the low-side gm amp as the voltage decreases below 1.35V. It is that low-side sense gm amplifier that gives the ISL28006 the proprietary ability to sense current all the way to 0V. Negative voltages on the R_{S+} or R_{S-} are beyond the sensing voltage range of this amplifier.

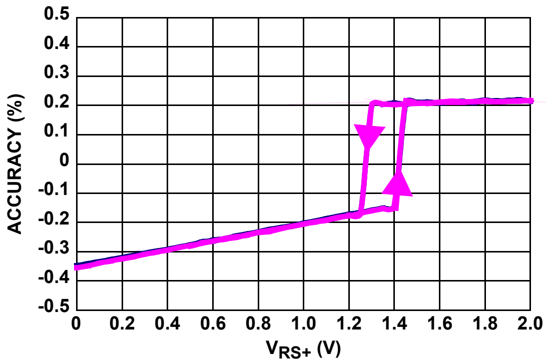


FIGURE 78. GAIN ACCURACY vs V_{RS+} = 0V TO 2V

Typical Application Circuit

Figure 80 shows the basic application circuit and optional protection components for switched-load applications. For applications where the load and the power source is permanently connected, only an external sense resistor is needed. For applications where fast transients are caused by hot plugging the source or load, external protection components may be needed. The external current limiting resistor (R_P) in Figure 80 may be required to limit the peak current through the internal ESD diodes to <20mA. This condition can occur in applications that experience high levels of in-rush current causing high peak voltages that can damage the internal ESD diodes. An R_P resistor value of 100Ω will provide protection for a 2V transient with the maximum of 20mA flowing through the input while adding only an additional 13µV (worse case over-temperature) of V_{OS}. Refer to Equation 3:

$$((R_P \times I_{RS-}) = (100\Omega \times 130nA) = 13\mu V) \quad \text{(EQ. 3)}$$

Switching applications can generate voltage spikes that can overdrive the amplifier input and drive the output of the amplifier into the rails, resulting in a long overload recover time. Capacitors C_M and C_D filter the common mode and differential voltage spikes.

Error Sources

There are 3 dominant error sources: gain error, input offset voltage error and Kelvin voltage error (see Figure 79). The gain error is dominated by the internal resistance matching tolerances. The remaining errors appear as sense voltage errors at the input to the amplifier. They are V_{OS} of the amplifier and Kelvin voltage errors. If the transient protection resistor is added, an additional V_{OS} error can result from the IxR voltage due to input bias current. The limiting resistor should only be added to the R_{S-} input, due to the high-side gm amplifier (gm_{HI}) sinking several micro amps of current through the R_{S+} pin.

Layout Guidelines

The Kelvin Connected Sense Resistor

The source of Kelvin voltage errors is illustrated in Figure 79. The resistance of 1/2 Oz copper is ~1mΩ per square with a TC of ~3900ppm/°C (0.39%/°C). When you compare this unwanted parasitic resistance with the total 1mΩ to 10mΩ resistance of the sense resistor, it is easy to see why the sense connection must be chosen very carefully. For example, consider a maximum current of 20A through a 0.005Ω sense resistor, generating a V_{SENSE} = 0.1 and a full scale output voltage of 10V (G = 100). Two side contacts of only 0.25 square per contact puts the V_{SENSE} input about 0.5 x 1mΩ away from the resistor end capacitor. If only 10A the 20A total current flows through the kelvin path to the resistor, you get an error voltage of 10mV (10A x 0.5sq x 0.001Ω/sq. = 10mV) added to the 100mV sense voltage for a sense voltage error of 10% (0.110V-0.1)/0.1V) x 100.

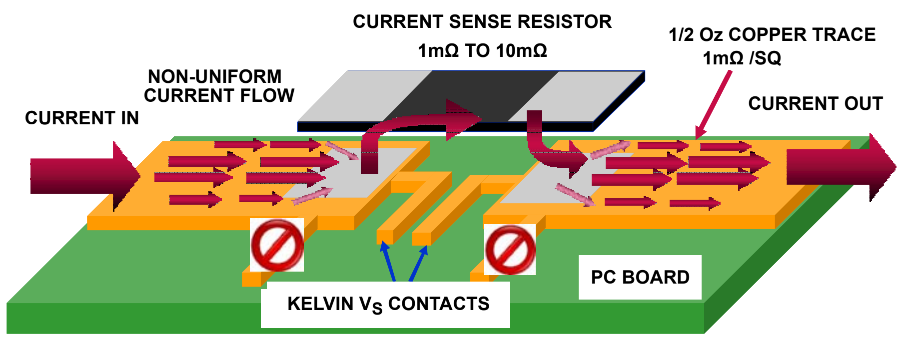


FIGURE 79. PC BOARD CURRENT SENSE KELVIN CONNECTION

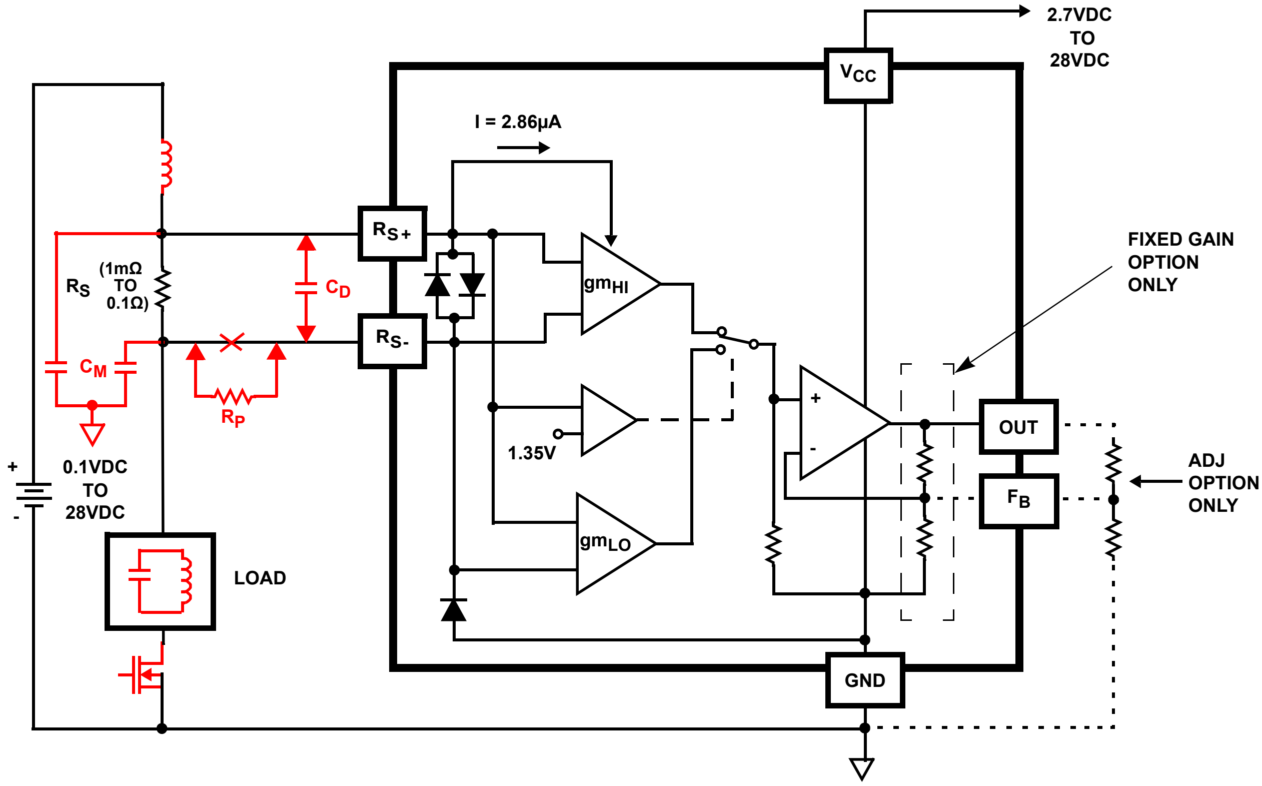


FIGURE 80. TYPICAL APPLICATION CIRCUIT

Overall Accuracy (V_{OA} %)

V_{OA} is defined as the total output accuracy Referred-to-Output (RTO). The output accuracy contains all offset and gain errors, at a single output voltage. Equation 4 is used to calculate the % total output accuracy.

$$V_{OA} = 100 \times \left(\frac{V_{OUT}actual - V_{OUT}expected}{V_{OUT}expected}\right) \quad \text{(EQ. 4)}$$

where

V_{OUT} Actual = V_{SENSE} x GAIN

Example: Gain = 100, For 100mV V_{SENSE} input we measure 10.1V. The overall accuracy (V_{OA}) is 1% as shown in Equation 5.

$$V_{OA} = 100 \times \left(\frac{10.1 - 10}{10}\right) = 1\% \quad \text{(EQ. 5)}$$

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 6:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 6)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 7:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 7)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_{CC} = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
November 22, 2013	FN6548.6	Added eight new Typical Performance Curves 1. Av=100 Capacitive Load Drive Gain vs Freq 2. Av=100 Capacitive Load Drive Phase vs Freq 3. Av=50 Capacitive Load Drive Gain vs Freq 4. Av=50 Capacitive Load Drive Phase vs Freq 5. Av=20 Capacitive Load Drive Gain vs Freq 6. Av=20 Capacitive Load Drive Phase vs Freq 7. High Side Operation Input Bias Currents 8. Low Side Operation Input Bias Currents Under Electrical Specifications Table: Changed parameter from Is to Icc to clarify supply current Ordering information table on page 3: Changed Note 4 location in the table.
April 12, 2011	FN6548.5	Converted to new template Page 1 - Changed headings for “Typical Application” and “Gain Accuracy vs VRS+ = 0V to 28V” to Figure titles (Figures 1 and 2). Page 1 - Updated Intersil Trademark statement at bottom of page 1 per directive from Legal. Page 7 - Updated over temp note in Min Max column of spec tables from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to new standard "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." Page 19 - Figure 69, Low side current detection schematic: Moved the LOAD from the ground side of the power side circuit to the high side.
September 2, 2010	FN6548.4	Added -T7A tape and reel options to Ordering Information Table for all packages.
May 12, 2010	FN6548.3	Added Note 4 to Part Marking Column in “Ordering Information” on page 3. Corrected hyperlinks in Notes 1 and 3 in “Ordering Information” on page 3.
April 8, 2010		Removed “Coming Soon” from evaluation boards in “Ordering Information” on page 3.
April 7, 2010		Added “Related Literature” on page 1 Updated Package Drawing Number in the “Ordering Information” on page 3 for the 20V, 50V and 100V options from MDP0038 to P50.64A. Revised package outline drawing from MDP0038 to P5.064A on page 24. MDP0038 package contained 2 packages for both the 5 and 6 Ld SOT-23. MDP0038 was obsoleted and the packages were separated and made into 2 separate package outline drawings; P5.064A and P6.064A. Changes to the 5 Ld SOT-23 were to move dimensions from table onto drawing, add land pattern and add JEDEC reference number.
March 10, 2010	FN6548.2	Releasing adjustable gain option. Added adjustable block diagram (Page 2), Added adjustable gain limits to electrical spec table, added Figures 47 through 60, Added +85°C curves to Figures 6 thru 14, 20 thru 28, 34 thru 42, and Figures 48 thru 56. Modified Figure 70.
February 4, 2010	FN6548.1	-Page 1: Edited last sentence of paragraph 2. Moved order of GAIN listings from 20, 50, 100 to 100, 50, 20 in the 3rd paragraph. Under Features ....removed "Low Input Offset Voltage 250μV, max" Under Features .... moved order of parts listing from 20, 50, 100 (from top to bottom) to 100, 50, 20. -Page 3: Removed coming soon on ISL28006FH50Z and ISL28006FH20Z and changes the order or listing them to 100, 50, 20. -Page 5: VOA test. Under conditions column ...deleted 20mV to. It now reads ... Vsense = 100mV SR test. Under conditions column ..deleted what was there. It now reads ... Pulse on RS+pin, See Figure 51 -Page 6: ts test. Removed Gain = 100 and Gain = 100V/V in both description and conditions columns respectively. -Page 9: Added VRS+= 12V to Figures 16, 17, 18. -Page 11: Added VRS+= 12V to Figures 30, 31, 32. -Page 13 & 14: Added VRS+= 12V to Figures 44, 45, 46. -Page 14 Added Figure 51 and adjusted figure numbers to account for the added figure. -Figs 8, 26, and 40 change "HIGH SIDE" to "VRS = 12V", where RS is subscript. -Figs 9, 27, and 41 change "LOW SIDE" to "VRS = 0.1V", where RS is subscript.
December 14, 2009	FN6548.0	Initial Release

About Intersil

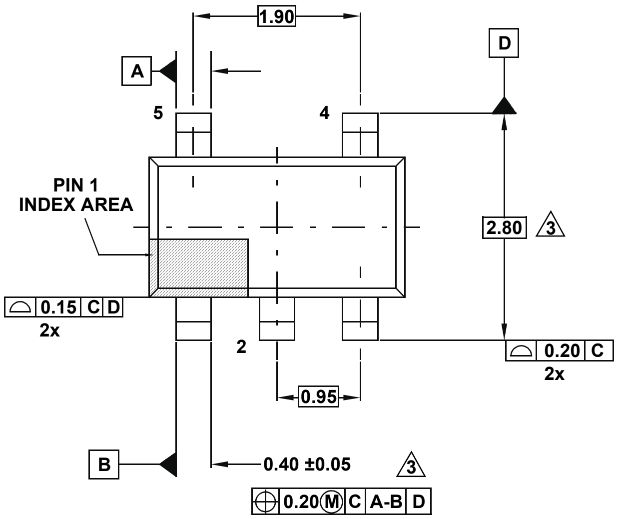
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

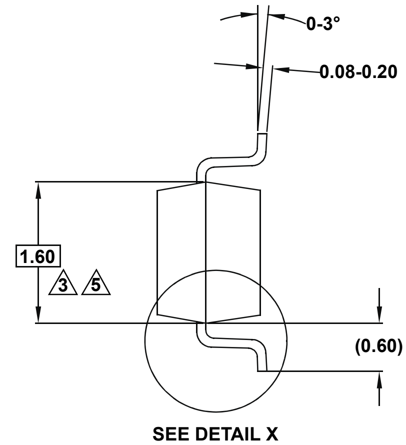
Package Outline Drawing

P5.064A

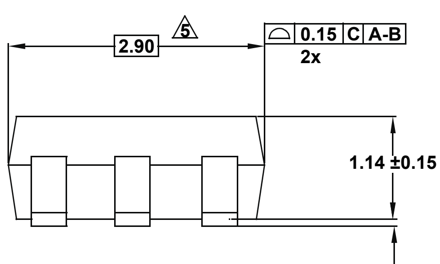
5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



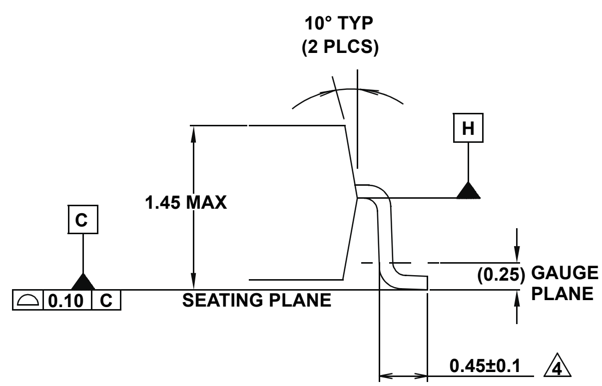
TOP VIEW



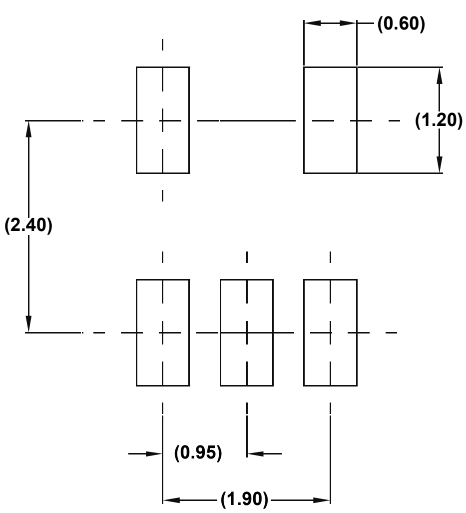
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

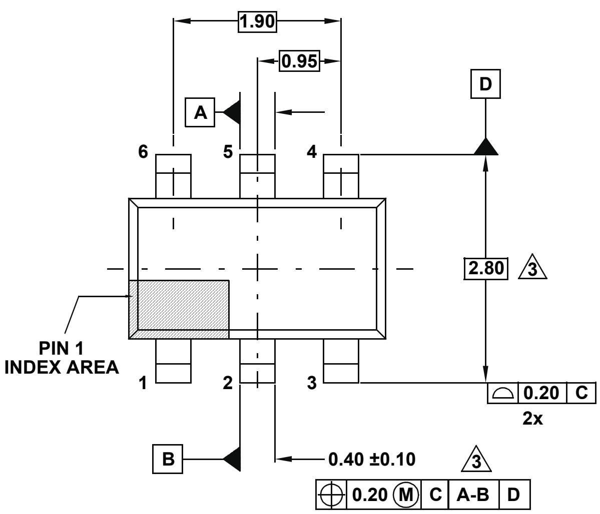
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

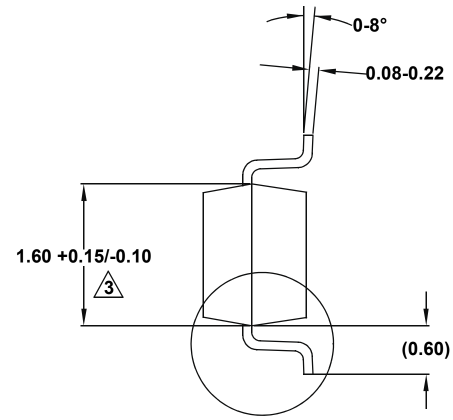
Package Outline Drawing

P6.064

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 4, 2/10

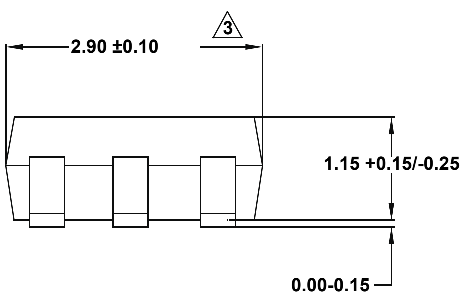


TOP VIEW

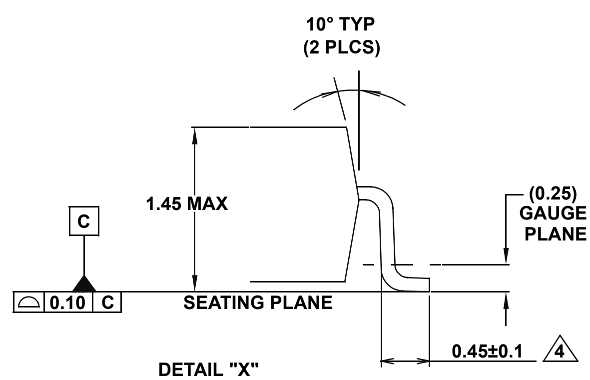


SEE DETAIL X

END VIEW



SIDE VIEW



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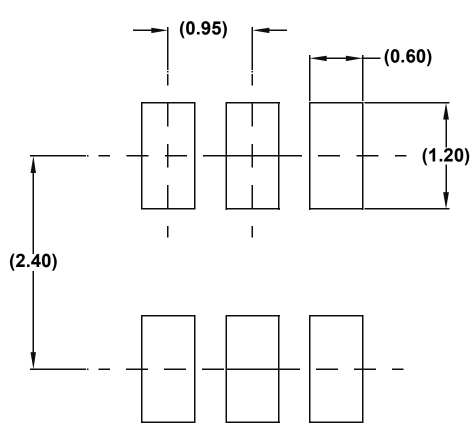

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. Package conforms to JEDEC MO-178AB.