# ISL28288, ISL28488

Dual and Quad Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Op Amp

FN6339
Rev 4.00
July 26, 2011

The ISL28288 and ISL28488 are dual and quad channel micropower operational amplifiers optimized for single supply operation over the 2.4V to 5.5V range. They can be operated from one lithium cell or two Ni-Cd batteries. For equivalent performance in a single channel op amp, reference EL8188.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages 10% above the positive supply rail and to 100mV below the negative supply. The output operation is rail-to-rail.

The ISL28288 and ISL28488 draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications. The ISL28288 (10 Ld MSOP only) contains a power-down enable pin that reduces the power supply current to typically less than 4µA in the disabled state.

## Related Literature

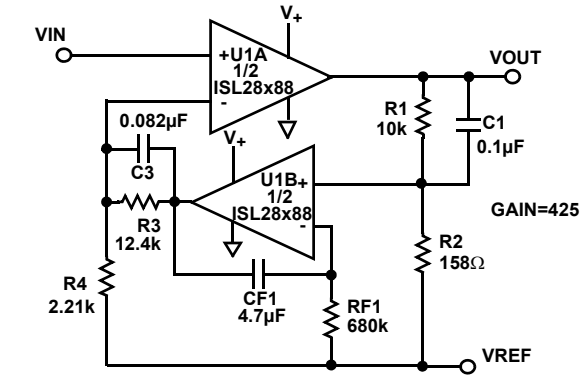
AN1344: ISL2828xEVAL1Z Evaluation Board User's Guide

## Features

- Low power 60µA typical supply current per amplifier
- 1.5mV max offset voltage
- 30pA max input bias current
- 250kHz typical gain-bandwidth product
- 105dB typical PSRR
- 100dB typical CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above $V_+$ and below $V_-$ (ground sensing)
- Rail-to-rail input and output (RRIO)
- Enable Pin - ISL28288 10 Ld MSOP package option only
- Pb-free (RoHS compliant)

## Applications

- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

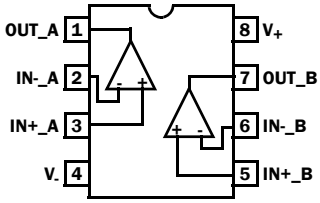



BANDPASS AMPLIFIER (0.05Hz TO 159Hz)

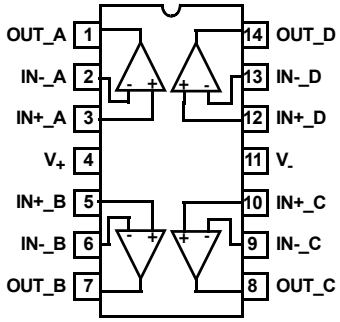
FIGURE 1. TYPICAL APPLICATION CIRCUIT

# Pin Configurations

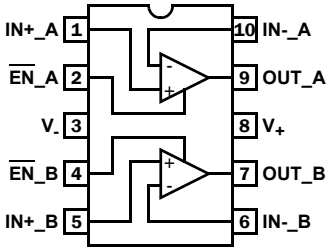
ISL28288
(8 LD SOIC)
TOP VIEW



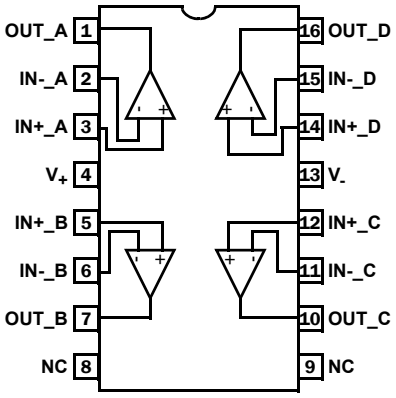

ISL28488
(14 LD TSSOP)
TOP VIEW




ISL28288
(10 LD MSOP)
TOP VIEW




ISL28488
(16 LD QSOP)
TOP VIEW




# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|
| ISL28288FUZ | 8288Z | 10 Ld MSOP | M10.118A |
| ISL28288FBZ | 28288 FBZ | 8 Ld SOIC | M8.15E |
| ISL28488FAZ (Note 4) | 28488 FAZ | 16 Ld QSOP | MDP0040 |
| ISL28488FVZ | 28488 FVZ | 14 Ld TSSOP | M14.173 |
| ISL28288EVAL1Z | Evaluation Board - 10 Ld MSOP | | |
| ISL28488EVAL1Z | Evaluation Board - 16 Ld QSOP | | |

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28288, ISL28488. For more information on MSL please see techbrief TB363
4. Not Recommended for New Designs.

## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage ..... 5.75V
Differential Input Current ..... 5mA
Differential Input Voltage ..... 0.5V
Input Voltage ..... $V_-$ - 0.5V to $V_+$ + 0.5V
ESD Tolerance
Human Body Model ..... 3kV
Machine Model ..... 300V
Charged Device Model ..... 1200V

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 8 Ld SOIC Package (Note5) | 125 | N/A |
| 10 Ld MSOP Package (Notes 5, 6) | 160 | 60 |
| 14 Ld TSSOP Package (Note 5) | 115 | N/A |
| 16 Ld QSOP Package (Note 5) | 100 | N/A |

Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Operating Conditions

Ambient Operating Temperature Range ..... -40°C to +125°C
Maximum Operating Junction Temperature ..... +125°C
Supply Voltage ..... 2.4V (±1.2V) to 5.5V (±2.75V)

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For $\theta_{JC}$, the "case temp" location is taken at the package top center.

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

$V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| **DC SPECIFICATIONS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | -1.5<br>**-2** | ±0.05 | 1.5<br>**2** | mV |
| $\frac{\Delta V_{OS}}{\Delta Time}$ | Long Term Input Offset Voltage Stability | ISL28288 | | 1.2 | | µV/Mo |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Voltage vs Temperature | | | 0.9 | | µV/°C |
| $I_{OS}$ | Input Offset Current | <br>-40°C to +85°C | -30<br>**-80** | ±5 | 30<br>**80** | pA |
| $I_B$ | Input Bias Current | <br>-40°C to +85°C | -30<br>**-80** | ±10 | 30<br>**80** | pA |
| CMIR | Common-Mode Voltage Range | Guaranteed by CMRR | **0** | | **5** | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 5V | 80<br>**75** | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_+$ = 2.4V to 5.5V | 85<br>**80** | 105 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 0.5V to 4.5V, $R_L$ = 100kΩ | 103<br>**102** | 109 | | dB |
| | | $V_O$ = 0.5V to 4.5V, $R_L$ = 1kΩ | | 95 | | dB |
| $V_{OL}$ | Output Voltage Swing, Low<br>$V_{OUT}$ - $V_-$ | $R_L$ = 100kΩ | | 3 | 6<br>**30** | mV |
| | | $R_L$ = 1kΩ | | 130 | 175<br>**225** | mV |

**Electrical Specifications** $V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage Swing, High<br>$V_+ - V_{OUT}$ | $R_L$ = 100kΩ | | 4 | 10<br>**30** | mV |
| | | $R_L$ = 1kΩ | | 120 | 200<br>**250** | mV |
| $I_{S,ON}$ | Quiescent Supply Current, Enabled | ISL28288 Per channel, all channels enabled. | | 60 | 78<br>**87.5** | µA |
| | | ISL28488 Per channel. | | 60 | 79<br>**87.5** | µA |
| $I_{S,OFF}$ | Quiescent Supply Current, Disabled (ISL28288 MSOP) | All channels disabled. | | 4 | 7<br>**9** | µA |
| $I_O+$ | Short Circuit Sourcing Capability | $R_L$ = 10Ω | 24<br>**20** | 31 | | mA |
| $I_O-$ | Short Circuit Sinking Capability | $R_L$ = 10Ω | | -26 | -24<br>**-20** | mA |
| $V_{SUPPLY}$ | Supply Operating Range | $V_+$ to $V_-$ | **2.4** | | **5.5** | V |
| $V_{\overline{EN}H}$ | $\overline{EN}$ Pin High Level (ISL28288 10 ld. MSOP) | | **2** | | | V |
| $V_{\overline{EN}L}$ | $\overline{EN}$ Pin Low Level (ISL28288 10 ld. MSOP) | | | | **0.8** | V |
| $I_{\overline{EN}H}$ | $\overline{EN}$ Pin Input High Current (ISL28288 10 ld. MSOP) | $V\overline{EN}$ = $V_+$ | | 0.8 | 1<br>**1.5** | µA |
| $I_{\overline{EN}L}$ | $\overline{EN}$ Pin Input Low Current (ISL28288 10 ld. MSOP) | $V\overline{EN}$ = $V_-$ | | 0 | **+0.1** | µA |
| **AC SPECIFICATIONS** | | | | | | |
| GBW | Gain Bandwidth Product | $A_V$ = 100, $R_F$ = 100kΩ, $R_G$ = 1kΩ, $R_L$ = 10kΩ to $V_{CM}$ | | 250 | | kHz |
| $e_n$ | Input Noise Voltage Peak-to-Peak | f = 0.1Hz to 10Hz | | 3 | | $µV_{P-P}$ |
| | Input Noise Voltage Density | $f_O$ = 1kHz | | 48 | | nV/√Hz |
| $i_n$ | Input Noise Current Density | $f_O$ = 1kHz | | 9 | | fA/√Hz |
| CMRR @ 60Hz | Input Common Mode Rejection Ratio | $V_{CM}$ = $1V_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | -70 | | dB |
| PSRR+ @ 120Hz | Power Supply Rejection Ratio ($V_+$) | $V_+$, $V_-$ = ±1.2V and ±2.5V, $V_{SOURCE}$ = $1V_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | -80 | | dB |
| PSRR- @ 120Hz | Power Supply Rejection Ratio ($V_-$) | $V_+$, $V_-$ = ±1.2V and ±2.5V $V_{SOURCE}$ = $1V_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | -60 | | dB |
| **TRANSIENT RESPONSE** | | | | | | |
| SR | Slew Rate | | | ±0.15 | | V/µs |
| $t_{\overline{EN}}$ | Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% Vout (ISL28288 10 ld. MSOP) | $V\overline{EN}$ = 5V to 0V, $A_V$ = -1, $R_G$ = $R_F$ = $R_L$ = 1k to $V_{CM}$ | | 2 | | µs |
| | Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% Vout (ISL28288 10 ld. MSOP) | $V\overline{EN}$ = 0V to 5V, $A_V$ = -1, $R_G$ = $R_F$ = $R_L$ = 1k to $V_{CM}$ | | 0.1 | | µs |

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

## Typical Performance Curves $v_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open

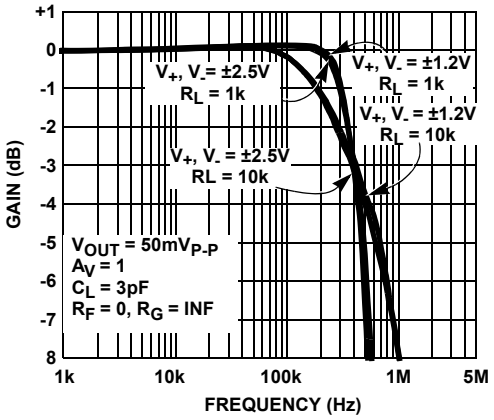



FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

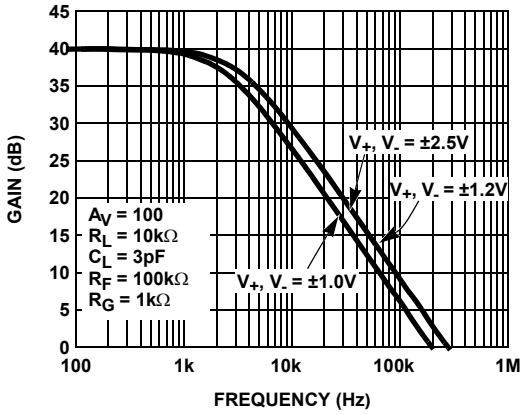



FIGURE 3. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

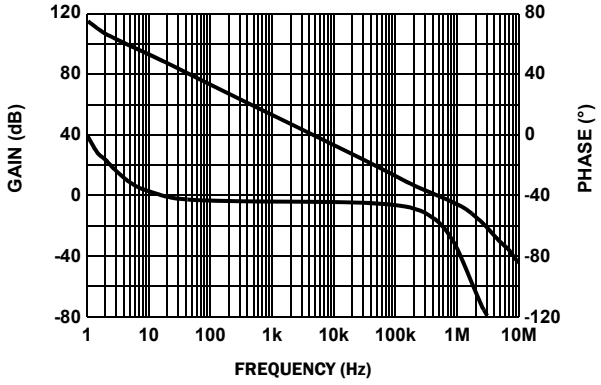



FIGURE 4. $A_{VOL}$ vs FREQUENCY @ 100kΩ LOAD

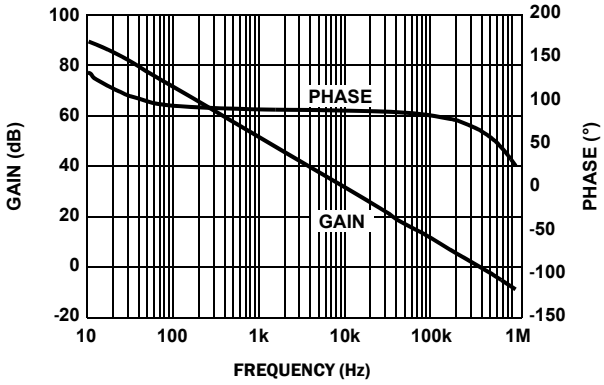



FIGURE 5. $A_{VOL}$ vs FREQUENCY @ 1kΩ LOAD

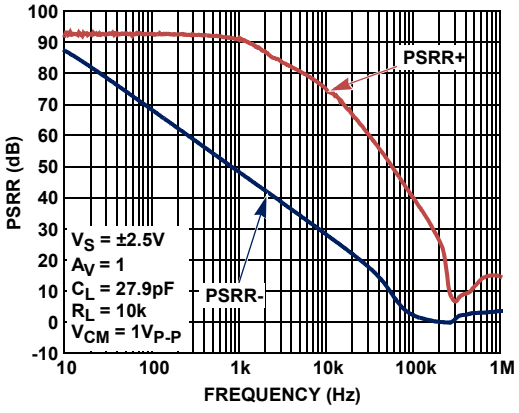



FIGURE 6. PSRR vs FREQUENCY

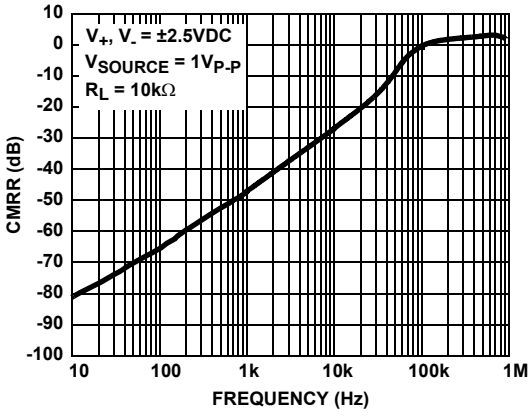



FIGURE 7. CMRR vs FREQUENCY

## Typical Performance Curves $v_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$ **(Continued)**

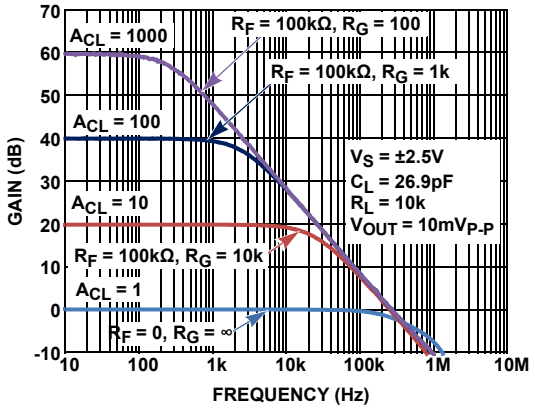



FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

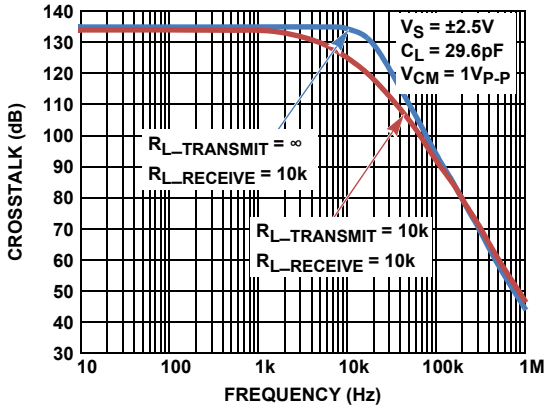



FIGURE 9. CROSSTALK vs FREQUENCY

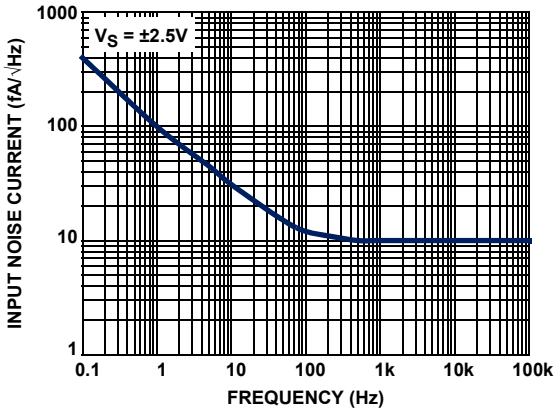



FIGURE 10. CURRENT NOISE vs FREQUENCY

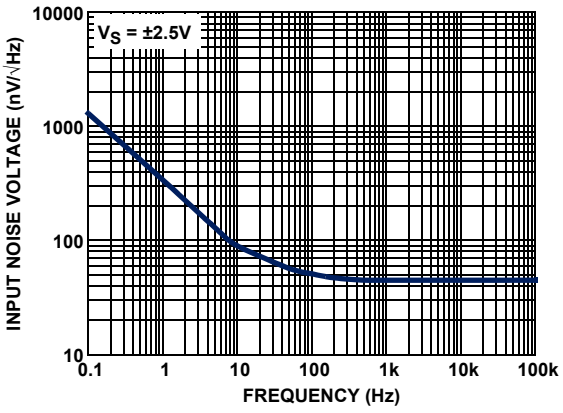



FIGURE 11. VOLTAGE NOISE vs FREQUENCY

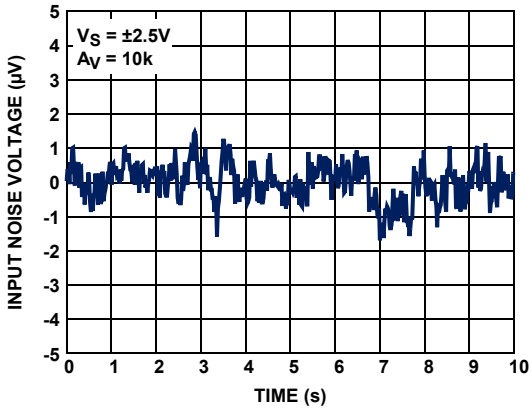



FIGURE 12. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

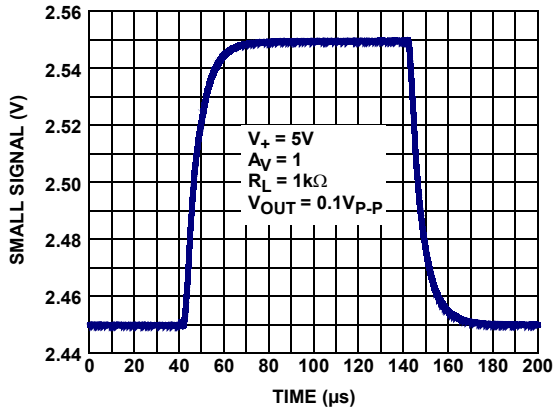



FIGURE 13. SMALL SIGNAL TRANSIENT RESPONSE

## Typical Performance Curves $v_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open **(Continued)**

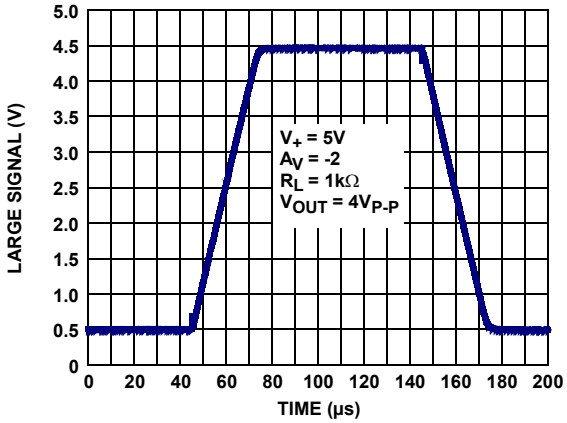



FIGURE 14. LARGE SIGNAL TRANSIENT RESPONSE

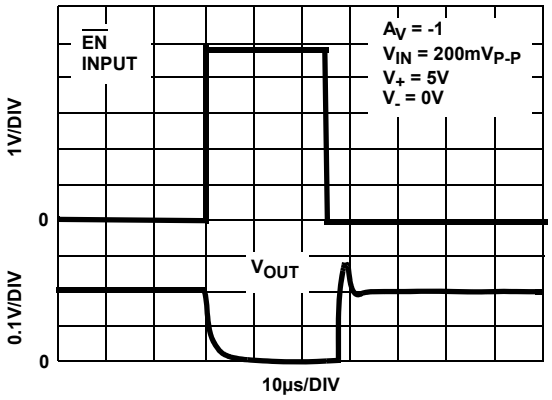



FIGURE 15. ENABLE TO OUTPUT DELAY TIME

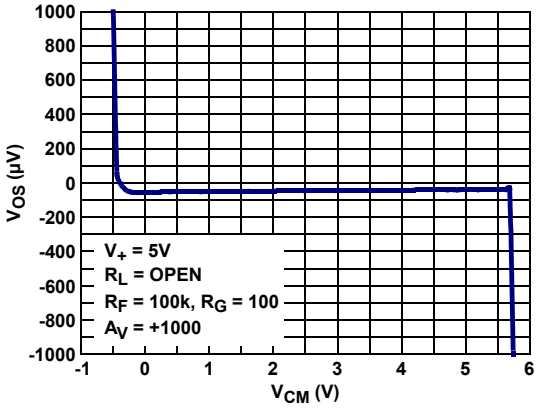



FIGURE 16. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

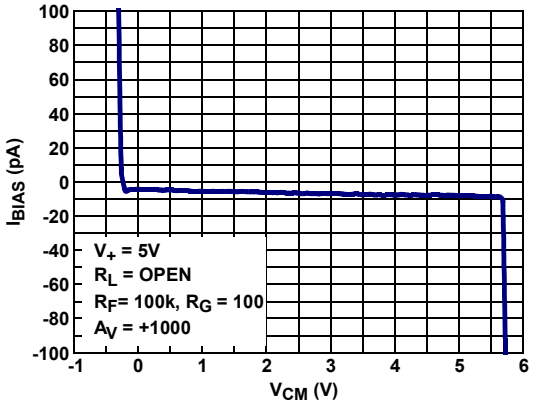



FIGURE 17. INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

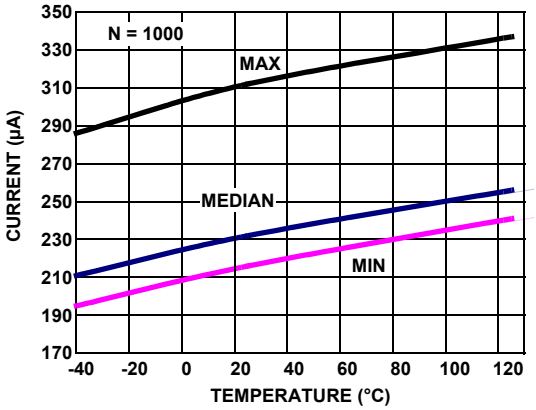



FIGURE 18. ISL28488 SUPPLY CURRENT FOR ALL CHANNELS vs TEMPERATURE $V_+$, $V_-$ = ±2.5V ENABLED, $R_L$ = INF

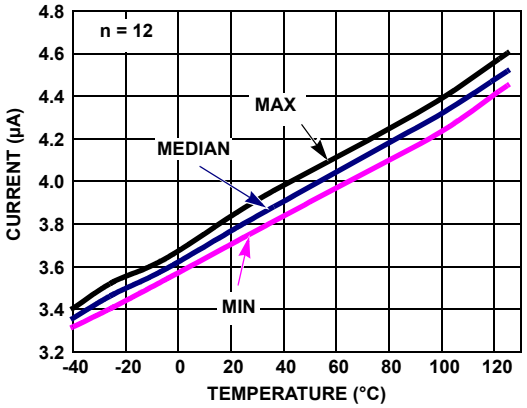



FIGURE 19. ISL28288 SUPPLY CURRENT vs TEMPERATURE $V_+$, $V_-$ = ±2.5V DISABLED, $R_L$ = INF

## Typical Performance Curves $v_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open **(Continued)**

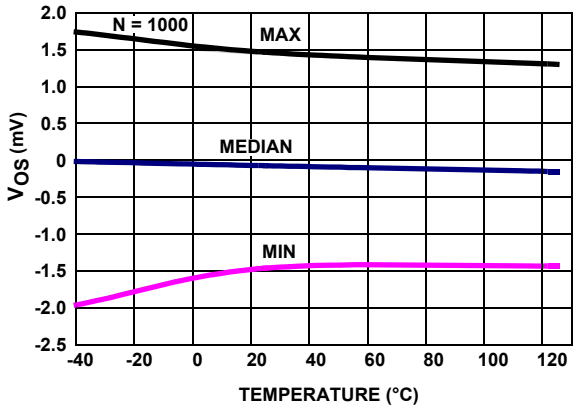



FIGURE 20. $V_{OS}$ vs TEMPERATURE, $V_{IN}$ = 0V, $V_+$, $V_-$ = ±2.5V

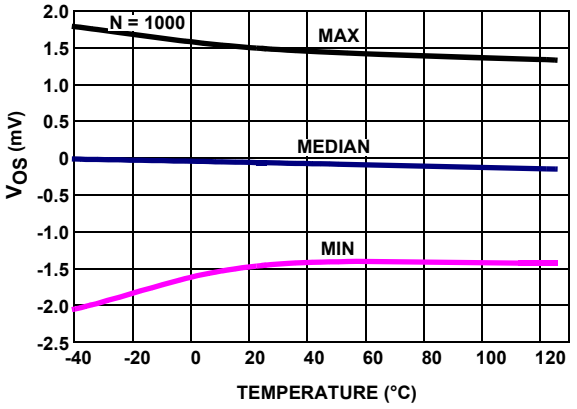



FIGURE 21. $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±1.2V

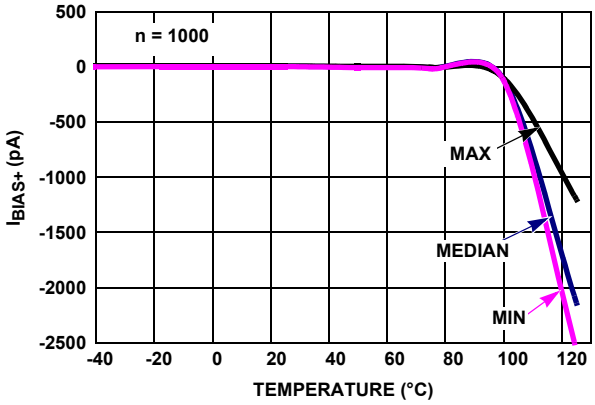



FIGURE 22. $I_{BIAS+}$ vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

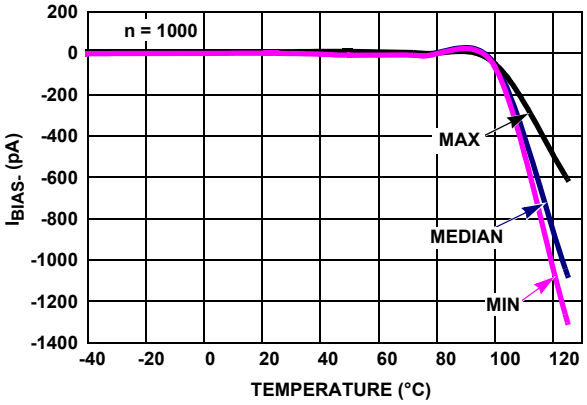



FIGURE 23. $I_{BIAS-}$ vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

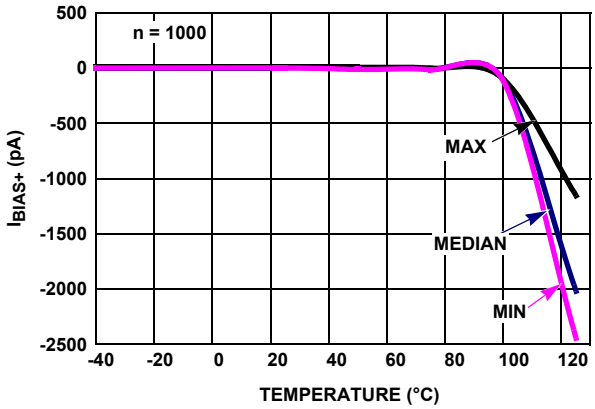



FIGURE 24. $I_{BIAS+}$ vs TEMPERATURE $V_+$, $V_-$ = ±1.2V

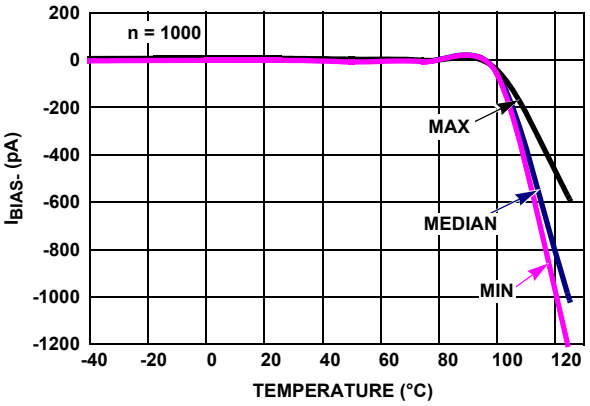



FIGURE 25. $I_{BIAS-}$ vs TEMPERATURE $V_+$, $V_-$ = ±-1.2V

## Typical Performance Curves $V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open **(Continued)**

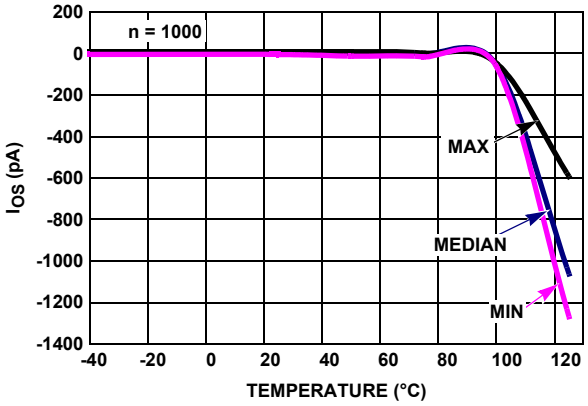



FIGURE 26. $I_{OS}$ vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

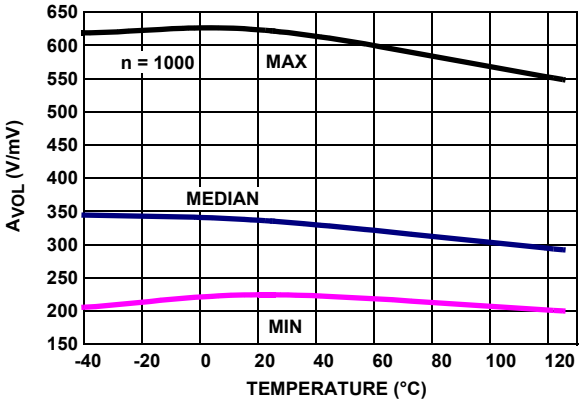



FIGURE 27. $A_{VOL}$ vs TEMPERATURE $V_+$, $V_-$ = ±2.5V, $R_L$ = 100k

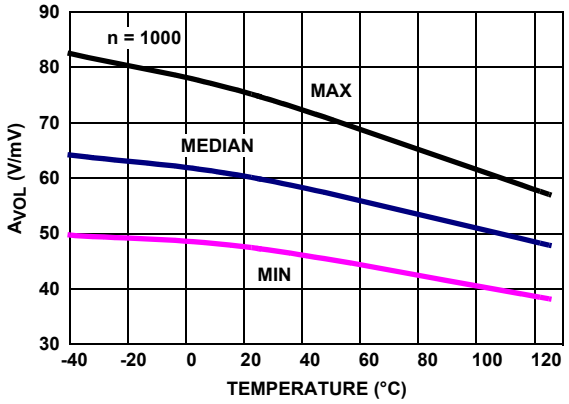



FIGURE 28. $A_{VOL}$ vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, $R_L$ = 1k

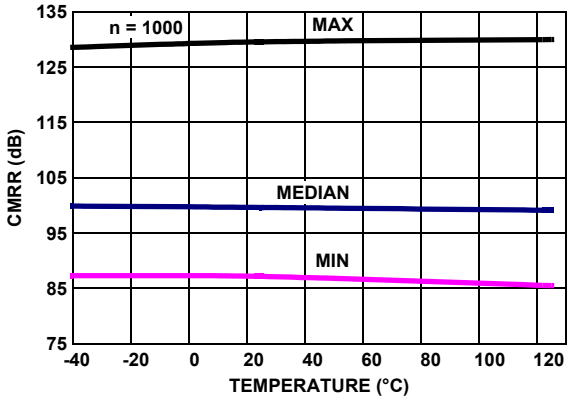



FIGURE 29. CMRR vs TEMPERATURE $V_{CM}$ = +2.5V TO -2.5V, $V_+$, $V_-$ = ±2.5V

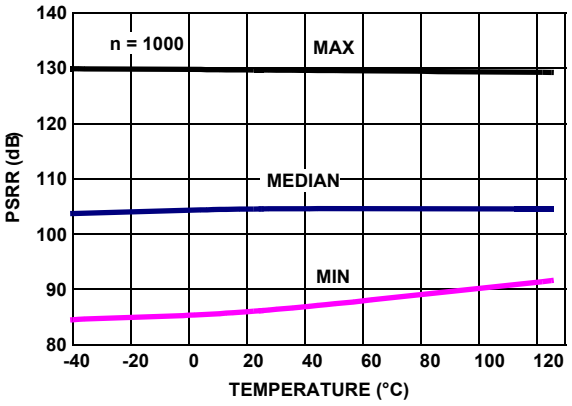



FIGURE 30. PSRR vs TEMPERATURE, $V_+$, $V_-$ = ±1.2V TO ±2.75V

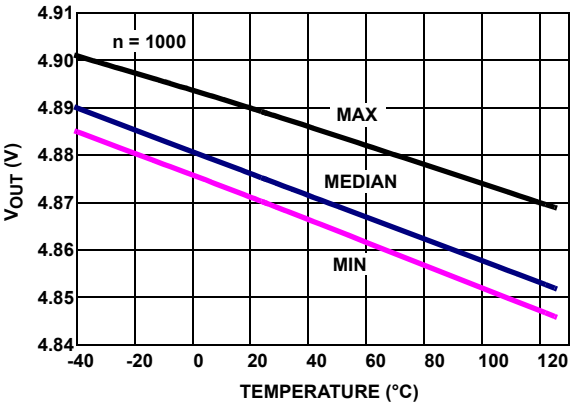



FIGURE 31. $V_{OUT}$ HIGH vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, $R_L$ = 1k

## Typical Performance Curves $v_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open **(Continued)**

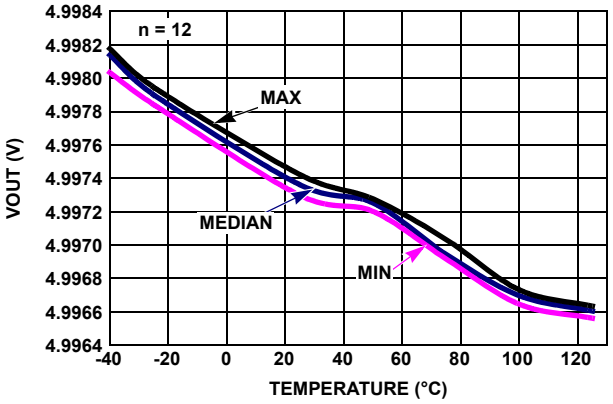



FIGURE 32. $V_{OUT}$ HIGH vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, $R_L$= 100k

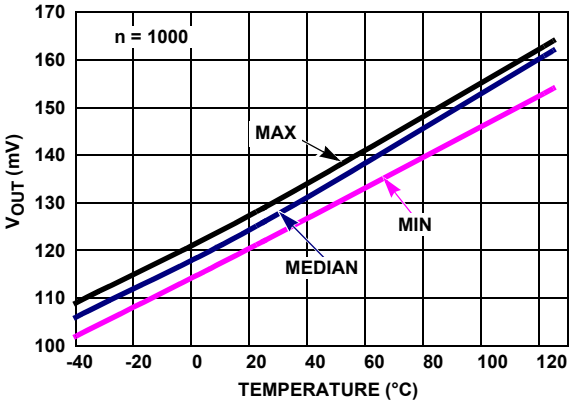



FIGURE 33. $V_{OUT}$ LOW vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, $R_L$= 1k

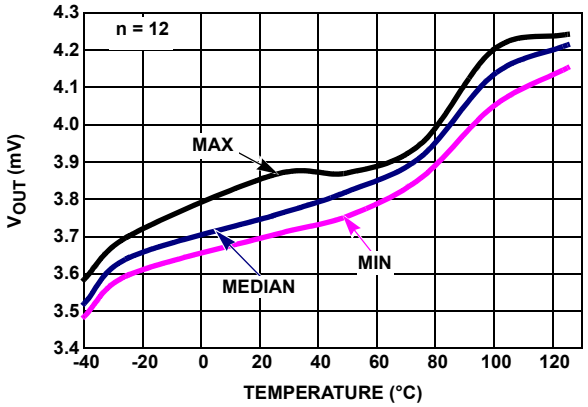



FIGURE 34. $V_{OUT}$ LOW vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, $R_L$= 100k

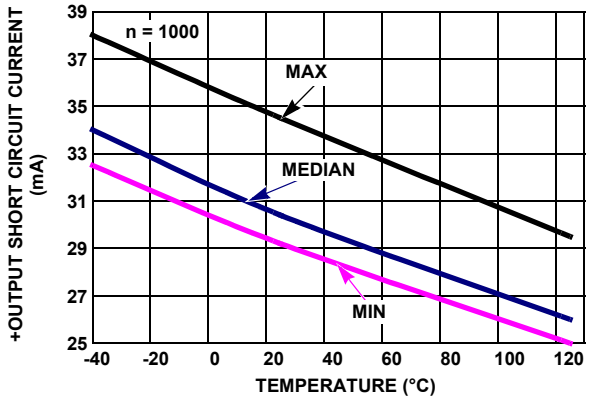



FIGURE 35. +OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE $V_{IN}$ = +2.5V, $R_L$ = 10, $V_+$, $V_-$ = ±2.5V

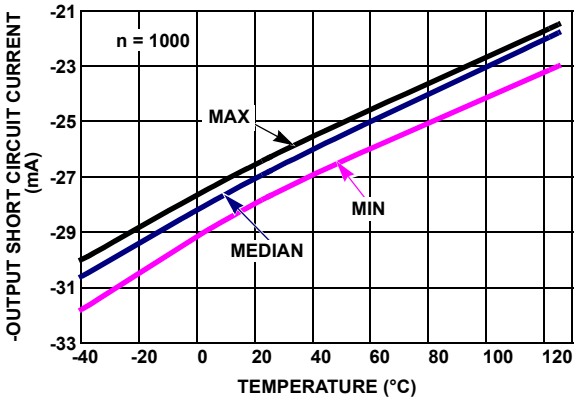
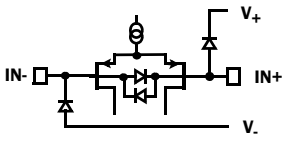


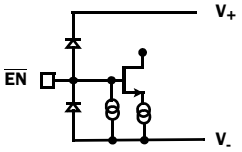

FIGURE 36. -OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE $V_{IN}$ = -2.5V, $R_L$ = 10, $V_+$, $V_-$ = ±2.5V

# Pin Descriptions

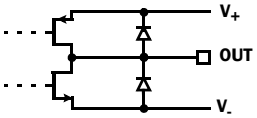
| ISL28288 (8 LD SOIC) | ISL28288 (10 LD MSOP) | ISL28488 (14 LD TSSOP) | ISL28488 (16 LD QSOP) | PIN NAME | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|---|---|---|
| 3 | 1 | 3 | 3 | IN+_A | Circuit 1 | Amplifier A non-inverting input |
| - | 2 | - | - | $\overline{EN}$_A | Circuit 2 | Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state. |
| 4 | 3 | 11 | 13 | V- | Circuit 4 | Negative power supply |
| - | 4 | - | - | $\overline{EN}$_B | Circuit 2 | Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state. |
| 5 | 5 | 5 | 5 | IN+_B | Circuit 1 | Amplifier B non-inverting input |
| 6 | 6 | 6 | 6 | IN-_B | Circuit 1 | Amplifier B inverting input |
| 7 | 7 | 7 | 7 | OUT_B | Circuit 3 | Amplifier B output |
| 8 | 8 | 4 | 4 | V+ | Circuit 4 | Positive power supply |
| 1 | 9 | 1 | 1 | OUT_A | Circuit 3 | Amplifier A output |
| 2 | 10 | 2 | 2 | IN-_A | Circuit 1 | Amplifier A inverting input |
| - | - | 8 | 10 | OUT_C | Circuit 3 | Amplifier C output |
| - | - | 9 | 11 | IN-_C | Circuit 1 | Amplifier C inverting input |
| - | - | 10 | 12 | IN+_C | Circuit 1 | Amplifier C non-inverting input |
| - | - | 12 | 14 | IN+_D | Circuit 1 | Amplifier D non-inverting input |
| - | - | 13 | 15 | IN-_D | Circuit 1 | Amplifier D inverting input |
| - | - | 14 | 16 | OUT_D | Circuit 3 | Amplifier D output |
| - | - | - | 8, 9 | NC | - | No internal connection |



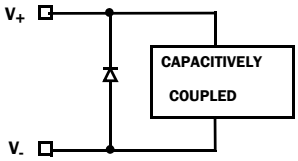

CIRCUIT 1




CIRCUIT 2




CIRCUIT 3




CIRCUIT 4

# Applications Information

## Introduction

The ISL28288 and ISL28488 are dual and quad CMOS rail-to-rail input, output (RRIO) micropower operational amplifiers. These devices are designed to operate from a single supply (2.4V to 5.5V) or dual supplies (±1.2V to ±2.75V) while drawing only 60µA of supply current per amplifier. This combination of low power and precision performance makes these devices suitable for solar and battery power applications.

## Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

These amplifiers achieve rail-to-rail input operation without sacrificing important precision specifications and degrading distortion performance. The devices’ input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current vs the common-mode voltage range gives us an undistorted behavior from typically 100mV below the negative rail and 10% higher than the $V_+$ rail (0.5V higher than $V_+$ when $V_+$ equals 5.5V).

## Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. There is an additional pair of back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to

exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA (as shown in Figure 37).

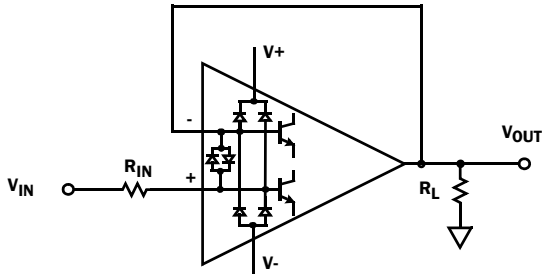



FIGURE 37. INPUT ESD DIODE CURRENT LIMITING - UNITY GAIN

## Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. With a 100kΩ load they will swing to within 4mV of the positive supply rail and within 3mV of the negative supply rail.

## Enable/Disable Feature

The ISL28288 (only MSOP package option), offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 4µA. By disabling the part, multiple ISL28288 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

## Using Only One Channel

If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 38).

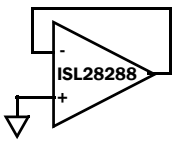



FIGURE 38. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

## Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

## Current Limiting

The ISL28288 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

## Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)
- $PD_{MAX}$ for each amplifier is calculated in Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- $T_{MAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier
- $V_S$ = Supply voltage (Magnitude of $V_+$ and $V_-$)
- $I_{MAX}$ = Maximum supply current of 1 amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application
- $R_L$ = Load resistance

## Application Circuits

### THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28x88 (see Figure 39) is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The amplifier's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the amplifier to run from a single 5V supply.

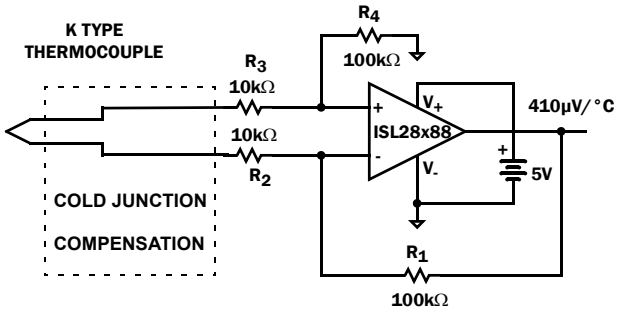



FIGURE 39. THERMOCOUPLE AMPLIFIER

## ECG AMPLIFIER

ECG amplifiers must extract millivolt low frequency AC signals from the skin of the patient while rejecting AC common mode interference and static DC potentials created at the electrode-to-skin interface. In Figure 40, the ISL28288 (U1) forms one of the multiple high gain AC band-pass amplifiers using active feedback. Amplifier U1B and RC RF1, CF1 form a high gain LP filtered amplifier with the corner frequency given by Equation 3:

$$f\text{-}HPF_{-3dB} = \frac{1}{2 \times Pi \times RF1 \times CF1} \quad \text{(EQ. 3)}$$

Inserting the low pass amplifier, U1B, in U1A's feedback loop results in an overall high-pass frequency response. Voltage divider pairs R1-R2 and R3-R4 set the overall amplifier pass-band gain. The DC input offset is cancelled by U1B at U1A's inverting input. Resistor divider pair, R3-R4 define the maximum input DC level that is cancelled, and is given by Equation 4:

$$V_{IN}DC = V_+ \times \left(\frac{R_4}{R_3 + R_4}\right) \quad \text{(EQ. 4)}$$

In the passband range, U1B's gain is +1 and the total signal gain is defined by the divider ratios according to Equation 5:

$$V_{OUT}U1\ GAIN = \frac{V_{OUT}}{V_{IN}} = \left(\frac{R_1 + R_2}{R_2}\right) \times \left(\frac{R_3 + R_4}{R_4}\right) \quad \text{(EQ. 5)}$$

At frequencies greater than the LPF corner, the R1-C1 and R3-C3 networks roll off U1A's gain to unity. Setting both R-C time constants to the same value simplifies to Equation 6:

$$f\text{-}LPF_{-3dB} = \frac{1}{2 \times Pi \times R_1 \times C_1} \quad \text{(EQ. 6)}$$

Right leg drive and reference amplifiers U2A and U2B form a DC feedback loop that applies a correction voltage at the Right Leg electrode to cancel out DC and low frequency body interference. The voltage at the $V_{CM}$ sense electrode is maintained at the reference voltage set by RF1-RF2.

With the values shown in Figure 40, the ECG circuit performance parameters are:

1. Supply Voltage Range = +2.4V to +5.5V
2. Total Supply Current Draw @ +5V = 500µA (typ)
3. Common-Mode Reference Voltage ($V_{CM}$) = $V_+/2$
4. Max DC Input Offset Voltage = $V_{CM}$ ±0.18V to ±0.41V
5. Passband Gain = 425V/V
6. Lower -3dB Frequency = 0.05Hz
7. Upper -3dB Frequency = 159Hz

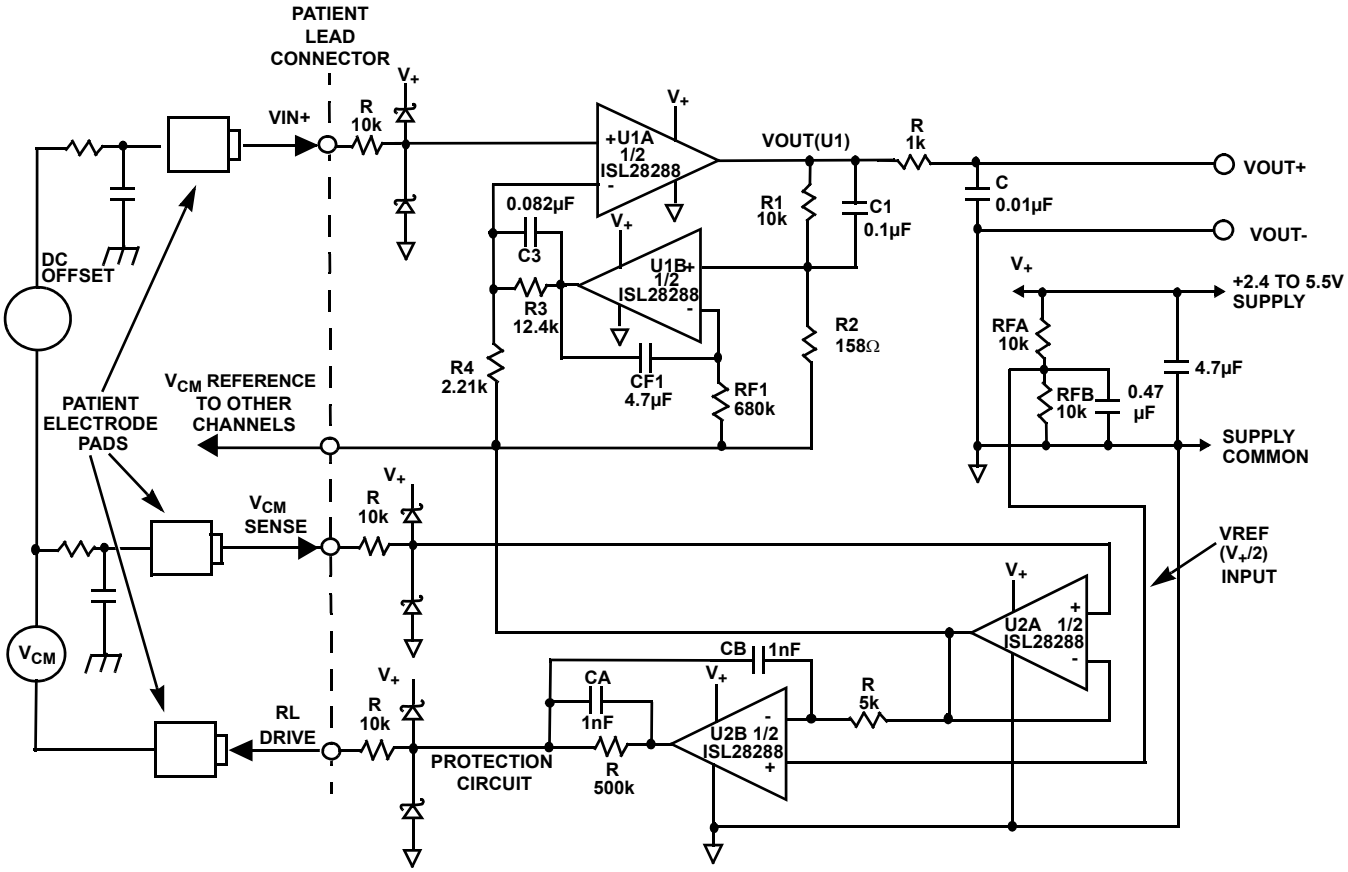



**FIGURE 40. ECG AMPLIFIER**

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| 7/12/11 | FN6339.4 | page 1 Features changed: "Low power 120uA..." to "Low power 60uA..."<br>page 4 Electrical Spec table IS,ON changed conditions and values from:<br>ISL28288, All channels enabled TYP 120, MAX 156, 175<br>ISL28488, All channels enabled TYP 240, MAX 315, 350<br>TO:<br>ISL28288, Per channel, all channels enabled TYP 60, MAX 78, 87.5<br>ISL28488, Per channel TYP 60, MAX 79, 87.5<br>page 4 Electrical Spec table IS,OFF updated description by adding MSOP to ISL28288<br>page 11 First paragraph second sentence of the Applications Information Introduction section changed "...while drawing only 120uA of supply current." To "...while drawing only 60uA of supply current per amplifier." |
| 6/16/11 | | Features on page 1 changed gain bw from 300 to 250kHz<br>Added Related Literature<br>Added Typ App Circuit<br>Updated PKG DWG Number to Ordering Information on page 2 for:<br>ISL28288FBZ from MDP0027 TO M8.15E, matching Intrepid<br>ISL28288FUZ from MDP0043 TO M10.118A<br>Added Note "Not Recommended for New Designs" for ISL28488FAZ (At Prenotification)<br>Removed "Supply Turn On Voltage Slew Rate . . . . . 1V/µs" from Abs Max on page 3<br>Added "Supply Voltage under Operating Conditions. . . . . 2.4V (±1.2V) to 5.5V (±2.75V)"<br>AVol room temp on page 3 min changed from 200V/mV to 103dB; over temp min changed from 190V/mV to 102dB; typ changed from 300V/mV to 109dB. For Rl = 1kohm, changed typ from 60V/mV to 95dB<br>Vout split into 2 parameters; Vol and Voh beginning onpage 3. For Output Voltage Swing, High, removed min specs, changed typs from 4.996V & 4.880V to 4 & 120mV; added max specs<br>Added Tjc Note on page 3<br>Changed GBW typ from 300kHz to 250kHz page 4<br>Removed min/max limits for SR page 4. Changed typ from +/-0.14V/us to +/-0.15V/us<br>Changed Note in Electrical Spec Table page 4 from: Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.<br>To: Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design<br>Revised FIGURE 6. PSRR vs FREQUENCY on page 5<br>Added Figures 8-11 frequency curves beginning on page 6<br>Updated Proper Layout Maximizes Performance sectionpage 12 by removing last part of paragraph and Figure<br>Replaced MDP0027 POD with updated M8.15E to meet new standard<br>Replaced M14.173 POD with updated version - Updated drawing to remove table and added land pattern<br>Replaced MDP0043 POD with M10.118A to meet new standard |
| 5-22-08 | FN6339.3 | Removed "coming soon" in ordering information, updated pb-free lead finish note to latest revision. |
| 3-17-08 | FN6339.2 | 1. Added 8ld. SO, 14 ld TSSOP package, pinout, and pin description.<br>2. Changed Io+, Io- specs<br>3. Updated Abs MAX supply voltage, Theta JAs, added CDM ESD spec<br>4. Changed spec. table noise current TYP from 0.1pA to 9fA<br>5. Updated noise plots (Fig.7, 8, 9)<br>6. Updated transient response plots (Fig 10, 11)<br>7. Added ECG circuit to applications section |
| 6-28-07 | FN6339.1 | Applied all Intersil Standards. Added New Part to datasheet. Changed Caution Statement per Legal's suggested verbiage. Ordering Information updated - added tape and reel note. Added note 1 to spec table for min and max. Updated POD's.<br>6/25/07 Following edits completed: 1) Datasheet description<br>3rd paragraph, last sentence. Changed "less than 10µA max" to "typically 4µA"<br>2) Datasheet description 3rd paragraph, last sentence. Change "the reduces the power" to "that reduces the power". 3) features change "60µA to 120µA typ supply current" remove per amplifier. 4) change to "30pA max". 5) change to 105 typical PSRR. 6) add 100 typical CMRR. 7) Page 2, Iio ± 80pA max limit for hot/cold temp |
| 9-20-06 | FN6339.0 | Initial Release |

# Products

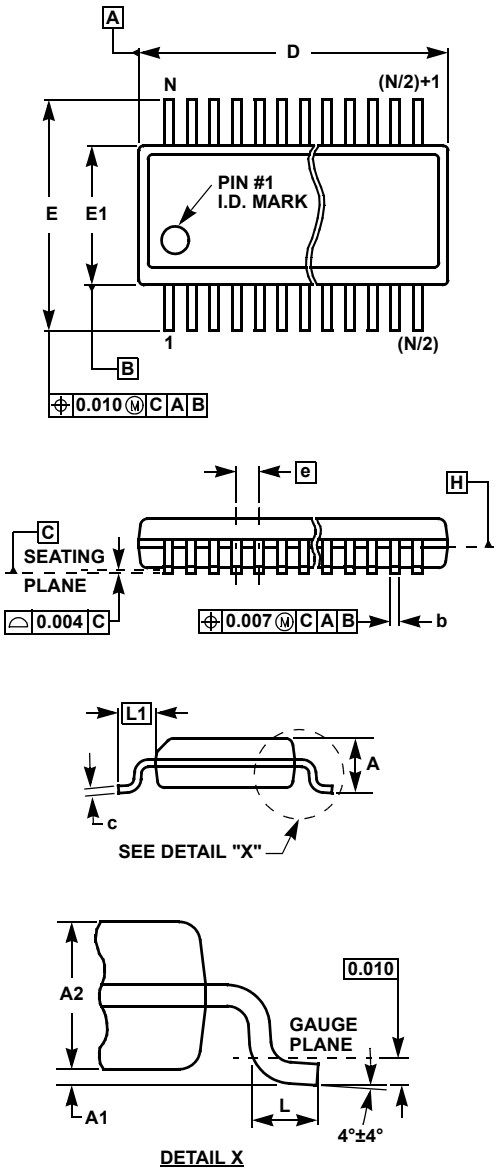
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28288, ISL28488

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

## *Quarter Size Outline Plastic Packages Family (QSOP)*




### MDP0040

**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

| SYMBOL | INCHES | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|
| | QSOP16 | QSOP24 | QSOP28 | | |
| A | 0.068 | 0.068 | 0.068 | Max. | - |
| A1 | 0.006 | 0.006 | 0.006 | ±0.002 | - |
| A2 | 0.056 | 0.056 | 0.056 | ±0.004 | - |
| b | 0.010 | 0.010 | 0.010 | ±0.002 | - |
| c | 0.008 | 0.008 | 0.008 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | ±0.004 | 2, 3 |
| e | 0.025 | 0.025 | 0.025 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | Basic | - |
| N | 16 | 24 | 28 | Reference | - |

Rev. F 2/07

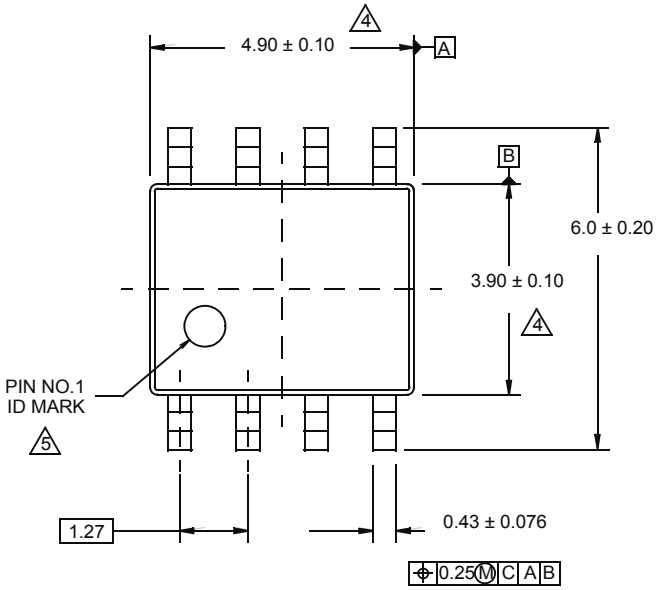
NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

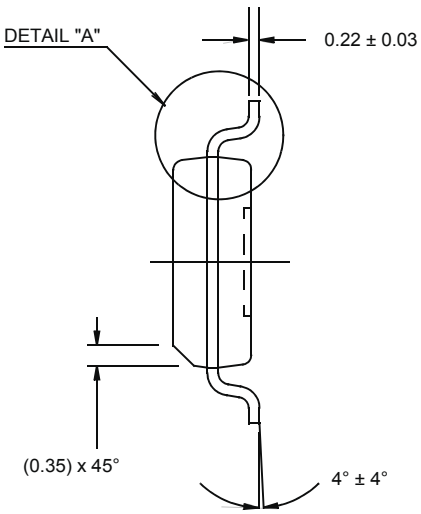
# Package Outline Drawing

## M8.15E

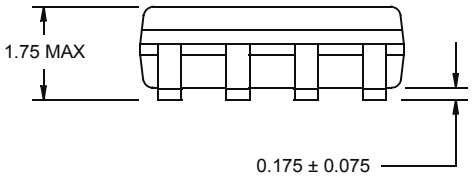
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**
**Rev 0, 08/09**



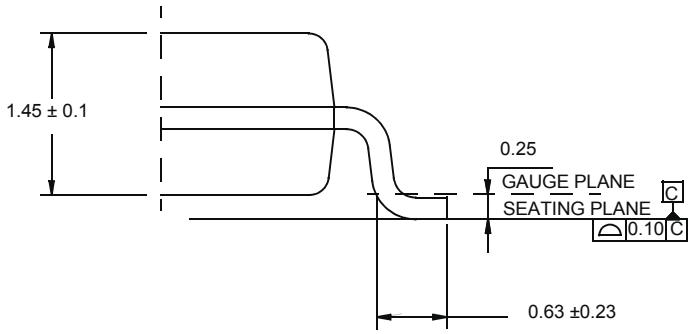

TOP VIEW



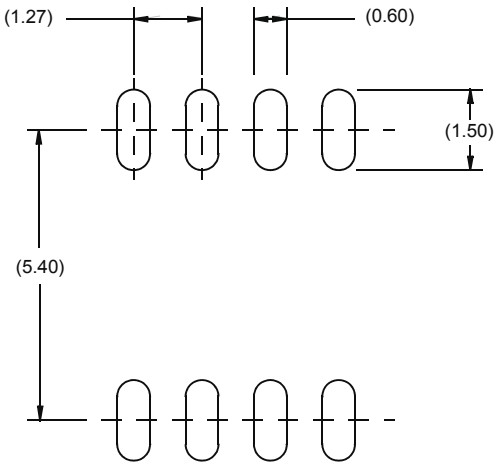

SIDE VIEW "B"




SIDE VIEW "A"




DETAIL "A"




TYPICAL RECOMMENDED LAND PATTERN

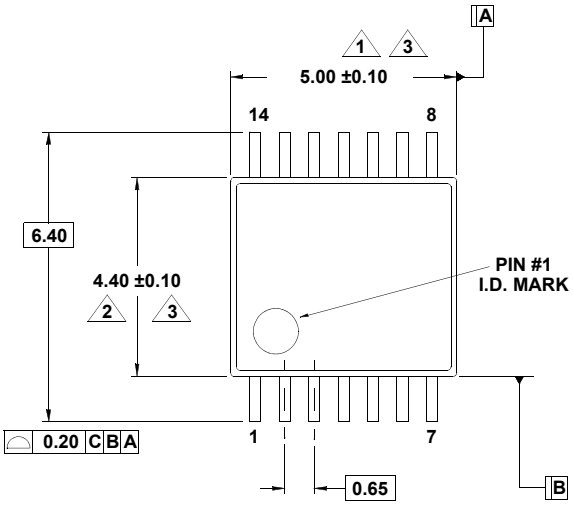
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

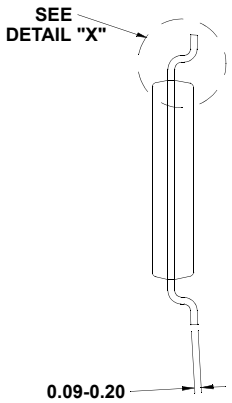
# Package Outline Drawing

## M14.173

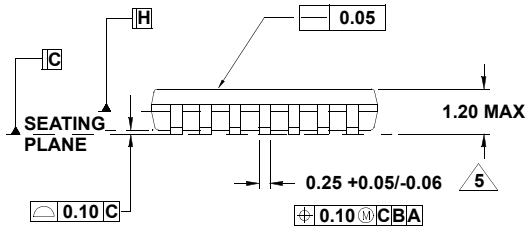
**14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**
**Rev 3, 10/09**



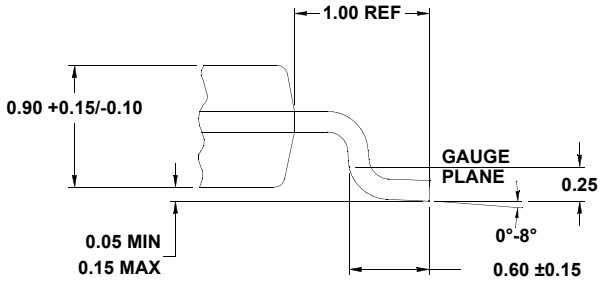

TOP VIEW



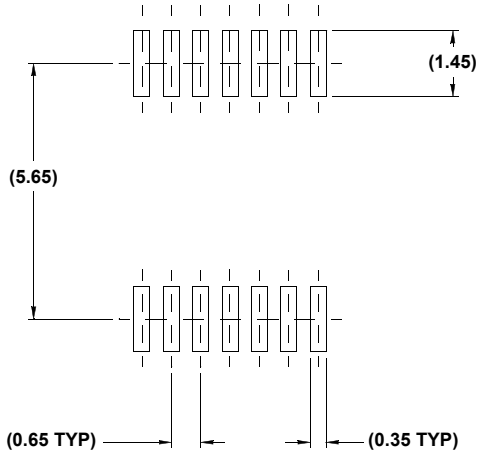

END VIEW




SIDE VIEW




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

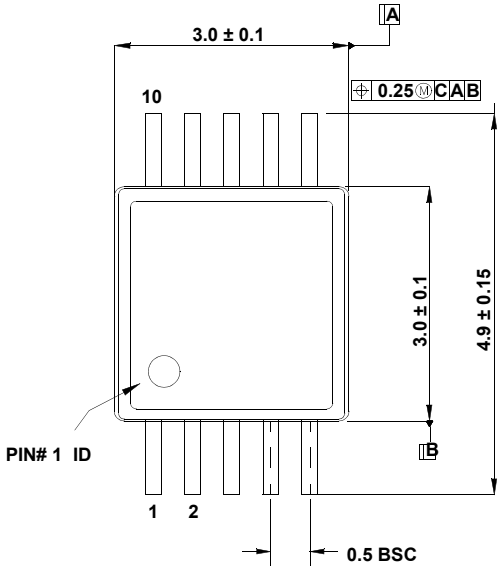
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

# Package Outline Drawing

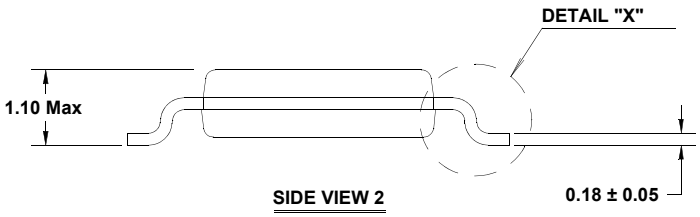
## M10.118A (JEDEC MO-187-BA)

**10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)**

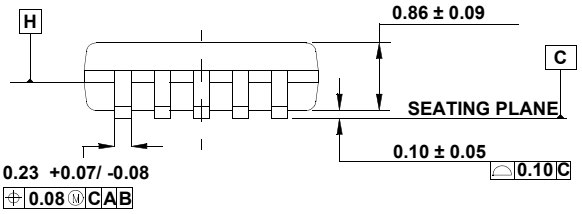
**Rev 0, 9/09**



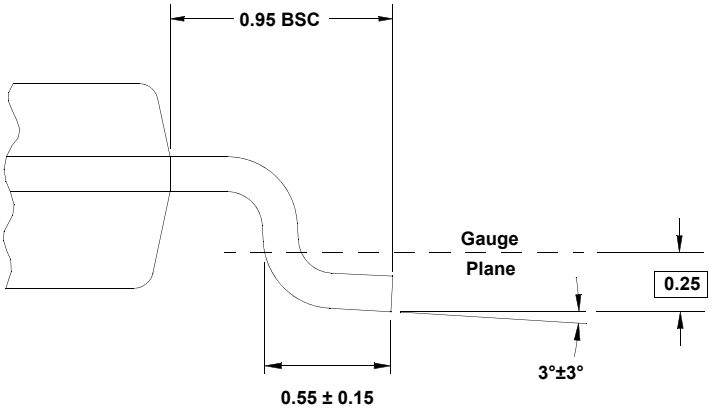

TOP VIEW



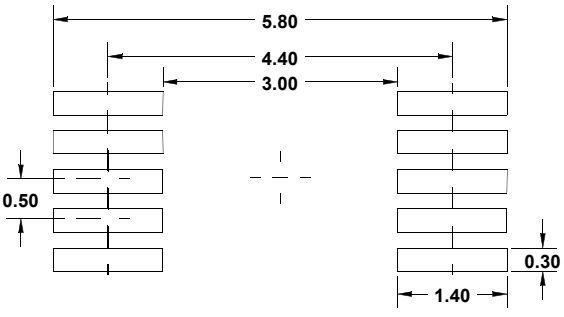

SIDE VIEW 2




SIDE VIEW 1




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

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