ISL32704E

Ultra-Low EMI, Smallest Package Isolated RS-485 Transceiver

FN8860
Rev.4.00
Feb 12, 2018

The ISL32704E is a galvanically isolated, differential bus transceiver designed for bidirectional data transmission and meeting the RS-485 and RS-422 standards for balanced communication. Each of the bus terminals, A and B, is protected against ±15kV ESD strikes without latch-up.

The device uses Giant Magnetoresistance (GMR) as isolation technology. A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The part is available in a 16 Ld QSOP package offering unprecedented miniaturization, and in a 16 Ld wide-body SOIC package providing true 8 millimeter creepage distance.

The ISL32704E delivers a minimum differential output voltage of 1.5V into a 54Ω differential load for excellent data integrity over long cable lengths.

The device is compatible with 3V and 5V input supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

Related Literature

For a full list of related documents, visit our website

- ISL32704E product page

Features

- 4Mbps data rate
- 2.5kV$_{RMS}$ isolation per UL 1577
- 600V$_{RMS}$ working voltage per VDE 0884
- 3V to 5V power supplies
- Single unit load receiver input
- Driver drives up to 150 unit loads
- 50kV/µs (typical), 30kV/µs (minimum) common-mode transient immunity
- 44000 years barrier life
- 15kV ESD bus-pin protection
- Thermal shutdown protection
- -40°C to +85°C temperature range
- Meets or exceeds ANSI RS-485
- 16 Ld QSOP and 0.3" true 8mm 16 Ld SOIC packages
- UL 1577 recognized
- VDE V0884-10 certified

Applications

- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators (i.e., RS-232 to RS-485)

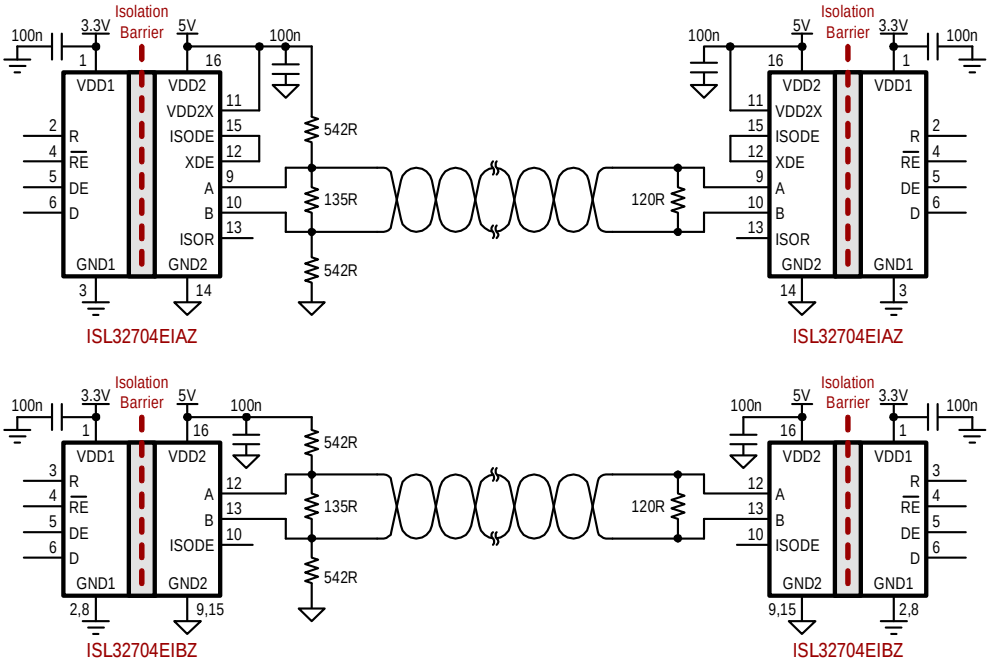


FIGURE 1. TYPICAL ISOLATED HIGH-SPEED RS-485 APPLICATIONS

Ordering Information

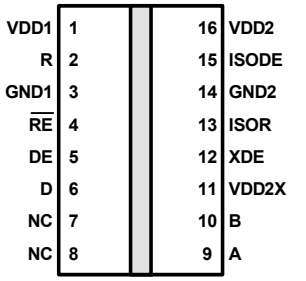
PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL32704EIAZ (Note 1)	32704EIAZ	-40 to +85	16 Ld QSOP	M16.15B
ISL32704EIBZ (Note 2)	32704EIBZ	-40 to +85	16 Ld SOIC	M16.3A
ISL32704EVAL1Z	Evaluation board for ISL32704EIAZ			
ISL32704EVAL2Z	Evaluation board for ISL32704EIBZ			

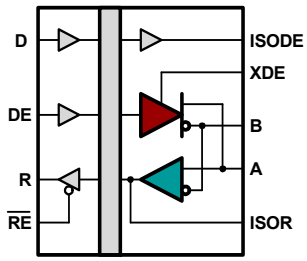
NOTES:

1. Add “-T7A” suffix for 250 unit or “-T” suffix for 2500 unit tape and reel options. Refer to TB347 for details about reel specifications.
2. Add “-T7A” suffix for 250 unit or “-T” suffix for 1000 unit tape and reel options. Refer to TB347 for details about reel specifications.
3. These Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL32704E product information page. For more information about MSL, see TB363.

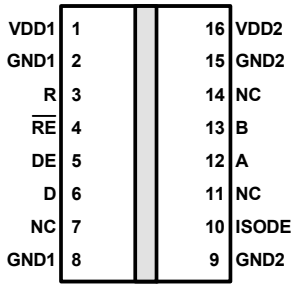
Pin Configurations

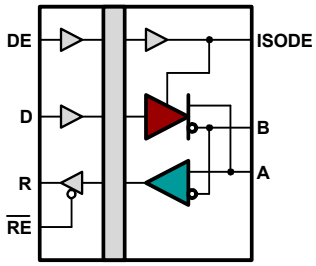
ISL32704E
(16 LD QSOP)
TOP VIEW





ISL32704E
(16 LD WB-SOIC)
TOP VIEW





Truth Table

TRANSMITTING					
INPUTS			OUTPUTS		
RE	DE	D	ISODE	B	A
X	1	1	1	0	1
X	1	0	1	1	0
0	0	X	0	High-Z	High-Z
1	0	X	0	High-Z	High-Z

Truth Table

RECEIVING			
INPUTS			OUTPUT
RE	DE	A-B	R
0	0	≥0.2V	1
0	0	≤-0.2V	0
0	0	Inputs Open/Shorted	1
1	1	X	High-Z
1	0	X	High-Z

Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
16 Ld SOIC	16 Ld QSOP		
1	1	VDD1	Input power supply.
3	2	R	Receiver output. R is high when A-B ≥ 200mV, and when A and B are floating. R is low when A-B ≤ -200mV.
2, 8	3	GND1	Input power supply ground return. Dual ground pins are connected internally.
4	4	$\overline{RE}$	Receiver output enable. R is enabled when $\overline{RE}$ is low. R is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND1.
5	5	DE	Driver output enable. The driver outputs, A and B, are enabled when DE is high. They are high impedance when DE is low. If the Tx enable function is not required, connect DE to VDD1 (Pin 1) through a 1kΩ or greater resistor.
6	6	D	Driver input. A low on D forces output A low and output B high. A high on D forces output A high and output B low.
7, 11, 14	7, 8	NC	No internal connection.
12	9	A	±15kV ESD protected, noninverting bus terminal. This pin is the noninverting receiver input when DE = 0 and the noninverting driver output when DE = 1.
13	10	B	±15kV ESD protected, inverting bus terminal. This pin is the inverting receiver input when DE = 0 and the inverting driver output when DE = 1.
-	11	VDD2X	Transceiver power supply. Connect to VDD2 (Pin 16).
-	12	XDE	External driver enable. Allows for enabling the driver from the bus side. Connect this pin to ISODE to control the driver from the controller side. This pin must not be left floating.
-	13	ISOR	Isolated receiver output for test purpose only. This pin is used for testing and should be left unconnected.
9, 15	14	GND2	Output power supply ground return. Dual ground pins are connected internally.
10	15	ISODE	Isolated DE output.
16	16	VDD2	Isolator output power supply.

Typical Operating Circuits

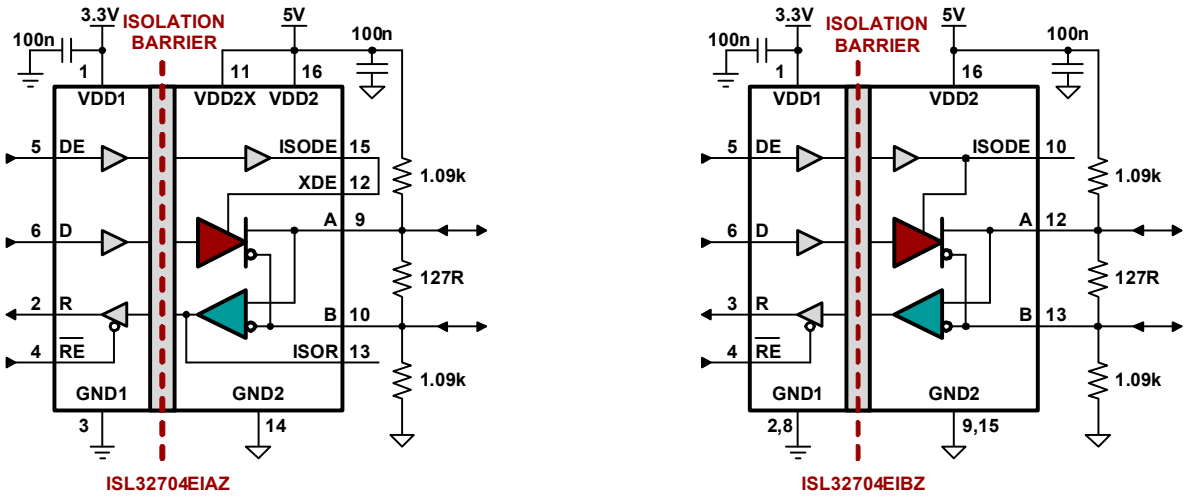


FIGURE 2. TYPICAL OPERATING CIRCUITS

Absolute Maximum Ratings (Note 17)

Supply Voltages (Note 7)
- VDD1 to GND1 ..... -0.5V to +7V
- VDD2 to GND2 ..... 7V

Input Voltages, D, DE, $\overline{RE}$ ..... -0.5V to (V_{DD1} +0.5V)

Input/Output Voltages
- A, B ..... -8V to +12.5V
- R ..... -0.5V to (V_{DD1} +1V)

Short-Circuit Duration, A, B ..... Continuous

ESD Rating ..... See "ESD PERFORMANCE" on page 5

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld WB-SOIC Package (Notes 5, 6)	34	17
16 Ld QSOP Package (Notes 5, 6)	63	35

Maximum Junction Temperature (Plastic Package) ....-55°C to +150°C

Maximum Storage Temperature Range .....-55°C to +150°C

Maximum Power Dissipation (WB-SOIC) 800mW

Maximum Power Dissipation (QSOP) 675mW

Solder Profile ..... Per JEDEC J-STD-020C, MSL1

Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

Supply Voltages
- V_{DD1} ..... 3.0V to 5.5V
- V_{DD2}, V_{DD2X} ..... 4.5V to 5.5V

High-Level Digital Input Voltage, V_{IH}
- V_{DD1} = 3.3V ..... 2.4V to V_{DD1}
- V_{DD1} = 5.0V ..... 3.0V to V_{DD1}

Low-Level Digital Input Voltage, V_{IL} .....0V to 0.8V

Input Voltage at any Bus Terminal (separately or common-mode), V_I, V_{IC} .....-7V to 12V

Differential Input Voltage (Note 8), V_{ID} .....-7V to 12V

High-Level Output Current (Driver), I_{OH} 60mA

High-Level Digital Output Current (Receiver), I_{OH} 8mA

Low-Level Output Current (Driver), I_{OL} .....-60mA

Low-Level Digital Output Current (Receiver), I_{OL} .....-8mA

Junction Temperature, T_J .....-40°C to +100°C

Ambient Operating Temperature, T_A .....-40°C to +85°C

Digital Input Signal Rise and Fall Times, t_{IR}, t_{IF} ..... DC Stable

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component soldered to a double-sided board.
6. For θ_{JC}, the "case temp" location is the center of the package top side.

Electrical Specifications

Test Conditions: T_{MIN} to T_{MAX}, V_{DD1} = V_{DD2} = 4.5V to 5.5V; unless otherwise stated (see (Note 7).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
Driver Line Output Voltage (V_A, V_B) (Note 7)	V_O	No load				V_{DD2}	V
Driver Differential Output Voltage (Note 8)	V_{OD1}	No load				V_{DD2}	V
Driver Differential Output Voltage (Note 8)	V_{OD2}	R_L = 54Ω		1.5	2.3	V_{DD2}	V
Change in Magnitude of Differential Output Voltage (Note 13)	ΔV_{OD}	R_L = 54Ω or 100Ω			0.01	0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω or 100Ω				3	V
Change in Magnitude of Driver Common-Mode Output Voltage (Note 13)	ΔV_{OC}	R_L = 54Ω or 100Ω			0.01	0.20	V
Bus Input Current (A, B) (Notes 10, 14)	I_{IN2}	DE = 0V	V_{IN} = 12V			1	mA
			V_{IN} = -7V	-0.8			mA
High-Level Input Current (D, DE, $\overline{RE}$)	I_{IH}	V_I = 3.5V				10	µA
Low-Level Input Current (D, DE, $\overline{RE}$)	I_{IL}	V_I = 0.4V		-10			µA
Absolute Short-Circuit Output Current	I_{OS}	DE = V_{DD1}, -7V ≤ V_A or V_B ≤ 12V				±250	mA
Supply Current	I_{DD1}	V_{DD1} = 5V			4	6	mA
		V_{DD1} = 3.3V			3	4	mA
Positive-Going Input Threshold Voltage	V_{TH+}	-7V ≤ V_{CM} ≤ 12V				200	mV
Negative-Going Input Threshold Voltage	V_{TH-}	-7V ≤ V_{CM} ≤ 12V		-200			mV

Electrical Specifications

Test Conditions: T_{MIN} to T_{MAX}, V_{DD1} = V_{DD2} = 4.5V to 5.5V; unless otherwise stated (see Note 7). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver Input Hysteresis	V_{HYS}	V_{CM} = 0V		70		mV
Differential Bus Input Capacitance	C_D			9	12	pF
Receiver Output High Voltage	V_{OH}	I_O = -20µA, V_{ID} = -50mV	V_{DD1} - 0.2	V_{DD1}		V
Receiver Output Low Voltage	V_{OL}	I_O = +20µA, V_{ID} = -200mV			0.2	V
High impedance Output Current	I_{OZ}	0.4V ≤ V_O ≤ (V_{DD2} - 0.5)	-1		1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	12			kΩ
Supply Current	I_{DD2}	DE = V_{DD1}, no load		5	16	mA
ESD PERFORMANCE						
RS-485 Bus Pins (A, B)		Human body model discharge to GND2		±15		kV
All Pins (R, $\overline{RE}$, D, DE)		Human body model discharge to GND1		±2		kV
SWITCHING CHARACTERISTICS						
V_{DD1} = 5V, V_{DD2} = 5V						
Data Rate	DR	R_L = 54Ω, C_L = 50pF	4			Mbps
Propagation Delay (Notes 8, 15)	t_{PD}	V_O = -1.5V to 1.5V, C_L = 15pF		48	150	ns
Pulse Skew (Notes 8, 16)	t_{SK} (P)	V_O = -1.5V to 1.5V, C_L = 15pF		6	15	ns
Output Enable Time to High Level	t_{PZH}	C_L = 15pF		33	50	ns
Output Enable Time to Low Level	t_{PZL}	C_L = 15pF		33	50	ns
Output Disable Time from High Level	t_{PHZ}	C_L = 15pF		33	50	ns
Output Disable Time from Low Level	t_{PLZ}	C_L = 15pF		33	50	ns
Common-Mode Transient Immunity	CMTI	V_{CM} = 1500 V_{DC}, $t_{TRANSIENT}$ = 25ns	30	50		kV/µs
V_{DD1} = 3.3V, V_{DD2} = 5V						
Data Rate	DR	R_L = 54Ω, C_L = 50pF	4			Mbps
Propagation Delay (Notes 9, 15)	t_{PD}	V_O = -1.5V to 1.5V, C_L = 15pF		48	150	ns
Pulse Skew (Notes 9, 16)	t_{SK} (P)	V_O = -1.5V to 1.5V, C_L = 15pF		6	20	ns
Output Enable Time to High Level	t_{PZH}	C_L = 15pF		33	50	ns
Output Enable Time to Low Level	t_{PZL}	C_L = 15pF		33	50	ns
Output Disable Time from High Level	t_{PHZ}	C_L = 15pF		33	50	ns
Output Disable Time from Low Level	t_{PLZ}	C_L = 15pF		33	50	ns
Common-Mode Transient Immunity	CMTI	V_{CM} = 1500 V_{DC}, $t_{TRANSIENT}$ = 25ns	30	50		kV/µs

NOTES: (applies to both driver and receiver sections)

7. All voltages on the isolator primary side are with respect to GND1. All line voltages and common-mode voltages on the isolator secondary or bus side are with respect to GND2.
8. Differential I/O voltage is measured at the noninverting bus terminal A with respect to the inverting terminal B.
9. Skew limit is the maximum propagation delay difference between any two devices at +25°C.
10. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
11. All typical values are at V_{DD1}, V_{DD2} = 5V or V_{DD1} = 3.3V and T_A = +25°C.
12. -7V < V_{CM} < 12V; 4.5 < V_{DD} < 5.5V.
13. ΔV_{OD} and ΔV_{OC} are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from one logic state to the other.
14. This applies for both power-on and power-off; refer to ANSI standard RS-485 for exact condition. The EIA/TIA-422 -B limit does not apply for a combined driver and receiver terminal.
15. Includes 10ns read enable time. Maximum propagation delay is 25ns after read assertion.
16. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
17. The relevant test and measurement methods are given in the "Electromagnetic Compatibility" on page 7.
18. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than "pin-to-pin" (see diagram in "Electromagnetic Compatibility" on page 7).

Insulation Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Creepage Distance (External)		Per IEC 60601	WB-SOIC	8.03	8.3		mm
			QSOP	3.2			mm
Total Barrier Thickness (Internal)				12	13		µm
Barrier Resistance	R_{IO}	500V			$>10^{14}$		Ω
Barrier Capacitance	C_{IO}	f = 1MHz			7		pF
Leakage Current		$240V_{RMS}$, 60Hz			0.2		μA_{RMS}
Comparative Tracking Index	CTI	Per IEC 60112		≥175			V_{RMS}
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	V_{IO}	At maximum operating temperature		1000			V_{RMS}
				1500			V_{DC}
Barrier Life		100°C, $1000V_{RMS}$, 60% CL activation energy			44000		Years

Magnetic Field Immunity (Note 17)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD1} = 5V, V_{DD2} = 5V						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	2800	3500		A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	4000	4500		A/m
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz to 1MHz	4000	4500		A/m
Cross-Axis Immunity Multiplier (Note 18)	K_X			2.5		
V_{DD1} = 3.3V, V_{DD2} = 5V						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	1000	1500		A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	1800	2000		A/m
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz to 1MHz	1800	2000		A/m
Cross-Axis Immunity Multiplier (Note 18)	K_X			2.5		

Safety and Approvals

VDE V 0884-10

Basic Isolation; VDE File Number 5016933-4880-0001/229067

- Working voltage (V_{IORM}) $600V_{RMS}$ ($848V_{PK}$); basic insulation, pollution degree 2
- Transient overvoltage (V_{IOTM}) $4000V_{PK}$
- Each part tested at $1590V_{PK}$ for 1s, 5pC partial discharge limit
- Samples tested at $4000V_{PK}$ for 60s, then $1358V_{PK}$ for 10s with 5pC partial discharge limit

SYMBOL	SAFETY-LIMITING VALUES	VALUE	UNIT
T_S	Safety Rating Ambient Temperature	180	°C
P_S	Safety Rating Power (180°C)	270	mW
I_S	Supply Current Safety Rating (total of supplies)	54	mA

UL 1577

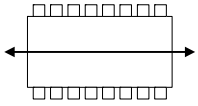
Component Recognition Program File Number: E483309

- Working voltage (V_{IORM}) $600V_{RMS}$ ($848V_{PK}$); basic insulation, pollution degree 2
- Transient overvoltage (V_{IOTM}) $4000V_{PK}$
- Each part tested at 3000 V_{RMS} ($4243V_{PK}$) for 1s
- Each lot samples tested at 2500 V_{RMS} ($3536V_{PK}$) for 60s

Electromagnetic Compatibility

The ISL32704E is fully compliant with generic EMC standards EN50081, EN50082-1, and the umbrella line-voltage standard for information technology equipment (ITE) EN61000. The isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. Compliance tests have been conducted in the following categories:

TABLE 1. COMPLIANCE TEST CATEGORIES

EN50081-1	EN50082-2	EN50204
Residential, Commercial, and Light Industrial: Methods EN55022, EN55014	Industrial Environment EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity) EN61000-4-4 (EFT) EN61000-4-6 (RFI Immunity) EN61000-4-8 (Power Frequency Magnetic Field immunity) EN61000-4-9 (Pulsed Magnetic Field) EN61000-4-10 (Damped Oscillatory Magnetic Field)	Radiated field from digital telephones
Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than "pin-to-pin" as shown on the right.		

Application Information

The ISL32704E is an isolated RS-485 transceiver designed for high-speed data transmission of up to 4Mbps.

RS-485 and Isolation

RS-485 is a differential (balanced) data transmission standard for use in long haul network or noisy environments. It is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on a bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

An important advantage of RS-485 is its wide common-mode range, which specifies that the driver outputs and the receiver inputs withstand signals ranging from +12V to -7V. This common-mode range is the sum of the ground potential difference between driver and receiver, V_{GPD}, the driver output common-mode offset, V_{OC}, and the longitudinally coupled noise along the bus lines, V_n: $V_{CM} = V_{GPD} + V_{OC} + V_n$.

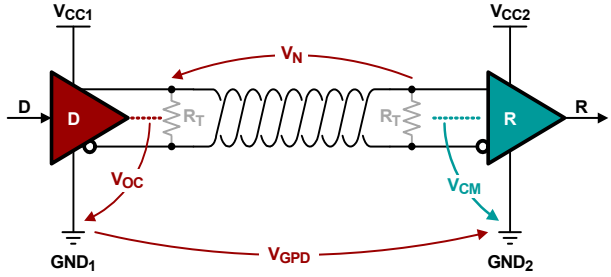


FIGURE 3. COMMON-MODE VOLTAGES IN A NON-ISOLATED DATA LINK

However, in networks using isolated transceivers, such as the ISL32704E, the supply and signal paths of the driver and receiver bus circuits are galvanically isolated from their local mains supplies and signal sources.

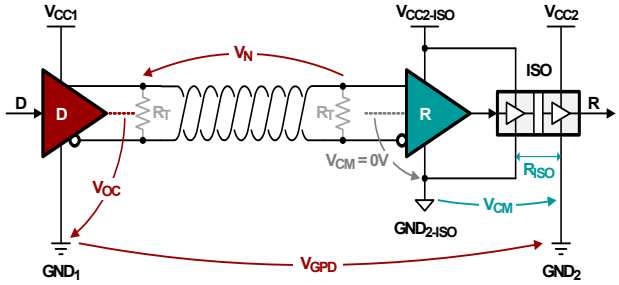


FIGURE 4. COMMON-MODE VOLTAGES IN AN ISOLATED DATA LINK

Because the ground potentials of isolated bus nodes are isolated from each other, the common-mode voltage of one node's output has no effect on the bus inputs of another node. This is because the common-mode voltage is dropping across the high-resistance isolation barrier of $10^{14}\Omega$. Thus, galvanic isolation extends the maximum allowable common-mode range of a data link to the maximum working voltage of the isolation barrier, which for the ISL32704E is $600V_{RMS}$.

Digital Isolator Principle

The ISL32704E utilizes a giant magneto-resistance (GMR) isolation. Figure 5 shows the principle operation of a single channel GMR isolator.

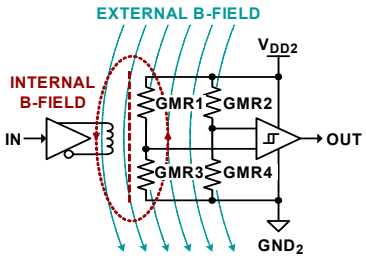


FIGURE 5. SINGLE CHANNEL GMR ISOLATOR

The input signal is buffered and drives a primary coil, which creates a magnetic field that changes the resistance of the GMR resistors 1 to 4. GMR1 to GMR4 form a Wheatstone bridge in order to create a bridge output voltage that only reacts to magnetic field changes from the primary coil. Large external magnetic fields, however, are treated as common-mode fields and are therefore suppressed by the bridge configuration. The bridge output is fed into a comparator whose output signal is identical in phase and shape to the input signal.

GMR Resistor in Detail

Figure 6 shows a GMR resistor consisting of ferromagnetic alloy layers, B1, B2, sandwiched around an ultra thin, nonmagnetic conducting middle layer A, typically copper. The GMR structure is designed so that, in the absence of a magnetic field, the magnetic moments in B1 and B2 face opposite directions, thus causing heavy electron scattering across layer A, which increases its resistance for current C drastically. When a magnetic field D is applied, the magnetic moments in B1 and B2 are aligned and electron scattering is reduced. This lowers the resistance of layer A and increases current C.

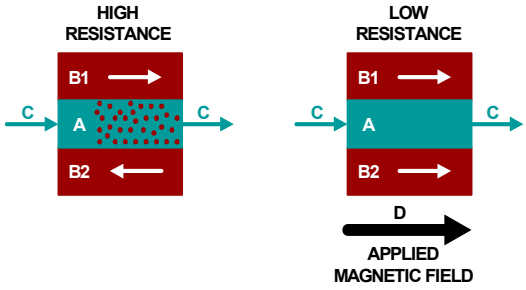


FIGURE 6. MULTI-LAYER GMR RESISTOR

Low Emissions

Because GMR isolators do not use fancy encoding schemes, such as RF carriers or high-frequency clocks, and do not include power transfer coils or transformers, their radiated emission spectrum is virtually undetectable.

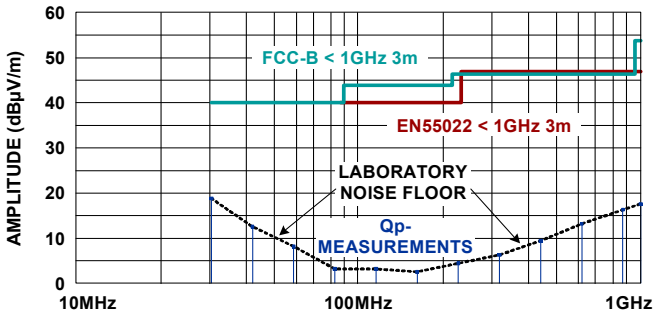


FIGURE 7. UNDETECTABLE EMISSIONS OF GMR ISOLATORS

Low EMI Susceptibility

Because GMR isolators have no pulse trains or carriers to interfere with, they also have very low EMI susceptibility.

For the list of compliance tests conducted on GMR isolators, refer to the "Electromagnetic Compatibility" on page 7.

Receiver (Rx) Features

This transceiver utilizes a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-485 specification.

The receiver input resistance meets the RS-485 Unit Load (UL) requirement of 12kΩ minimum. The receiver includes a "fail-safe if open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating). The receiver output is tri-statable via the active low $\overline{RE}$ input.

Driver (Tx) Features

The RS-485 driver is a differential output device that delivers at least 1.5V across a 54Ω purely differential load. The driver features low propagation delay skew to maximize bit width and to minimize EMI.

The driver in the ISL32704E is tri-statable via the active high DE input. The outputs of the ISL32704E driver are not slew rate limited, so faster output transition times allow data rates of at least 4Mbps.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst-case bus contentions undamaged. The ISL32704E transmitters meet this requirement via driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stage incorporates short-circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification. In the event of a major short-circuit condition, the device also includes a thermal shutdown feature that disables the driver whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The driver automatically re-enables after the die temperature drops about 15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. The receiver stays operational during thermal shutdown.

Dynamic Power Consumption

The isolator within the ISL32704E achieves its low power consumption from the way it transmits data across the barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input signal. Since the current pulses are narrow, about 2.5ns, the power consumption is independent of the mark-to-space ratio and solely depends on frequency.

TABLE 2. SUPPLY CURRENT INCREASE WITH DATA RATE

DATA RATE (Mbps)	I_{DD1} (mA)	I_{DD2} (mA)
1	0.15	0.15
4	0.6	0.6

Power Supply Decoupling

Both supplies, V_{DD1} and V_{DD2}, must be bypassed with 100nF ceramic capacitors. These should be placed as close as possible to the supply pins for proper operation.

DC CORRECTNESS

The ISL32704E incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power-up, the bus outputs follow the truth tables on page 2. The DE input should be held low during power-up to prevent false drive data pulses on the bus. This can be accomplished by connecting a 10kΩ pull-down resistor between DE and GND1.

Data Rate, Cables, and Terminations

RS-485 is intended for network lengths up to 4000 feet, but the maximum system data rate decreases as the transmission length increases. Devices operating at 4Mbps are typically limited to lengths less than 100 feet, but are capable of driving up to 350 feet of cable when allowing for some jitter of 5%.

Twisted pair is the cable of choice for RS-485 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

To minimize reflections, proper termination is imperative when using this high data rate transceiver. In point-to-point or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω for RS-485) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible. A useful guideline for determining the maximum stub lengths is given with Equation 1.

$$L_S \leq \frac{t_r}{10} \times v \times c \qquad \text{(EQ. 1)}$$

where:

- L_S is the stub length (ft)
- t_r is the driver rise time (s)
- c is the speed of light (9.8×10^8 ft/s)
- v is the signal velocity as a percentage of c.

To ensure the receiver output of the ISL32704E is high when the bus is not actively driven, fail-safe biasing of the bus lines is recommended. Figure 8 shows the proper termination of a high-speed data link with fail-safe biasing.

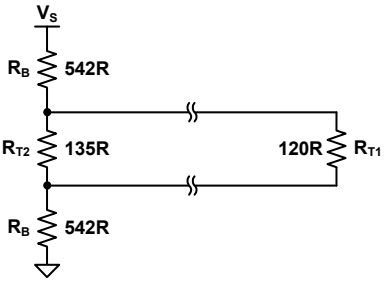


FIGURE 8. FAIL-SAFE BIASING FOR HIGH-SPEED DATA LINKS

Here the termination resistor value at the cable end without fail-safe biasing equals the characteristic cable impedance: $R_{T1} = Z_0$. The values for R_B and R_{T2} are calculated using Equations 2 and 3.

$$R_B \geq \frac{V_S}{V_{AB}} \times \frac{Z_0}{4} \qquad \text{(EQ. 2)}$$

$$R_{T2} = \frac{2R_B \times Z_0}{2R_B - Z_0} \qquad \text{(EQ. 3)}$$

where:

- R_B are the fail-safe biasing resistors
- R_{T2} is the termination resistor in the fail-safe biasing network
- V_S is the minimum transceiver supply voltage
- V_{AB} is the minimum bus voltage of the undriven bus
- Z_0 is the characteristic cable impedance

Note, the resistor values in Figure 8 have been calculated for $V_S = 4.5V$, $V_{AB} = 0.25V$, and $Z_0 = 120Ω$.

Transient Protection

Protecting the ISL32704E against transients exceeding the device's transient immunity requires the addition of an external TVS. For this purpose, Semtech's RClamp0512TQ was chosen due to its high transient protection levels, low junction capacitance, and small form factor.

TABLE 3. RCLAMP0512 TVS FEATURES

PARAMETER		SYMBOL	VALUE	UNIT
ESD (IEC61000-4-2)	Air	V_{ESD}	±30	kV
	Contact	V_{ESD}	±30	kV
EFT (IEC61000-4-4)		V_{EFT}	±4	kV

TABLE 3. RCLAMP0512 TVS FEATURES (Continued)

PARAMETER	SYMBOL	VALUE	UNIT
Surge (IEC61000-4-5)	V_{SURGE}	±1.3	kV
Junction Capacitance	C_J	3	pF
Form Factor	-	1 x 0.6	mm

The TVS is implemented between the bus lines and isolated ground (GND2).

Since transient voltages on the bus lines are referenced to Earth potential, aka Protective Earth (PE), a high-voltage capacitor (C_{HV}) is inserted between GND2 and PE, providing a low-impedance path for high-frequency transients.

Note that the connection from the PE point on the isolated side to the PE point on the non-isolated side (Earth) is usually made via the metal chassis of the equipment, or via a short, thick wire of low-inductance.

A high-voltage resistor (R_{HV}) is added in parallel to C_{HV} to prevent the build-up of static charges on floating grounds (GND2) and cable shields (typically used in Profibus). The bill of materials for the circuit in Figure 9 is listed in Table 4.

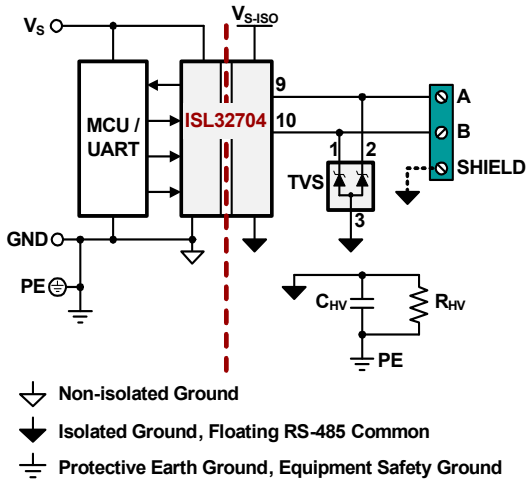


FIGURE 9. TRANSIENT PROTECTION FOR ISL32704E

TABLE 4. BOM FOR CIRCUIT IN Figure 9

NAME	FUNCTION	ORDER NO.	VENDOR
TVS	170W (8µs, 20µs) 2-LINE PROTECTOR	RCLAMP0512TQ	SEMTECH
C_{HV}	4.7nF, 2kV, 10% CAPACITOR	1812B472K202NT	NOVACAP
R_{HV}	1MΩ, 2kV, 5% RESISTOR	HVC12061M0JT3	TT-ELECTRONICS

Pinout Differences Between Packages

The wide-body version (ISL32704EIBZ) has a single output power supply pin, VDD2, supplying the bus side of the isolation module and the transceiver module.

This package also provides two ground pins for each supply. The GND1 pins are internally connected between Pins 2 and 8 and the GND2 pins between Pins 9 and 15. This allows for increased layout flexibility.

The wide-body version also provides an isolated DE output, ISODE, that can be used in PROFIBUS™ applications to monitor the state of the isolated drive enable node.

The QSOP version (ISL32704EIAZ) is designed for application flexibility and maximum space saving in dense PCB designs. This package provides an isolated DE output (ISODE) and a separate DE input on the bus side (XDE). XDE can be used to enable the driver from the bus side, or when connected to ISODE, enable the driver from the DE input on the controller side.

Two separate output supply pins are available, VDD2 for the isolation module and VDD2X for the transceiver module. Both pins should be connected externally for normal operation, or can be used separately for testing and troubleshooting.

The QSOP version also has an “ISOR” output that is isolated from the receiver output “R” on the controller side. This pin is used for testing and usually left open, but it could be used for bus-side monitoring purposes in special circumstances.

Figures 10 and 11 show the typical device connections for both package versions.

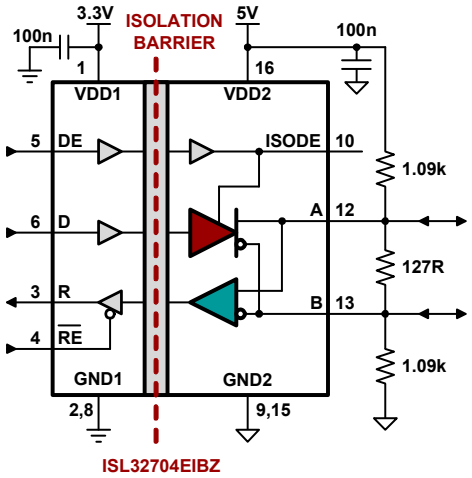


FIGURE 10. TYPICAL WB-SOIC TRANSCEIVER CONNECTIONS

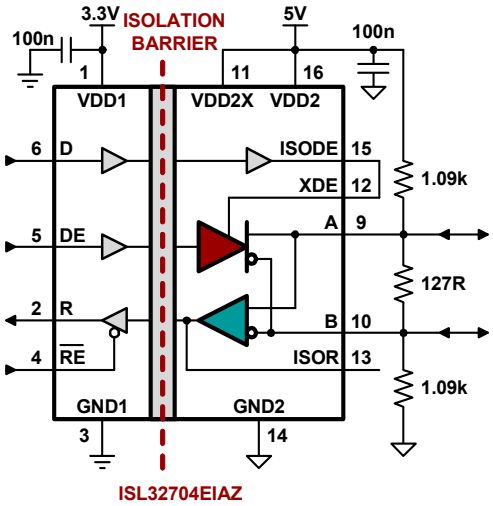


FIGURE 11. TYPICAL QSOP TRANSCEIVER CONNECTIONS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

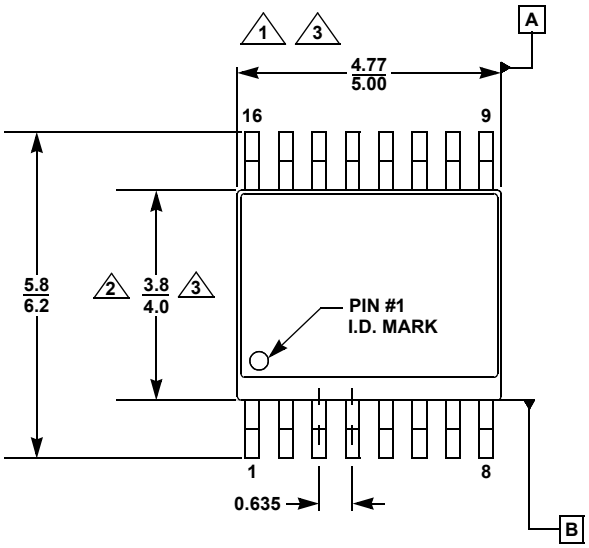
DATE	REVISION	CHANGE
Feb 12, 2018	FN8860.4	Updated Note 1 and added Note 2. Updated VDE and UL certification file numbers. Updated Thermal Information (Theta JA, JC values) -Changed the 16ld WB-SOIC Package from 60, 12 to 34, 17. -Changed the 16ld QSOP Package from 60, 10 to 63, 35. POD M16.3A - updated from rev 0 to rev 1. Changes: Updated Typical Recommended Land Pattern dimensions lead height from 2.2 to 1.7, lead width from 0.6 to 0.51, and body center to center from 9.2 to 9.75. Removed About Intersil section.
Mar 29, 2017	FN8860.3	Added WB-SOIC information throughout document. Updated Feature bullets Updated Notes 5 and 6.
Feb 10, 2017	FN8860.2	On page 2, Ordering Information, changed ISL32704EIAZ-EVALZ to ISL32704EVAL1Z.
Jan 19, 2017	FN8860.1	Updated Figure 1 on page 1 and Figure 2 on page 3. Changed from dual to single failsafe biasing. On page 2, Ordering Information, added ISL32704EIAZ-EVALZ and Note 1 for tape and reel and quantity. On page 7 in VDE V 0884-11 (Certification Pending) and UL 1577 sections, changed from “Standard” to “Basic” isolation.
Dec 12, 2016	FN8860.0	Initial Release

Package Outline Drawing

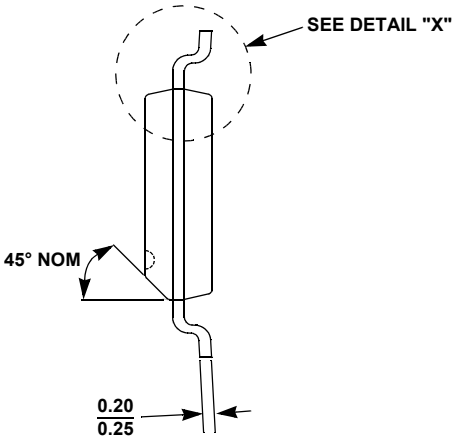
For the most recent package outline drawing, see M16.15B.

M16.15B

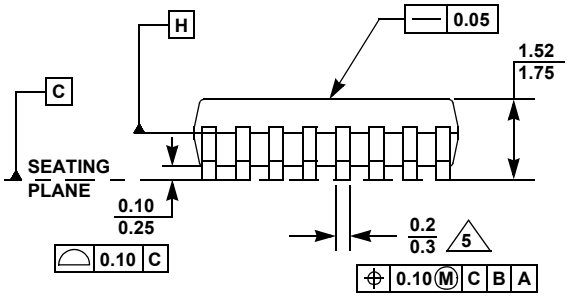
16 LEAD QUARTER-SIZE SMALL OUTLINE PLASTIC PACKAGE (QSOP)
Rev 0, 9/16



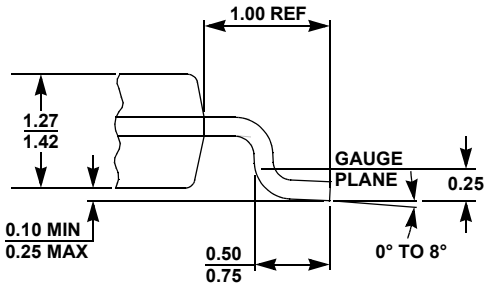
TOP VIEW



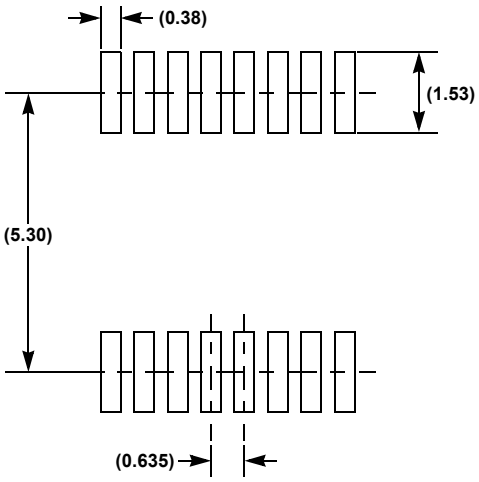
END VIEW



SIDE VIEW



DETAIL X



TYPICAL RECOMMENDED LAND PATTERN

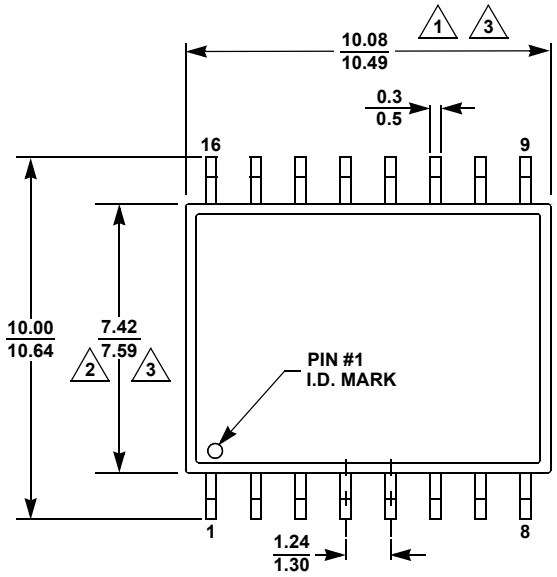
NOTES:

1. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion.
6. Dimension in ( ) are for reference only.
7. Pin spacing is a BASIC dimension; tolerances do not accumulate.
8. Dimensions are in mm.

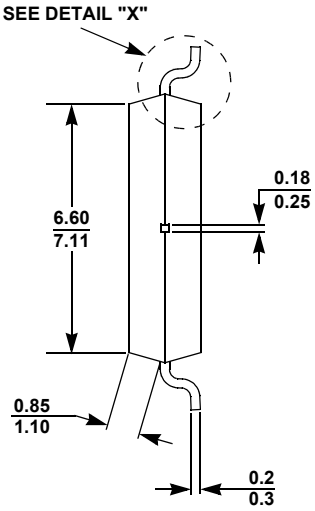
Package Outline Drawing

For the most recent package outline drawing, see M16.3A.

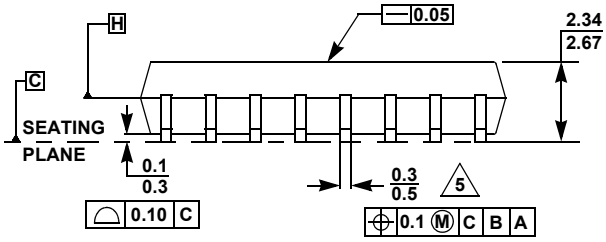
M16.3A
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOICW)
Rev 1, 6/17



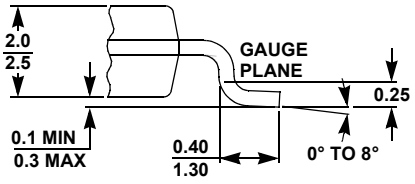
TOP VIEW



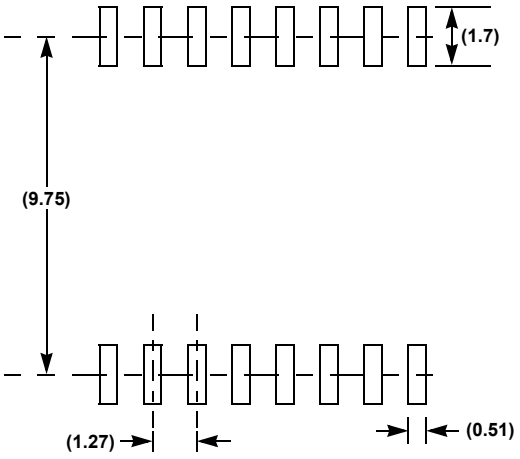
END VIEW



SIDE VIEW



DETAIL X



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

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2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
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