

ISL5857

12-bit, +3.3V, 260+MSPS, High Speed D/A Converter

FN6079  
Rev 3.00  
October 7, 2015

The **ISL5857** is a 12-bit, 260+MSPS (Mega Samples Per Second), CMOS, high speed, low power, D/A (digital-to-analog) converter designed specifically for use in high performance communication systems such as base transceiver stations utilizing 2.5G or 3G cellular protocols.

This device complements the ISL5x57 family of high speed converters, which include 10, 12, and 14-bit devices.

**Applications**

- Cellular Infrastructure - single or multicarrier: IS-136, IS-95, GSM, EDGE, CDMA2000, WCDMA, TDS-CDMA
- BWA infrastructure
- Medical/test instrumentation
- Wireless communication systems
- High resolution imaging systems
- Arbitrary waveform generators

**Features**

- Low power . . . . . 103mW with 20mA output at 130MSPS
- Adjustable full scale output current. . . . . 2mA to 20mA
- +3.3V power supply
- 3V LVCMOS compatible inputs
- Excellent spurious free dynamic range (73dBc to Nyquist,  $f_S = 130\text{MSPS}$ ,  $f_{OUT} = 10\text{MHz}$ )
- UMTS adjacent channel power = 70dB at 19.2MHz
- EDGE/GSM SFDR = 90dBc at 11MHz in 20MHz window
- Pin compatible, 3.3V, lower power replacement for the AD9752 and HI5860
- Pb-free (RoHS compliant)

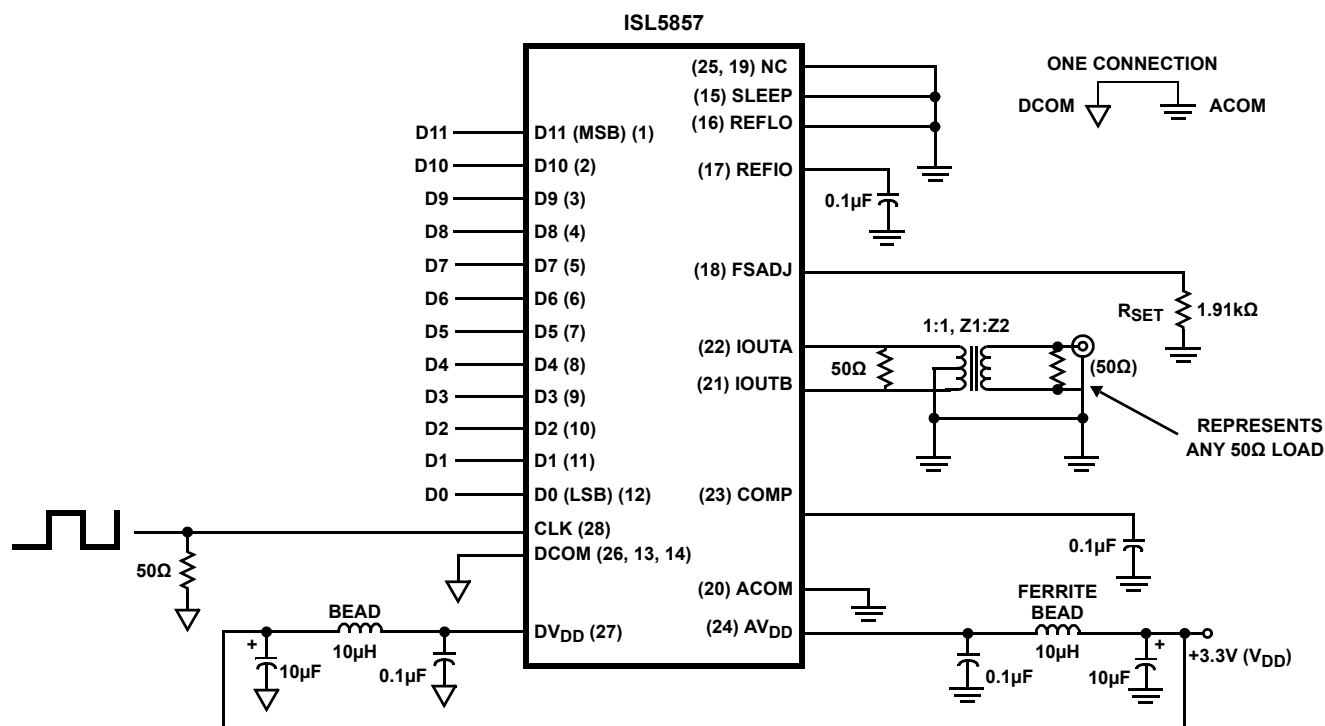


FIGURE 1. TYPICAL APPLICATIONS CIRCUIT

# Functional Block Diagram

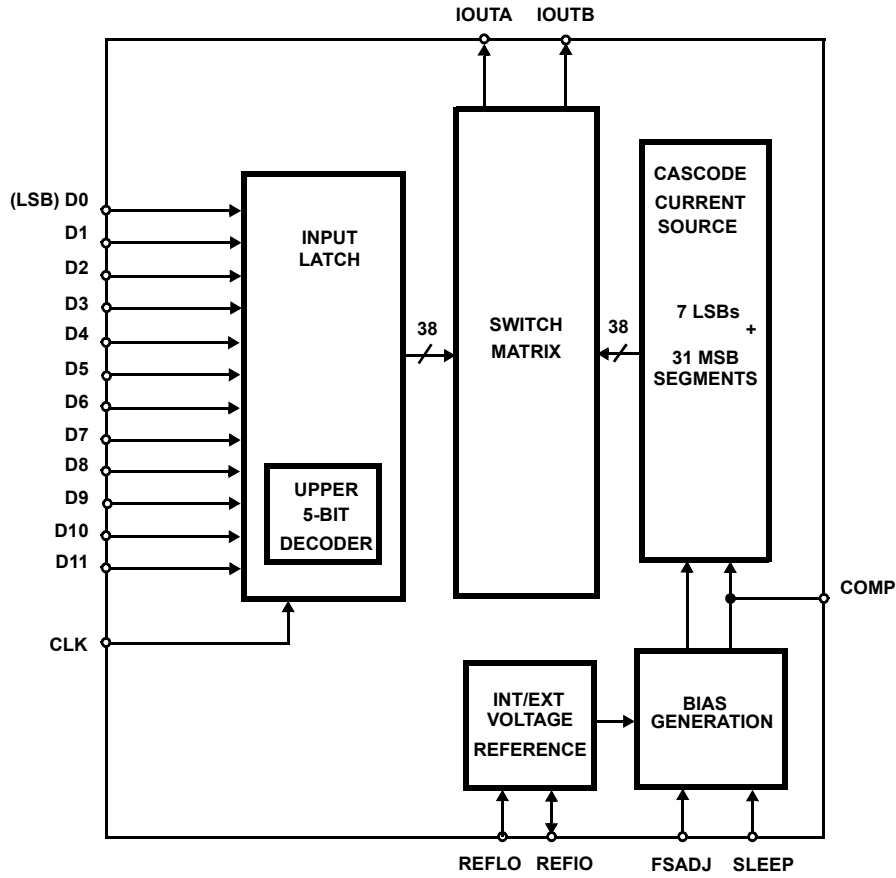
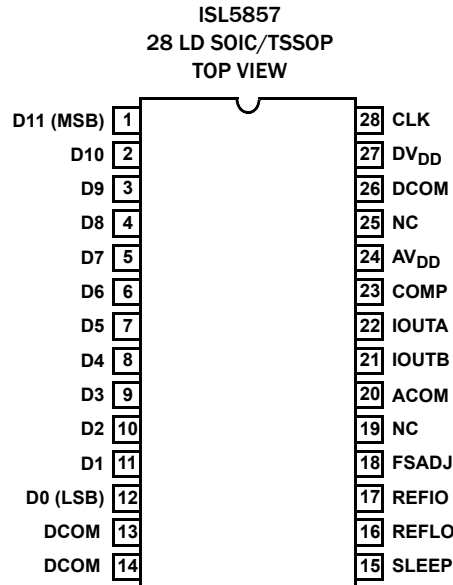


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

# Pin Configuration



## Pin Descriptions

PIN NO.	PIN NAME	DESCRIPTION
1 through 12	D11 (MSB) Through D0 (LSB)	Digital data Bit 11, (Most Significant Bit) through Digital Data Bit 0, (Least Significant Bit).
15	SLEEP	Control pin for power-down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal 20 $\mu$ A active pull-down current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV <sub>DD</sub> to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1 $\mu$ F capacitor to ground when internal reference is enabled.
18	FSADJ	Full scale current adjust. Use a resistor to ground to adjust full scale output current. Full scale output current = $32 \times V_{FSADJ}/R_{SET}$ .
19, 25	NC	No Connect. These should be grounded, but can be left disconnected.
21	IOUTB	The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is achieved when all input bits are set to binary 1.
23	COMP	Connect 0.1 $\mu$ F capacitor to ACOM.
24	AV <sub>DD</sub>	Analog supply (+3.0V to +3.6V).
20	ACOM	Connect to analog ground.
26, 13, 14	DCOM	Connect to digital ground.
27	DV <sub>DD</sub>	Digital supply (+3.0V to +3.6V).
28	CLK	Clock input.

## Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #	CLOCK SPEED
ISL5857IBZ No longer available or supported, recommended replacement part: ISL5857IAZ	ISL5857IBZ	-40 to +85	28 Ld SOIC	M28.3	260MHz
ISL5857IAZ	ISL 5857IAZ	-40 to +85	28 Ld TSSOP	M28.173	260MHz

### NOTES:

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see product information page for [ISL5857](#). For more information on MSL, please see tech brief [TB363](#).

## Absolute Maximum Ratings

Digital Supply Voltage $DV_{DD}$ to DCOM	+3.6V
Analog Supply Voltage $AV_{DD}$ to ACOM	+3.6V
Grounds, ACOM TO DCOM	-0.3V to +0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP)	$DV_{DD} + 0.3V$
Reference Input Voltage Range	$AV_{DD} + 0.3V$
Analog Output Current ( $I_{OUT}$ )	24mA

## Thermal Information

Thermal Resistance (Typical, <a href="#">Note 3</a> )	$\theta_{JA}$ (°C/W)
SOIC Package	75
TSSOP Package	110
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Pb-free Reflow Profile	see <a href="#">TB493</a>

## Operating Conditions

Temperature Range ..... -40°C to 85°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air. See Tech Brief [TB379](#).

**Electrical Specifications**  $AV_{DD} = DV_{DD} = +3.3V$ ,  $V_{REF} = \text{Internal } 1.2V$ ,  $I_{OUTFS} = 20mA$ ,  $T_A = +25^\circ C$  for all typical values. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ C \text{ TO } 85^\circ C$			UNITS
		MIN	TYP	MAX	
<b>SYSTEM PERFORMANCE</b>					
Resolution		<b>12</b>	-	-	Bits
Integral Linearity Error, INL	"Best fit" straight line ( <a href="#">Note 10</a> )	<b>-1.25</b>	$\pm 0.5$	<b>+1.25</b>	LSB
Differential Linearity Error, DNL	( <a href="#">Note 10</a> )	<b>-1</b>	$\pm 0.5$	<b>+1</b>	LSB
Offset Error, $I_{OS}$	$I_{OUTA}$ ( <a href="#">Note 10</a> )	<b>-0.006</b>		<b>+0.006</b>	% FSR
Offset Drift Coefficient	( <a href="#">Note 10</a> )	-	0.1	-	ppm FSR/°C
Full Scale Gain Error, FSE	With external reference ( <a href="#">Notes 4, 10</a> )	<b>-3</b>	$\pm 0.5$	<b>+3</b>	% FSR
	With internal reference ( <a href="#">Notes 4, 10</a> )	<b>-3</b>	$\pm 0.5$	<b>+3</b>	% FSR
Full Scale Gain Drift	With external reference ( <a href="#">Note 10</a> )	-	$\pm 50$	-	ppm FSR/°C
	With internal reference ( <a href="#">Note 10</a> )	-	$\pm 100$	-	ppm FSR/°C
Full Scale Output Current, $I_{FS}$		<b>2</b>	-	<b>20</b>	mA
Output Voltage Compliance Range	( <a href="#">Note 5</a> )	<b>-1.0</b>	-	<b>1.25</b>	V
<b>DYNAMIC CHARACTERISTICS</b>					
Maximum Clock Rate, $f_{CLK}$		<b>260</b>	300	-	MHz
Output Rise Time	Full scale step	-	1.5	-	ns
Output Fall Time	Full scale step	-	1.5	-	ns
Output Capacitance		-	10	-	pF
Output Noise	$I_{OUTFS} = 20mA$	-	50	-	$\mu A/\sqrt{Hz}$
	$I_{OUTFS} = 2mA$	-	30	-	$\mu A/\sqrt{Hz}$
<b>AC CHARACTERISTICS</b> (Using <a href="#">Figure 15</a> with $R_{DIFF} = 50\Omega$ and $R_{LOAD} = 50\Omega$ , Full scale output = -2.5dBm)					
Spurious Free Dynamic Range, SFDR Within a Window	$f_{CLK} = 210MSPS$ , $f_{OUT} = 80.8MHz$ , 30MHz span ( <a href="#">Notes 6, 10</a> )	-	73	-	dBc
	$f_{CLK} = 210MSPS$ , $f_{OUT} = 40.4MHz$ , 30MHz span ( <a href="#">Notes 6, 10</a> )	-	80	-	dBc
	$f_{CLK} = 130MSPS$ , $f_{OUT} = 20.2MHz$ , 20MHz span ( <a href="#">Notes 6, 10</a> )	-	85	-	dBc

**Electrical Specifications**  $V_{DD} = DV_{DD} = +3.3V$ ,  $V_{REF} = \text{Internal } 1.2V$ ,  $I_{OUTFS} = 20mA$ ,  $T_A = +25^\circ C$  for all typical values. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ C \text{ TO } 85^\circ C$			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range, SFDR to Nyquist ( $f_{CLK}/2$ )	$f_{CLK} = 260\text{MSPS}$ , $f_{OUT} = 80.8\text{MHz}$ (Notes 6, 10)	-	47	-	dBc
	$f_{CLK} = 260\text{MSPS}$ , $f_{OUT} = 40.4\text{MHz}$ (Notes 6, 10)	-	60	-	dBc
	$f_{CLK} = 260\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ (Notes 6, 10)	-	62	-	dBc
	$f_{CLK} = 210\text{MSPS}$ , $f_{OUT} = 80.8\text{MHz}$ (Notes 6, 10)	-	51	-	dBc
	$f_{CLK} = 210\text{MSPS}$ , $f_{OUT} = 40.4\text{MHz}$ (Notes 6, 10, 12)	-	60	-	dBc
	$f_{CLK} = 200\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ , $T = 25^\circ C$ (Notes 6, 10)	<b>60</b>	62	-	dBc
	$f_{CLK} = 200\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ , $T = -40^\circ C \text{ to } 85^\circ C$ (Notes 6, 10)	<b>58</b>	-	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 50.5\text{MHz}$ (Notes 6, 10)	-	57	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 40.4\text{MHz}$ (Notes 6, 10)	-	62	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ (Notes 6, 10)	-	69	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 10.1\text{MHz}$ (Notes 6, 10)	-	73	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 5.05\text{MHz}$ , $T = 25^\circ C$ (Notes 6, 10)	<b>70</b>	77	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 5.05\text{MHz}$ , $T = -40^\circ C \text{ to } 85^\circ C$ (Notes 6, 10)	<b>68</b>	-	-	dBc
	$f_{CLK} = 100\text{MSPS}$ , $f_{OUT} = 40.4\text{MHz}$ (Notes 6, 10)	-	60	-	dBc
	$f_{CLK} = 80\text{MSPS}$ , $f_{OUT} = 30.3\text{MHz}$ (Notes 6, 10)	-	63	-	dBc
	$f_{CLK} = 80\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ (Notes 6, 10)	-	69	-	dBc
	$f_{CLK} = 80\text{MSPS}$ , $f_{OUT} = 10.1\text{MHz}$ (Notes 6, 10, 12)	-	70	-	dBc
	$f_{CLK} = 80\text{MSPS}$ , $f_{OUT} = 5.05\text{MHz}$ (Notes 6, 10)	-	76	-	dBc
	$f_{CLK} = 50\text{MSPS}$ , $f_{OUT} = 20.2\text{MHz}$ (Notes 6, 10)	-	68	-	dBc
	$f_{CLK} = 50\text{MSPS}$ , $f_{OUT} = 10.1\text{MHz}$ (Notes 6, 10)	-	73	-	dBc
$f_{CLK} = 50\text{MSPS}$ , $f_{OUT} = 5.05\text{MHz}$ (Notes 6, 10)	-	77	-	dBc	
Spurious Free Dynamic Range, SFDR in a Window with Eight Tones	$f_{CLK} = 210\text{MSPS}$ , $f_{OUT} = 28.3\text{MHz to } 45.2\text{MHz}$ , 2.1MHz spacing, 50MHz Span (Notes 6, 10, 12)	-	65	-	dBc
	$f_{CLK} = 130\text{MSPS}$ , $f_{OUT} = 17.5\text{MHz to } 27.9\text{MHz}$ , 1.3MHz spacing, 35MHz Span (Notes 6, 10)	-	68	-	dBc
	$f_{CLK} = 80\text{MSPS}$ , $f_{OUT} = 10.8\text{MHz to } 17.2\text{MHz}$ , 811kHz spacing, 15MHz Span (Notes 6, 10)	-	75	-	dBc
	$f_{CLK} = 50\text{MSPS}$ , $f_{OUT} = 6.7\text{MHz to } 10.8\text{MHz}$ , 490kHz spacing, 10MHz Span (Notes 6, 10)	-	77	-	dBc
Spurious Free Dynamic Range, SFDR in a Window with EDGE or GSM	$f_{CLK} = 78\text{MSPS}$ , $f_{OUT} = 11\text{MHz}$ , in a 20MHz window, RBW = 30kHz (Notes 6, 10, 12)	-	90	-	dBc
Adjacent Channel Power Ratio, ACPR with UMTS	$f_{CLK} = 76.8\text{MSPS}$ , $f_{OUT} = 19.2\text{MHz}$ , RBW = 30kHz (Notes 6, 10, 12)	-	70	-	dB
<b>VOLTAGE REFERENCE</b>					
Internal Reference Voltage, $V_{FSADJ}$	Pin 18 voltage with internal reference	<b>1.2</b>	1.23	<b>1.3</b>	V
Internal Reference Voltage Drift		-	$\pm 40$	-	ppm/ $^\circ C$
Internal Reference Output Current Sink/Source Capability	Reference is not intended to be externally loaded	-	0	-	$\mu A$
Reference Input Impedance		-	1	-	M $\Omega$
Reference Input Multiplying Bandwidth	(Note 10)	-	1.0	-	MHz

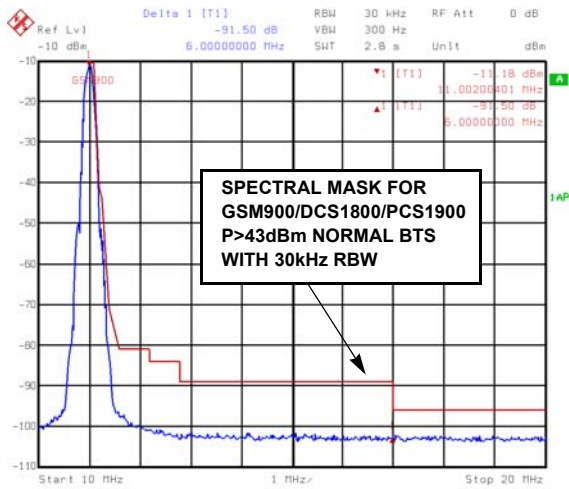
**Electrical Specifications**  $AV_{DD} = DV_{DD} = +3.3V$ ,  $V_{REF} = \text{Internal } 1.2V$ ,  $I_{OUTFS} = 20mA$ ,  $T_A = +25^\circ C$  for all typical values. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

PARAMETER	TEST CONDITIONS	$T_A = -40^\circ C \text{ TO } 85^\circ C$			UNITS
		MIN	TYP	MAX	
<b>DIGITAL INPUTS</b> D11-D0, CLK					
Input Logic High Voltage with 3.3V Supply, $V_{IH}$	(Note 5)	<b>2.3</b>	3.3	-	V
Input Logic Low Voltage with 3.3V Supply, $V_{IL}$	(Note 5)	-	0	<b>1.0</b>	V
Sleep Input Current, $I_{IH}$		<b>-25</b>	-	<b>+25</b>	$\mu A$
Input Logic Current, $I_{IH}$ , $I_{IL}$		<b>-20</b>	-	<b>+20</b>	$\mu A$
Clock Input Current, $I_{IH}$ , $I_{IL}$		<b>-10</b>	-	<b>+10</b>	$\mu A$
Digital Input Capacitance, $C_{IN}$		-	5	-	pF
<b>TIMING CHARACTERISTICS</b>					
Data Setup Time, $t_{SU}$	See Figure 17	-	1.5	-	ns
Data Hold Time, $t_{HLD}$	See Figure 17	-	1.5	-	ns
Propagation Delay Time, $t_{PD}$	See Figure 17	-	1	-	Clock Period
CLK Pulse Width, $t_{PW1}$ , $t_{PW2}$	See Figure 17 (Note 5)	<b>0.9</b>	-	-	ns
<b>POWER SUPPLY CHARACTERISTICS</b>					
$AV_{DD}$ Power Supply	(Note 11)	<b>2.7</b>	3.3	<b>3.6</b>	V
$DV_{DD}$ Power Supply	(Note 11)	<b>2.7</b>	3.3	<b>3.6</b>	V
Analog Supply Current ( $I_{AVDD}$ )	3.3V, $I_{OUTFS} = 20mA$	-	27.5	<b>28.5</b>	mA
	3.3V, $I_{OUTFS} = 2mA$	-	10	-	mA
Digital Supply Current ( $I_{DVDD}$ )	3.3V (Note 7)	-	3.7	<b>5</b>	mA
	3.3V (Note 8)	-	6.5	<b>8</b>	mA
Supply Current ( $I_{AVDD}$ ) Sleep Mode	3.3V, $I_{OUTFS} = \text{Don't Care}$	-	1.5	-	mA
Power Dissipation	3.3V, $I_{OUTFS} = 20mA$ (Note 7)	-	103	<b>111</b>	mW
	3.3V, $I_{OUTFS} = 20mA$ (Note 8)	-	110	<b>120</b>	mW
	3.3V, $I_{OUTFS} = 20mA$ (Note 9)	-	157	-	mW
	3.3V, $I_{OUTFS} = 2mA$ (Note 7)	-	45	-	mW
Power Supply Rejection	Single supply (Note 10)	<b>-0.125</b>	-	<b>+0.125</b>	%FSR/V

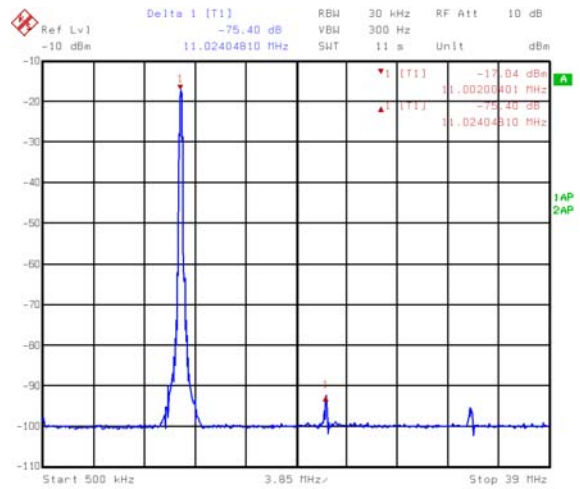
**NOTES:**

- Gain Error measured as the error in the ratio between the full scale output current and the current through  $R_{SET}$  (typically  $625\mu A$ ). Ideally the ratio should be 32.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- Spectral measurements made with differential transformer coupled output and no external filtering. For multitone testing, the same pattern was used at different clock rates, producing different output frequencies but at the same ratio to the clock rate.
- Measured with the clock at 130MSPS and the output frequency at 5MHz.
- Measured with the clock at 200MSPS and the output frequency at 20MHz.
- Measured with the clock at 260MSPS and the output frequency at 40MHz.
- See "Definition of Specifications" on page 9.
- Recommended operation is from 3.0V to 3.6V. Operation below 3.0V is possible with some degradation in spectral performance. Reduction in analog output current may be necessary to maintain spectral performance.
- See "Typical Performance Plots" on page 7.

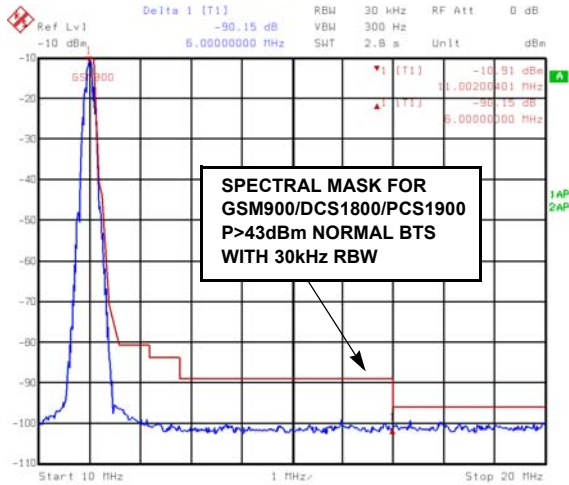
**Typical Performance Plots** (+3.3V Supply, Using [Figure 15](#) with  $R_{DIFF} = 100\Omega$  and  $R_{LOAD} = 50\Omega$ )



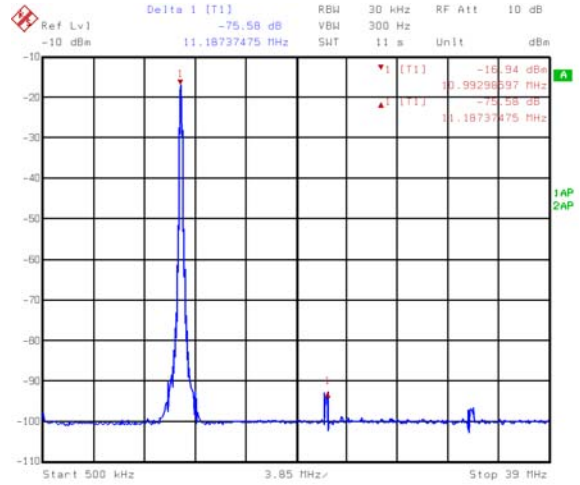
**FIGURE 3. EDGE AT 11MHz, 78MSPS CLOCK**  
(91+dBc AT  $\Delta f = +6$ MHz)



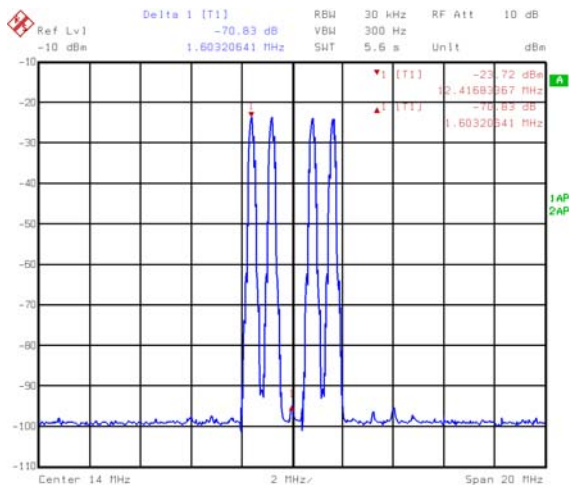
**FIGURE 4. EDGE AT 11MHz, 78MSPS CLOCK**  
(75dBc - NYQUIST, 6dB PAD)



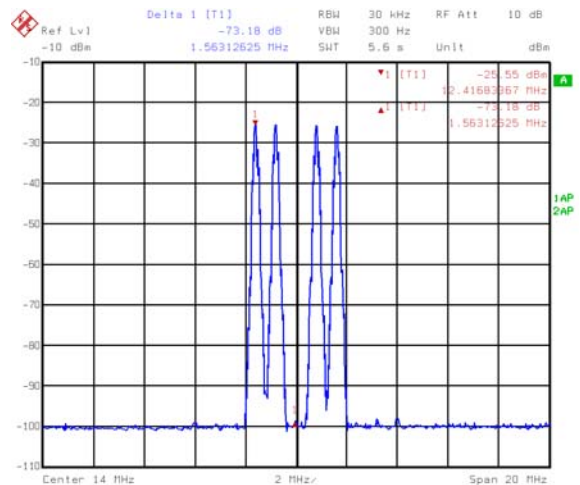
**FIGURE 5. GSM AT 11MHz, 78MSPS CLOCK**  
(90+dBc AT  $\Delta f = +6$ MHz, 3dB PAD)



**FIGURE 6. GSM AT 11MHz, 78MSPS CLOCK**  
(75dBc - NYQUIST, 9dB PAD)



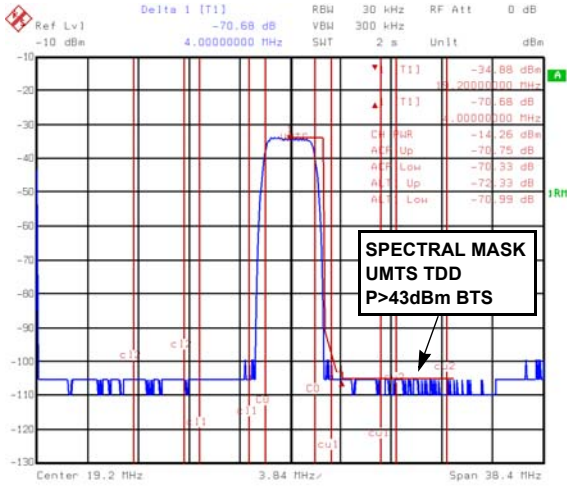
**FIGURE 7. FOUR EDGE CARRIERS AT 12.4 to 15.6MHz, 800kHz SPACING, 78MSPS (71dBc - 20MHz WINDOW)**



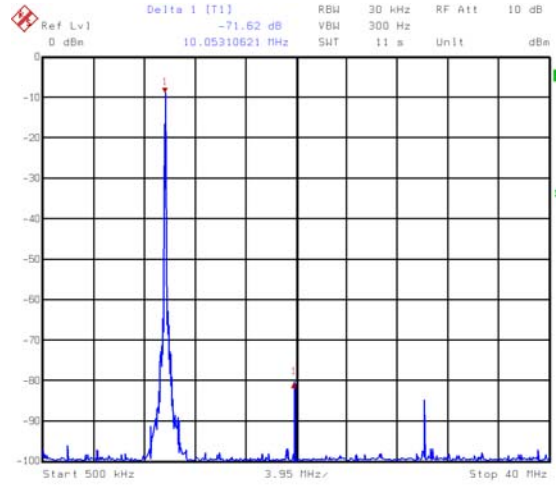
**FIGURE 8. FOUR GSM CARRIERS AT 12.4 to 15.6MHz, 78MSPS (73dBc - 20MHz WINDOW, 6dB PAD)**



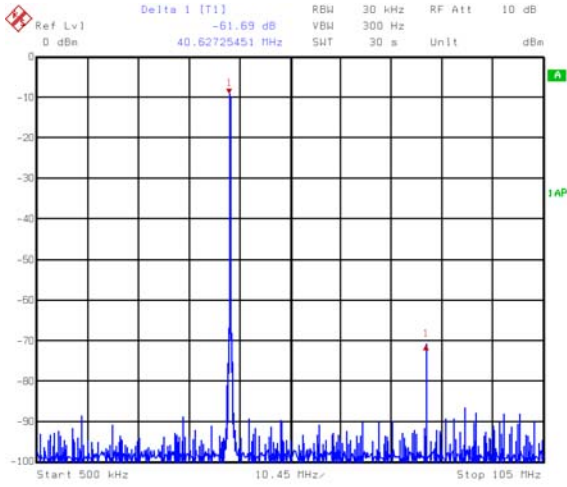
**Typical Performance Plots** (+3.3V Supply, Using [Figure 15](#) with  $R_{DIFF} = 100\Omega$  and  $R_{LOAD} = 50\Omega$ ) (Continued)



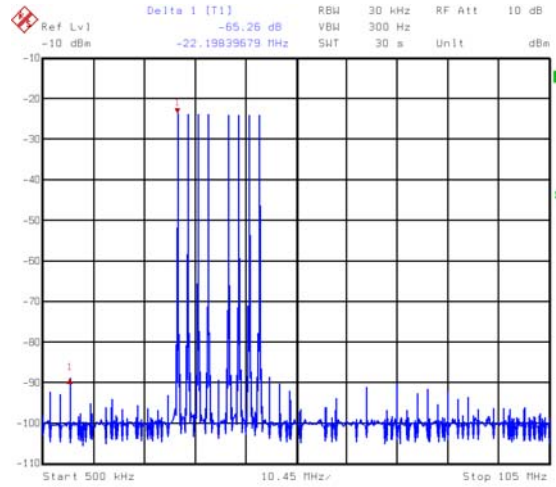
**FIGURE 9. UMTS AT 19.2MHz, 76.8MSPS (70dB 1st ACPR, 70dB 2nd ACPR)**



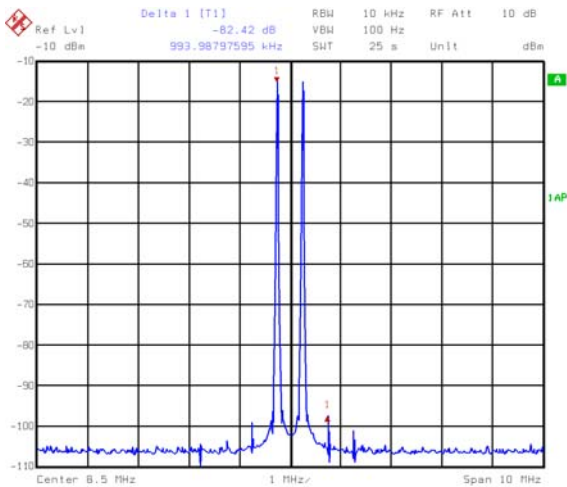
**FIGURE 10. ONE TONE AT 10.1MHz, 80MSPS CLOCK (71dBc - NYQUIST, 6dB PAD)**



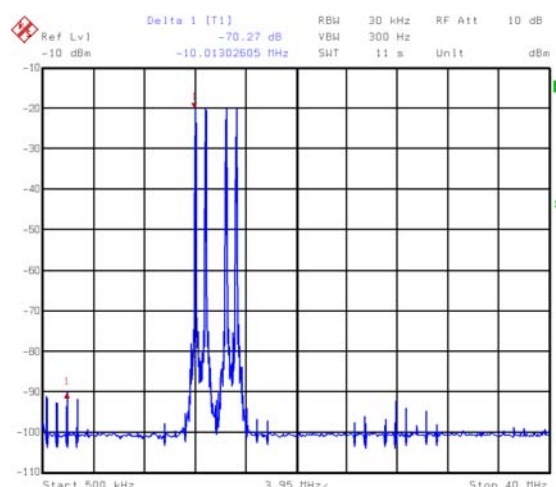
**FIGURE 11. ONE TONE AT 40.4MHz, 210MSPS CLOCK (61dBc - NYQUIST, 6dB PAD)**



**FIGURE 12. EIGHT TONES (CREST FACTOR = 8.9) AT 37MHz, 210MSPS CLOCK, 2.1MHz SPACING (65dBc - NYQUIST)**



**FIGURE 13. TWO TONES (CF = 6) AT 8.5MHz, 50MSPS CLOCK, 500kHz SPACING (82dBc - 10MHz WINDOW, 6dB PAD)**



**FIGURE 14. FOUR TONES (CF = 8.1) AT 14MHz, 80MSPS CLOCK, 800kHz SPACING (70dBc - NYQUIST, 6dB PAD)**



## Definition of Specifications

**Adjacent Channel Power Ratio, ACPR**, is the ratio of the average power in the adjacent frequency channel (or offset) to the average power in the transmitted frequency channel.

**Differential Linearity Error, DNL**, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

**EDGE, Enhanced Data for Global Evolution**, a TDMA standard for cellular applications which uses 200kHz BW, 8-PSK modulated carriers.

**Full Scale Gain Drift**, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from  $T_{MIN}$  to  $T_{MAX}$ . It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either  $T_{MIN}$  or  $T_{MAX}$ . The units are ppm of FSR (full scale range) per °C.

**Full Scale Gain Error**, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through  $R_{SET}$ ).

**GSM, Global System for Mobile Communication**, a TDMA standard for cellular applications which uses 200kHz BW, GMSK modulated carriers.

**Integral Linearity Error, INL**, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

**Internal Reference Voltage Drift**, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either  $T_{MIN}$  or  $T_{MAX}$ . The units are ppm per °C.

**Offset Drift**, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage at IOUTA through a known resistance as the temperature is varied from  $T_{MIN}$  to  $T_{MAX}$ . It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either  $T_{MIN}$  or  $T_{MAX}$ . The units are ppm of FSR (full scale range) per °C.

**Offset Error**, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage of IOUTA through a known resistance. Offset error is defined as the maximum *deviation* of the IOUTA output current from a value of 0mA.

**Output Voltage Compliance Range**, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

**Power Supply Rejection**, is measured using a single power supply. The nominal supply voltage is varied  $\pm 10\%$  and the change in the DAC full scale output is noted.

**Reference Input Multiplying Bandwidth**, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the

amplitude of the output waveform is 0.707 (-3dB) of its original value.

**Spurious Free Dynamic Range, SFDR**, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

**Total Harmonic Distortion, THD**, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

**UMTS, Universal Mobile Telecommunications System**, a W-CDMA standard for cellular applications which uses 3.84MHz modulated carriers.

## Detailed Description

The ISL5857 is a 12-bit, current out, CMOS, digital to analog converter. The maximum update rate is at least 260+MSPS and can be powered by a single power supply in the recommended range of +3.0V to +3.6V. It consumes less than 120mW of power when using a +3.3V supply, the maximum 20mA of output current, and the data switching at 210MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain worst-case transition points, such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at these major transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems and accuracy.

## Digital Inputs and Termination

The ISL5857 digital inputs are guaranteed to 3V LVCMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are long 50Ω lines, then 50Ω termination resistors should be placed as close to the converter inputs as possible connected to the digital ground plane (if separate grounds are used). These termination resistors are not likely needed as long as the digital waveform source is within a few inches of the DAC. For pattern drivers with very high speed edge rates, it is recommended that the user consider series termination (50Ω to 200Ω) prior to the DAC's inputs in order to reduce the amount of noise.

## Power Supply

Separate digital and analog power supplies are recommended. The allowable supply range is +2.7V to +3.6V. The recommended supply range is +3.0V to 3.6V (nominally +3.3V) to maintain optimum SFDR. However, operation down to +2.7V is possible with some degradation in SFDR. Reducing the analog output current can help the SFDR at +2.7V. The SFDR values stated in the table of specifications were obtained with a +3.3V supply.

## Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane.

## Noise Reduction

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the converter's power supply pins, AV<sub>DD</sub> and DV<sub>DD</sub>. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV<sub>DD</sub> and to the analog ground for AV<sub>DD</sub>. Additional filtering of the power supplies on the board is recommended.

## Voltage Reference

The internal voltage reference of the device has a nominal value of +1.23V with a ±40ppm/°C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (16) selects the reference. The internal reference can be selected if pin 16 is tied low (ground). If an external reference is desired, then pin 16 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 17. The full scale output current of the converter is a function of the voltage reference used and the value of R<sub>SET</sub>. I<sub>OUT</sub> should be within the 2mA to 20mA range, though operation below 2mA is possible with performance degradation.

If the internal reference is used, V<sub>FSADJ</sub> will equal approximately 1.2V (pin 18). If an external reference is used, V<sub>FSADJ</sub> will equal the external reference. The calculation for I<sub>OUT</sub> (Full Scale) is:

$$I_{OUT}(\text{Full Scale}) = (V_{FSADJ}/R_{SET}) \times 32$$

If the full scale output current is set to 20mA by using the internal voltage reference (1.2V) and a 1.91kΩ R<sub>SET</sub> resistor, then the input coding to output current will resemble the following:

**TABLE 1. INPUT CODING vs OUTPUT CURRENT WITH INTERNAL REFERENCE AND RSET = 1.91kΩ**

INPUT CODE (D11-D0)	IOUTA (mA)	IOUTB (mA)
11 11111 11111	20	0
10 00000 00000	10	10
00 00000 00000	0	20

## Analog Output

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single-ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0V to 1.25V. R<sub>OUT</sub> (the impedance loading each current output)

should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$$V_{OUT} = I_{OUT} \times R_{OUT}$$

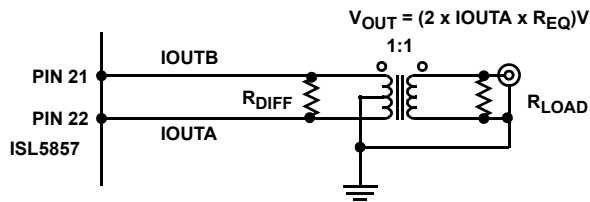
The most effective method for reducing the power consumption is to reduce the analog output current, which dominates the supply current. The maximum recommended output current is 20mA.

## Differential Output

IOUTA and IOUTB can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. With R<sub>DIFF</sub> = 50Ω and R<sub>LOAD</sub> = 50Ω, the circuit in [Figure 15](#) will provide a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA (used for the electrical specifications table). Values of R<sub>DIFF</sub> = 100Ω and R<sub>LOAD</sub> = 50Ω were used for the typical performance curves. The center tap in [Figure 15](#) must be grounded.

In the circuit in [Figure 16](#), the user is left with the option to ground or float the center tap. The DC voltage that will exist at either IOUTA or IOUTB if the center tap is floating is I<sub>OUTDC</sub> × (R<sub>A</sub>/R<sub>B</sub>) V because R<sub>DIFF</sub> is DC shorted by the transformer. If the center tap is grounded, the DC voltage is 0V. Recommended values for the circuit in [Figure 16](#) are R<sub>A</sub> = R<sub>B</sub> = 50Ω, R<sub>DIFF</sub> = 100Ω, assuming R<sub>LOAD</sub> = 50Ω. The performance of [Figures 15](#) and [16](#) is basically the same, however leaving the center tap of [Figure 16](#) floating allows the circuit to find a more balanced virtual ground, theoretically improving the even order harmonic rejection, but likely reducing the signal swing available due to the output voltage compliance range limitations.

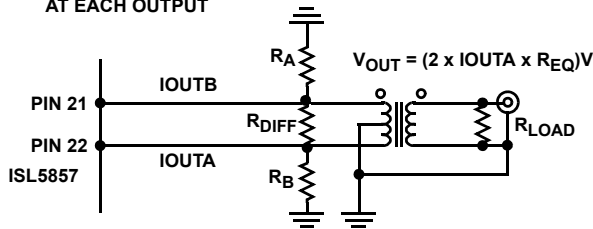
$R_{EQ} = 0.5 \times (R_{LOAD} // R_{DIFF})$   
AT EACH OUTPUT



$R_{LOAD}$  REPRESENTS THE  
LOAD SEEN BY THE TRANSFORMER

FIGURE 15. OUTPUT LOADING FOR DATASHEET MEASUREMENTS

$R_{EQ} = 0.5 \times (R_{LOAD} // R_{DIFF} // R_A)$ , WHERE  $R_A = R_B$   
AT EACH OUTPUT



$R_{LOAD}$  REPRESENTS THE  
LOAD SEEN BY THE TRANSFORMER

FIGURE 16. ALTERNATIVE OUTPUT LOADING

### Propagation Delay

The converter requires two clock rising edges for data to be represented at the output. Each rising edge of the clock captures the present data word and outputs the previous data. The propagation delay is therefore 1/CLK, plus <2ns of processing. See [Figure 17](#).

### Test Service

Intersil offers customer-specific testing of converters with a service called Testdrive. To submit a request, fill out the Testdrive form. The form can be found by doing an 'entire site search' at [www.intersil.com](http://www.intersil.com) on the words 'DAC Testdrive'. Or, send a request to the technical support center.

## Timing Diagram

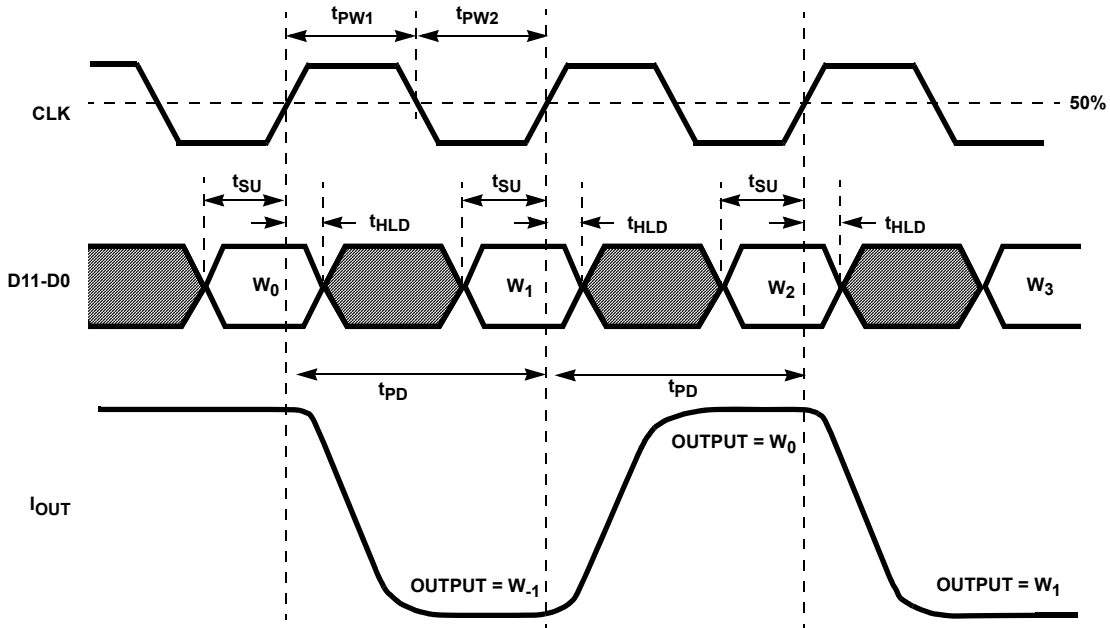


FIGURE 17. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 7, 2015	FN6079.3	Updated Ordering Information on page 3.
May 14, 2015	FN6079.2	<p>Updated entire datasheet applying Intersil's new standards.</p> <p>Moved the Typical Application Circuit to page 1, Pin Configuration to page 2, and Ordering Information Table to page 3.</p> <p>Removed obsolete products from the ordering information table on page 3.</p> <p>Added Notes 2 and 3 to the Ordering Information Table.</p> <p>Added the Part Marking column to the Ordering Information Table.</p> <p>Removed (-2.5dBm) from the following sentence under "Differential Output" on page 10: "With RDIFF = 50Ω and RLOAD = 50Ω, the circuit in Figure 1.3 will provide a 500mV (-2.5dBm) signal at the output of the transformer if the full scale output current of the DAC is set to 20mA (used for the electrical specifications table)."</p> <p>Added Revision History and About Intersil Verbiage</p> <p>Updated POD M28.3 to latest revision.</p> <ul style="list-style-type: none"> <li>-Change made from Rev 0 to Rev 1 was adding land pattern</li> </ul> <p>Updated POD M28.173 to latest revision.</p> <ul style="list-style-type: none"> <li>-Changes made from Rev 0 to Rev 1 was converting to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.</li> </ul>

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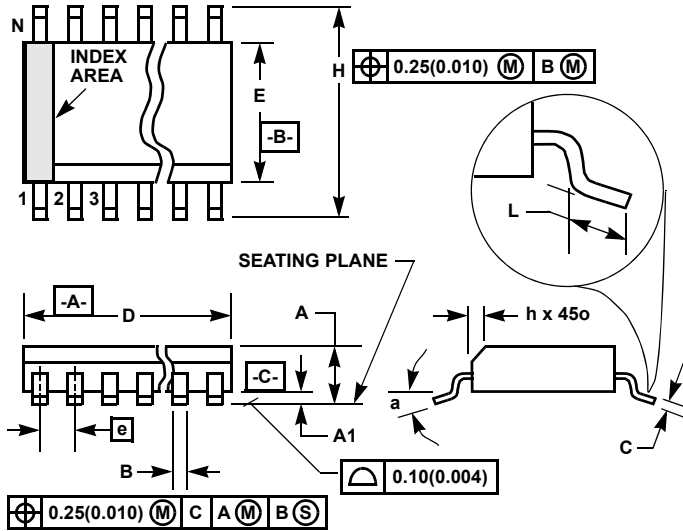
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**Small Outline Plastic Packages (SOIC)**



**M28.3 (JEDEC MS-013-AE ISSUE C)  
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

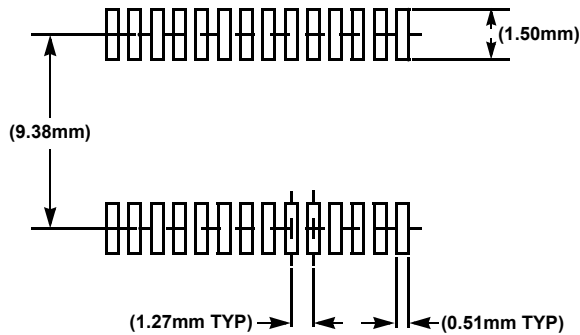
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

Rev. 1, 1/13

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**TYPICAL RECOMMENDED LAND PATTERN**

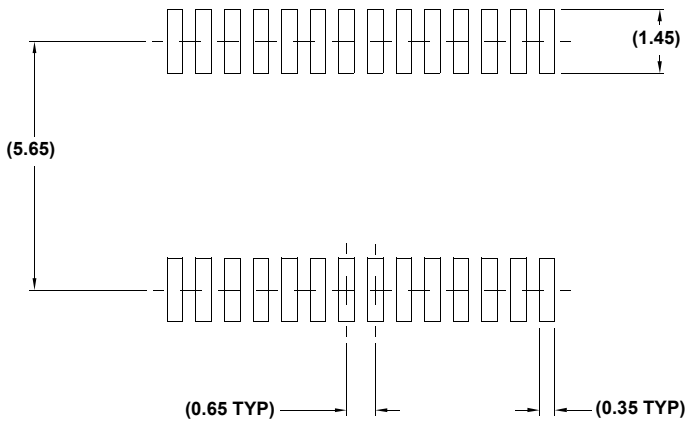
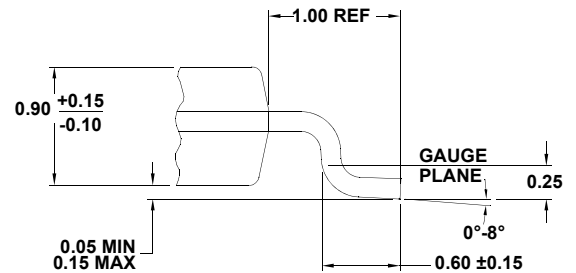
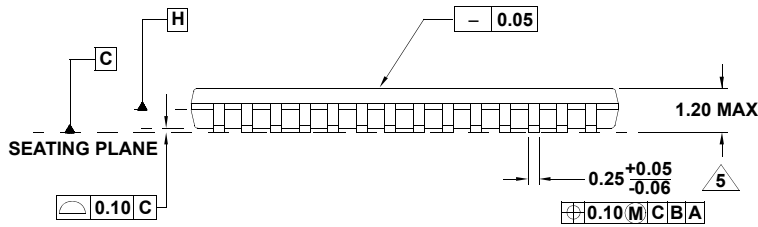
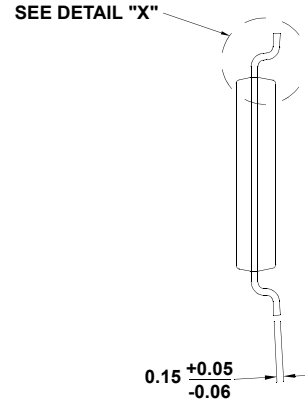
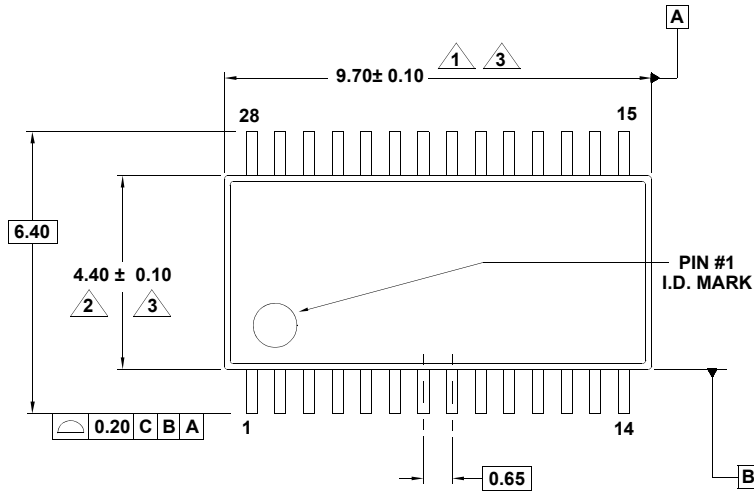


# Package Outline Drawing

## M28.173

28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

Rev 1, 5/10



NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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[MCP48FVB14T-20E/ST](#) [MCP48FEB08T-E/MQ](#) [MCP47FEB08T-E/MQ](#) [MCP48FVB08T-20E/ST](#) [MCP48FEB04T-20E/ST](#) [MCP47FEB04T-](#)  
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