ISL59911

250MHz Triple Differential Receiver/ Equalizer with I2C Interface

FN7548
Rev 0.00
September 2, 2011

The ISL59911 is a triple channel differential receiver and equalizer optimized for RGB and YPbPr video signals. It contains three high speed differential receivers with programmable frequency compensation. The ISL59911 features manual or automatic offset calibration and ±4dB of gain adjustment range with a resolution of 0.1dB.

The ISL59911 has a bandwidth of 250MHz and consumes only 110mA from a ±5V supply in normal operation.

When deasserted, the ENABLE pin puts the amplifiers into a low power, high impedance state, minimizing power when not needed and also allowing multiple devices to be connected in parallel, allowing two or more ISL59911 devices to function as a multiplexer.

The ISL59911 can also directly decode the sync signals encoded onto the common modes of three pairs of Cat 5 cable (by an ISL59311, EL4543, or similar device) or it can output the actual common mode voltages for each of the three channels.

The ISL59911 is available in a 32 Ld QFN package and is specified for operation over the full -40°C to +85°C temperature range.

Features

- 250MHz -3dB bandwidth
- 5 Adjustable EQ bands: 100MHz, 20MHz, 6MHz, 1MHz, and 200kHz
- 3rd-order lowpass filter at output with programmable corner
- ±4dB fine gain control with 0.1dB (7-bit) resolution
- Offset calibration minimizes output offset voltage
- Decodes H_{SYNC} and V_{SYNC} signals embedded in common mode
- I^2C interface with four unique addresses
- ±5V supplies @ 110mA
- 32 Ld 5mm x 6mm QFN package

Applications

- KVM monitor extension
- Digital signage
- General-purpose twisted-pair receiving and equalization
- High-resolution security video

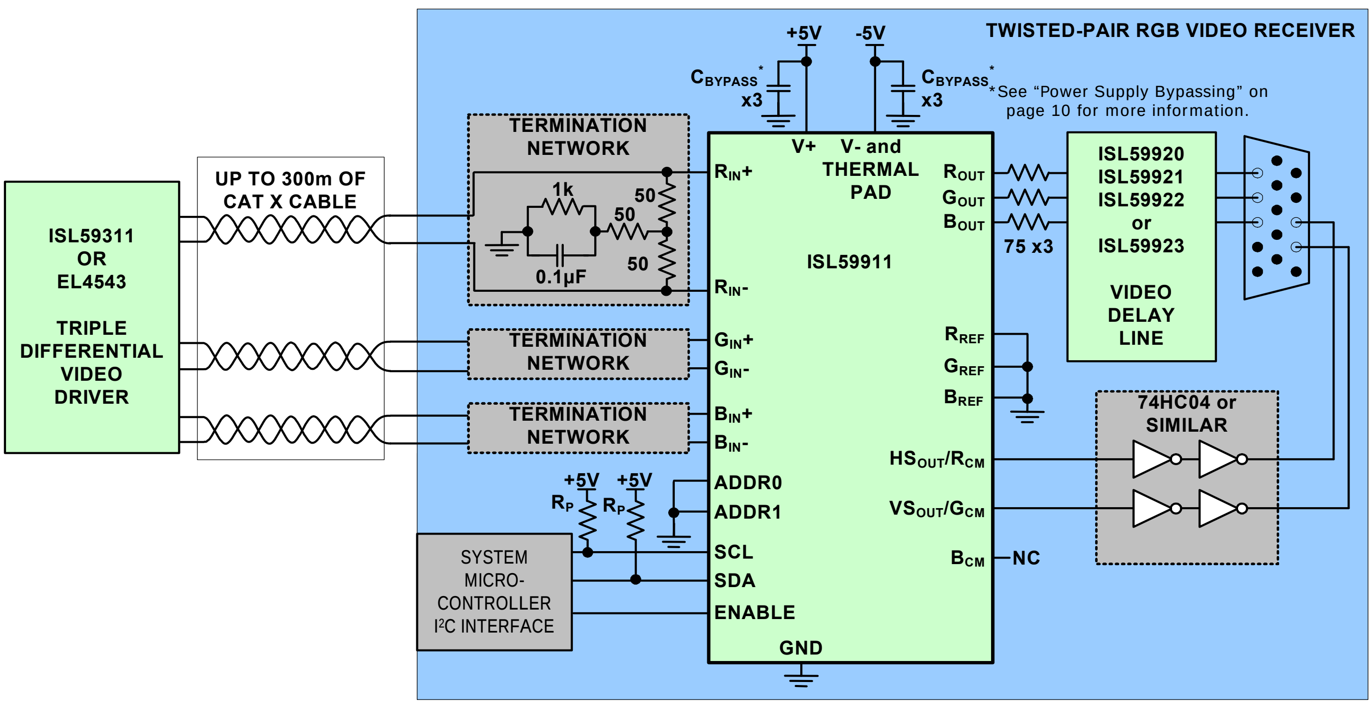
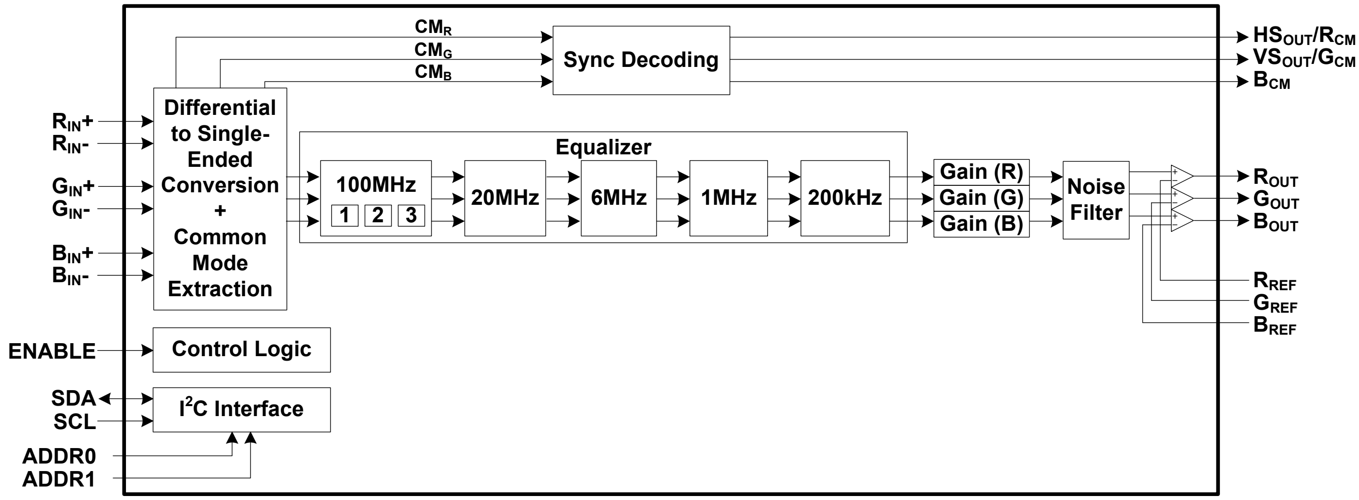


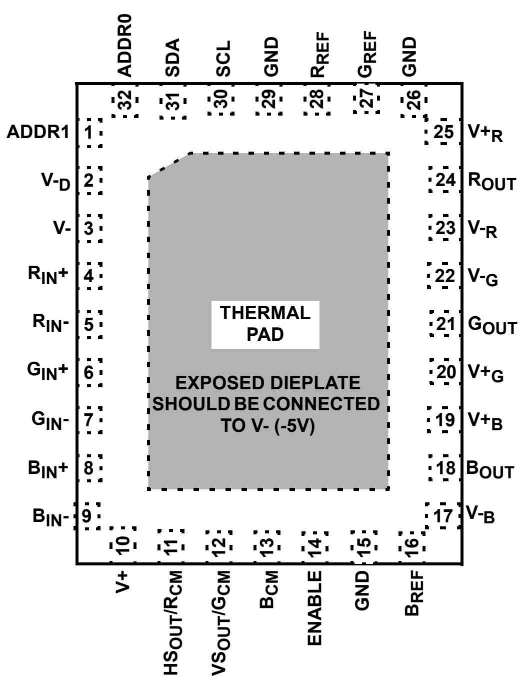
FIGURE 1. TYPICAL APPLICATION CIRCUIT

Block Diagram



Pin Configuration

ISL59911
(32 LD QFN)
TOP VIEW



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL59911IRZ	59911 IRZ	32 Ld QFN	L32.5x6C
ISL59911IRZ-EVALZ	Evaluation Board		

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL59911. For more information on MSL please see techbrief TB363.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	ADDR1	Digital Input. I^2C Address select bit 1, used with ADDR0 to select the ISL59911 I^2C address (see "ISL59911 Serial Communication" on page 13). **Note: If power supply sequencing cannot be guaranteed, ADDR1 must be held low during power-up.** See "Power Supply Sequencing" on page 10 for more information.
2	$V\text{-}_D$	Power Supply Pin. -5V for internal digital logic (internal logic operates between GND and $V\text{-}_D$). Connect to the same -5V supply as V-.
3	V-	Power Supply Pin. -5V supply for analog core of chip, also tied to thermal pad. Connect to a -5V supply.
4	$R_{IN}+$	Analog Input. Red positive differential input
5	$R_{IN}-$	Analog Input. Red negative differential input
6	$G_{IN}+$	Analog Input. Green positive differential input
7	$G_{IN}-$	Analog Input. Green negative differential input
8	$B_{IN}+$	Analog Input. Blue positive differential input
9	$B_{IN}-$	Analog Input. Blue negative differential input
10	V+	Power Supply Pin. +5V supply for analog core of chip. Connect to a +5V supply.
11	HS_{OUT}/R_{CM}	Output configuration (Note 4) = 0: Digital Output. Decoded Horizontal Sync signal Output configuration (Note 4) = 1: Analog Output. Red common-mode voltage at inputs
12	VS_{OUT}/G_{CM}	Output configuration (Note 4) = 0: Digital Output. Decoded Vertical Sync signal Output configuration (Note 4) = 1: Analog Output. Green common-mode voltage at inputs
13	B_{CM}	Output configuration (Note 4) = 0: Digital Output. Logic low Output configuration (Note 4) = 1: Analog Output. Blue common-mode voltage at inputs
14	ENABLE	Digital Input. Chip enable logic signal. 0V: All analog circuitry turned off to reduce current. 5V: Normal operation.
15	GND	Power Supply Pin. Ground reference for ISL59911. This pin must be tied to GND.
16	B_{REF}	Analog Input. Blue channel analog offset reference voltage. Typically tied to GND.
17	$V\text{-}_B$	Power Supply Pin. -5V supply for blue output buffer. Connect to the same -5V supply as V-.
18	B_{OUT}	Analog Output. Blue output voltage referenced to B_{REF} pin.
19	$V+_B$	Power Supply Pin. +5V supply for blue output buffer. Connect to the same +5V supply as V+.
20	$V+_G$	Power Supply Pin. +5V supply for green output buffer. Connect to the same +5V supply as V+.
21	G_{OUT}	Analog Output. Green output voltage referenced to G_{REF} pin.
22	$V\text{-}_G$	Power Supply Pin. -5V supply for green output buffer. Connect to the same -5V supply as V-.
23	$V\text{-}_R$	Power Supply Pin. -5V supply for red output buffer. Connect to the same -5V supply as V-.
24	R_{OUT}	Analog Output. Red output voltage referenced to R_{REF} pin.
25	$V+_R$	Power Supply Pin. +5V supply for red output buffer. Connect to the same +5V supply as V+.
26	GND	Power Supply Pin. Ground reference for ISL59911.
27	G_{REF}	Analog Input. Green channel analog offset reference voltage. Typically tied to GND.
28	R_{REF}	Analog Input. Red channel analog offset reference voltage. Typically tied to GND.
29	GND	Power Supply Pin. Ground reference for ISL59911. This pin must be tied to GND.
30	SCL	Digital Input. I^2C Clock Input
31	SDA	Digital Input/Open-Drain Digital Output. I^2C Data Input/Output
32	ADDR0	Digital Input. I^2C Address select bit 0, used with ADDR1 to select the ISL59911 I^2C address.
Thermal Pad	Thermal Pad	Power Supply Pin. Connect to -5V supply plane with multiple vias to reduce thermal resistance and more effectively spread heat from the ISL59911 to the PCB.

NOTE:

4. Output Configuration is controlled via Configuration Register 0x01, bit 0.

Absolute Maximum Ratings (T_A = +25°C)

$V+ = V+_R = V+_G = V+_B$, $V- = V-_R = V-_G = V-_B = V-_D$
Supply Voltage between V+ and V- 12V
Maximum Absolute Slew Rate of V+ and V- . . . . . ±1V/µs
Maximum Continuous Output Current per Channel . . . . . ±30mA
Power Dissipation . . . . . See "Power Dissipation" on page 12
Pin Voltages . . . . . V- - 0.5V to V+ + 0.5V
ESD Ratings
Human Body Model (tested per JESD22-A114) 7000V
Machine Model (Tested per JESD22-A115) 300V
Charged Device Model (Tested per JESD22C101C) 2000V
Latch Up (Tested per JESD78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN (Notes 5, 6)	31	2.1

Storage Temperature . . . . . -65°C to +150°C
Die Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
V+ Supply Range . . . . . 4.5V to 5.5V
V- Supply Range . . . . . -4.5V to -5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V+ = V+_R = V+_G = V+_B = +5V$, $V- = V-_R = V-_G = V-_B = V-_D = -5V$, T_A = +25°C, all registers at default settings (equalizer stages set to minimum boost, noise filter set to max bandwidth, x2 gain mode, $GAIN_{DC}$ = 0dB), all analog inputs at 0V, auto offset calibration executed, R_L = 5pF || (75Ω + 75Ω) to GND, thermal pad connected to -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
POWER SUPPLY						
Positive Supply Voltage (V+)	$V+ = V+_R = V+_G = V+_B$		4.5		5.5	V
Negative Supply Voltage (V-)	$V- = V-_R = V-_G = V-_B = V-_D$		-4.5		-5.5	V
Operating Current (I_D+)	Sum of currents into all V+ pins			110	140	mA
Operating Current (I_D-)	Sum of currents out of all V- pins, including thermal pad			105	130	mA
Disabled Current ($I_D+_{DISABLED}$)	Sum of currents into all V+ pins	ENABLE = 0V		2.5	3.5	mA
Disabled Current ($I_D-_{DISABLED}$)	Sum of currents into all V- pins, including thermal pad	ENABLE = 0V		0.35	2.5	mA
$PSRR_{DC}$	Power Supply Rejection Ratio			55		dB
AC PERFORMANCE						
BW	Full Power Bandwidth			250		MHz
$GAIN_{100MHz}$	Maximum Boost @ 100MHz	All three 100MHz filters set to maximum		26		dB
$GAIN_{20MHz}$	Maximum Boost @ 20MHz	20MHz filter set to maximum		9.5		dB
$GAIN_{6MHz}$	Maximum Boost @ 6MHz	6MHz filter set to maximum		7.5		dB
$GAIN_{1MHz}$	Maximum Boost @ 1MHz	1MHz filter set to maximum		3.1		dB
$GAIN_{0.2MHz}$	Maximum Boost @ 200kHz	200kHz filter set to maximum		0.75		dB
$GAIN_{DC}$	DC Gain Adjustment Range			±4		dB
f_{NOISE_MIN}	-3dB Corner Freq of Noise Filter, High	Noise Filter Register = 0x0		250		MHz
f_{NOISE_MAX}	-3dB Corner Freq of Noise Filter, Low	Noise Filter Register = 0xF		50		MHz
SR_{DIFF}	Output Slew Rate	V_{IN} = -1V to +1V		1		V/ns
THD	Total Harmonic Distortion	f = 10MHz, 0.7V_{P-P} input sine wave	-45	-60		dBc

Electrical Specifications $V+ = V+_R = V+_G = V+_B = +5V$, $V- = V-_R = V-_G = V-_B = V-_D = -5V$, $T_A = +25°C$, all registers at default settings (equalizer stages set to minimum boost, noise filter set to max bandwidth, x2 gain mode, $GAIN_{DC}$ = 0dB), all analog inputs at 0V, auto offset calibration executed, R_L = 5pF || (75Ω + 75Ω) to GND, thermal pad connected to -5V, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
BW_{CM}	Common Mode Amplifier Bandwidth	10k || 5pF load		24		MHz
SR_{CM}	Common Mode Slew Rate	V_{IN} = -0.5V to +1.5V		0.1		V/ns
INPUT CHARACTERISTICS						
CMIR	Common-mode Input Range	Differential signal passed undistorted. Effective headroom is reduced by the p-p amplitude of differential swing divided by 2.		-3.2/+4.0		V
CMRR	Common-mode Rejection Ratio	Measured at 100kHz		88		dB
		Measured at 10MHz		58		dB
C_{INDIFF}	Differential Input Capacitance	Capacitance between V_{INP} and V_{INM}		0.5		pF
R_{INDIFF}	Differential Input Resistance	Resistance between V_{IN}+ and V_{IN}- (due to common mode input resistance)		20		kΩ
C_{INCM}	CM Input Capacitance	Capacitance from V_{IN}+ and V_{IN}- to GND		1.3		pF
R_{INCM}	CM Input Resistance	Resistance from V_{IN}+ and V_{IN}- to GND		25		kΩ
V_{INDIFF_P-P}	Max P-P Differential Input Range	Delta V_{IN}+ - V_{IN}- when slope gain falls to 0.9	1.9			V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Voltage Swing			±2.75		V
I_{OUT}	Output Drive Current	R_L = 10Ω, V_{IN}+ - V_{IN}- = ±2V		±22		mA
$V(V_{OUT})_{OS}$	Output Offset Voltage	Post-offset calibration	-20	-8	+5	mV
$R(V_{CM})$	CM Output Resistance of VCM_R/G/B (CM Output Mode)	At 100kHz		2.5		Ω
Gain	Gain	x1 mode x2 mode	0.95 1.9	1.0 2.0	1.05 2.1	V/V
ΔGain	Channel-to-Channel Gain Mismatch	x1 and x2 modes			±3	%
O_{NOISE}	Integrated Noise at Output Inputs @ GND through 50Ω.	0m of Equalization (Nominal) 300m of Equalization		4 20		mV_{RMS}
$SYNCOUT_{HI}$	High Level output on VS/HS_{OUT}	10k || 5pF load, SYNC Output Mode	V+ - 1.5			V
$SYNCOUT_{LO}$	Low Level output on VS/HS_{OUT}	10k || 5pF load, SYNC Output Mode			0.4	V
SCL, SDA PINS						
f_{MAX}	Maximum I^2C Operating Frequency		400			kHz
V_{OL}	SDA Output Low Level	V_{SINK} = 6mA			0.4	V
V_{IH}	Input High Level		3			V
V_{IL}	Input Low Level				1.5	V
V_{HYST}	Input Hysteresis			0.55		V
$I_{LEAKAGE}$	Input Leakage Current				±1	µA
t_{GLITCH}	Maximum Width of Glitch on SCL (or SDA) Guaranteed to be Rejected		50			ns
ENABLE, ADDR0, ADDR1 PINS						
V_{IH}	Input High Level		3			V
V_{IL}	Input Low Level				0.8	V
$I_{LEAKAGE}$	Input Leakage Current				±1	µA

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

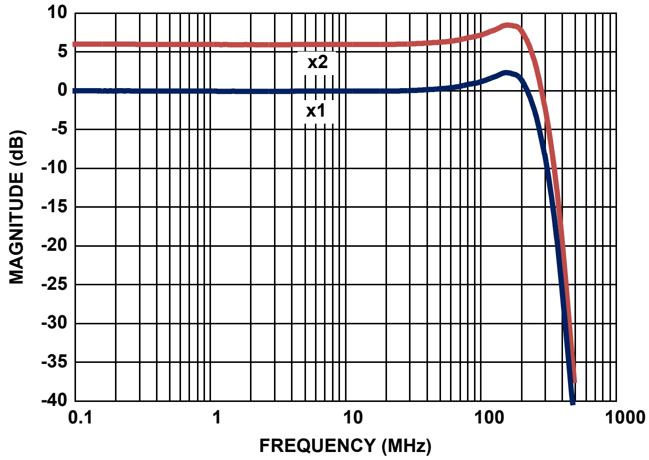


FIGURE 2. NOMINAL FREQUENCY RESPONSE WITH DEFAULT SETTINGS

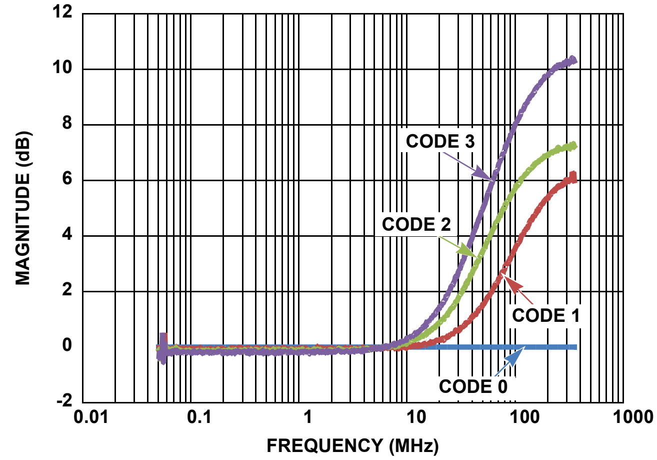


FIGURE 3. FREQUENCY RESPONSE vs 100MHz BITS 1:0

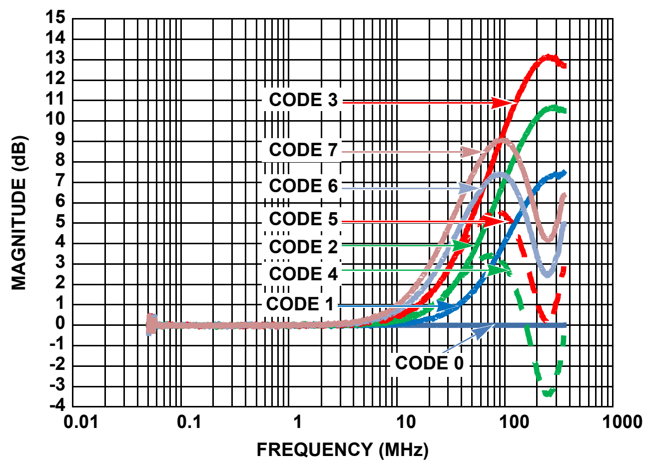


FIGURE 4. FREQUENCY RESPONSE vs 100MHz BITS 4:2

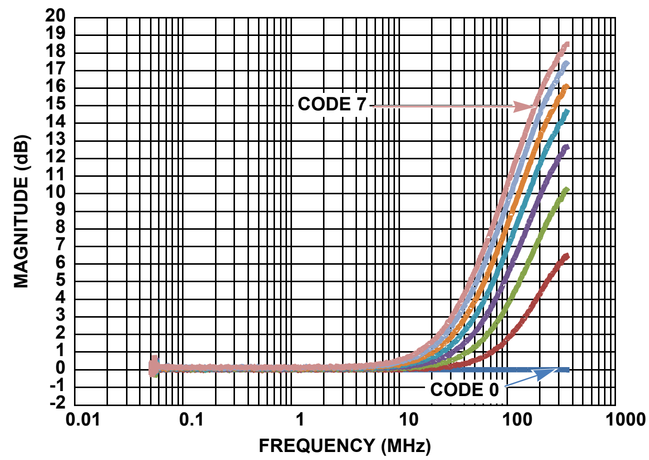


FIGURE 5. FREQUENCY RESPONSE vs 100MHz BITS 7:5

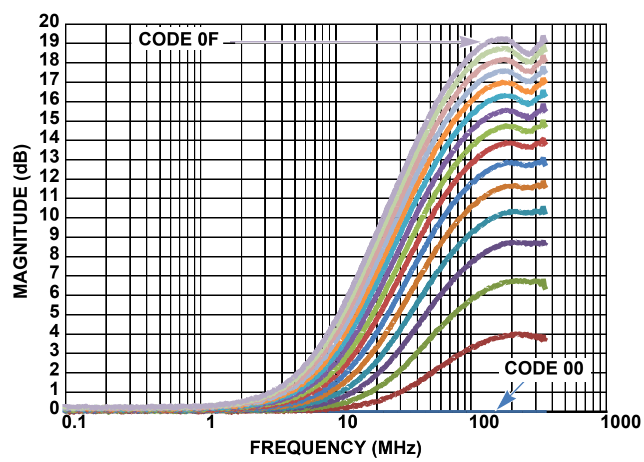


FIGURE 6. FREQUENCY RESPONSE vs 20MHz BITS 7:4

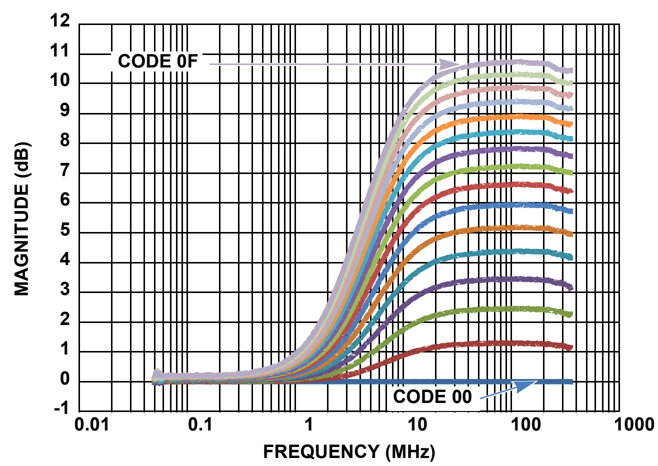


FIGURE 7. FREQUENCY RESPONSE vs 6MHz BITS 3:0

Typical Performance Curves (Continued)

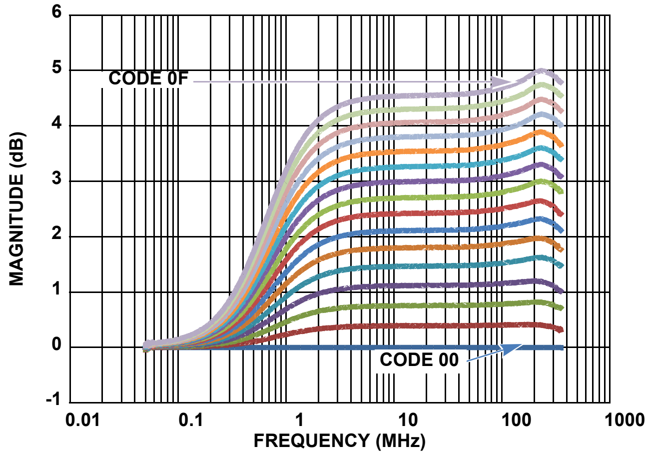


FIGURE 8. FREQUENCY RESPONSE vs 1MHz BITS 7:4

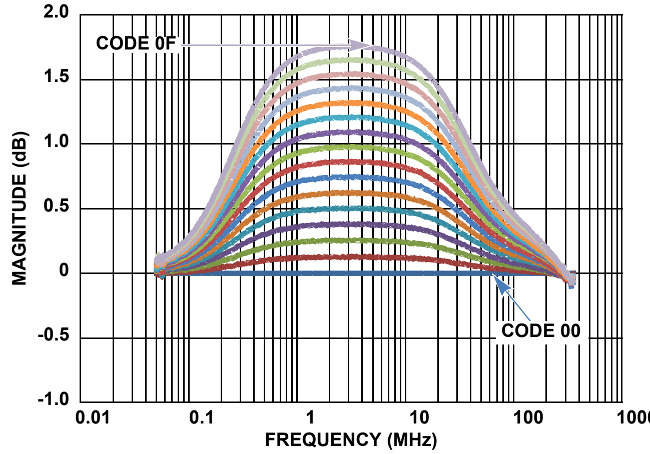


FIGURE 9. FREQUENCY RESPONSE vs 200kHz BITS 3:0

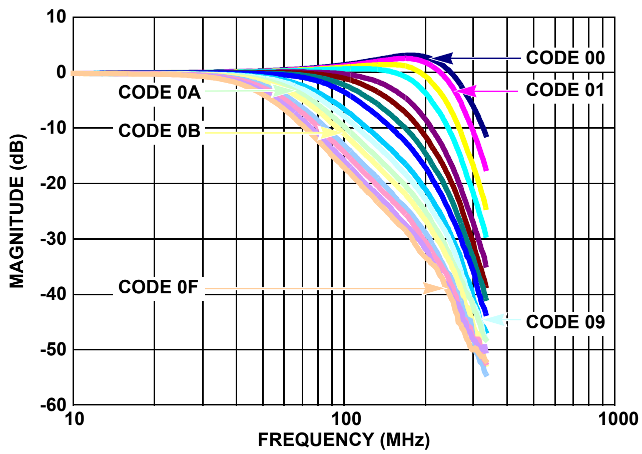


FIGURE 10. FREQUENCY RESPONSE vs LOW PASS FILTER BITS 3:0

Register Listing

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Device ID (read only)	3:0	Device Revision	0 = initial silicon, 1 = first revision, etc.
		7:4	Device ID	0x10 = ISL59911
0x01	General Configuration (0x02)	0	Output Configuration	0: H_{SYNC} + V_{SYNC} (like EL9111 and ISL59910) 1: V_{CM} (like EL9112 and ISL59913)
		1	Nominal Gain	0: 0dB (1V/V) 1: 6dB (2V/V)
		2	Power Down	0: Normal Operation 1: Low power mode, all amplifiers turned off
0x02	High Adjust (0x00)	1:0	100MHz Stage 1	00b: Min boost 11b: Max boost
		4:2	100MHz Stage 2	000b: Min boost 111b: Max boost
		7:5	100MHz Stage 3	000b: Min boost 111b: Max boost
0x03	Mid Adjust (0x00)	3:0	6MHz	0000b: Min boost 1111b: Max boost
		7:4	20MHz	0000b: Min boost 1111b: Max boost
0x04	Low Adjust (0x00)	3:0	200kHz	0000b: Min boost 1111b: Max boost
		7:4	1MHz	0000b: Min boost 1111b: Max boost
0x05	Noise Filter Adjust (0x00)	3:0	Noise Filter	Adjusts -3dB frequency of noise filter at output 0x0: Max frequency 0xF: Min frequency
0x06	Red Channel Gain (0x40)	6:0	Red Gain	0x00: -6dB 0x40: 0dB 0x7F: +6dB Note: Due to gain trim at production test, the minimum guaranteed usable gain range is ±4dB.
0x07	Green Channel Gain (0x40)	6:0	Green Gain	0x00: -6dB 0x40: 0dB 0x7F: +6dB Note: Due to gain trim at production test, the minimum guaranteed usable gain range is ±4dB.
0x08	Blue Channel Gain (0x40)	6:0	Blue Gain	0x00: -6dB 0x40: 0dB 0x7F: +6dB Note: Due to gain trim at production test, the minimum guaranteed usable gain range is ±4dB.
0x09	Red Channel Manual Offset (0x00) (Default is auto-calibrated)	6:0	Red Offset	0x00: -400mV Offset 0x7F: +400mV Offset (Output Referred)
		7	Manual Offset Control (Red)	0: Offset is auto calibrated - value in bits 6:0 is ignored 1: Offset DAC set to value in bits 6:0
0x0A	Green Channel Manual Offset (0x00) (Default is auto-calibrated)	6:0	Green Offset	0x00: -400mV Offset 0x7F: +400mV Offset (Output Referred)
		7	Manual Offset Control (Green)	0: Offset is auto calibrated - value in bits 6:0 is ignored 1: Offset DAC set to value in bits 6:0

Register Listing (Continued)

ADDRESS	REGISTER (DEFAULT VALUE)	BIT(S)	FUNCTION NAME	DESCRIPTION
0x0B	Blue Channel Manual Offset (0x00) (Default is auto-calibrated)	6:0	Blue Offset	0x00: -400mV Offset 0x7F: +400mV Offset (Output Referred)
		7	Manual Offset Control (Blue)	0: Offset is auto calibrated - value in bits 6:0 is ignored 1: Offset DAC set to value in bits 6:0
0x0C	Offset Calibration Control (0x00)	0	Start Cal	Set to 1 to initiate offset calibration. Bit is reset to 0 when calibration is complete (in ~3µs or less).
		1	Cal Mode	0: Analog inputs disconnected from external pins and internally shorted together during calibration. 1: Analog inputs remain connected to external circuitry during calibration. Useful for calibrating out system-wide offsets. External offsets of up to ~±160mV can be eliminated.
		2	Short Inputs	0: Normal operation 1: Inputs shorted together (independent of the Cal Mode bit)
0x0D - 0x12	Reserved	7:0	Reserved	Reserved. Do not write anything to these addresses.
0x13	Initialization	7:0	Initialization	After initial power on, write 0x06 to this register, followed by a write of 0x00 to this register.

NOTE: All registers are read/write unless otherwise noted.

Applications Information

ISL59911 Overview

Differential video signals sent over long distances of twisted pair wire encounter are increasingly attenuated as frequency and distance increase, resulting in loss of high frequency detail (blurring). The exact loss characteristic is a function of the wire gauge, whether the pairs are shielded or unshielded, the dielectric of the insulation, and the length of the wire. The loss mechanism is primarily skin effect.

The signal can be restored by applying a filter with the inverse transfer function of the cable to the far end signal. The ISL59911 is designed to compensate for losses due to long cables, and incorporates the functionality and flexibility to match a wide variety of loss characteristics.

Power Supply Sequencing

Power to the ISL59911's negative supply pins should be applied before the positive supply ramps. As shown in Figure 11, V- should reach -3V before V+ reaches 1V.

If this power supply sequence cannot be guaranteed, then the ADDR1 pin must be held low during power-up until V- has crossed -3V.

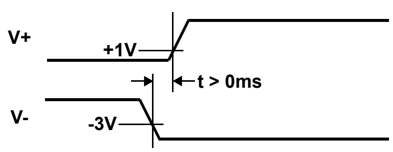


FIGURE 11. POWER SUPPLY SEQUENCING

If this power supply sequencing requirement is not met *and* if ADDR1 is high, there is a small chance that the ISL59911 factory trim will become permanently corrupted.

Power Supply Bypassing

For best performance, all ICs need bypass capacitors across some or all of their power supply pins. The best high-frequency decoupling is achieved with a 0.1µF capacitor between each power supply pin and GND. Adjacent supply pins (pins 2 and 3, 19 and 20, 22 and 23, and 25 and 26) can share the same decoupling capacitor. Keep the path to both pins as short as possible to minimize inductance and resistance. Pins 3 and 10 provide power to the internal equalizer, while supply pins between pin 17 and pin 25 provide power to the analog output buffers. For best performance, the equalizer supplies should be somewhat isolated from the buffer supplies. A separate path back to the power source should be adequate.

A 10µF capacitor on each of the V+ and V- supplies provides sufficient low-frequency decoupling. The 10µF capacitors do not need to be particularly close to the ISL59911 to be effective, but should still have a low-impedance path to the supply rails.

In many mixed-signal ICs, separation of the analog and digital supplies and grounds is critical to prevent digital noise from appearing on the analog signals. Because the digital logic in the ISL59911 is only active during a one-time configuration, the analog and digital supply pins (and grounds) can be connected together, simplifying PCB layout and routing.

Input Termination

The differential input signal from a Cat x cable should have a characteristic impedance of 100Ω and is therefore terminated by the two 50Ω resistors across the differential inputs, as shown in Figure 1 on page 1. The 50Ω resistor and 0.1µF capacitor connected to the midpoint keep the AC impedance low at high frequencies, providing common-mode AC termination while allowing the low-frequency component of the common mode (containing the embedded H and V sync signals) to move freely. The 1k resistor provides a higher-impedance DC path to ground, so the common mode voltage is set to 0V when no cable is connected.

Device Initialization

To ensure that the ISL59911 functions properly, the following steps must be taken after initial power-up:

1. Ensure that the ENABLE pin is high.
2. Through the serial interface, write 0x06 to register 0x13, then write 0x00 to the same register. This ensures that the DC gain of the device is accurate.
3. Perform an offset calibration by setting bit 0 of register 0x0C to 1. The bit is automatically resets to 0 upon completion of calibration. If offset calibration is not performed, the ISL59911 may have large DC offsets.

Communicating with the ISL59911

The ISL59911 is controlled through the industry standard I^2C serial interface. Adjustments to the frequency response over five distinct frequency bands, gain and offset fine-tuning, and several other functions are made through this interface as described in the Register Listing starting on page 8. This level of control enables much more accurate and flexible response matching than previous solutions.

The ISL59911 also has an external Chip Enable (ENABLE) pin, allowing hardware control of whether the chip is operating or in a low-power standby mode.

Programming the ISL59911 for a Specific Cable and Length

Determining the optimum settings for the ISL59911's multiple equalizer frequencies, gain, and low pass filter can initially seem quite challenging. To equalize any cable type of any length, transmit a step (a pure white screen works well, since the video in H_{SYNC} region is black) and adjust the filters, starting at 200kHz and working up to 100MHz, so that the response at the receive end is as flat as possible. Once the response is flat, the gain should be adjusted as necessary to compensate for the DC losses.

This technique is not usually practical in the field, where the best solution is a lookup table for each cable type. Table 1 shows the best values for a typical Cat 5 cable.

TABLE 1. Cat 5 LOOK-UP TABLE

Length (m)	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6-8
0	0x00	0x00	0x00	0x00	0x40
25	0x20	0x11	0x10	0x00	0x40
50	0x24	0x22	0x21	0x01	0x44
75	0x25	0x33	0x31	0x01	0x44
100	0x49	0x44	0x42	0x01	0x48
125	0x69	0x55	0x53	0x02	0x48
150	0x89	0x75	0x62	0x02	0x4C
175	0x92	0x86	0x72	0x04	0x4C
200	0x96	0x96	0x82	0x06	0x50
225	0x97	0xA7	0x93	0x08	0x50
250	0xB7	0xB8	0xB2	0x09	0x54
275	0xD7	0xC9	0xC3	0x0A	0x54
300	0xF7	0xEA	0xD2	0x0C	0x58

Offset Calibration

Historically, programmable video equalizer ICs have had large and varying offset voltages, often requiring external circuitry and/or manual trim to reduce the offset to acceptable levels. The ISL59911 improves upon this by adding an offset calibration circuit that, when triggered by setting bit 0 of I^2C register 0x0C, shorts the inputs together internally, compares the R_{OUT}, G_{OUT}, and B_{OUT} voltages to their corresponding R_{REF}, G_{REF}, and B_{REF} voltages and uses a DAC with a successive-approximation technique to minimize the delta between them (see Figure 12).

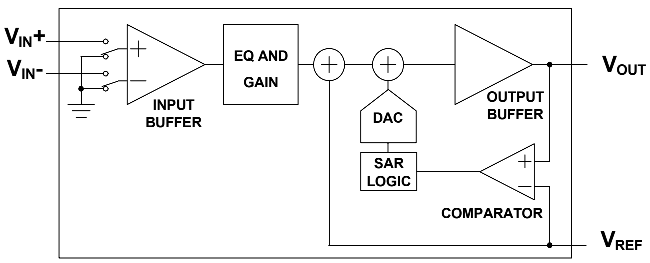


FIGURE 12. OFFSET CALIBRATION (ONE CHANNEL SHOWN)

When the ISL59911 is first powered up, the offset error is undefined until an offset calibration is performed. The output offset voltage of the ISL59911 also varies as the filter and gain settings are adjusted. To minimize offset, always perform an offset calibration after finalizing the filter and gain settings.

An offset calibration only takes about 3µs, so offset calibrations can be performed after *every* register write without adding significant time to the adjustment process. This minimizes offset throughout the entire equalization adjustment procedure.

Output Signals

The R_{OUT}, G_{OUT}, and B_{OUT} outputs can drive either a standard 75Ω video load in x1 gain mode or a 150Ω source-terminated load (75Ω in series at source end [ISL59911 output pin], plus 75Ω termination to ground at receive end) in x2 mode. If the output of the ISL59911 is going directly into an ISL59920 or similar delay line, termination to ground is not necessary, however, a ~75Ω series resistor at each output pin will help isolate the outputs from the PCB trace capacitance, improving the flatness of the frequency response.

When ENABLE is low, the R_{OUT}, G_{OUT}, and B_{OUT} outputs are put in a high-impedance state, allowing multiple ISL59911 devices to be configured as a multiplexer by paralleling their outputs and using ENABLE to select the active RGB channel.

Common Mode and H_{SYNC}/V_{SYNC} Outputs

In addition to the incoming differential video signals, the ISL59911 also processes the common mode voltage on the differential inputs and can output the signal in one of two ways (as determined by the Output Configuration bit in register 0x01).

When the Output Configuration bit is set to 0 (the default), the common mode input voltages are sent to comparators that decode the voltage into H_{SYNC} and V_{SYNC} signals according to the EL4543/ISL59311 standard encoding scheme shown in Figure 13 and in Table 2 on page 11. The H_{SYNC} signal appears on the HS_{OUT}/R_{CM} pin, the V_{SYNC} signal on VS_{OUT}/G_{CM}. The B_{CM} output pin is held at a logic low (0v).

To minimize noise coupling into the analog section from the sync output drivers, the HS_{OUT} and VS_{OUT} outputs have limited current drive, and should be buffered by 74HC04 or similar CMOS buffers, as shown in Figure 1, before driving any significant loads (such as a VGA cable).

When the Output Configuration bit is set to 1, buffered versions of the three common mode input voltages are available on the R_{CM}, G_{CM}, and B_{CM} pins. Making the raw common mode signal available allows for custom encoding schemes and/or transmission of analog signals on the video signals' common mode.

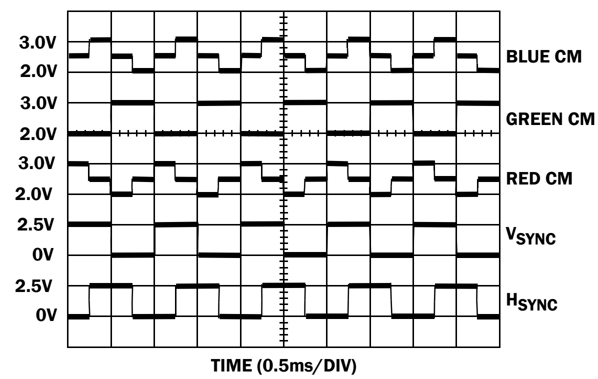


FIGURE 13. H AND V SYNC SIGNAL ENCODING

TABLE 2. H AND V SYNC DECODING

RED CM	GREEN CM	BLUE CM	H_{SYNC}	V_{SYNC}
2.5V	3.0V	2.0V	Low	Low
3.0V	2.0V	2.5V	Low	High
2.0V	3.0V	2.5V	High	Low
2.5V	2.0V	3.0V	High	High

Power Dissipation

The ISL59911 is designed to operate with ±5V supply voltages. The supply currents are tested in production and guaranteed to be less than 140mA per channel. Operating at ±5V power supply, the total power dissipation is shown by Equation 1:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + 3(V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 1)}$$

Where:

- PD_{MAX} = Maximum power dissipation
- V_S = Supply voltage = 5V
- I_{MAX} = Maximum quiescent supply current = 140mA
- V_{OUTMAX} = Maximum output voltage swing of the application = 2V
- The 3 term comes from the number of channels
- R_L = Load resistance = 150Ω
- PD_{MAX} = 1.4W

θ_{JA} required for long term reliable operation can be calculated. This is done using Equation 2:

$$\theta_{JA} = (T_J - T_A)/PD = (46°C)/W \quad \text{(EQ. 2)}$$

Where:

T_J is the maximum junction temperature (+150°C)

T_A is the maximum ambient temperature (+85°C)

For a 32 Ld QFN package in a proper layout PCB heatsinking copper area, 31°C/W θ_{JA} thermal resistance can be achieved. To disperse the heat, the bottom heatspreader must be soldered to the PCB. Heat flows through the heatspreader to the circuit board copper, then spreads and converts to air. Thus the PCB copper plane becomes the heatsink. This has proven to be a very effective technique. A separate application note that details the 32 pin QFN PCB design considerations is available.

ISL59911 Serial Communication

Overview

The ISL59911 uses the I^2C serial bus protocol for communication with its host (master). SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

1. The host selects the ISL59911 it wishes to communicate with.
2. The host writes the initial ISL59911 Configuration Register address it wishes to write to or read from.
3. The host writes to or reads from the ISL59911s Configuration Register. The ISL59911s internal address pointer auto increments, so to read registers 0x00 through 0x1B, for example, one would write 0x00 in step 2, then repeat step three 28 times, with each read returning the next register value.

The ISL59911 has a 7-bit address on the serial bus, 10001<a1><a0>b, where 10001 is fixed and a0 and a1 are the state of the ADDR0 and ADDR1 pins, respectively. This allows up to four ISL59911 devices to be independently controlled by the same serial bus.

To control more than four devices (or more than two, if ADDR1 is tied low as discussed in “Power Supply Sequencing” on page 10) from a single I^2C host, use a “chip select” signal for each device. For example, in the firmware, the host can fix the I^2C address to 1000101b for all devices, selecting the device to be communicated to by taking its ADDR0 pin high while the ADDR0 pins of all other devices remain low. The selected device recognizes its current address (1000101b) and respond normally, while the remaining devices will have an address of 1000100b and therefore ignore the communication. This requires one additional GPIO for each ISL59911, but it permits as many ISL59111 devices to be controlled as desired, without any additional external logic.

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 14). The ISL59911 continuously monitors the SDA and SCL lines for the start condition and does not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a $R/\overline{W}$ bit, indicating if the next transaction is a Read ($R/\overline{W}$ = 1) or a Write ($R/\overline{W}$ = 0). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 15).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 14), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

The I^2C spec requires that data on the serial bus must be valid for the entire time SCL is high (Figure 16). To ensure incoming data has settled, data written to the ISL59911 is latched on a delayed version of the rising edge of SCL.

When the contents of the ISL59911 are being read, the SDA line is updated after the falling edge of SCL, delayed and deglitched in the same manner.

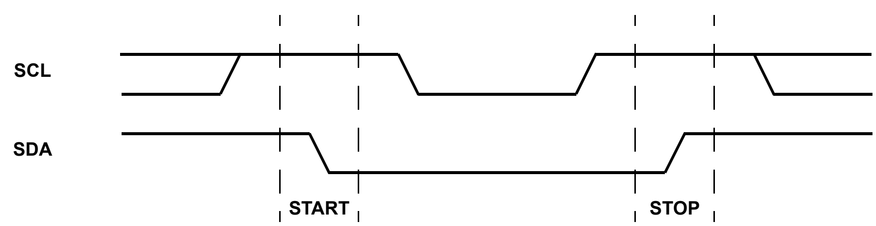


FIGURE 14. VALID START AND STOP CONDITIONS

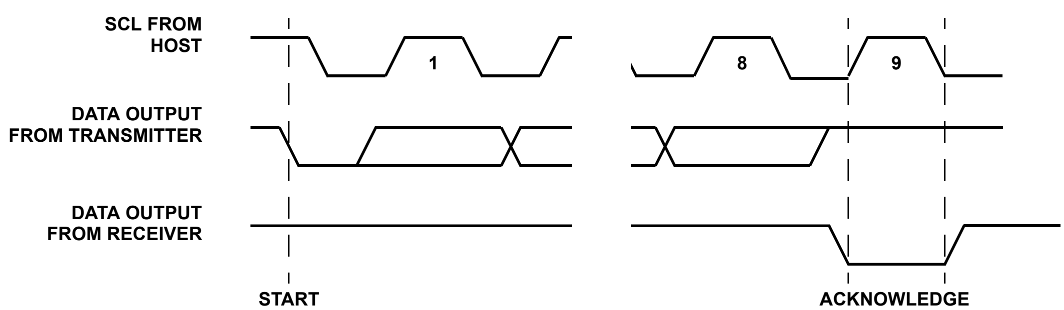


FIGURE 15. ACKNOWLEDGE RESPONSE FROM RECEIVER

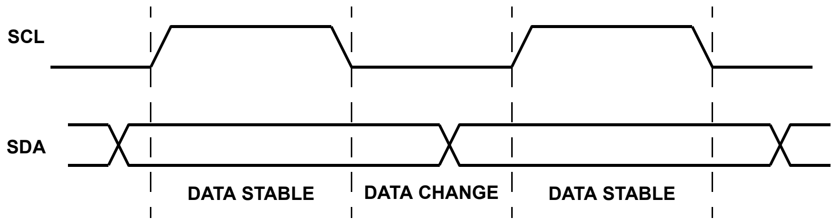


FIGURE 16. VALID DATA CHANGES ON THE SDA BUS

Configuration Register Write

Figure 17 shows two views of the steps necessary to write one or more words to the Configuration Register.

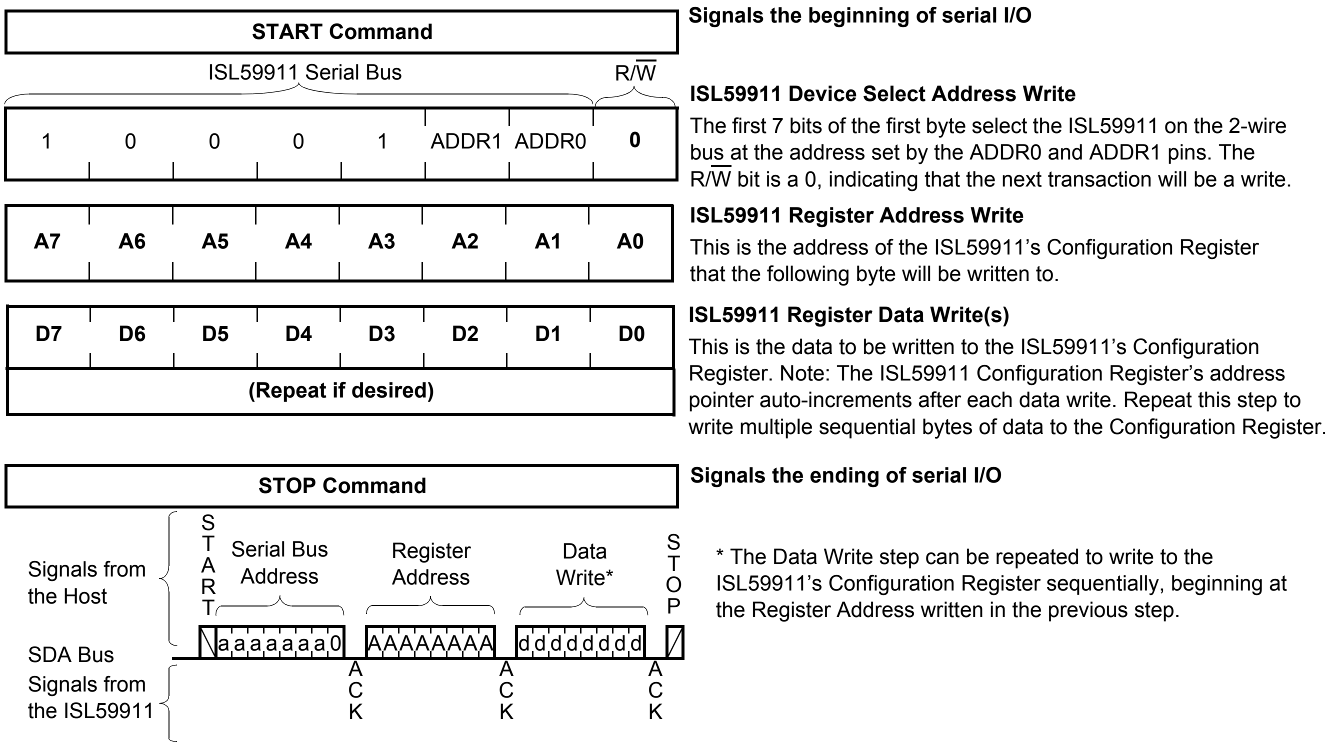


FIGURE 17. CONFIGURATION REGISTER WRITE

Configuration Register Read

Figure 18 shows two views of the steps necessary to read one or more words from the Configuration Register.

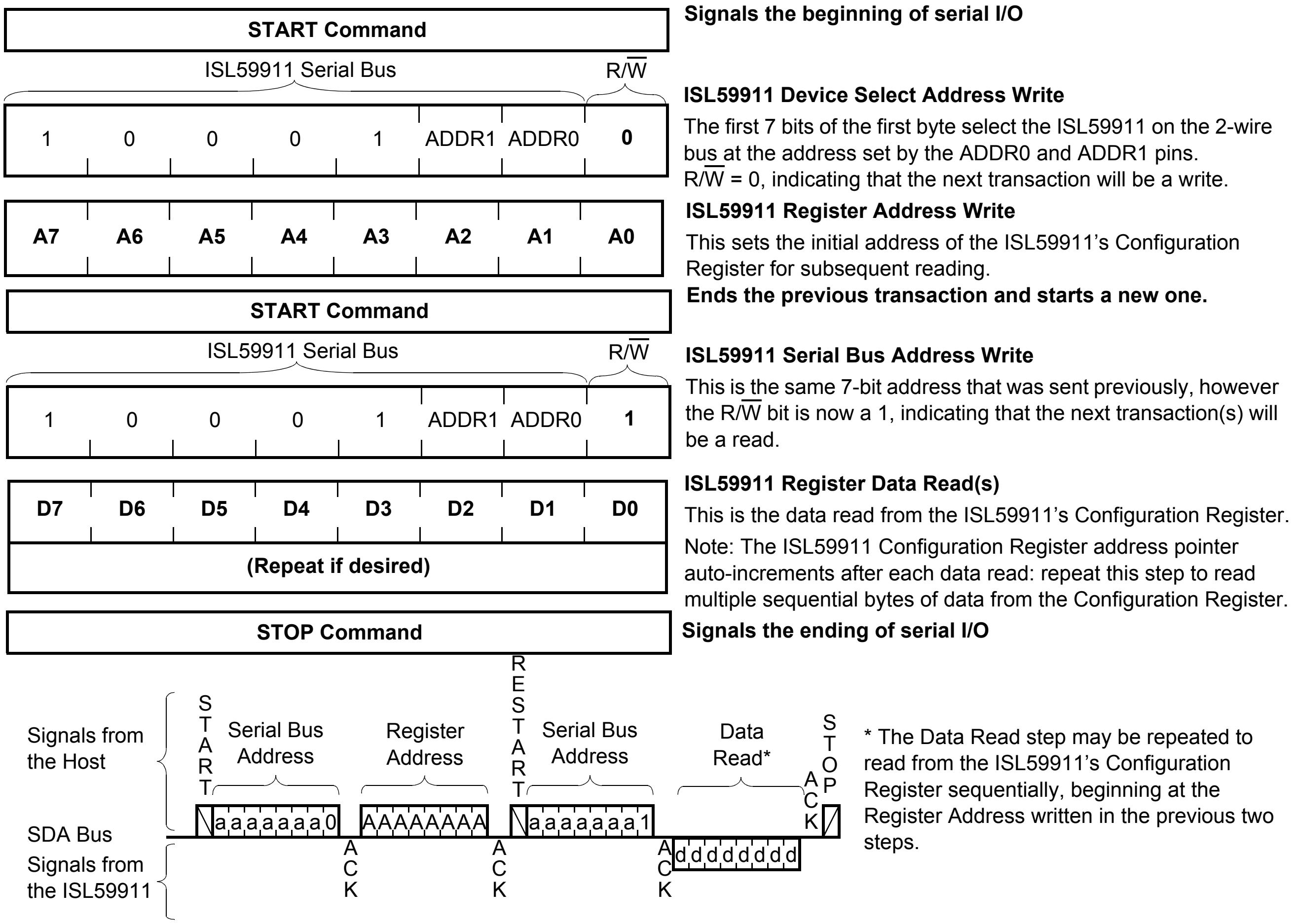


FIGURE 18. CONFIGURATION REGISTER READ

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
9/2/11	FN7548.0	Initial Release.

Products

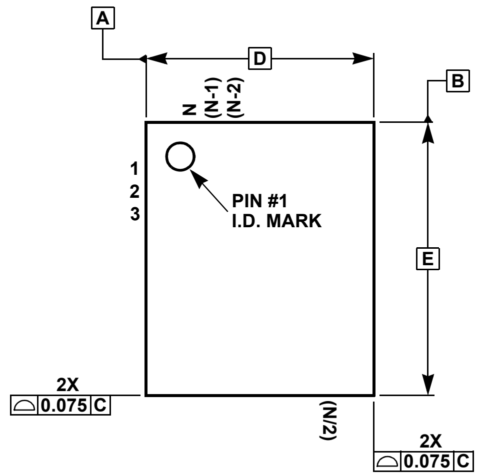
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL59911

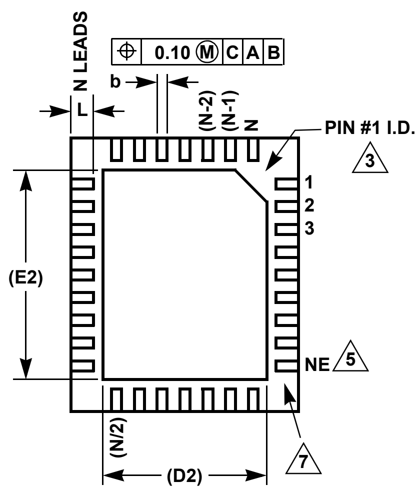
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

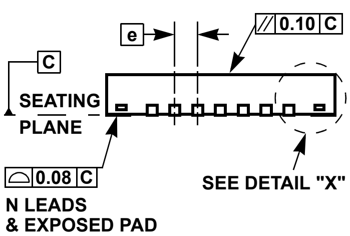
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



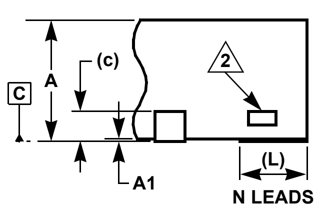
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

L32.5x6C (One of 10 Packages in MDP0046)

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
D		5.00 BSC		-
D2		3.50 REF		-
E		6.00 BSC		-
E2		4.50 REF		-
L	0.35	0.40	0.45	-
b	0.23	0.25	0.27	-
c		0.20 REF		-
e		0.50 BSC		-
N		32 REF		4
ND		7 REF		6
NE		9 REF		5

Rev 0 9/05

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.