ISL6161

Dual Power Distribution Controller

FN9104
Rev.7.00
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The ISL6161 is a hot swap dual supply power distribution controller that can be used in PCI Express (PCIe) applications.

Two external N-channel MOSFETs are driven to distribute and control power while providing load fault isolation. At turn-on, the gate of each external N-channel MOSFET is charged with a 10µA current source. Capacitors on each gate create a programmable ramp (soft turn-on) to control in-rush currents, as Figure 1 shows. A built-in charge pump supplies the gate drive for the 12V supply N-channel MOSFET switch.

Two external current sense resistors and FETs provide overcurrent (OC) protection. When the current through either resistor exceeds the user programmed value, the controller enters Current Regulation mode. The timeout capacitor, C_{TIM}, starts charging as the controller enters the timeout period. When C_{TIM} charges to a 2V threshold, both N-Channel MOSFETs are latched off. In the event of a hard and fast fault of at least three times the programmed current limit level, the N-channel MOSFET gates are pulled low immediately before entering the timeout period. The controller is reset by a rising edge on the $\overline{\text{ENABLE}}$ pin.

The ISL6161 constantly monitors both output voltages and reports either one being low on the PGOOD output as a low. The 12V PGOOD Voltage Threshold (Vth) is ~10.8V and the 3.3V Vth is ~2.85V nominally.

Related Literature

For a full list of related documents, visit our website

- ISL6161 product information page

Features

- Hot swap dual power distribution and control for +12V and +3.3V rails
- Provides fault isolation
- Programmable current regulation level
- Programmable timeout
- Charge pump allows the use of N-channel MOSFETs
- Power-good and OC latch indicators
- Adjustable turn-on ramp
- Protection during turn-on
- Two levels of current limit detection provide fast response to varying fault conditions
- 1µs response time to dead short
- 3µs response time to 200% current overshoot
- Pb-free available (RoHS compliant)

Applications

- PCIe applications
- Power distribution and control
- Hot plug and hot swap components

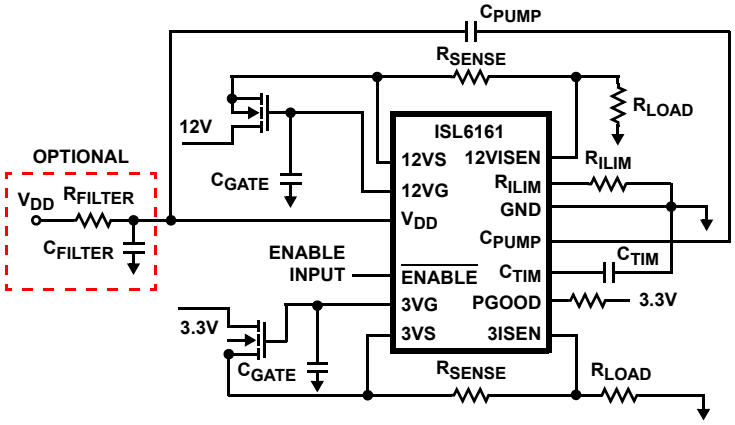


FIGURE 1. TYPICAL APPLICATION DIAGRAM

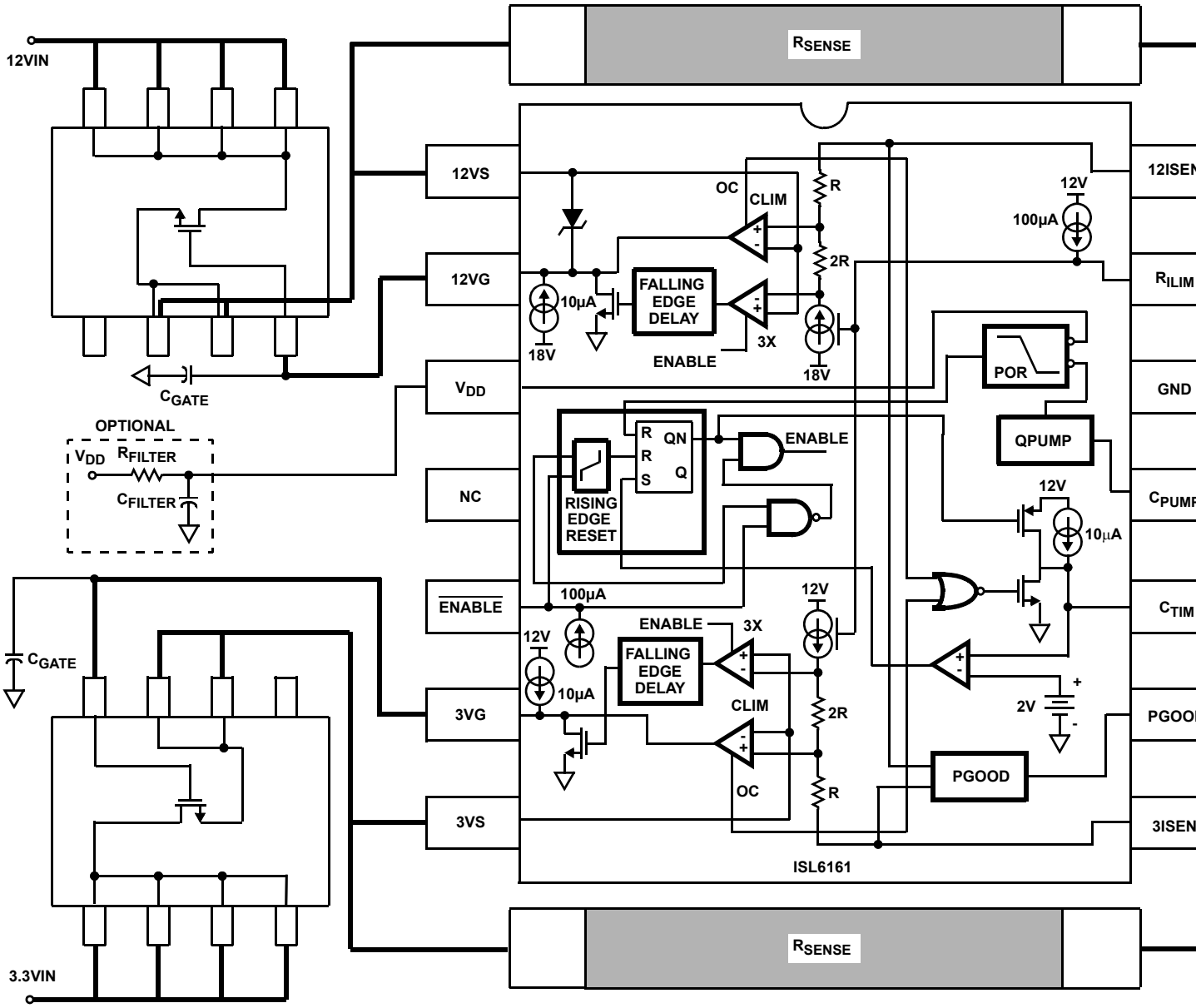


FIGURE 2. SIMPLIFIED SCHEMATIC (for 14 LD SOIC)

Ordering Information

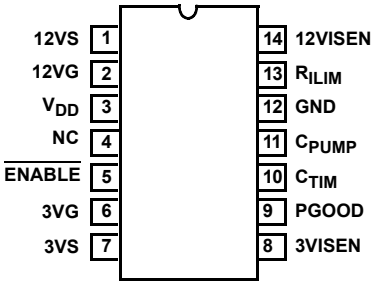
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL6161IVZA-T	6161IVZ	-40 to +85	2.5k	16 Ld TSSOP	M16.173
ISL6161CBZA	6161CBZ	0 to +70	-	14 Ld SOIC	M14.15
ISL6161CBZA-T	6161CBZ	0 to +70	2.5k	14 Ld SOIC	M14.15

NOTE:

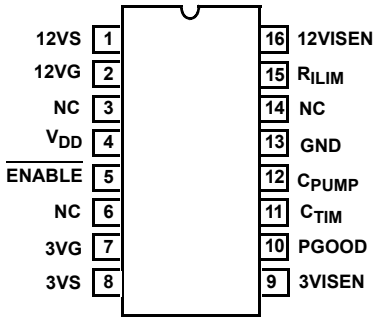
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL6161 product information. For more information about MSL, refer to TB363.

Pin Configurations

14 LD SOIC
TOP VIEW



16 LD TSSOP
TOP VIEW



Pin Descriptions

PIN # SOIC	PIN # TSSOP	SYMBOL	FUNCTION	DESCRIPTION
1	1	12VS	12V Source	Connect to the associated external N-channel MOSFET switch source to sense output voltage.
2	2	12VG	12V Gate	Connect to the associated N-channel MOSFET switch gate. A capacitor from this node to ground sets the turn-on ramp. At turn-on, this capacitor will be charged to ~17.4V by a 10µA current source.
3	4	V_{DD}	Chip Supply	Connect to the 12V supply. This can be connected directly to the +12V rail supplying the load voltage or to a dedicated V_{DD} +12V supply. If connecting to the +12V rail supplying the load voltage, pay special attention to V_{DD} decoupling to prevent sagging as heavy loads are switched on.
4	3,6,14	NC	Not Connected	Not connected.
5	5	$\overline{\text{ENABLE}}$	Enable/Reset	Turns on and resets the chip. Both outputs turn on when this pin is driven low. After a current limit timeout, the chip is reset by the rising edge of a reset signal applied to the $\overline{\text{ENABLE}}$ pin. This input has 100µA pull-up capability, which is compatible with 3V and 5V open drain and standard logic.
6	7	3VG	3V Gate	Connect to the gate of the external 3V N-channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on, this capacitor will be charged to ~11.9V by a 10µA current source.
7	8	3VS	3V Source	Connect to the source side of 3V external N-channel MOSFET switch to sense output voltage.
8	9	3VISEN	3V Current Sense	Connect to the load side of the 3V sense resistor to measure the voltage drop across this resistor between the 3VS and 3VISEN pins.
9	10	PGOOD	Power-Good Indicator	Indicates that all output voltages are within specification. PGOOD is driven by an open drain N-Channel MOSFET. It is pulled low when any output is not within specification.
10	11	C_{TIM}	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor controls the time between the onset of current limit and chip shutdown (current limit timeout). The duration of current limit timeout (in seconds) = 200kΩ x C_{TIM} (Farads).
11	12	C_{PUMP}	Charge Pump Capacitor	Connect a 0.1µF capacitor between this pin and V_{DD} (Pin 3). Provides charge storage for the 12VG drive.
12	13	GND	Chip Ground	Chip ground.
13	15	R_{ILIM}	Current Limit Set Resistor	A resistor connected between this pin and ground determines the current level at which current limit is activated. This current is determined by the ratio of the R_{ILIM} resistor to the sense resistor (R_{SENSE}). The current at current limit onset is equal to 10µA x (R_{ILIM}/R_{SENSE}). The ISL6161 can accommodate either a 10kΩ resistor (OC Vth = 100mV) or a 4.99kΩ resistor for a lower trip (OC Vth = 53mV). See Table 2 on page 7 for more details.
14	16	12VISEN	12V Current Sense	Connect to the load side of the sense resistor to measure the voltage drop across this resistor.

Absolute Maximum Ratings $T_A = 25°C$

V_{DD} . . . . . -0.3V to +16V
12VG, C_{PUMP} . . . . . -0.3V to 21V
12VISEN, 12VS . . . . . -5V to V_{DD} + 0.3V
3VISEN, 3VS . . . . . -5V to 7.5V
PGOOD, R_{ILIM} . . . . . -0.3V to 7.5V
$\overline{ENABLE}$, C_{TIM}, 3VG . . . . . -0.3V to V_{DD} + 0.3V
ESD Classification . . . . . 2kV (Class 2)

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
14 Ld SOIC Package	67
16 Ld TSSOP Package	94

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . Refer to TB493

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +10.5V to +13.2V
Temperature Range (T_A)
ISL6161IVZA . . . . . -40°C to +85°C
ISL6161CBZA . . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379 for details.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 12V, C_{VG} = 0.01µF, C_{TIM} = 0.1µF, R_{SENSE} = 0.1Ω, C_{BULK} = 220µF, ESR = 0.5W, T_A = T_J = -40°C to +85°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
12V CONTROL						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	V_{IL12V}	R_{ILIM} = 10kΩ	92	100	108	mV
		R_{ILIM} = 5kΩ	47	53	59	mV
3x Current Limit Threshold Voltage (Voltage Across Sense Resistor)	3 x V_{IL12V}	R_{ILIM} = 10kΩ	250	300	350	mV
		R_{ILIM} = 5kΩ	100	165	210	mV
±20% Current Limit Response Time (Current within 20% of Regulated Value)	20%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	2	-	µs
±10% Current Limit Response Time (Current within 10% of Regulated Value)	10%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	4	-	µs
±1% Current Limit Response Time (Current within 1% of Regulated Value)	1%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	10	-	µs
Response Time to Dead Short	RT_{SHORT}	C_{12VG} = 0.01µF	-	500	-	ns
Gate Turn-On Time	t_{ON12V}	C_{12VG} = 0.01µF	-	12	-	ms
Gate Turn-On Current	I_{ON12V}	C_{12VG} = 0.01µF	8	10	12	µA
3x Gate Discharge Current	3Xdisl	12VG = 18V	-	0.75	-	A
12V Undervoltage Threshold	$12V_{VUV}$		10.5	10.8	11.0	V
Charge Pumped 12VG Voltage	V12VG	C_{PUMP} = 0.1µF	16.8	17.3	17.9	V
3.3V CONTROL						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	V_{IL3V}	R_{ILIM} = 10kΩ	92	100	108	mV
		R_{ILIM} = 5kΩ	47	53	59	mV
3x Current Limit Threshold Voltage (Voltage Across Sense Resistor)	3 x V_{IL3V}	R_{ILIM} = 10kΩ	250	300	350	mV
		R_{ILIM} = 5kΩ	100	155	210	mV
±20% Current Limit Response Time (Current within 20% of Regulated Value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	2	-	µs
±10% Current Limit Response Time (Current within 10% of Regulated Value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	4	-	µs

Electrical Specifications V_{DD} = 12V, C_{VG} = 0.01µF, C_{TIM} = 0.1µF, R_{SENSE} = 0.1Ω, C_{BULK} = 220µF, ESR = 0.5W, T_A = T_J = -40°C to +85°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
±1% Current Limit Response Time (Current within 1% of Regulated Value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	10	-	µs
Response Time To Dead Short	RT_{SHORT}	C_{VG} = 0.01µF	-	500		ns
Gate Turn-On Time	t_{ON3V}	C_{VG} = 0.01µF	-	5	-	ms
Gate Turn-On Current	I_{ON3V}	C_{VG} = 0.01µF	8	10	12	µA
3x Gate Discharge Current	3xdisI	C_{VG} = 0.01µF, ENABLE = Low		0.75	-	A
3.3V Undervoltage Threshold	$3.3V_{VUV}$		2.7	2.85	3.0	V
3.3VG High Voltage	3VG		11.2	11.9	-	V
SUPPLY CURRENT AND IO SPECIFICATIONS						
V_{DD} Supply Current	I_{VDD}		4	8	10	mA
V_{DD} POR Rising Threshold			9.5	10.0	10.7	V
V_{DD} POR Falling Threshold			9.0	9.4	9.8	V
Current Limit Timeout	t_{ILIM}	C_{TIM} = 0.1µF	-	20	-	ms
$\overline{\text{ENABLE}}$ Pull-Up Voltage	PWRN_V	$\overline{\text{ENABLE}}$ Pin Open	1.8	2.4	3.2	V
$\overline{\text{ENABLE}}$ Rising Threshold	PWR_Vth		1.1	1.5	2	V
$\overline{\text{ENABLE}}$ Hysteresis	PWR_hys		0.1	0.2	0.3	V
$\overline{\text{ENABLE}}$ Pull-Up Current	PWRN_I		60	80	100	µA
Current Limit Timeout Threshold (C_{TIM})	C_{TIM}_Vth		1.8	2	2.2	V
C_{TIM} Charging Current	C_{TIM}_I		8	10	12	µA
C_{TIM} Discharge Current	C_{TIM}_disI		1.7	2.6	3.5	mA
C_{TIM} Pull-Up Current	C_{TIM}_disI	V_{CTIM} = 8V	3.5	5	6.5	mA
R_{ILIM} Pin Current Source Output	R_{ILIM}_Io		90	100	110	µA
Charge Pump Output Current	Qpmp_Io	C_{PUMP} = 0.1µF, C_{PUMP} = 16V	320	560	900	µA
Charge Pump Output Voltage	Qpmp_Vo	No Load	17.2	17.4	-	V
Charge Pump Output Voltage - Loaded	Qpmp_VIo	Load Current = 100µA	16.2	16.7	-	V
Charge Pump POR Rising Threshold	Qpmp + Vth		15.6	16	16.5	V
Charge Pump POR Falling Threshold	Qpmp - Vth		15.2	15.7	16.2	V

ISL6161 Description and Operation

The ISL6161 is a multi-featured +12V and +3.3V dual power supply distribution controller. Its features include programmable Current Regulation (CR) limiting and time to latch off.

At turn-on, the gate capacitor of each external N-channel MOSFET is charged with a 10µA current source. These capacitors create a programmable ramp (soft turn-on). A charge pump supplies the gate drive for the 12V supply control FET switch, driving that gate to 17V.

The load currents pass through two external current sense resistors. When the voltage across either resistor quickly exceeds the user programmed Current Regulation Voltage Threshold (CRVth) level, the controller enters current regulation. The CRVth is set by the external resistor value on the R_{ILIM} pin. At this time, the timeout capacitor, C_{TIM}, starts charging with a 10µA current source and the controller enters the timeout period. The timeout period length is set by the single external capacitor (see Table 1 on page 7) placed from the C_{TIM} pin (Pin 10) to ground and is characterized by a lowered gate drive voltage to the appropriate external N-channel MOSFET. When C_{TIM} charges to 2V, an internal comparator is tripped, and both N-channel MOSFETs are latched off. If the voltage across the sense resistors rises slowly in response to an OC condition, CR mode is entered at ~95% of the programmed CR level. This is due to the necessary hysteresis and response time in the CR control circuitry.

TABLE 1. C_{TIM} RECOMMENDATIONS

C_{TIM} CAPACITOR (µF)	NOMINAL TIME-OUT PERIOD (ms)
0.022	4.4
0.047	9.4
0.1	20

NOTE:

6. Nominal time-out period in seconds = C_{TIM} x 200kΩ.

Table 2 shows R_{SENSE} and R_{ILIM} recommendations and the resulting CR level for the specified PCIe add-in card connector sizes. First select an R_{ILIM} value for the appropriate CRVth, then choose the R_{SENSE} value for the desired OC trip. Other applications can select either 4.99kΩ or 10kΩ for R_{ILIM}; the accuracy of the CRVth is measured for both. Values below 4.99kΩ are not recommended due to possible noise sensitivity. Values between 4.99kΩ and 10kΩ can be used, but are not measured for accuracy.

TABLE 2. R_{SENSE} AND R_{ILIM} RECOMMENDATIONS

PCIe ADD-IN CARD CONNECTOR	R_{ILIM} (kΩ)	3.3V R_{SENSE} (mΩ), NOMINAL CR (A)	12V R_{SENSE} (mΩ), NOMINAL CR (A)	NOMINAL CRVth (mV)
X1	10	30, 3.3	150, 0.7	100
	4.99	15, 3.5	90, 0.6	53
X4/X8	10	30, 3.3	40, 2.5	100
	4.99	15, 3.5	20, 2.6	53
X16	10	30, 3.3	16, 6.3	100
	4.99	15, 3.5	8, 6.6	53

NOTE:

7. Nominal CR Vth = R_{ILIM} x 10µA = OC x R_{SENSE}

The ISL6161 responds to a load short (defined as a current level three times the OC set point with a fast transition) by immediately driving the relevant N-channel MOSFET gate to 0V in ~3µs. The gate voltage is then slowly ramped up, soft-starting the N-channel MOSFET to the programmed current regulation limit level. This is the start of the timeout period if the abnormal load condition still exists. The programmed current regulation level is held until either the OC event ends or the timeout period expires. If the OC event ends, the N-channel MOSFET is fully enhanced and the C_{TIM} charging current is diverted away from the capacitor. If the timeout period expires before the OC event ends, then both gates are quickly pulled to 0V, turning off both N-Channel MOSFETs simultaneously.

Upon any UV condition, the PGOOD signal will pull low when tied high through a resistor to the logic supply. This pin is a fault indicator, but is not the OC latch-off indicator. For an OC latch-off indication, monitor C_{TIM} (Pin 10). This pin will rise rapidly to 12V when the timeout period expires. See Figure 2 on page 2 for an OC latch-off circuit suggestion.

The ISL6161 is reset by a rising edge on the $\overline{ENABLE}$ pin and is turned on by the $\overline{ENABLE}$ pin being driven low.

Application Considerations

In a non PCIe, motor drive application, **current loop stabilization** is facilitated through a small value resistor in series with the gate timing capacitor. As the ISL6161 drives a highly inductive current load, instability characterized by the gate voltage repeatedly ramping up and down may occur. Stability can be easily enhanced by substituting a larger gate resistor. Improve stability by eliminating long point-to-point wiring to the load.

The $\overline{ENABLE}$ internal pull-up makes the ISL6161 well suited for implementation on either side of the connector in which a motherboard prebiased condition or a load board staggered connection is present. In either case, the ISL6161 turns on in Soft-Start mode, protecting the supply rail from sudden current loading.

During the **timeout delay period** with the ISL6161 in current limit mode, the V_{GS} of the external N-channel MOSFETs is reduced, driving the N-channel MOSFET switch into a high $r_{DS(ON)}$ state. Thus, avoid extended timeout periods, because the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the MOSFET manufacturer's datasheet for SOA information.

With the high levels of inrush current (highly capacitive loads and motor start-up currents), **choosing the current regulation (CR) level** is crucial to provide both protection and still allow for this inrush current without latching off. Consider this in addition to the timeout delay when choosing MOSFETs for your design.

Physical layout of the R_{SENSE} resistors is critical to avoid inadvertently lowering the CR and trip levels. Ideally, trace routing between the R_{SENSE} resistors and the ISL6161 should be as direct and as short as possible with zero current in the sense lines.

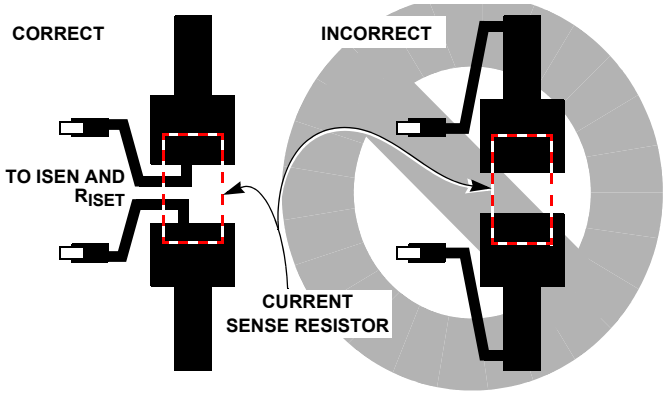


FIGURE 3. SENSE RESISTOR PCB LAYOUT

Monitor the xISEN pins to **detect open loads**. Although gated off, the external FET I_{DSS} will cause the xISEN pins to float above ground to some voltage when no load is attached. If this is not desired, 5k resistors from the xISEN pins to ground will prevent the outputs from floating when the external switch FETs are disabled and the outputs are open.

For **PCIe applications,** the ISL6161 and the ISL6118 provide the fundamental hotswap function for the +12V and +3.3V main rails and the +3.3V auxiliary rails, respectively, as shown in "PCI Express Implementation" on page 10.

Typical Performance Curves

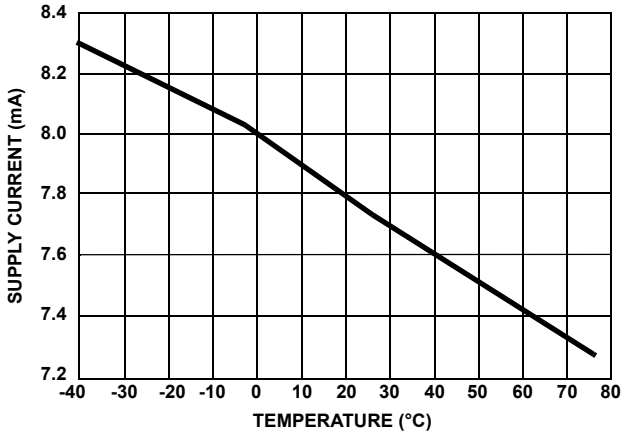


FIGURE 4. SUPPLY CURRENT

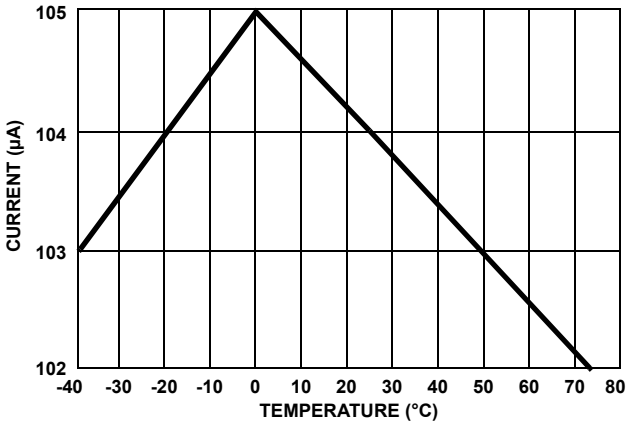


FIGURE 5. R_{ILIM} SOURCE CURRENT

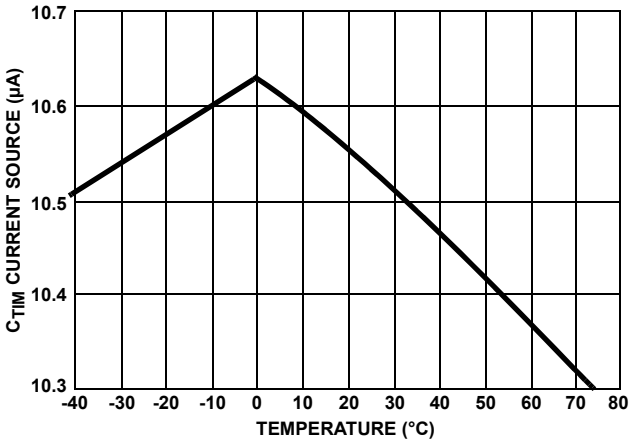


FIGURE 6. C_{TIM} CURRENT SOURCE

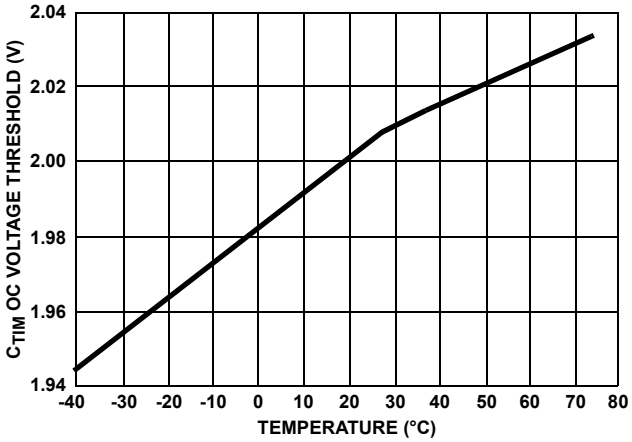


FIGURE 7. C_{TIM} OC VOLTAGE THRESHOLD

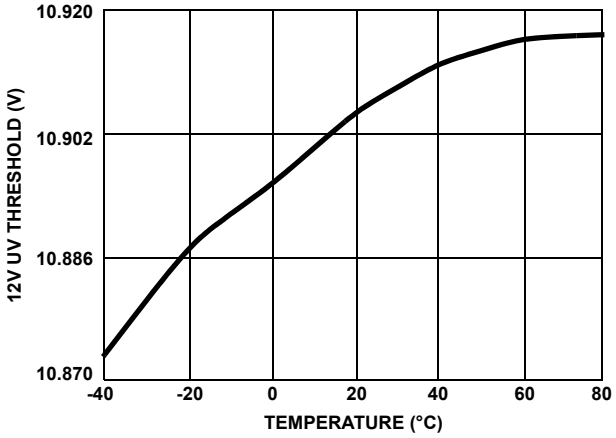


FIGURE 8. 12V UV THRESHOLD

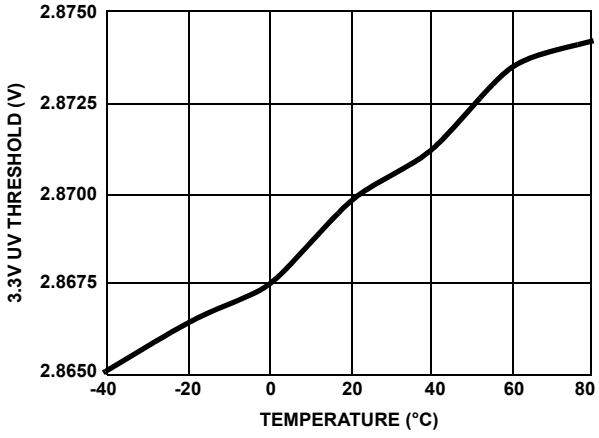


FIGURE 9. 3.3V UV THRESHOLD

Typical Performance Curves (Continued)

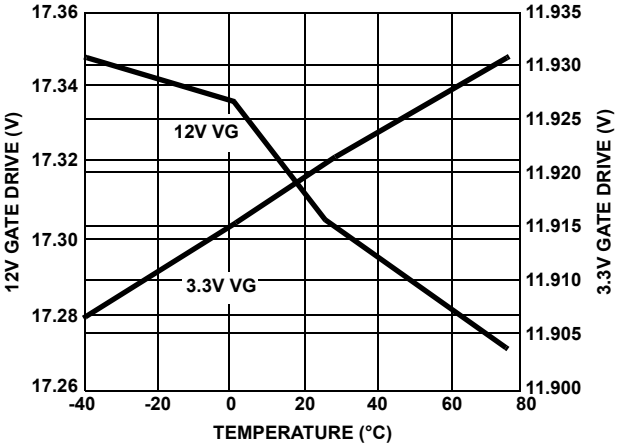


FIGURE 10. 12V, 3.3V GATE DRIVE

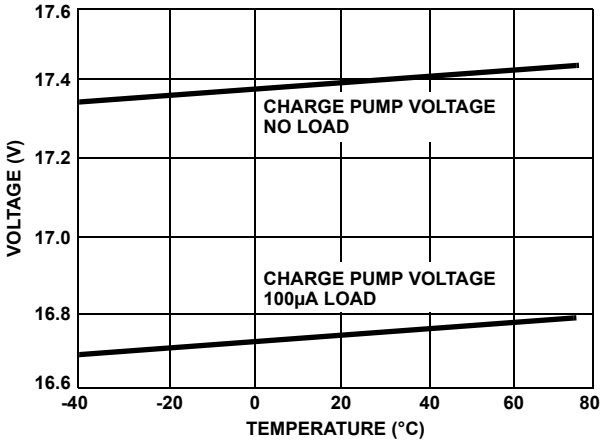


FIGURE 11. PUMP VOLTAGE

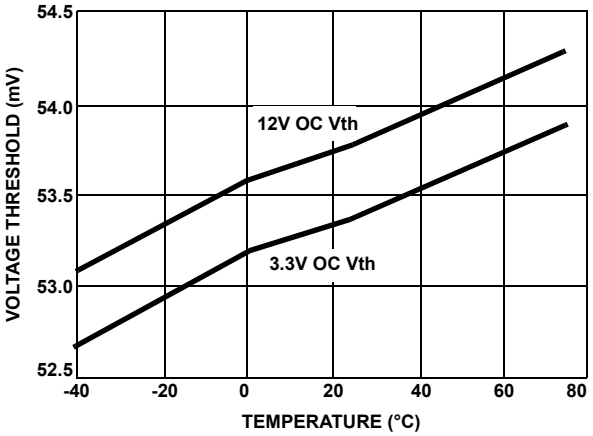


FIGURE 12. OC VOLTAGE THRESHOLD WITH R_{LIM} = 5kΩ

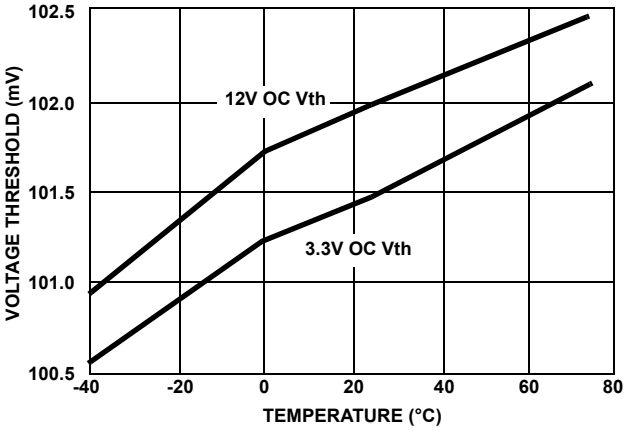


FIGURE 13. OC VOLTAGE THRESHOLD WITH R_{LIM} = 10kΩ

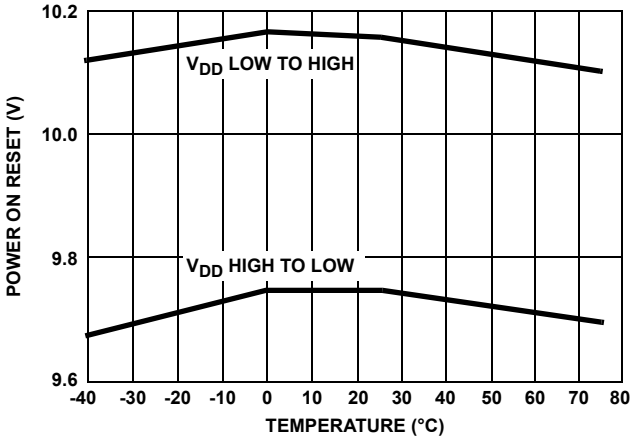


FIGURE 14. POWER-ON RESET VOLTAGE THRESHOLD

PCI Express Implementation

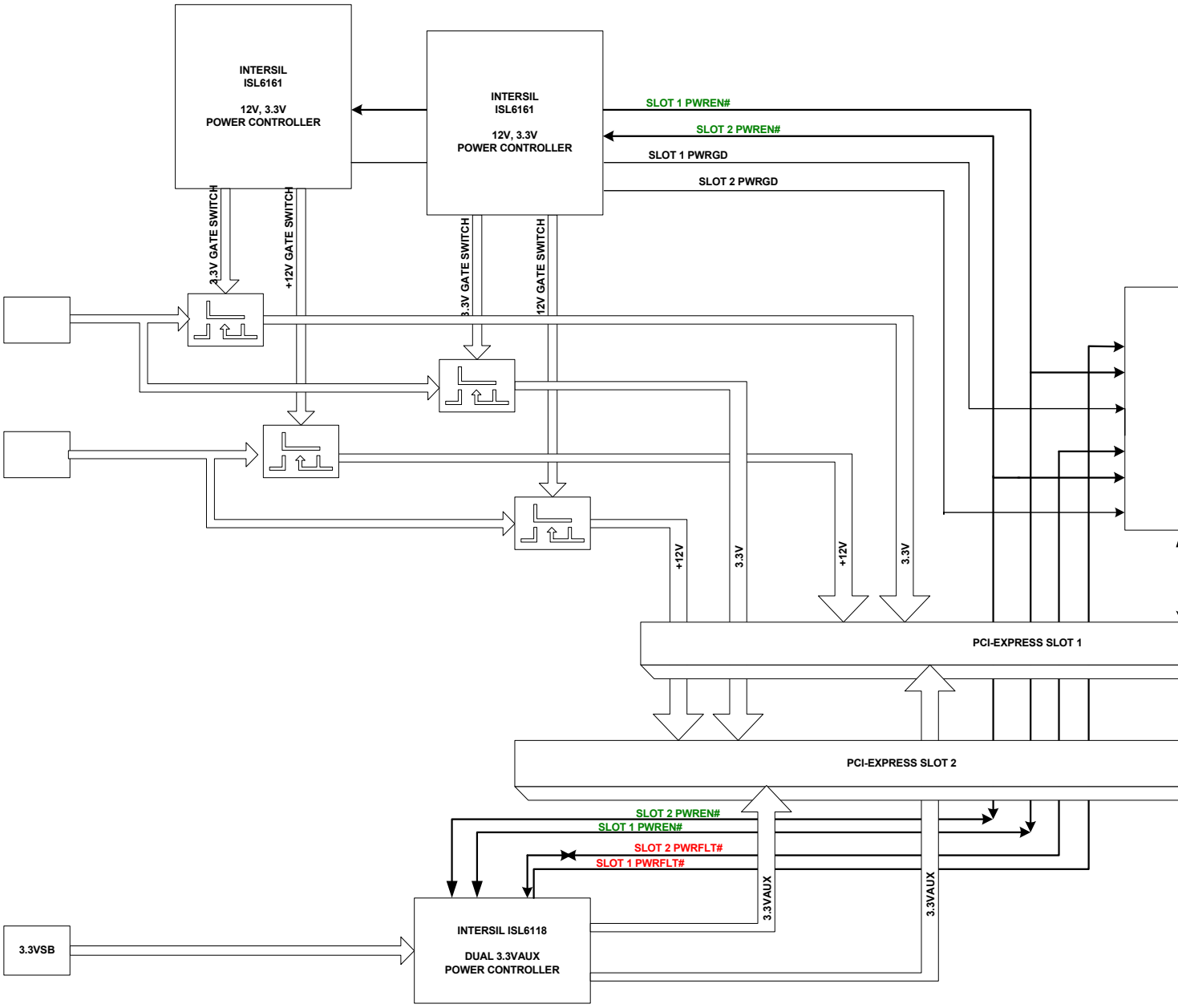


FIGURE 15. PCI EXPRESS IMPLEMENTATION OF THE ISL6161 AND ISL6118

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 16, 2018	FN9104.7	Updated Ordering information table by removing ISL6161IVZA, adding tape and reel parts, adding tape and reel unit column, and updating Note 1. Updated Disclaimer.
Jan 23, 2018	FN9104.6	-Applied new Header/Footer. -Added Related Literature section to page 1. -Cleaned up simplified schematic on page 2. -Added ISL6161IVZA Information throughout document. -Added MSL note (Note 3). -Clarified R_{ILIM} in Pin Descriptions table on page 4. -Fixed unit typo on page 9. -Added caption to figure on page 10. -Removed About Intersil verbiage. Updated Disclaimer.
December 3, 2015	FN9104.5	Added Rev History and About Intersil Verbiage. Updated Ordering Information on page 1. Updated POD M14.15 to most current version. Rev change is as follows: Added land pattern and moved dimensions from table onto drawing.

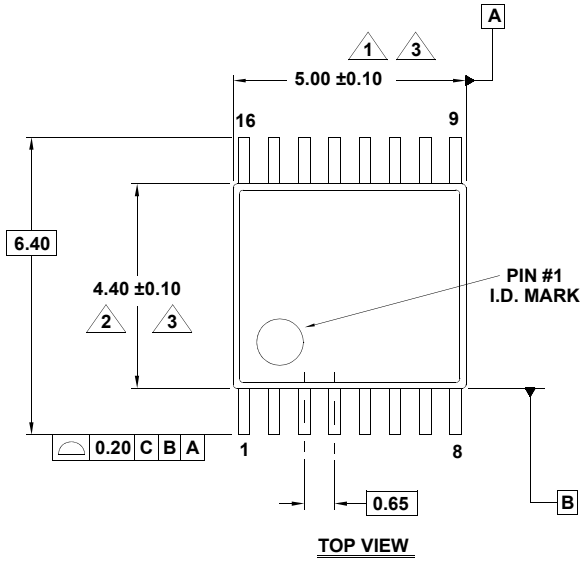
Package Outline Drawings

For the most recent package outline drawing, see M16.173.

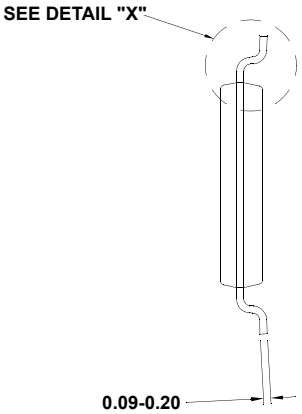
M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

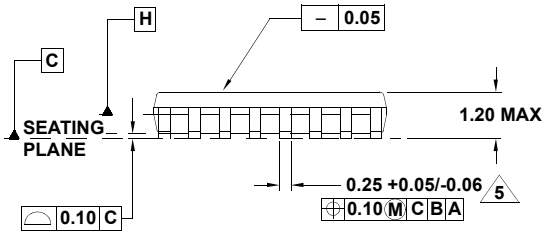
Rev 2, 5/10



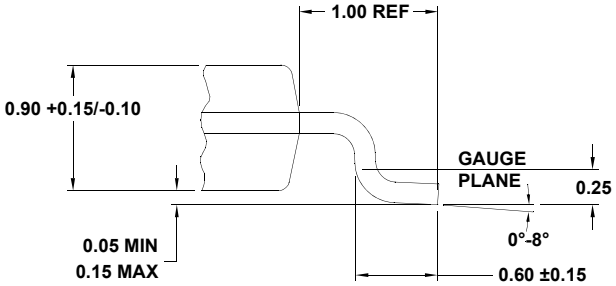
TOP VIEW



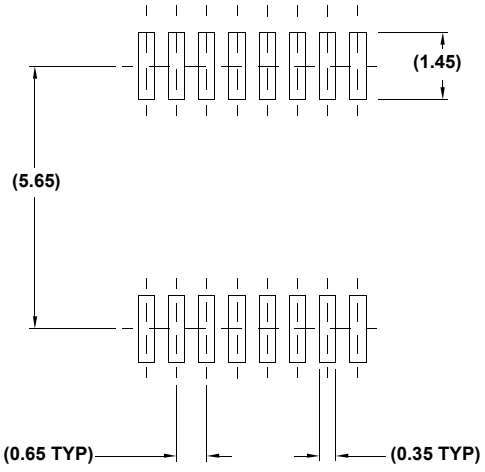
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

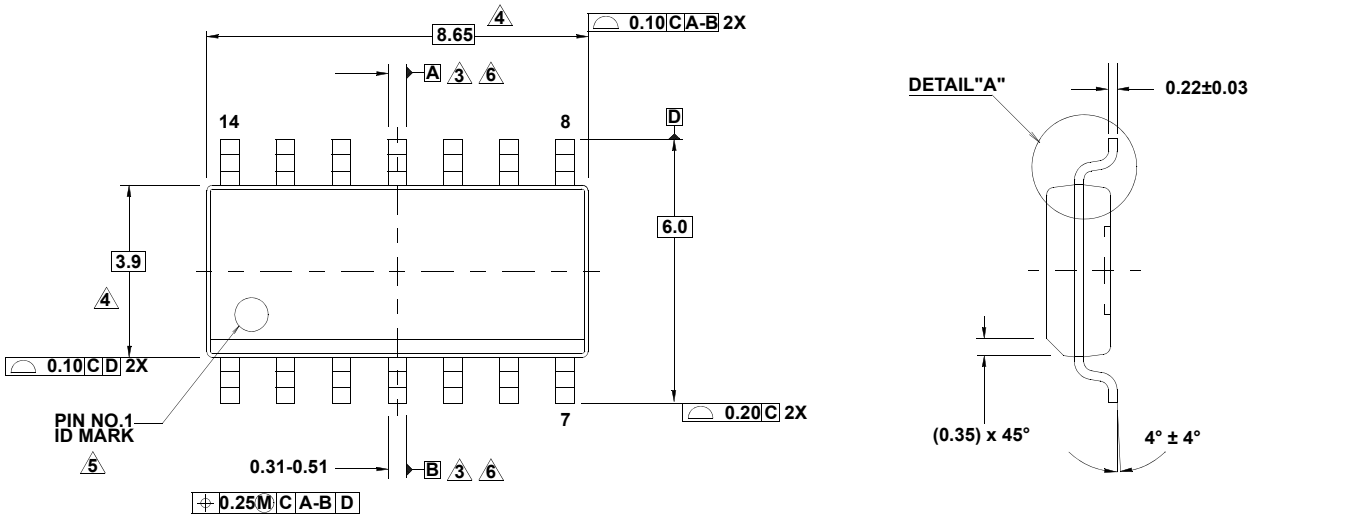
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

M14.15

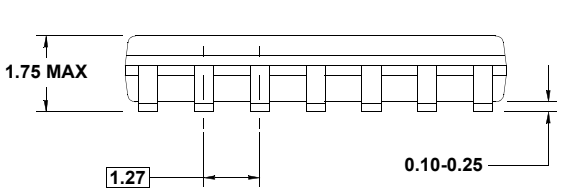
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 10/09

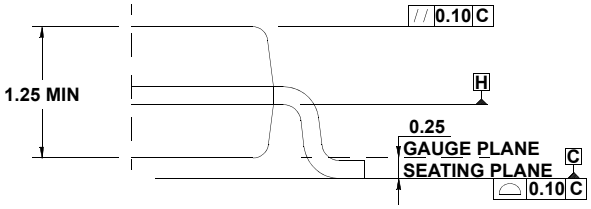
For the most recent package outline drawing, see M14.15.



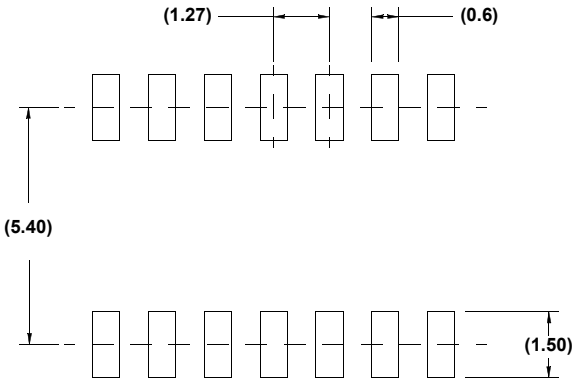
TOP VIEW



SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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(Rev.4.0-1 November 2017)

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