Data Sheet | November 15, 2004 | FN9052.2

Dual 5V Synchronous Buck Pulse-Width Modulator (PWM) Controller for DDRAM Memory V_{DDQ} and V_{TT} Termination

The ISL6530 provides complete control and protection for dual DC-DC converters optimized for high-performance DDRAM memory applications. It is designed to drive low cost N-channel MOSFETs in synchronous-rectified buck topology to efficiently generate 2.5V V_{DDQ} for powering DDRAM memory, V_{REF} for DDRAM differential signalling, and V_{TT} for signal termination. The ISL6530 integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The V_{DDQ} output of the converter is maintained at 2.5V through an integrated precision voltage reference. The V_{REF} output is precisely regulated to 1/2 the memory power supply, with a maximum tolerance of ±1% over temperature and line voltage variations. V_{TT} accurately tracks V_{REF}. During V2_SD sleep mode, the V_{TT} output is maintained by a low power window regulator.

The ISL6530 provides simple, single feedback loop, voltage-mode control with fast transient response. It includes two phase-locked 300kHz triangle-wave oscillators which are displaced 90^{o} to minimize interference between the two PWM regulators. The regulators feature error amplifiers with a 15MHz gain-bandwidth product and 6V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The ISL6530 protects against over-current conditions by inhibiting PWM operation. The ISL6530 monitors the current in the V_{DDQ} regulator by using the $r_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

Ordering Information

PART NUMBER	TEMP RANGE(^{o}C)	PACKAGE	PKG. DWG. #
ISL6530CB*	0 to 70	24 Lead SOIC	M24.3
ISL6530CBZ* (See Note)	0 to 70	24 Lead SOIC (Pb-free)	M24.3
ISL6530CR*	0 to 70	32 Lead 5x5 QFN	L32.5x5
ISL6530CRZ* (See Note)	0 to 70	32 Lead 5x5 QFN (Pb-free)	L32.5x5
ISL6530EVAL1, 2	Evaluation Board		

* Add "-T" suffix for tape and reel option.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

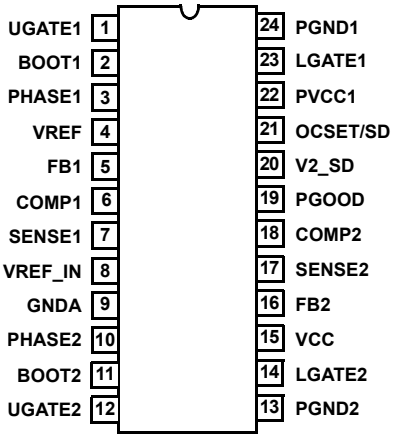
- Provides V_{DDQ}, V_{REF}, and V_{TT} voltages for one- and two-channel DDRAM memory systems
- Excellent voltage regulation
  - V_{DDQ} = 2.5V ±2% over full operating range
  - V_{REF} = (V_{DDQ}÷2) ±1% over full operating range
  - V_{TT} = V_{REF} ± 30mV
- Supports 'S3' sleep mode
  - V_{TT} is held at V_{DDQ}÷2 via low power window regulator to minimize wake-up time
- Fast transient response
  - Full 0% to 100% duty ratio
- Operates from +5V input
- Overcurrent fault monitor on VDD
  - Does not require extra current sensing element
  - Uses MOSFET's $r_{DS(ON)}$
- Drives inexpensive N-Channel MOSFETs
- Small converter size
  - 300kHz fixed frequency oscillator
- 24 Lead, SOIC or 32 Lead, 5mm×5mm QFN
- Pb-Free Available (RoHS Compliant)

Applications

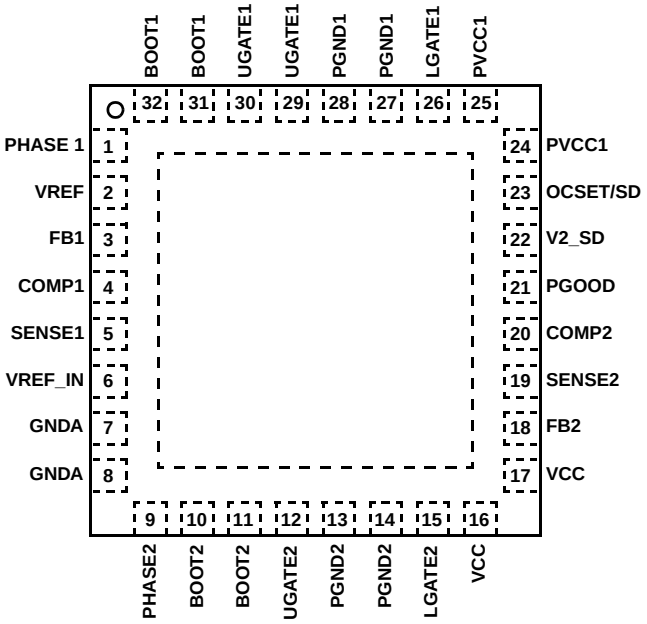
- V_{DDQ}, V_{TT}, and VREF regulation for DDRAM memory systems
  - Main Memory in AMD® Athlon™ and K8™, Pentium® III, Pentium IV, Transmeta, PowerPC™, AlphaPC™, and UltraSparc® based computer systems
  - Video memory in graphics systems
- High-power tracking DC-DC regulators

Pinouts

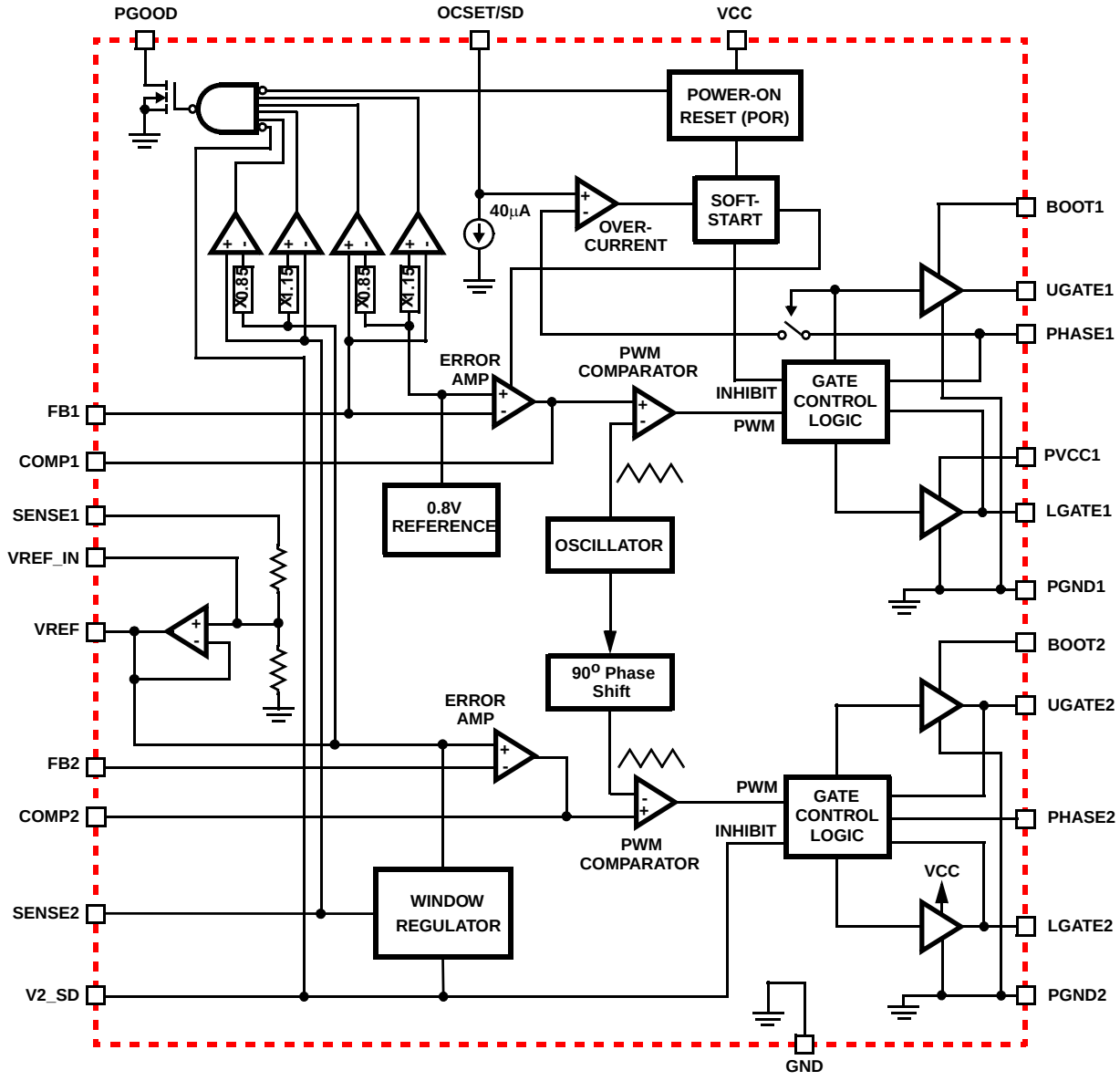
24 LEAD (SOIC)
TOP VIEW



32 LEAD (QFN)
TOP VIEW



Block Diagram



Typical Application

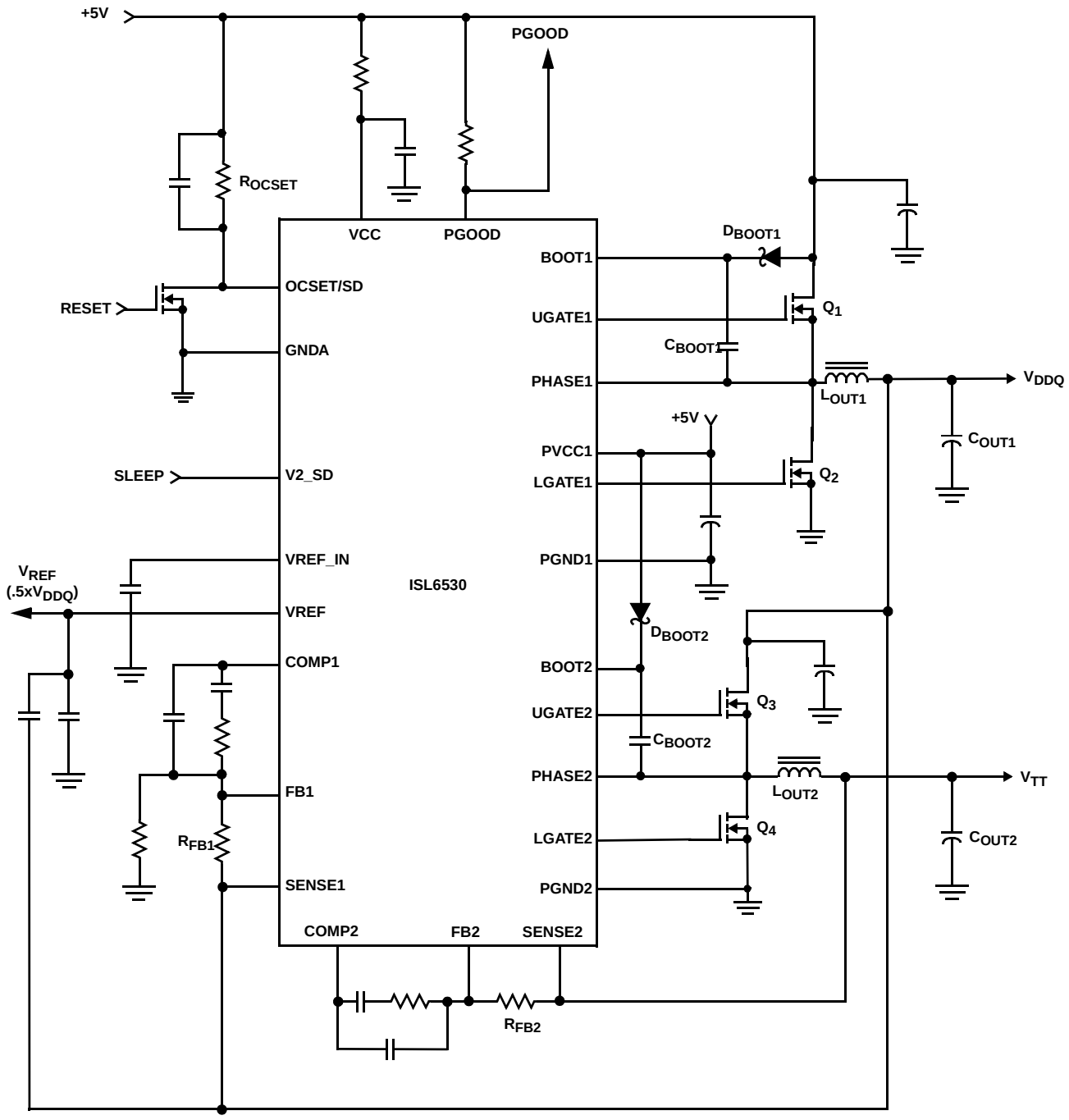


FIGURE 1. TYPICAL APPLICATION FOR ISL6530

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +7.0V
Boot Voltage, V_{BOOTn} - V_{PHASEn} . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, V_{CC} . . . . . +5V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package (Note 1)	65	N/A
QFN Package (Note 2)	33	4

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead tips only)
For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. $\theta_{JC,}$ the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

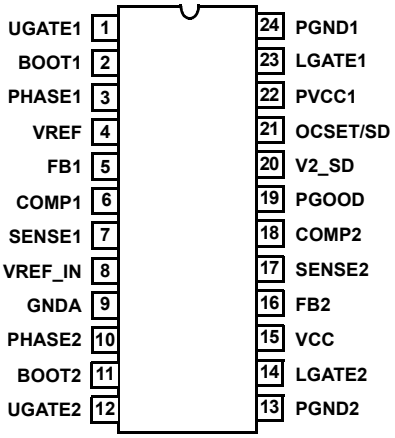
Electrical Specifications

Recommended Operating Conditions with Vcc = 5V, Unless Otherwise Noted

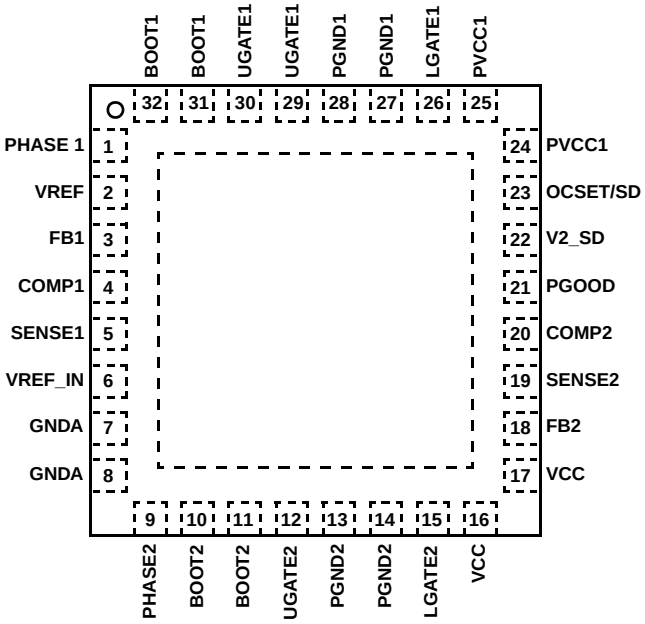
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{CC}	OCSET/SD = V_{CC}; UGATE1, UGATE2, LGATE1, and LGATE2 Open	-	5	-	mA
Shutdown Supply		OCSET/SD = 0V	-	3	-	mA
POWER-ON RESET						
Rising V_{CC} Threshold		$V_{OCSET/SD}$ = 4.5V	4.25	-	4.5	V
Falling V_{CC} Threshold		$V_{OCSET/SD}$ = 4.5V	3.75	-	4.0	V
OSCILLATOR						
Free Running Frequency		V_{CC} = 5	275	300	325	kHz
REFERENCES						
Reference Voltage (V2 Error Amp Reference)	V_{VREF}	SENSE1 = 2.5V	49.5	50	50.5	%SENSE1
V1 Error Amp Reference Voltage Tolerance			-	-	2	%
V1 Error Amp Reference	V_{REF}	V_{CC} = 5	-	0.8	-	V
ERROR AMPLIFIERS						
DC Gain			-	82	-	dB
Gain-Bandwidth Product	GBW		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/µs
WINDOW REGULATOR						
Load Current			-	±10	-	mA
Output Voltage Error		V2_SD = VCC; ±10mA load on V2	-	±7		%
GATE DRIVERS						
Upper Gate Source (UGATE1 and 2)	I_{UGATE}	V_{CC} = 5V, V_{UGATE} = 2.5V	-	-1	-	A
Upper Gate Sink (UGATE1 and 2)	I_{UGATE}	$V_{UGATE-PHASE}$ = 2.5V	-	1	-	A
Lower Gate Source (LGATE1 and 2)	I_{LGATE}	V_{CC} = 5V, V_{LGATE} = 2.5V	-	-1	-	A
Lower Gate Sink (LGATE1 and 2)	I_{LGATE}	V_{LGATE} = 2.5V	-	2	-	A
PROTECTION						
OCSET/SD Current Source	I_{OCSET}	V_{OCSET} = 4.5VDC	34	40	46	µA
OCSET/SD Disable Voltage	V_{RESET}		-	0.8	-	V

Functional Pin Description

24 LEAD (SOIC)
TOP VIEW



32 LEAD (QFN)
TOP VIEW



BOOT1 and BOOT2

These pins provide bias voltage to the upper MOSFET drivers. A single capacitor bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

UGATE1 and UGATE2

Connect UGATE1 and UGATE2 to the corresponding upper MOSFET gate. These pins provide the gate drive for the upper MOSFETs. UGATE2 is also monitored by the adaptive shoot through protection to determine when the upper FET of the V_{TT} regulator has turned off.

LGATE1 and LGATE2

Connect LGATE1 and LGATE2 to the corresponding lower MOSFET gate. These pins provide the gate drive for the lower MOSFETs. These pins are monitored by the adaptive shoot through protection to determine when the lower FET has turned off.

PGND1 and PGND2

These are the power ground connections for the gate drivers of the PWM controllers. Tie these pins to the ground plane through the lowest impedence connection available.

OCSET/SD

A resistor (R_{OCSET}) connected from this pin to the drain of the upper MOSFET of the V_{DDQ} regulator sets the overcurrent trip point. R_{OCSET}, an internal 40µA current source (I_{OCS}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the V_{DDQ} converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{r_{DS(ON)}}$$

An overcurrent trip cycles the soft-start function.

Pulling the OCSET/SD pin to ground resets the ISL6530 and all external MOSFETS are turned off allowing the two output voltage power rails to float.

PGOOD

A high level on this open-drain output indicates that both the V_{DDQ} and V_{TT} regulators are within normal operating voltage ranges.

GNDA

Signal ground for the IC. Tie this pin to the ground plane through the lowest impedence connection available.

VCC

The 5V bias supply for the chip is connected to this pin. This pin is also the positive supply for the lower gate driver, LGATE2. Connect a well decoupled 5V supply to this pin.

V2_SD

A high level on the V2_SD input places the V2 controller into “sleep” mode. In sleep mode, both UGATE2 and LGATE2 are driven low, effectively floating the V_{TT} supply.

While the V_{TT} supply "floats", it is held to about 50% of V_{DDQ} via a low current window regulator which drives V_{TT} via the SENSE2 pin. The window regulator can overcome up to at least ±10mA of leakage on V_{TT}.

While V2_SD is high, PGOOD is low.

PHASE1 and PHASE2

Connect PHASE1 and PHASE2 to the corresponding upper MOSFET source. This pin is used as part of the upper MOSFET bootstrapped drives. PHASE1 is used to monitor the voltage drop across the upper MOSFET of the V_{DDQ} regulator for over-current protection. The PHASE1 pin is monitored by the adaptive shoot through protection circuitry to determine when the upper FET of the V_{DDQ} supply has turned off.

FB1, COMP1, FB2, and COMP2

COMP1, COMP2, FB1, and FB2 are the available external pins of the error amplifiers. The FB1 and FB2 pins are the inverting inputs of each error amplifier and the COMP1 and COMP2 pins are the associated outputs. An appropriate AC network across these pins is used to compensate the voltage-controlled feedback loop of each converter.

VREF and VREF_IN

VREF produces a voltage equal to one half of the voltage on SENSE1. This low current output is connected to the VREF input of the DDRAM devices being powered. This same voltage is used as the reference input of the V_{TT} error amplifier. Thus V_{TT} is controlled to 50% of V_{DDQ}.

VREF_IN is used as an option to overdrive the internal resistor divider network that sets the voltage for both VREF_OUT and the reference voltage for the V_{TT} supply. A 100pF capacitor between VREF_IN and ground is recommended for proper operation.

PVCC1

This is the positive supply for the lower gate driver, LGATE1. PVCC1 is connected to a well decoupled 5V.

SENSE1 and SENSE2

Both SENSE1 and SENSE2 are connected directly to the regulated outputs of the V_{DDQ} and V_{TT} supplies, respectively. SENSE1 is used as an input to create the voltage at VREF_OUT and the reference voltage for the V_{TT} supply. SENSE2 is used as the regulation point for the window regulator that is enabled in V2_SD mode.

Functional Description

Overview

The ISL6530 contains control and drive circuitry for two synchronous buck PWM voltage regulators. Both regulators utilize 5V bootstrapped output topology to allow use of low cost N-channel MOSFETs. The regulators are driven by 300kHz clocks. The clocks are phase locked and displaced 90^o to minimize noise coupling between the controllers.

The first regulator includes a precision 0.8V reference and is intended to provide the proper V_{DDQ} to a DDRAM memory system. The V_{DDQ} controller implements overcurrent protection utilizing the $r_{DS(ON)}$ of the upper MOSFET. Following a fault condition, the V_{DDQ} regulator is softstarted via a digital softstart circuit.

Included in the ISL6530 is a precision V_{REF} reference output. V_{REF} is a buffered representation of $.5xV_{DDQ}$. V_{REF} is derived via a precision internal resistor divider connected to the SENSE1 terminal.

The second PWM regulator is designed to provide V_{TT} termination for the DDRAM signal lines. The reference to the V_{TT} regulator is V_{REF}. Thus the V_{TT} regulator provides a termination voltage equal to $.5xV_{DDQ}$. The drain of the upper MOSFET of the V_{TT} supply is connected to the regulated V_{DDQ} voltage. The V_{TT} controller is designed to enable both sinking and sourcing current on the V_{TT} rail.

Two benefits result from the ISL6530 dual controller topology. First, as VREF is always $.5xV_{DDQ}$, the V_{TT} supply will track the V_{DDQ} supply during softstart cycles. Second, the overcurrent protection incorporated into the V_{DDQ} supply will simultaneously protect the V_{TT} supply.

Initialization

The ISL6530 automatically initializes upon application of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input bias supply voltage at the VCC pin. The POR function initiates soft-start operation after the 5V bias supply voltage exceeds its POR threshold.

Soft-Start

The POR function initiates the digital soft start sequence. The PWM error amplifier reference input for the VDDQ regulator is clamped to a level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). This method provides a rapid and controlled output voltage rise. The soft start sequence typically takes about 7ms.

With the V_{TT} regulator reference held at $\frac{1}{2} \cdot V_{DDQ}$ it will automatically track the ramp of the V_{DDQ} softstart, thus enabling a soft-start for V_{TT}.

Figure 2 shows the soft-start sequence for a typical application. At t0, the +5V VCC bias voltage starts to ramp. Once the voltage on VCC crosses the POR threshold at time t1, both outputs begin their soft-start sequence. The triangle waveforms from the PWM oscillators are compared to the rising error amplifier output voltage. As the error amplifier voltage increases, the pulse-widths on the UGATE pins increase to reach their steady-state duty cycle at time t2.

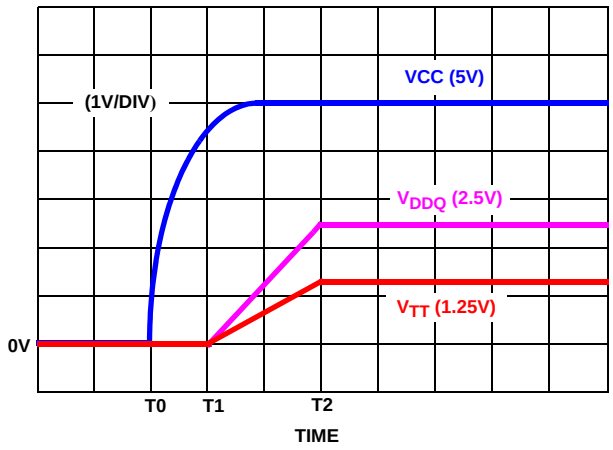


FIGURE 2. SOFT-START INTERVAL

Shoot-Through Protection

A shoot-through condition occurs when both the upper MOSFET and lower MOSFET are turned on simultaneously, effectively shorting the input voltage to ground. To protect the regulators from a shoot-through condition, the ISL6530 incorporates specialized circuitry which insures that complementary MOSFETs are not ON simultaneously.

The adaptive shoot-through protection utilized by the V_{DDQ} regulator looks at the lower gate drive pin, LGATE1, and the phase node, PHASE1, to determine whether a MOSFET is ON or OFF. If PHASE1 is below 0.8V, the upper gate is defined as being OFF. Similarly, if LGATE1 is below 0.8V, the lower MOSFET is defined as being OFF. This method of shoot-through protection allows the V_{DDQ} regulator to source current only.

Due to the necessity of sinking current, the V_{TT} regulator employs a modified protection scheme from that of the V_{DDQ} regulator. If the voltage from UGATE2 or from LGATE2 to GND is less than 0.8V, then the respective MOSFET is defined as being OFF and the other MOSFET is turned ON.

Since the voltage of the lower MOSFET gates and the upper MOSFET gate of the V_{TT} supply are being measured to determine the state of the MOSFET, the designer is encouraged to consider the repercussions of introducing external components between the gate drivers and their respective MOSFET gates before actually implementing such measures. Doing so may interfere with the shoot-through protection.

Power Down Mode

DDRAM systems include a sleep state in which the V_{DDQ} voltage to the memories is maintained, but signaling is suspended. During this mode the V_{TT} termination voltage is no longer needed. The only load placed on the V_{TT} bus is the leakage of the associated signal pins of the DDRAM and memory controller ICs.

When the V2_SD input of the ISL6530 is driven high, the V_{TT} regulator is placed into a “sleep” state. In the sleep state the main V_{TT} regulator is disabled, with both the upper and lower MOSFETs being turned off. The V_{TT} bus is maintained at close to .5xVdd via a low current window regulator which drives V_{TT} via the SENSE2 pin. Maintaining V_{TT} at .5xV_{DDQ} consumes negligible power and enables rapid wake-up from sleep mode without the need of softstarting the V_{TT} regulator. During this power down mode, PGOOD is held LOW.

Output Voltage Selection

The output voltage of the V_{DDQ} regulator can be programmed to any level between V_{IN} (i.e. +5V) and the internal reference, 0.8V. An external resistor divider is used to scale the output voltage relative to the reference voltage and feed it back to the inverting input of the error amplifier, see Figure 3. However, since the value of R1 affects the values of the rest of the compensation components, it is advisable to keep its value less than 5kΩ. R4 can be calculated based on the following equation:

$$R4 = \frac{R1 \times 0.8V}{V_{OUT1} - 0.8V}$$

If the output voltage desired is 0.8V, simply route VOUT1 back to the FB pin through R1, but do not populate R4.

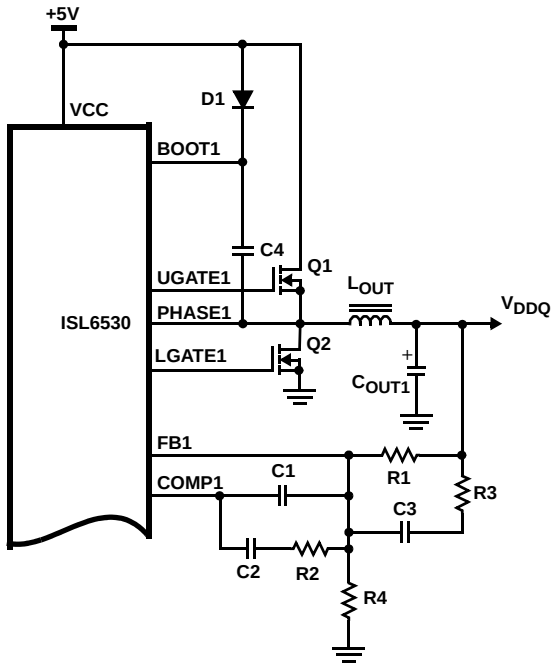


FIGURE 3. OUTPUT VOLTAGE SELECTION OF V_{DDQ}

V_{TT} Reference Overdrive

The ISL6530 allows the designer to bypass the internal 50% tracking of V_{DDQ} that is used as the reference for V_{TT}. The ISL6530 was designed to divide down the V_{DDQ} voltage by 50% through two internal matched resistances. These resistances are typically 200kΩ.

One method that may be employed to bypass the internal V_{TT} reference generation is to supply an external reference directly to the V_{REF_IN} pin. When doing this the SENSE1 pin must remain unconnected. Caution must be exercised when using this method as the V_{TT} regulator does not employ a soft-start of its own.

A second method would be to overdrive the internal resistors. Figure 4 shows how to implement this method. The external resistors used to overdrive the internal resistors should be less than 2kΩ and have a tolerance of 1% or better. This method still supplies a buffer between the resistor network and any loading on the V_{REF} pin. If there is no loading on the V_{REF} pin, then no buffering is necessary and the reference voltage created by the resistor network can be tied directly to V_{REF}.

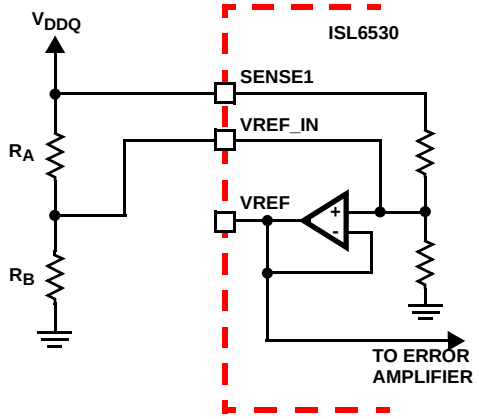


FIGURE 4. V_{TT} REFERENCE OVERDRIVE

Converter Shutdown

Pulling and holding the OCSET/SD pin below 0.8V will shutdown both regulators. During this state, PGOOD will be held LOW. Upon release of the OCSET/SD pin, the IC enters into a soft start cycle which brings both outputs back into regulation.

Voltage Monitoring

The ISL6530 offers a PGOOD signal that will communicate whether the regulation of both V_{DDQ} and V_{TT} are within ±15% of regulation, the V2_SD pin is held low and the bias voltage of the IC is above the POR level. If all the criteria above are true, the PGOOD pin will be at a high impedence level. When one or more of the criteria listed above are false, the PGOOD pin will be held low.

Overcurrent Protection

The overcurrent function protects the converter from a shorted output by using the upper MOSFET on-resistance, $r_{DS(ON)}$, of V_{DDQ} to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the overcurrent trip level (see Figure 1). An internal 40µA (typical) current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET of V_{DDQ} (also referenced to V_{IN}) exceeds the voltage across R_{OCSET} , the overcurrent function initiates a soft-start sequence.

Figure 5 illustrates the protection feature responding to an over current event on V_{DDQ}. At time T0, an over current condition is sensed across the upper MOSFET of the V_{DDQ} regulator. As a result, both regulators are quickly shutdown and the internal soft-start function begins producing soft-start ramps. The delay interval seen by the output is equivalent to three soft-start cycles. The fourth internal soft-start cycle initiates a normal soft-start ramp of the output, at time T1. Both outputs are brought back into regulation by time t2, as long as the overcurrent event has cleared.

Had the cause of the overcurrent still been present after the delay interval, the overcurrent condition would be sensed and both regulators would be shut down again for another delay interval of three soft-start cycles. The resulting hiccup mode style of protection would continue to repeat indefinitely.

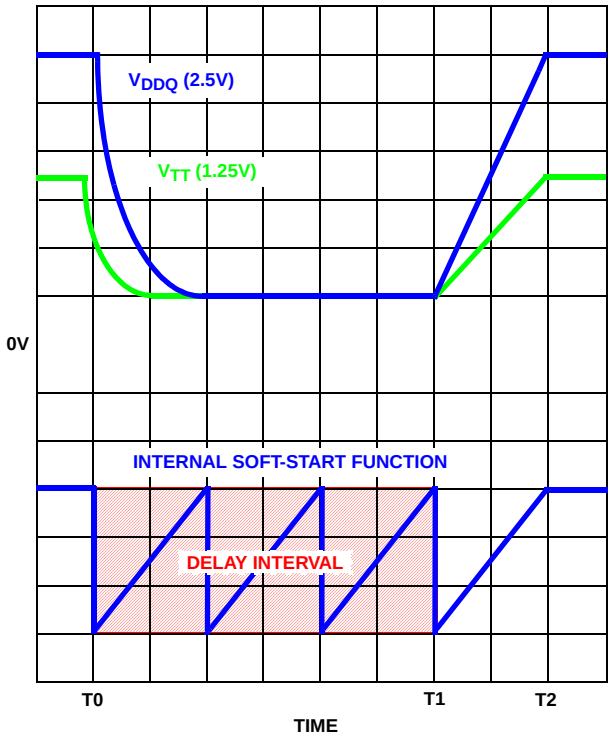


FIGURE 5. OVERCURRENT PROTECTION RESPONSE

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (40µA typical). The OC trip point varies mainly due to the MOSFET

$r_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled *Output Inductor Selection*.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Current Sinking

The ISL6530 V_{TT} regulator incorporates a MOSFET shoot-through protection method which allows the converter to sink current as well as source current. Care should be exercised when designing a converter with the ISL6530 when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the input rail of the regulator. If there is nowhere for this current to go, such as to other distributed loads on the rail or through a voltage limiting protection device, the capacitance on this rail will absorb the current. This situation will allow the voltage level of the input rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of any components attached to the input rail, then those components may experience an irreversible failure or experience stress that may shorten their lifespan. Ensuring that there is a path for the current to flow other than the capacitance on the rail will prevent this failure mode.

To insure that the current does not boost up the input rail voltage of the V_{TT} regulator, it is recommended that the input rail of the V_{TT} regulator be the output of the V_{DDQ} regulator. The current being sunk by the V_{TT} regulator will be fed into the V_{DDQ} rail and then drawn into the DDR SDRAM memory module and back into the V_{TT} regulator. Figure 6 shows the recommended configuration and the resulting current loop.

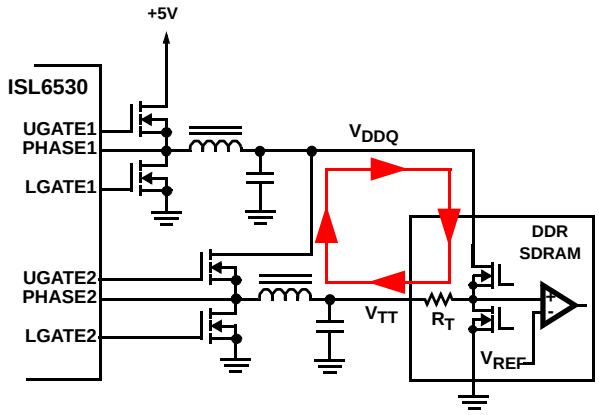


FIGURE 6. V_{TT} CURRENT SINKING LOOP

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 300kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes the voltage spikes in the converters.

As an example, consider the turn-off transition of the PWM MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the ISL6530. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 7 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power

nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

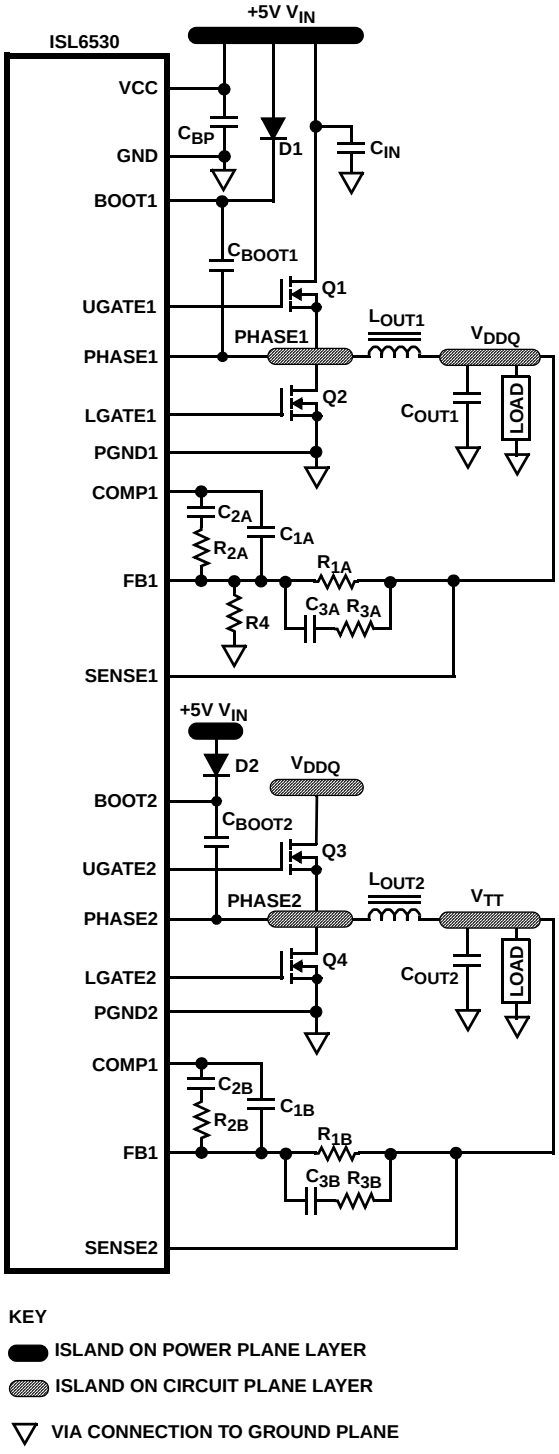


FIGURE 7. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

The switching components should be placed close to the ISL6530 first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper MOSFET and lower diode and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position the bypass capacitor, C_{BP}, close to the VCC pin with a via directly to the ground plane. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors for both regulators should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.

Feedback Compensation

Figure 8 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the ISL6530) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 7. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick gain (R_2/R_1) for desired converter bandwidth.
2. Place first zero below filter's double pole (~75% F_{LC}).
3. Place second zero at filter's double pole.
4. Place first pole at the ESR zero.
5. Place second pole at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin - repeat if necessary.

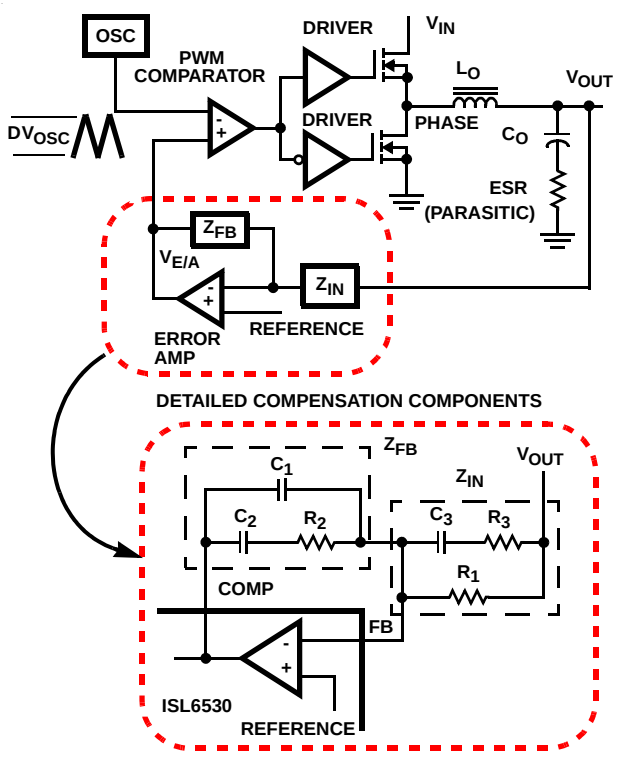


FIGURE 8. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figure 9 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 9. Using the above guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed loop gain is constructed on the graph of Figure 9 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

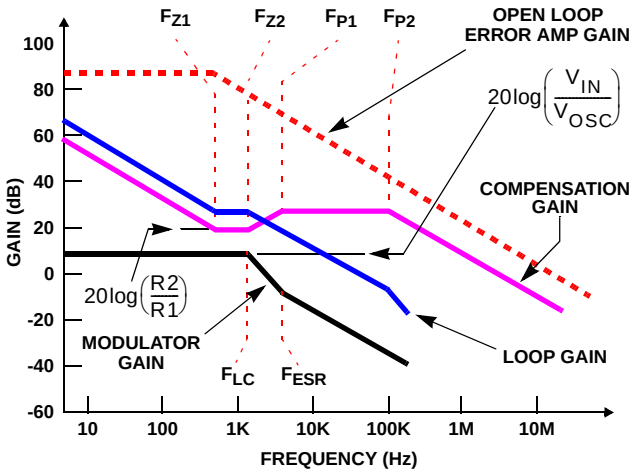


FIGURE 9. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern digital ICs can produce high transient load slew rates. High-frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6530 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through the following equation:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left({I_{OUT_{MAX}}}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge currentrating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6530 requires two N-Channel power MOSFETs for each PWM regulator. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. The V_{DDQ} regulator will only source current while the V_{TT} regulator can sink and source. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6530 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses.

LOSSES WHILE SOURCING CURRENT

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

LOSSES WHILE SINKING CURRENT

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the combined switch ON and OFF time, and
f_s is the switching frequency.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Given the reduced available gate bias voltage (5V), logic-level or sub-logic-level transistors should be used for both N-MOSFETs. Caution should be exercised when using devices with very low gate thresholds (V_{TH}). The shoot-through protection circuitry may be circumvented by these MOSFETs. Very high dv/dt transitions on the phase node may cause the Miller capacitance to couple the lower gate with the phase node and cause an undesireable turn on of the lower MOSFET while the upper MOSFET is on.

Bootstrap Component Selection

External bootstrap components, a diode and capacitor, are required to provide sufficient gate enhancement to the upper MOSFET. The internal MOSFET gate driver is supplied by the external bootstrap circuitry as shown in Figure 10. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle, when D_{BOOT} conducts, to a voltage of VCC less the boot diode drop, V_D, plus the voltage rise across Q_{LOWER}.

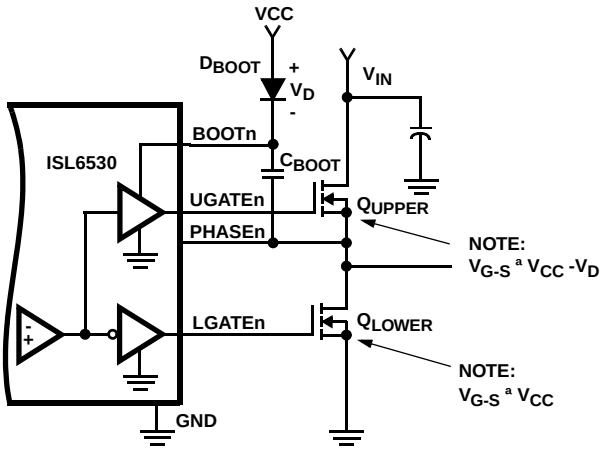


FIGURE 10. UPPER GATE DRIVE BOOTSTRAP

Just after the PWM switching cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is at its lowest point during the switching cycle. The charge lost on the bootstrap capacitor will be equal to the charge transferred to the equivalent gate-source capacitance of the upper MOSFET as shown:

$$Q_{GATE} = C_{BOOT} \times (V_{BOOT1} - V_{BOOT2})$$

where Q_{GATE} is the maximum total gate charge of the upper MOSFET, C_{BOOT} is the bootstrap capacitance, V_{BOOT1} is the bootstrap voltage immediately before turn-on, and V_{BOOT2} is the bootstrap voltage immediately after turn-on.

The bootstrap capacitor begins its refresh cycle when the gate drive begins to turn-off the upper MOSFET. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the switching frequency and duty cycle.

The minimum bootstrap capacitance can be calculated by rearranging the previous equation and solving for C_{BOOT}.

$$C_{BOOT} \geq \frac{Q_{GATE}}{V_{BOOT1} - V_{BOOT2}}$$

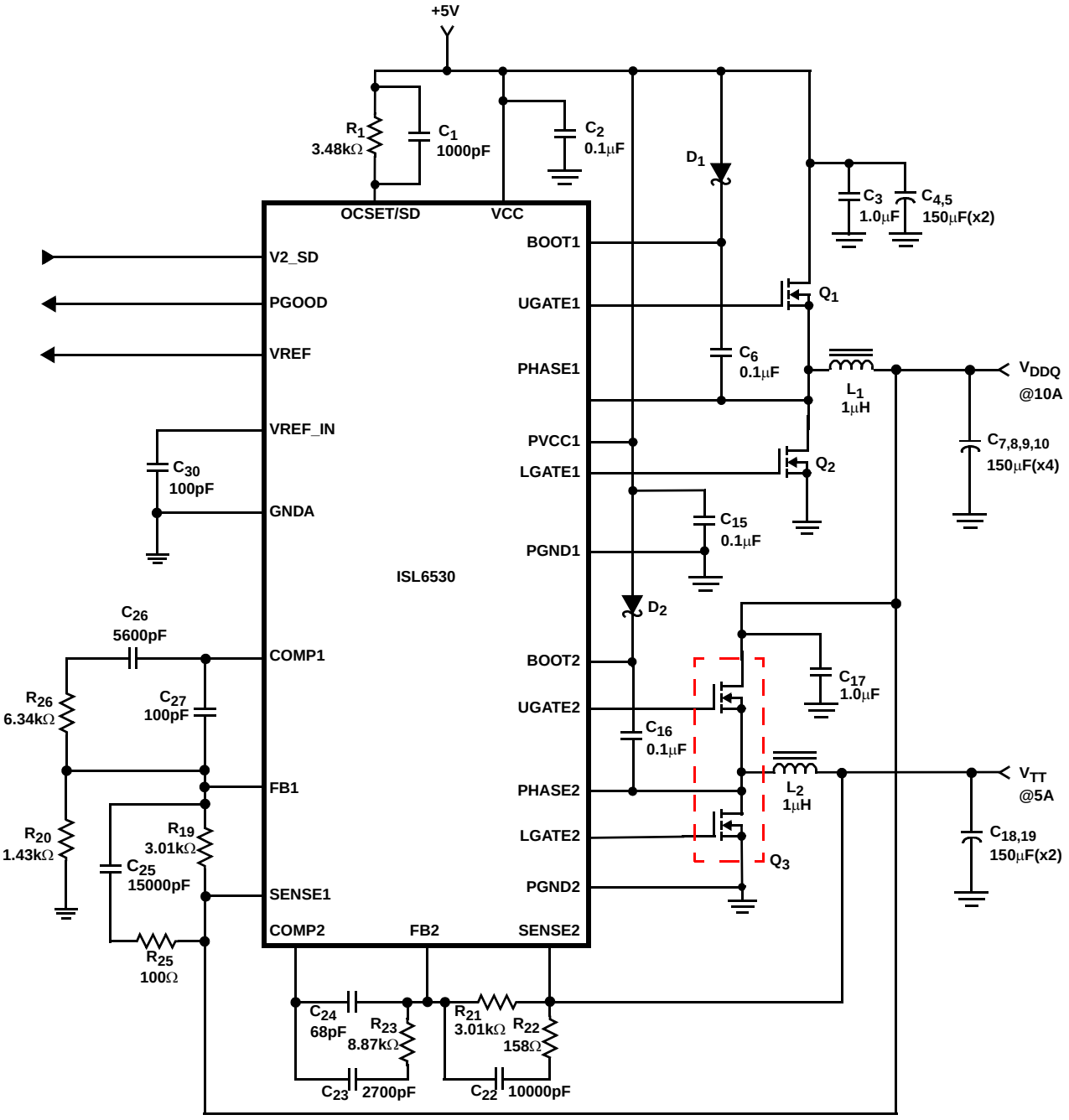
Typical gate charge values for MOSFETs considered in these types of applications range from 20 to 100nC. Since the voltage drop across Q_{LOWER} is negligible, V_{BOOT1} is simply VCC - V_D. A Schottky diode is recommended to minimize the voltage drop across the bootstrap capacitor during the on-time of the upper MOSFET. Initial calculations with V_{BOOT2} no less than 4V will quickly help narrow the bootstrap capacitor range.

For example, consider an upper MOSFET is chosen with a maximum gate charge, Q_g, of 100nC. Limiting the voltage drop across the bootstrap capacitor to 1V results in a value of no less than 0.1µF. The tolerance of the ceramic capacitor should also be considered when selecting the final bootstrap capacitance value.

A fast recovery diode is recommended when selecting a bootstrap diode to reduce the impact of reverse recovery charge loss. Otherwise, the recovery charge, Q_{RR}, would have to be added to the gate charge of the MOSFET and taken into consideration when calculating the minimum bootstrap capacitance.

ISL6530 DC-DC Converter Application Circuit

Figure 11 shows an application circuit for a DDR SDRAM power supply, including V_{DDQ} (+2.5V) and V_{TT} (+1.25V). Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN9993.



Component Selection Notes:

C4,5,7,8,9,10,18,19 - Each 150mF, Panasonic EEF-UE0J151R

D1,2 - Each 30mA Schottky Diode, MA732

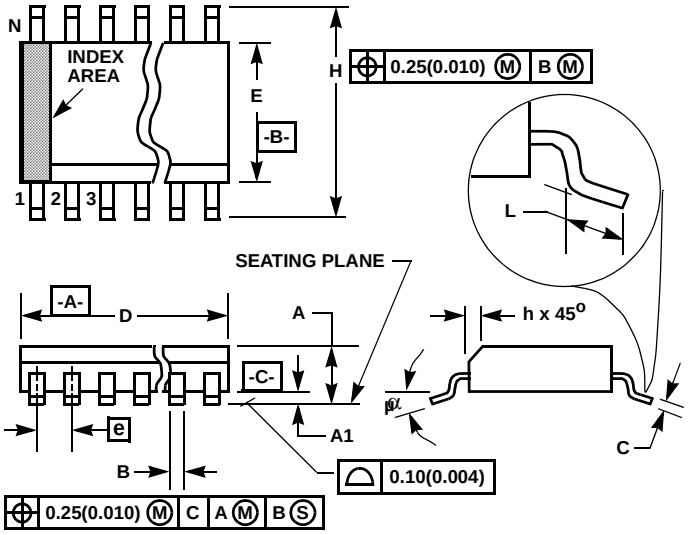
L1,2 - Each 1mH Inductor, Panasonic P/N ETQ-P6F1ROSFA

Q1,2 - Each Fairchild MOSFET; ITF86130DK8

Q3 - Fairchild MOSFET; ITF86110DK8

FIGURE 11. DDR SDRAM VOLTAGE REGULATOR

Small Outline Plastic Packages (SOIC)



NOTES:

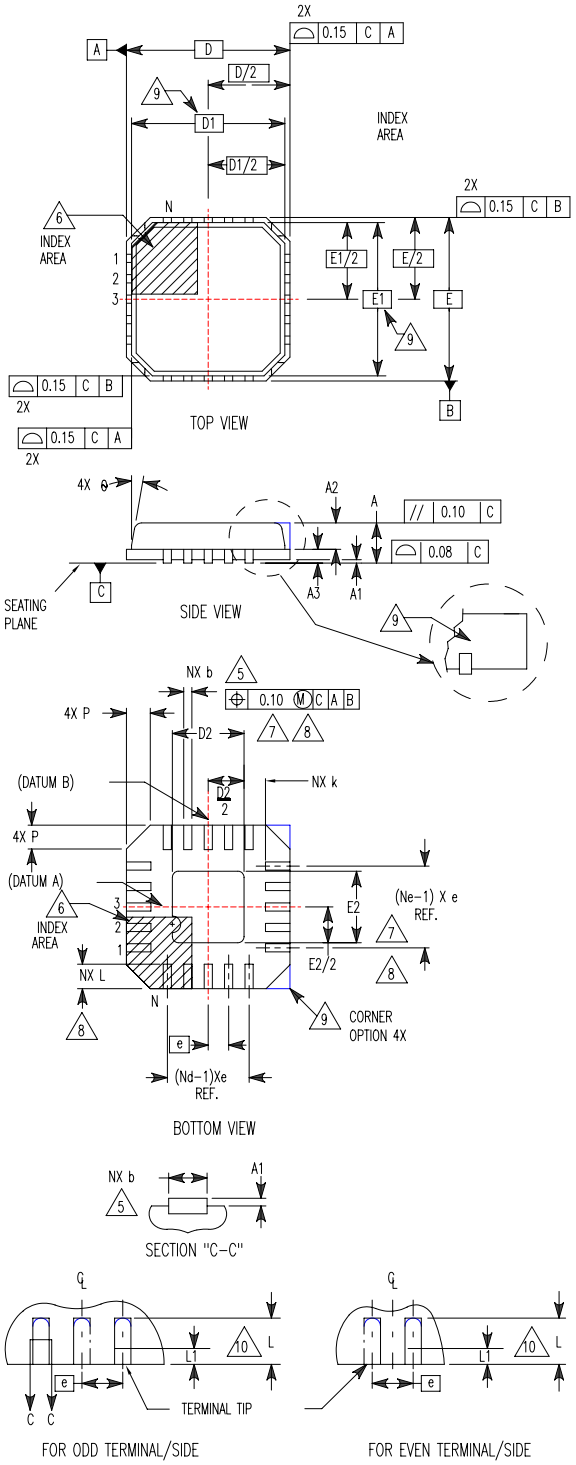
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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