ISL76120

Automotive Grade USB 2.0 High/Full Speed Multiplexer

FN6711
Rev 3.00
January 9, 2015

The Intersil ISL76120 dual 2:1 multiplexer IC is a single supply part that can operate from a single 2.7V to 5.5V supply. It contains two SPDT (Single Pole/Double Throw) switches configured as a DPDT. The part was designed for switching between USB high-speed and USB full-speed sources in portable battery powered products.

The normally-closed (NC) FSx switches can swing rail-to-rail and were specifically designed to pass USB full speed data signals (12Mbps) that range from 0V to 3.6V. The normally-open (NO) HSx switches have high bandwidth and low capacitance and were specifically designed to pass USB high speed data signals (480Mbps) with minimal distortion.

The part can be used in a variety of automotive entertainment and infotainment applications where consumer USB devices such as Portable Media Players (PMPs) are to be connected to embedded systems. The product allows switching between a high-speed transceiver and a full-speed transceiver while connected to a single USB host. Additionally, the part can be used for charge control of PMPs.

The digital logic inputs are 1.8V logic compatible when operated with a 2.7V to 3.6V supply. The part has an enable pin to open all switches. It can be used to facilitate proper bus disconnect and connection when switching between the USB sources.

The ISL76120 is available in a 10 Ld 3mmx3mm TDFN package. It operates across a temperature range of -40°C to +105°C.

Features

- High speed (480Mbps) and full speed (12Mbps) signaling capability per USB 2.0
- 1.8V logic compatible (2.7V to +3.6V supply)
- Enable pin to open all switches, simplifies multiple USB client management
- -3dB frequency
  - HSx switches 880MHz
  - FSx switches 550MHz
- Crosstalk at 1MHz . . . . . -70dB
- Off-isolation at 100kHz . . . . . -98dB
- Single supply operation (V_{DD}) . . . . . 2.7V to 5.5V
- Available in TDFN package
- Robust ESD rating . . . . . > 8.5kV HBM
- Ultra-low operating current 60nA
- -40°C to +105°C Operation
- AEC-Q100 qualified component
- Pb-Free (RoHS Compliant)

Applications

- Automotive
  - USB docks
  - MP3 and PMP player attach kits
  - Infotainment systems
- After market automotive options

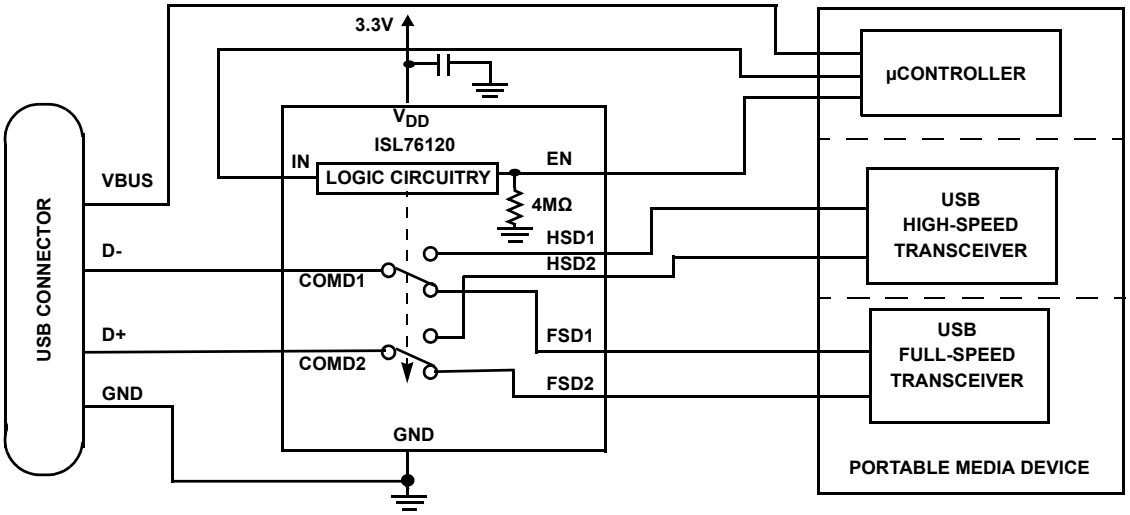
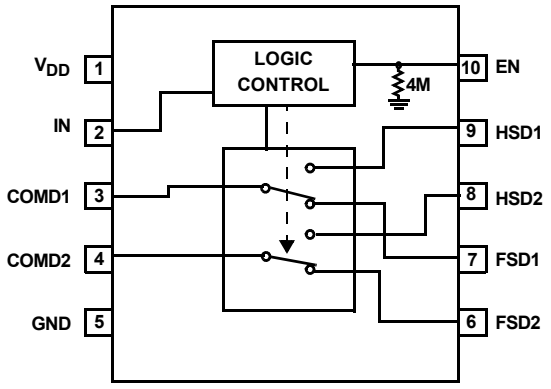


FIGURE 1. APPLICATION BLOCK DIAGRAM

Pin Configuration

ISL76120
(10 LD TDFN)
TOP VIEW



NOTE:
1. ISL76120 Switches Shown for IN = Logic “0” and EN = Logic “1”.

Truth Table

ISL76120			
EN	IN	FSD1, FSD2	HSD1, HSD2
1	0	ON	OFF
1	1	OFF	ON
0	X	OFF	OFF

Logic “0” when ≤0.5V, Logic “1” when ≥1.4V with a 2.7V to 3.6V Supply. X = Don’t Care

Pin Descriptions

ISL76120		
PIN NUMBER	NAME	FUNCTION
1	V_{DD}	Power Supply
2	IN	Select Logic Control Input
3	COMD1	USB Common Port
4	COMD2	USB Common Port
5	GND	Ground Connection
6	FSD2	Full Speed USB Differential Port
7	FSD1	Full Speed USB Differential Port
8	HSD2	High Speed USB Differential Port
9	HSD1	High Speed USB Differential Port
10	EN	Bus Switch Enable

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL76120ARTZ	6120	-40 to +105	10 Ld 3x3 TDFN	L10.3x3A

NOTES:
2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for ISL76120. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to 6.0V
Input Voltages
FSD2, FSD1, HSD2, HSD1 (Note 5) . . . . . - 1V to ((V_{DD}) +0.3V)
IN, EN (Note 5) . . . . . -0.3V to ((V_{DD}) +0.3V)
Output Voltages
COMD1, COMD2 (Note 5) . . . . . -1V to 5V
Continuous Current (HSD2, HSD1, FSD2, FSD1) . . . . . ±40mA
Peak Current (HSD2, HSD1, FSD2, FSD1)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 TDFN Package (Notes 6, 7)	50	9

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
V_{DD} Supply Voltage Range . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Signals on FSD1, FSD2, HSD1, HSD2, COMD1, COMD2, EN, IN exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 8). **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
ANALOG SWITCH CHARACTERISTICS						
NC Switches (FSD1, FSD2)						
Analog Signal Voltage Range, V_{ANALOG}	V_{DD} = 3.3V, IN = 0V, EN = 3.3V	Full	**0**	-	**V_{DD}**	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = 0V to 3.3V (see Figure 5)	+25	-	7	10	Ω
		Full	-	7.8	**15**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = Voltage at max r_{ON} over signal range of 0V to 3.3V (Note 12)	+25	-	0.1	1.2	Ω
		Full	-	0.7	**1.4**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = 0V to 3.3V (Note 11)	+25	-	4	6	Ω
		Full	-	4.1	**8**	Ω
OFF Leakage Current, $I_{FSX(OFF)}$	V+ = 3.6V, IN = 3.6V, EN = 0V and 3.6V, V_{COMx} = 0.3V, 3V, V_{FSX} = 3V, 0.3V	+25	-20	0.4	20	nA
		Full	**-70**	0.6	**70**	nA
ON Leakage Current, $I_{FSX(ON)}$	V+ = 3.6V, IN = 0V, EN = 3.6V, V_{COMx} = 0.3V, 3V, V_{FSX} = 0.3V, 3V	+25	-20	2	20	nA
		Full	**-70**	4.7	**70**	nA
NO Switches (HSD1, HSD2)						
Analog Signal Voltage Range, V_{ANALOG}	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V	Full	**0**	-	**V_{DD}**	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 1mA, V_{HSD2} or V_{HSD1} = 3.3V (see Figure 4)	+25	-	25	30	Ω
		Full	-	29	**35**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = 0V to 400mV (see Figure 4)	+25	-	4.5	6	Ω
		Full	-	5.1	**9**	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = Voltage at max r_{ON}, Voltage at max r_{ON} over signal range of 0V to 400mV (Note 12)	+25	-	0.2	1.3	Ω
		Full	-	0.7	**1.5**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = 0V to 400mV (Note 11)	+25	-	0.4	1	Ω
		Full	-	0.43	**1.5**	Ω

Electrical Specifications

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 8).
Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
OFF Leakage Current, $I_{HSD2(OFF)}$ or $I_{HSD1(OFF)}$	V_{DD} = 3.6V, IN = 0V, EN = 0 and 3.6V, V_{COMD1} or V_{COMD2} = 3V, 0.3V, V_{HSD2} or V_{HSD1} = 0.3V, 3V	+25	-20	0.3	20	nA
		Full	**-70**	1	**70**	nA
ON Leakage Current, $I_{HSD2(ON)}$ or $I_{HSD1(ON)}$	V_{DD} = 3.6V, IN = 3.6V, EN = 3.6V, V_{COMD1} or V_{COMD2} = 0.3V, 3.0V, V_{HSD2} or V_{HSD1} = 0.3V, 3.0V	+25	-20	4.8	20	nA
		Full	**-70**	5	**70**	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF (see Figure 2)	+25	-	25	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF (see Figure 2)	+25	-	15	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF (see Figure 3)	+25	-	7	-	ns
Skew, t_{SKEW} (HSx Switch)	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 720ps at 480Mbps, (Duty Cycle = 50%) (see Figure 8)	+25	-	50	-	ps
Total Jitter, t_J (HSx Switch)	V_{DD} =3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 720ps at 480Mbps	+25	-	210	-	ps
Propagation Delay, t_{PD} (HSx Switch)	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF (see Figure 8)	+25	-	250	-	ps
Skew, t_{SKEW} (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, t_R = t_F = 12ns at 12Mbps, (Duty Cycle = 50%) (see Figure 8)	+25	-	0.15	-	ns
Rise/Fall Time Mismatch, t_M (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, t_R = t_F = 12ns at 12Mbps, (Duty Cycle = 50%)	+25	-	10	-	%
Total Jitter, t_J (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, t_R = t_F = 12ns at 12Mbps	+25	-	1.6	-	ns
Propagation Delay, t_{PD} (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF (see Figure 8)	+25	-	0.9	-	ns
Crosstalk	V_{DD} = 3.3V, R_L = 45Ω, f = 1MHz (see Figure 7)	+25	-	-70	-	dB
Off Isolation	V_{DD} = 3.3V, R_L = 45Ω, f = 100kHz	+25	-	-98	-	dB
FSx Switch -3dB Bandwidth	Signal = -10dBm, 1.0VDC offset, R_L = 45Ω, C_L = 5pF	+25	-	550	-	MHz
HSx Switch -3dB Bandwidth	Signal = -10dBm, 0.2VDC offset, R_L = 45Ω, C_L = 5pF	+25	-	880	-	MHz
HSx OFF Capacitance, C_{HSxOFF}	f = 1MHz, V_{DD} = 3.3V, IN = 0V, EN = 3.3V, V_{HSD1} or V_{HSD2} = V_{COMx} = 0V (see Figure 6)	+25	-	6	-	pF
FSx OFF Capacitance, C_{FSxOFF}	f = 1MHz, V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, V_{FSD1} or V_{FSD2} = V_{COMx} = 0V (see Figure 6)	+25	-	9	-	pF
COM ON Capacitance, $C_{COMX(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, V_{HSD1} or V_{HSD2} = V_{COMx} = 0V (see Figure 6)	+25	-	12	-	pF
COM ON Capacitance, $C_{COMX(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 0V, EN = 3.3V, V_{FSD1} or V_{FSD2} = V_{COMx} = 0V (see Figure 6)	+25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**	-	**5.5**	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, IN = 0V or 3.6V, EN = 0V or 3.6V	+25	-	20	60	nA
		Full	-	114	**250**	nA

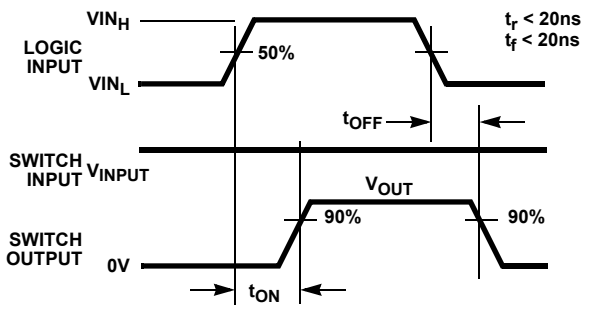
Electrical Specifications Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 8). **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}, V_{ENL}	V_{DD} = 2.7V to 3.6V	+25	-	-	0.5	V
Input Voltage High, V_{INH}, V_{ENH}	V_{DD} = 2.7V to 3.6V	+25	1.4	-	-	V
Input Current, I_{INL}, I_{ENL}	V_{DD} = 3.6V, IN = 0V, EN = 0V	Full	-	10	-	nA
Input Current, I_{INH}	V_{DD} = 3.6V, IN = 3.6V	Full	-	10	-	nA
Input Current, I_{ENH}	V_{DD} = 3.6V, EN = 3.6V	Full	-	1	-	µA

NOTES:

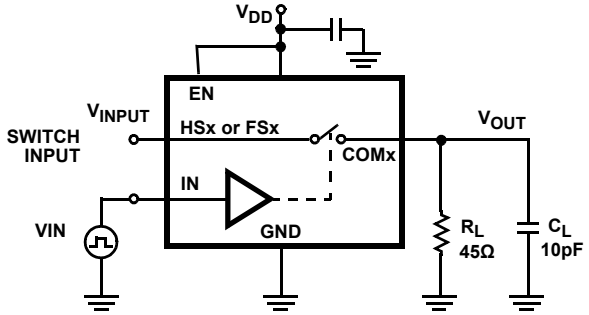
8. V_{LOGIC} = Input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
11. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal voltage range.
12. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between HSD2 and HSD1 or between FSD2 and FSD1.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 2B. TEST CIRCUIT

FIGURE 2. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

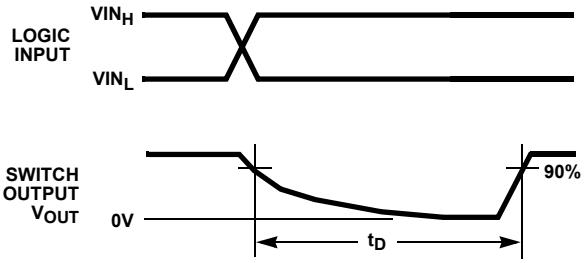
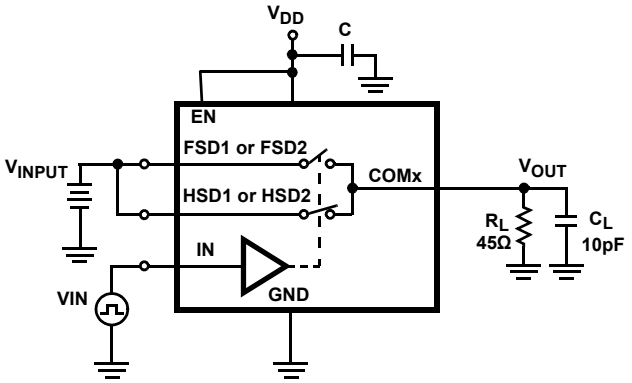


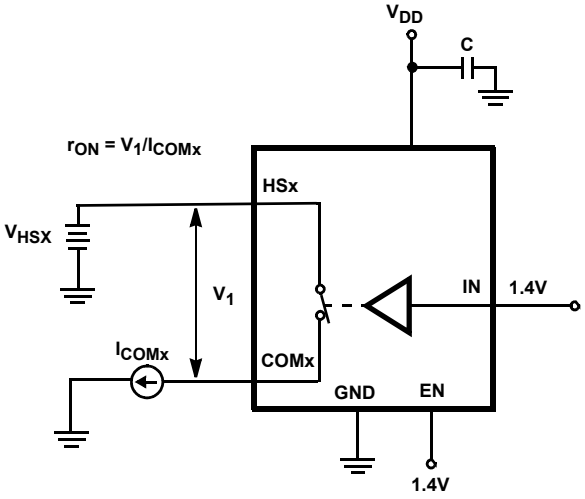
FIGURE 3A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

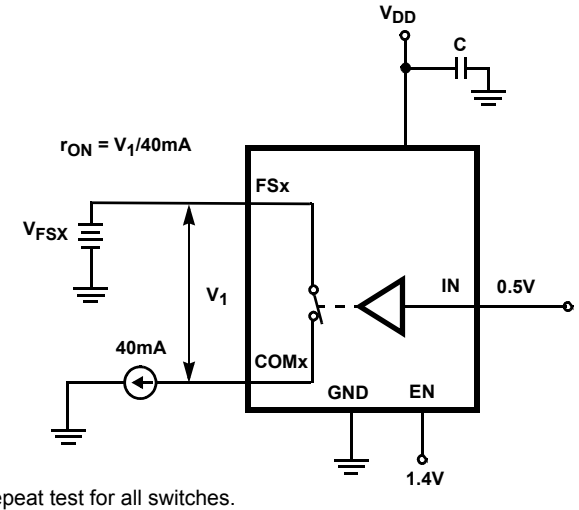
FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

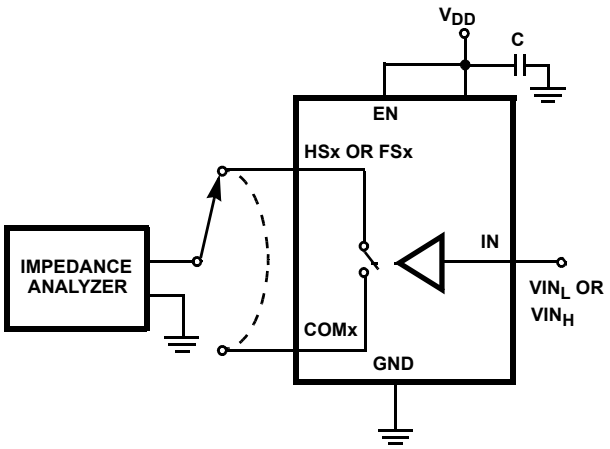
FIGURE 4. HSx SWITCH r_{ON} TEST CIRCUIT



Repeat test for all switches.

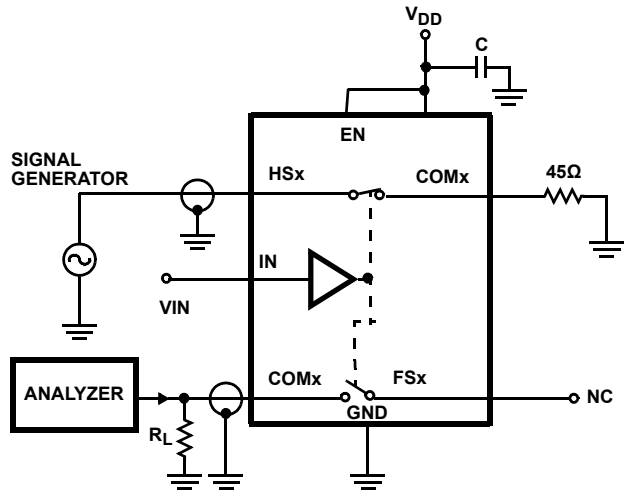
FIGURE 5. FSx SWITCH r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



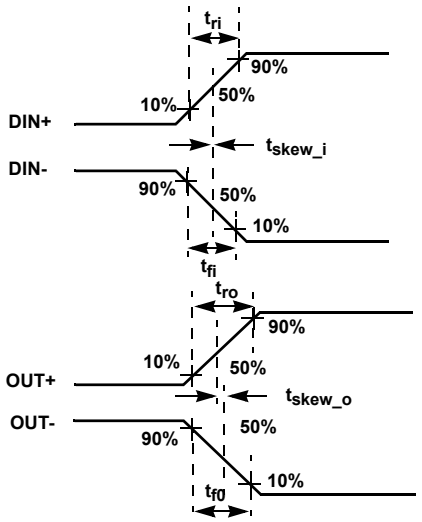
Repeat test for all switches.

FIGURE 6. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 7. CROSSTALK TEST CIRCUIT



$|t_{ro}-t_{ri}|$ Change Due to Switch for Rising Input and Rising Output Signals.

$|t_{fo}-t_{fi}|$ Change Due to Switch for Falling Input and Falling Output Signals.

$|t_{skew\_0}|$ Skew through the Switch for Output Signals.

$|t_{skew\_i}|$ Skew through the Switch for Input Signals.

FIGURE 8A. MEASUREMENT POINTS

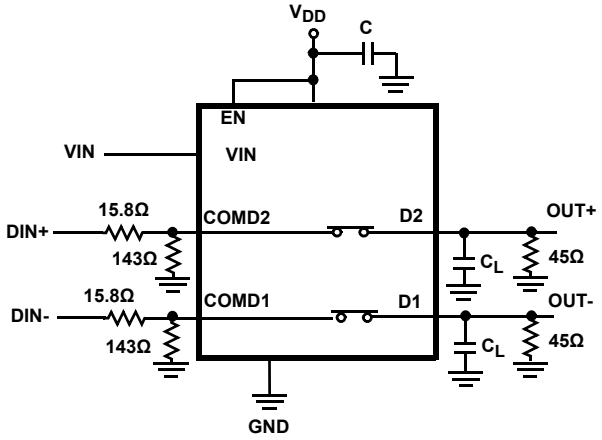
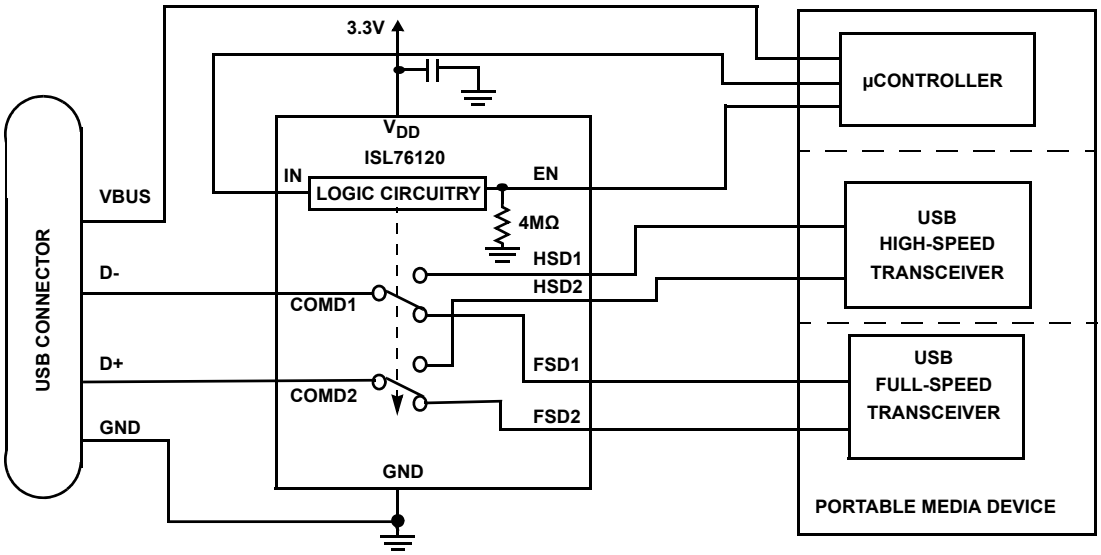


FIGURE 8B. TEST CIRCUIT

FIGURE 8. SKEW TEST

Application Block Diagram



Detailed Description

The ISL76120 device is a dual single pole/double throw (SPDT) analog switch that operates from a single DC power supply in the range of 2.7V to 5.5V. It was designed to function as a dual 2-to-1 multiplexer to select between a USB high-speed transceiver and a USB full-speed transceiver in automotive applications. It is offered in a TDFN package for use in automotive Portable Media Player docking stations and Apple iPod type players. The device has an enable pin to open all switches.

The part consists of two full speed (FSx) switches and two high-speed (HSx) switches. The FSx switches can swing from 0V to V_{DD}. They were designed to pass USB full-speed (12Mbps) differential data signals with minimal distortion. The HSx switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion.

The ISL76120 was designed for automotive USB applications such as docking stations for Portable Media Players and other general purpose USB connections that have both high-speed and full-speed transceivers and need to multiplex between these USB sources to a single USB host (computer). This functionality is shown in the "Application Block Diagram" on page 8.

A detailed description of the two types of switches are provided in the following sections.

FSx Switches (FSD1, FSD2)

The two FSx switches (FSD1, FSD2) are bidirectional switches that can pass rail-to-rail signals. They were specifically designed to pass USB full-speed (12Mbps) differential signals and meet the USB 2.0 full-speed signal quality specifications see Figure 9.

The FSx switches can also pass USB high speed signals (480Mbps) but do not quite meet the USB 2.0 high speed signal quality eye diagram compliance requirement.

The maximum signal range for the FSx switches is from -1V to V_{DD}. The signal voltage should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1V.

When operated with a 2.7V to 3.6V supply, the FSx switches are active (turned ON) whenever the IN logic control voltage is ≤0.5V and the EN logic voltage ≥1.4V.

HSx Switches (HSD1, HSD2)

The two HSx switches (HSD2, HSD1) are bidirectional switches that can pass rail-to-rail signals. The ON-resistance is low and well matched between the HSD1 and HSD2 switches over the USB high-speed signal range, ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases.

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high-speed signal quality specifications (see Figures 10 and 11).

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling (see Figure 12).

The maximum signal range for the HSx switches is from -1V to V_{DD}. The signal voltage should not be allow to exceed the V_{DD} voltage rail or go below ground by more than -1V.

The HSx switches are active (turned ON) whenever the IN voltage is ≥1.4V and the EN logic voltage is ≥1.4V when operated with a 2.7V to 3.6V supply.

ISL76120 Operation

The discussion that follows will discuss using the ISL76120 in the "Application Block Diagram" on page 8.

POWER

The power supply connected at the V_{DD} (pin 1) provides the DC bias voltage required by the ISL76120 part for proper operation. The ISL76120 can be operated with a V_{DD} voltage in the range of 2.7V to 5.5V. When used in a USB application, the V_{DD} voltage should be kept in the range of 3.0V to 5.5V to ensure you get the proper signal levels for good signal quality.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the V_{DD} pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the V_{DD} pin as possible.

LOGIC CONTROL

The state of the ISL76120 device is determined by the voltage at the IN pin (pin 2) and the EN pin (pin 10). IN is only active when the EN pin is logic "1" (High). Refer to the "Truth Table" on page 2.

The EN pin is internally pulled low through a 4MΩ resistor to ground. For logic "0" (Low) it can be driven low or allowed to Float. The IN pin must be driven low or high and cannot be left floating.

Logic Control Voltage Levels

EN = Logic "0" (Low) when V_{EN} ≤0.5V or Floating.
EN = Logic "1" (High) when V_{EN} ≥1.4V
IN = Logic "0" (Low) when V_{IN} ≤0.5V.
IN = Logic "1" (High) when V_{IN} ≥1.4V

Full-speed Mode

If the IN pin = Logic “0” and the EN pin = Logic “1”, the part will be in the full-speed mode. In this mode, the FSD1 and FSD2 switches are ON and the HSD1 and HSD2 switches are OFF (high impedance). In a typical application, V_{DD} will be in the range of 2.8V to 3.6V and will be connected to the battery or LDO of the portable media device. When a computer or USB hub is plugged into the common USB connector and the part is in the full-speed mode, a link will be established between the full-speed driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 12Mbps.

High-speed Mode

If the IN pin = Logic “1” and the EN pin = Logic “1”, the part will go into high-speed mode. In high-speed mode, the HSD1 and HSD2 switches are ON and the FSD1 and FSD2 switches are OFF (high impedance). When a USB cable from a computer or USB hub is connected at the common USB connector and the part is in the high-speed mode, a link will be established between the high-speed driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 480Mbps.

All Switches OFF Mode

If the IN pin = Logic “0” or Logic “1” and the EN pin = Logic “0”, all of the switches will turn OFF (high impedance).

The all OFF state can be used to switch between the two USB sections of the media player. When disconnecting from one USB device to the other USB device, you can momentarily put the ISL76120 switch in the “all off” state in order to get the computer to disconnect from the one device so it can properly connect to the other USB device when that channel is turned ON.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified.

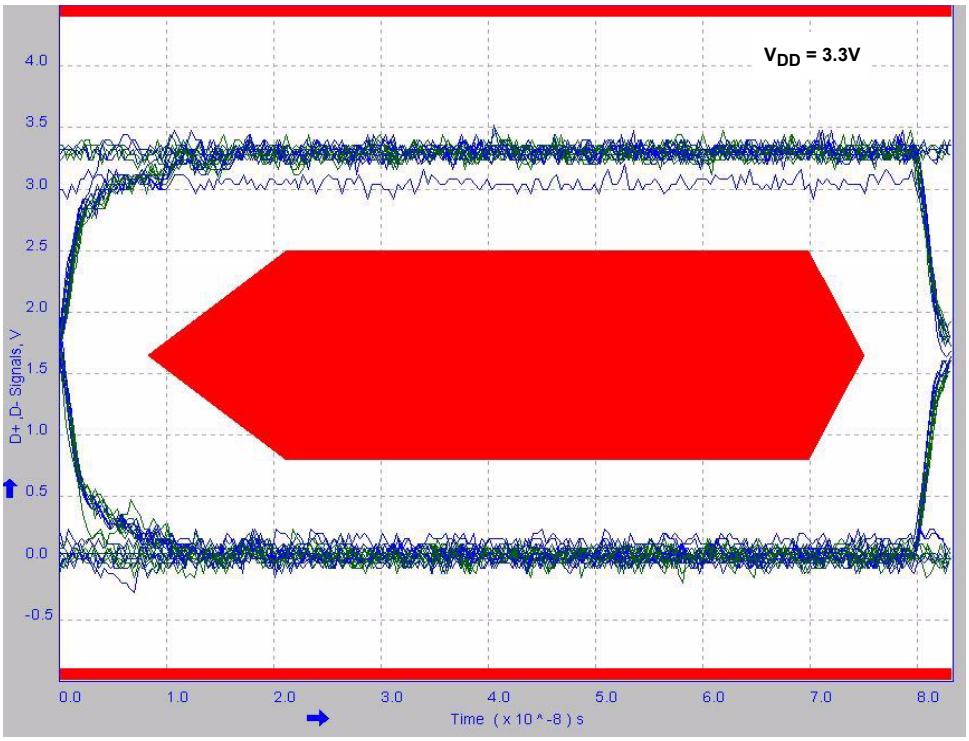


FIGURE 9. EYE PATTERN: 12MBPS USB SIGNAL WITH FSx SWITCHES IN THE SIGNAL PATH

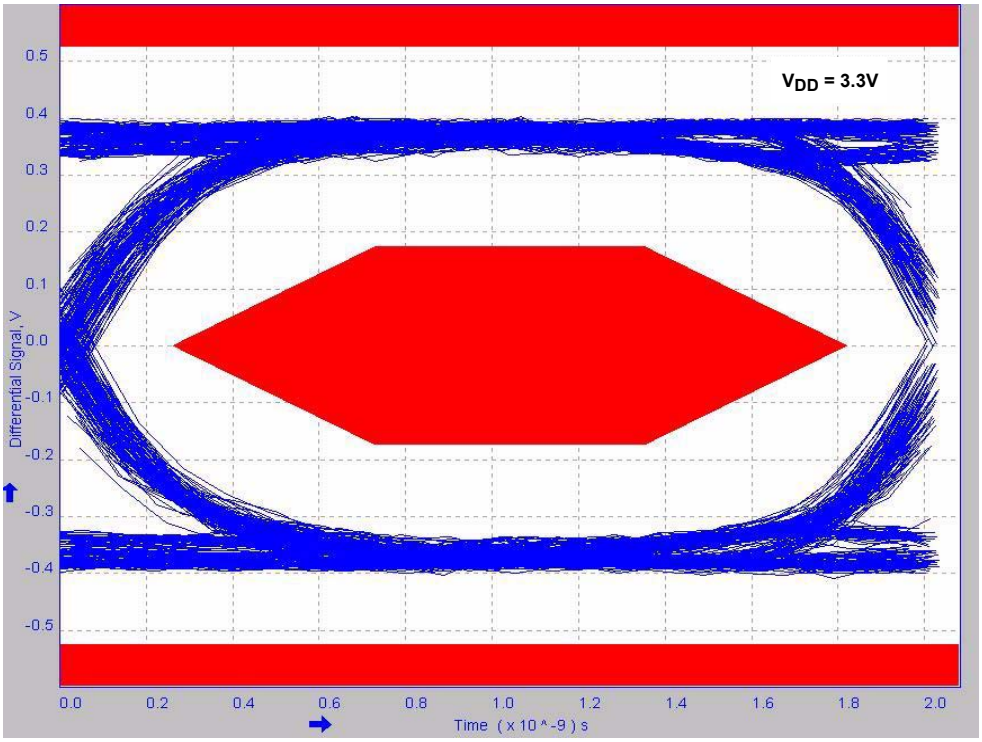


FIGURE 10. EYE PATTERN WITH FAR END MASK: 480MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

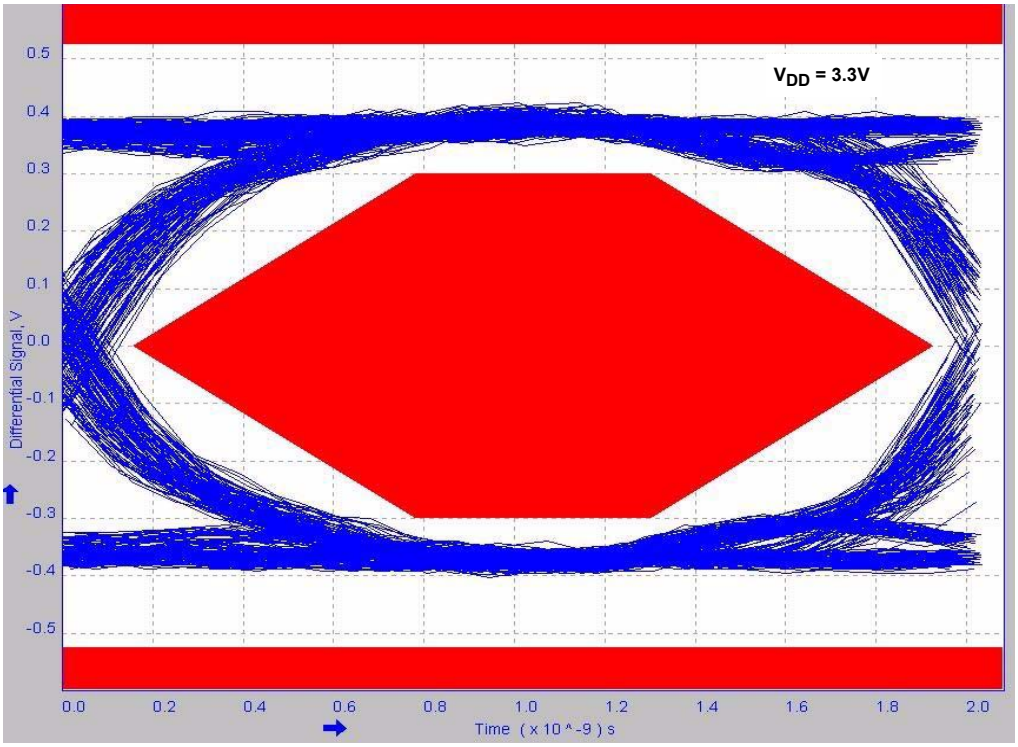


FIGURE 11. EYE PATTERN WITH NEAR END MASK: 480MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

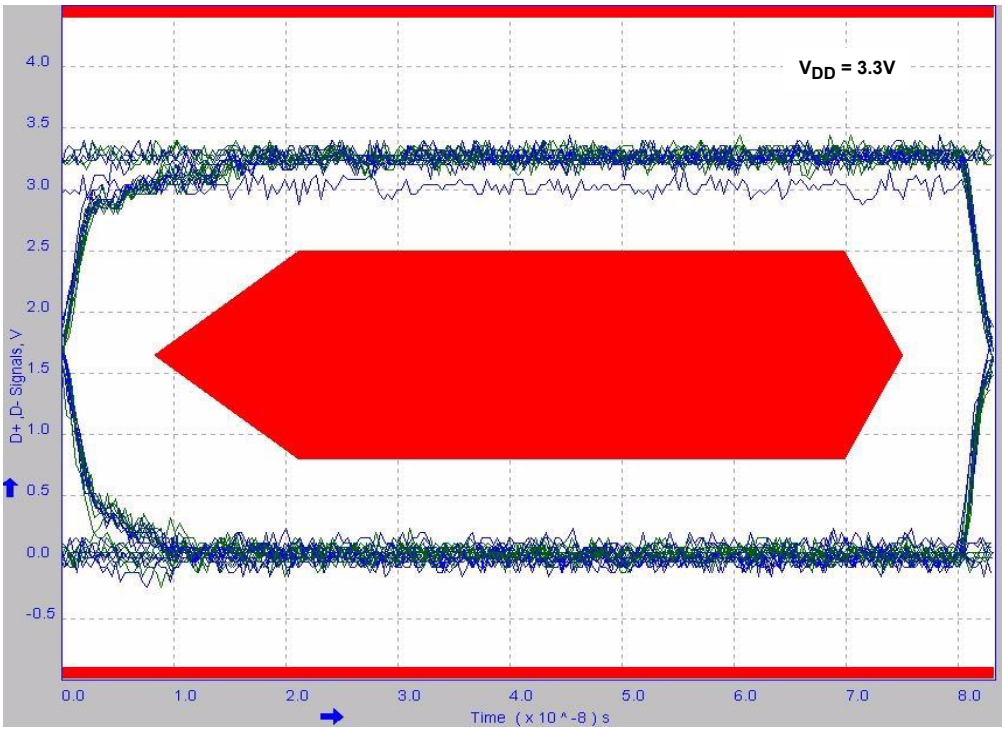


FIGURE 12. EYE PATTERN: 12MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

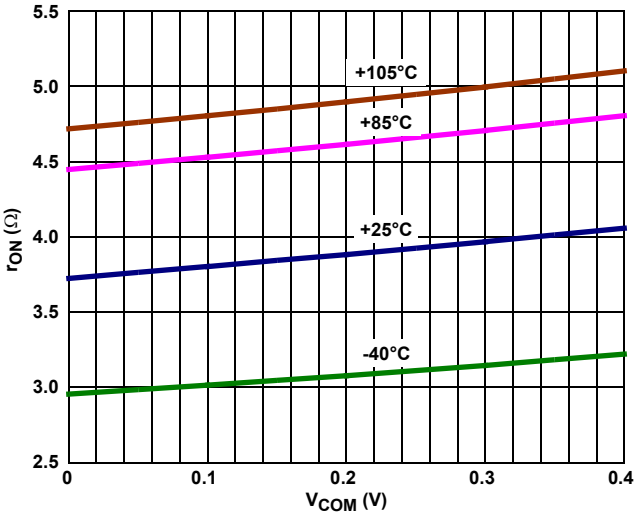


FIGURE 13. HSx SWITCH ON-RESISTANCE vs SWITCH VOLTAGE

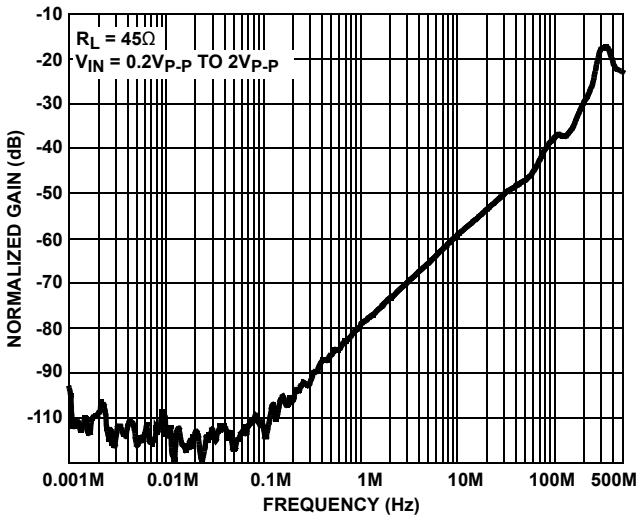


FIGURE 14. OFF-ISOLATION

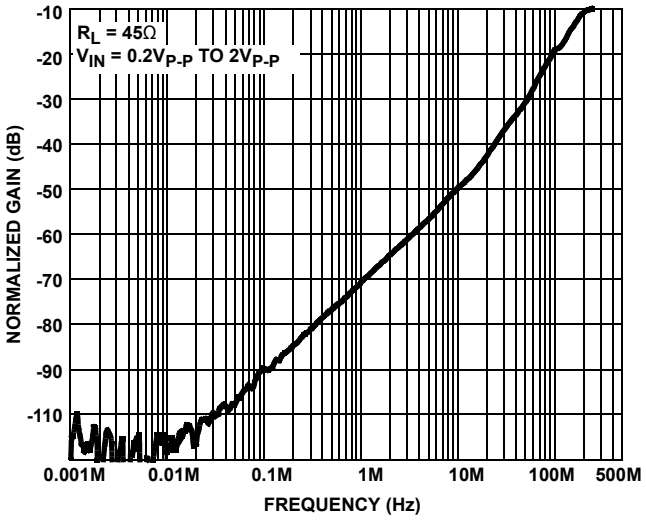


FIGURE 15. CROSSTALK

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (TDFN Paddle Connection: Tie to GND or Float)

TRANSISTOR COUNT:

98

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 9, 2015	FN6711.3	Converted to new template and implemented Intersil Standards. Added Revision History. In "Thermal Information" on page 3 changed theta JA from 55°C/W to 50°C/W. Added theta JC of 9°C/W. Revised Note 6 with new statement: Theta-JA is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379. Added Note 7: For theta-JC, the "case temperature" location is the center of the exposed metal pad on the package underside. Updated POD L10.3x3A with following changes: Added Typical Recommended Land Pattern Converted to new format by moving dimensions from table onto drawing (no dimension changes).

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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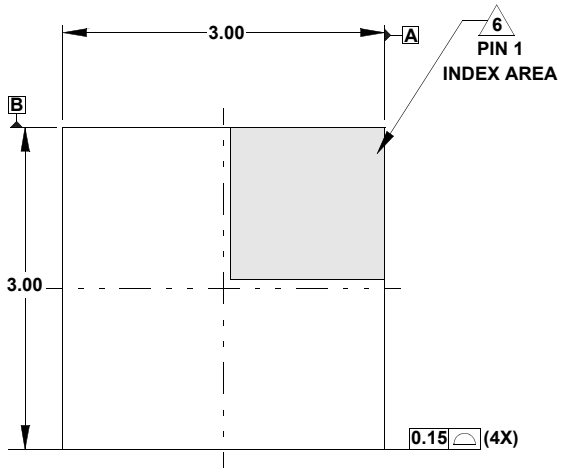
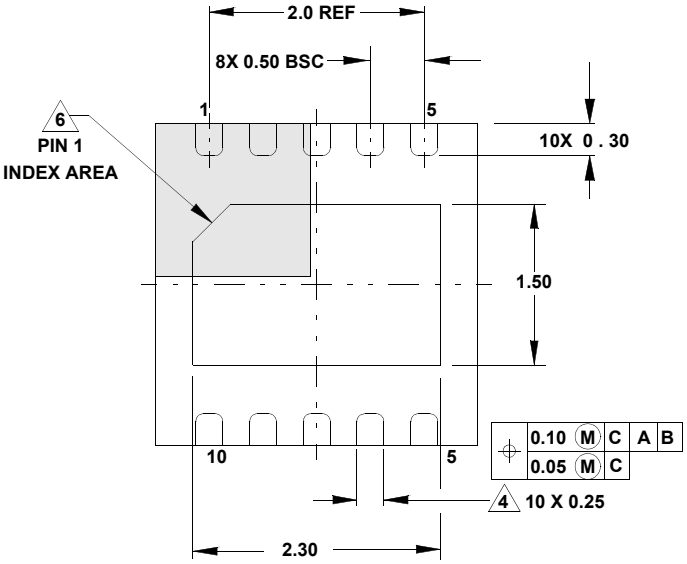
Package Outline Drawing

L10.3x3A

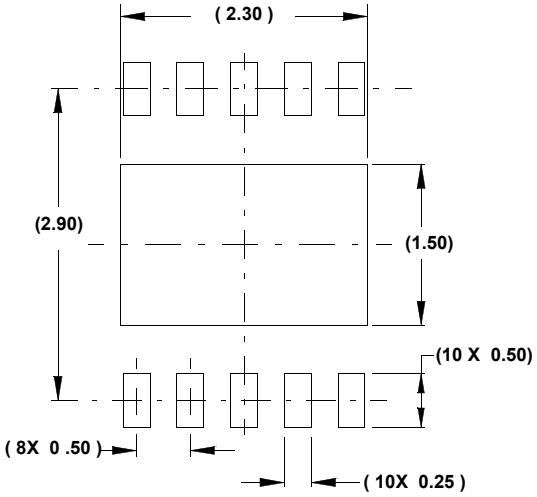
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



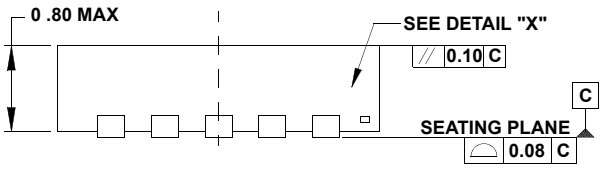
TOP VIEW



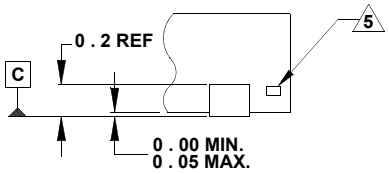
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).

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