# ISL76321

16-Bit Long-Reach Video Automotive Grade SERDES with Bi-directional Side-Channel

FN7803
Rev 2.00
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The ISL76321 is a serializer/deserializer of LVCMOS parallel video data. The video data presented to the serializer on the parallel LVCMOS bus is serialized into a high-speed differential signal. This differential signal is converted back to parallel video at the remote end by the deserializer. It also transports auxiliary data bi-directionally over the same link during the video vertical retrace interval. $I^2C$ bus mastering allows the placement of external slave devices on the remote side of the link. An $I^2C$ controller can be placed on either side of the link allowing bidirectional $I^2C$ communication through the link to the external devices on the other side. Both chips can be fully configured from a single controller or independently by local controllers.

## Related Literature

- ISL34341 Data Sheet "WSVGA 24-Bit Long-Reach Video SERDES with Bi-directional Side-Channel"

## Features

- 16-bit RGB transport over a single differential pair
- 6MHz to 50MHz pixel clock rates
- AEC-Q100 qualified component
- Bi-directional auxiliary data transport without extra bandwidth and over the same differential pair
- Hot-plugging with automatic resynchronization every HSYNC
- $I^2C$ bus mastering to the remote side of the link with a controller on either the serializer or deserializer
- Selectable clock edge for parallel data output
- DC-balanced with industry standard 8b/10b line code allows AC-coupling, providing immunity against ground shifts
- 16 programmable settings each for transmitter amplitude boost and pre-emphasis and receiver equalization, allow for longer cable lengths and higher data rates
- Slew rate control and spread spectrum capability on outputs reduce the potential for EMI
- Same device for serializer and deserializer simplifies inventory

## Applications

- Video entertainment systems
- Remote cameras

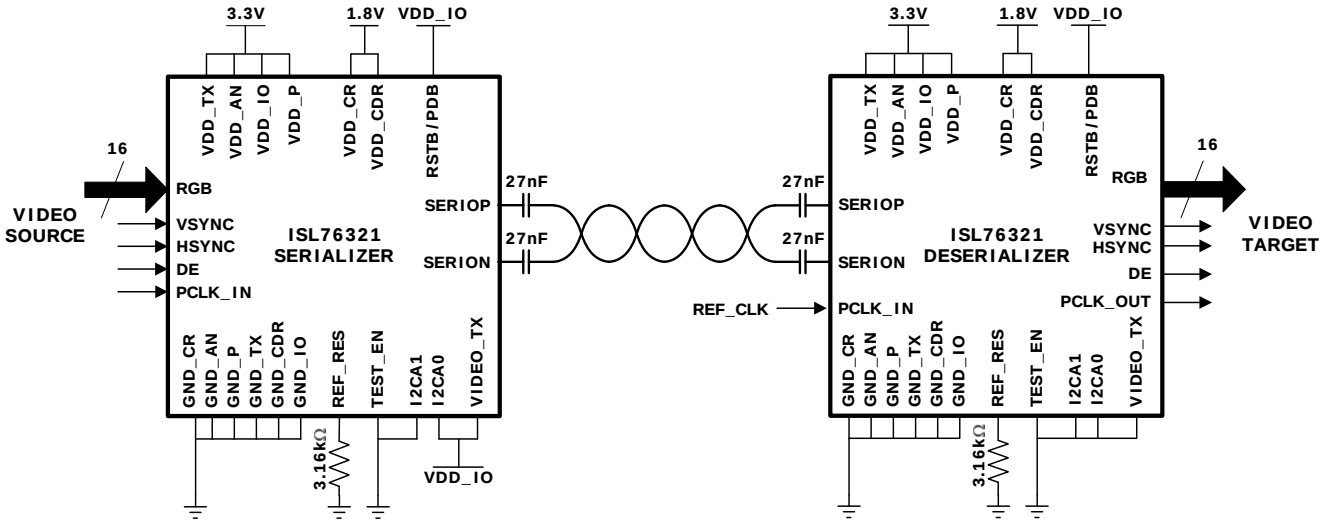
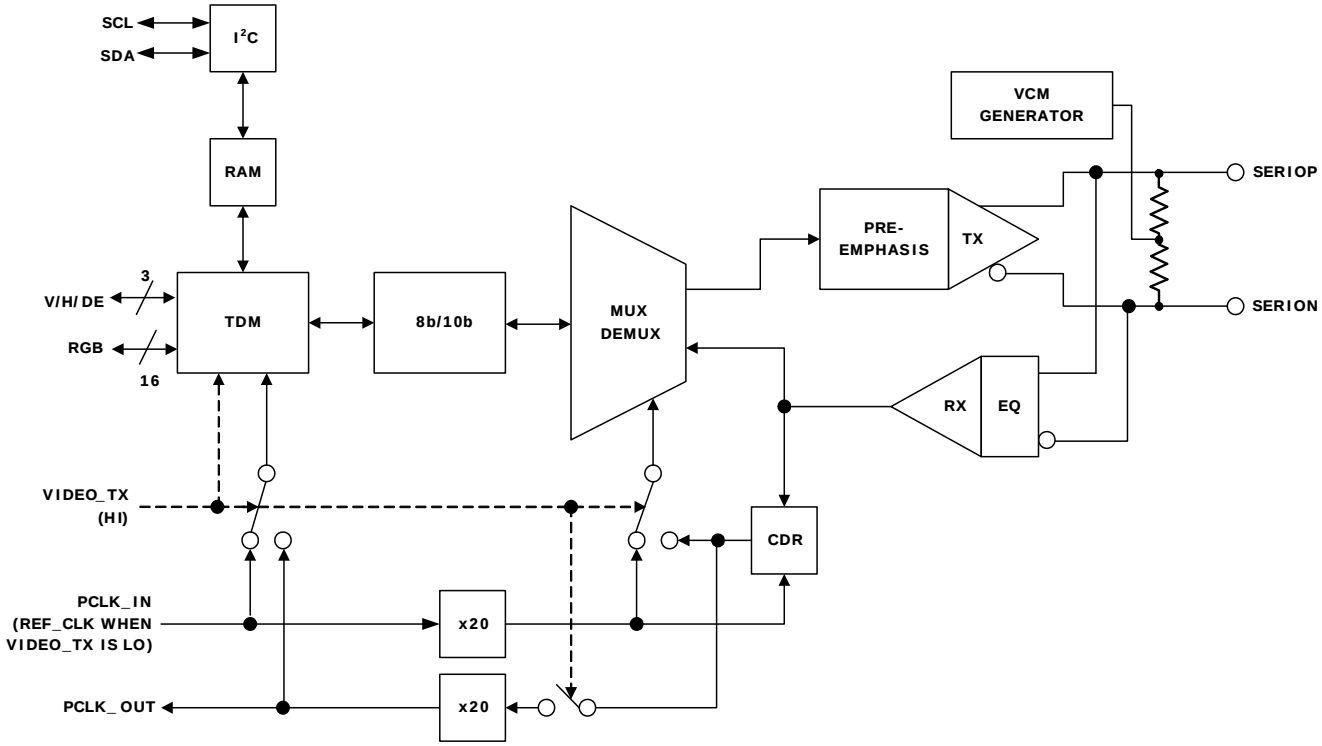


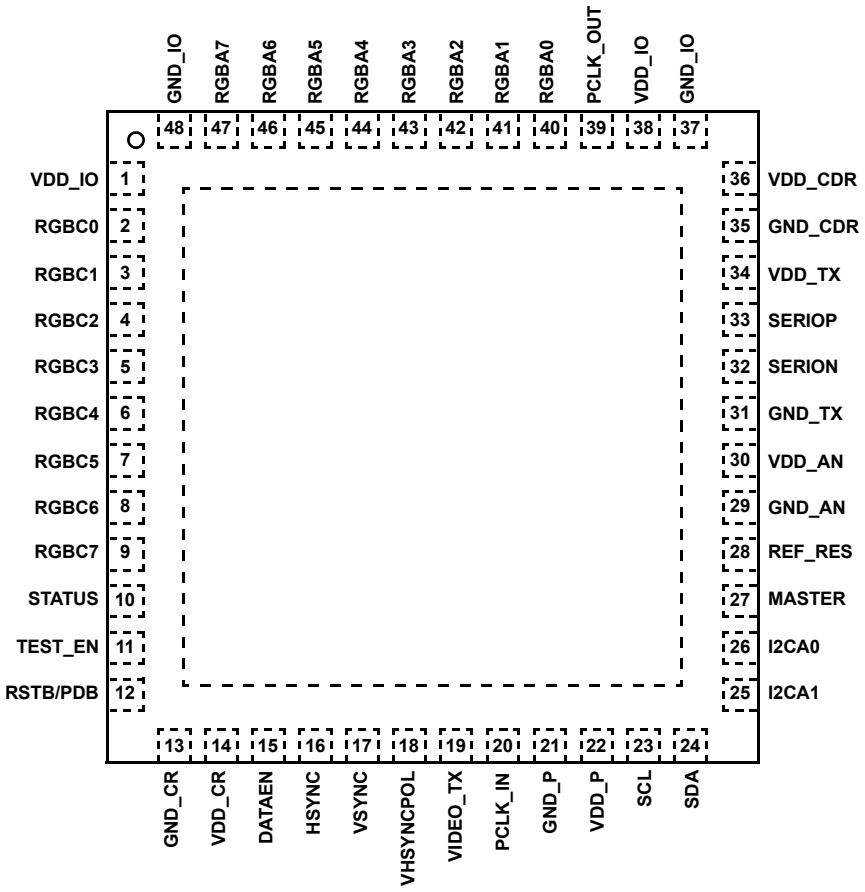

FIGURE 1. TYPICAL APPLICATION

# Block Diagram



# Pin Configuration

ISL76321
(48 LD QFN)
TOP VIEW




# Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION | |
|---|---|---|---|
| | | SERIALIZER | DESERIALIZER |
| 47, 46<br>45, 44<br>43, 42<br>41, 40<br>9, 8<br>7, 6<br>5, 4<br>3, 2 | RGBA7, RGBA6<br>RGBA5, RGBA4<br>RGBA3, RGBA2<br>RGBA1, RGBA0<br>RGBC7, RGBC6<br>RGBC5, RGBC4<br>RGBC3, RGBC2<br>RGBC1, RGBC0 | Parallel video data LVCMOS inputs with Hysteresis | Parallel video data LVCMOS outputs |
| 16 | HSYNC | Horizontal (line) Sync LVCMOS input with Hysteresis | Horizontal (line) Sync LVCMOS output |
| 17 | VSYNC | Vertical (frame) Sync LVCMOS input with Hysteresis | Vertical (frame) Sync LVCMOS output |
| 15 | DATAEN | Video Data Enable LVCMOS input with Hysteresis | Video Data Enable LVCMOS output |
| 20 | PCLK_IN | Pixel clock LVCMOS input | PLL reference clock LVCMOS input |
| 39 | PCLK_OUT | Default; not used | Recovered clock LVCMOS output |
| 33, 32 | SERIOP, SERION | High-speed differential serial I/O | High speed differential serial I/O |

## Pin Descriptions (Continued)

| PIN NUMBER | PIN NAME | DESCRIPTION | |
|---|---|---|---|
| | | SERIALIZER | DESERIALIZER |
| 18 | VHSYNCPOL | CMOS input for HSYNC and VSYNC Polarity<br>1: HSYNC & VSYNC active low<br>0: HSYNC & VSYNC active high | |
| 19 | VIDEO_TX | CMOS input for video flow direction<br>1: Video serializer<br>0: Video deserializer | |
| 24, 23 | SDA, SCL (Note 1) | $I^2C$ Interface Pins ($I^2C$ DATA, $I^2C$ CLK), weak internal pull-up | |
| 25, 26 | I2CA[1:0] (Note 1) | $I^2C$ Device Address | |
| 27 | MASTER | $I^2C$ Master Mode<br>1: Master<br>0: Slave | |
| 12 | RSTB/PDB | CMOS input for Reset and Power-down. For normal operation, this pin should be driven high. When this pin is taken low, the device will be reset. If this pin stays low, the device will be in PD mode. | |
| 10 | STATUS | CMOS output for Receiver Status:<br>1: Valid 8b/10b data received<br>0: No valid data detected<br>Note: serializer and deserializer switch roles during side-channel reverse traffic | |
| 28 | REF_RES | Analog bias setting resistor connection; use 3.16kΩ ±1% to ground | |
| 21 | GND_P (Note 2) | PLL Ground | |
| 37, 48 | GND_IO (Note 2) | Digital (Parallel and Control) Ground | |
| 35 | GND_CDR (Note 2) | Analog (Serial) Data Recovery Ground | |
| 31 | GND_TX (Note 2) | Analog (Serial) Output Ground | |
| 29 | GND_AN (Note 2) | Analog Bias Ground | |
| 13 | GND_CR (Note 2) | Core Logic Ground | |
| 14 | VDD_CR | Core Logic VDD | |
| 34 | VDD_TX | Analog (Serial) Output VDD | |
| 30 | VDD_AN | Analog Bias VDD | |
| 36 | VDD_CDR | Analog (Serial) Data Recovery VDD | |
| 1, 38 | VDD_IO (Note 1) | Digital (Parallel and Control) VDD | |
| 22 | VDD_P | PLL VDD | |
| 11 | TEST_EN | Must be connected to ground | |
| Exposed Pad | PAD | Must be connected to ground, not an electrical connection | |

NOTES:

1. Pins with the same name are internally connected together. However, this connection must NOT be used for connecting together external components or features.
2. The various differently-named Ground pins are internally weakly connected. They must be tied together externally. The different names are provided to assist in minimizing the current loops involved in bypassing the associated supply VDD pins. In particular, for ESD testing, they should be considered a common connection.

# Ordering Information

| PART NUMBER (Notes 3, 4, 5) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| ISL76321ARZ | ISL76321 ARZ | -40 to +105 | 48 Ld QFN | L48.7x7C |

NOTES:

3. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL76321. For more information on MSL please see techbrief TB363.

## Absolute Maximum Ratings

Supply Voltage
- VDD_P to GND_P, VDD_TX to GND_TX, VDD_IO to GND_IO . . -0.5V to 4.6V
- VDD_CDR to GND_CDR, VDD_CR to GND_CR . . . . . -0.5V to 2.5V
- Between any pair of GND_P, GND_TX, GND_IO, GND_CDR, GND_CR . . . . . -0.1V to 0.1V

3.3V Tolerant LVTTL/LVCMOS
- Input Voltage . . . . . -0.3V to VDD_IO +0.3V

Differential Input Voltage . . . . . -0.3V to VDD_IO + 0.3V
Differential Output Current . . . . . Short Circuit Protected
LVTTL/LVCMOS Outputs . . . . . Short Circuit Protected
ESD Rating
- Human Body Model (Tested per JESD22-A114E)
  - All pins . . . . . 4kV
  - SERIOP/N (All VDD Connected, all GND Connected) . . . . . 8kV
- Machine Model (Tested per JESD-A115-A) . . . . . 200V
- Charge Device Model (Tested per AEC-Q100-011-B) . . . . . 2000V

Latch-up (Tested per JESD-78B; Class2, Level A) . . . . . 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ | $\theta_{JC}$ (°C/W) |
|---|---|---|
| QFN Package (Notes 6, 7) . . . . . | 32 | 3.7 |

Maximum Power Dissipation . . . . . 327mW
Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Operating Temperature Range . . . . . -40°C to +105°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

6. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, $T_A$ = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY VOLTAGE** | | | | | | |
| VDD_CDR, VDD_CR | | | **1.7** | 1.8 | **1.9** | V |
| VDD_TX, VDD_P, VDD_AN, VDD_IO | | | **3.0** | 3.3 | **3.6** | V |
| **SERIALIZER POWER SUPPLY CURRENTS** | | | | | | |
| Total 1.8V Supply Current | | PCLK_IN = 45MHz | | 62 | **80** | mA |
| Total 3.3V Supply Current | | (Note 8) | | 40 | **52** | mA |
| **DESERIALIZER POWER SUPPLY CURRENTS** | | | | | | |
| Total 1.8V Supply Current | | PCLK_IN = 45MHz | | 66 | **76** | mA |
| Total 3.3V Supply Current | | (Note 8) | | 50 | **63** | mA |
| **POWER-DOWN SUPPLY CURRENT** | | | | | | |
| Total 1.8V Power-Down Supply Current | | RSTB = GND | | 10 | | mA |
| Total 3.3V Power-Down Supply Current | | | | 0.5 | | mA |
| **PARALLEL INTERFACE** | | | | | | |
| High Level Input Voltage | $V_{IH}$ | | **2.0** | | | V |
| Low Level Input Voltage | $V_{IL}$ | | | | **0.8** | V |
| Input Leakage Current | $I_{IN}$ | | **-1** | ±0.01 | **1** | µA |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA, VDD_IO = 3.0V | **2.6** | | | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 4.0mA, VDD_IO = 3.6V | | | **0.4** | V |
| Output Short Circuit Current | $I_{OSC}$ | | | | **35** | mA |

**Electrical Specifications** Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, $T_A$ = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| Output Rise and Fall Times | $t_{OR}/t_{OF}$ | Slew rate control set to min $C_L$ = 8pF | | 1 | | ns |
| | | Slew rate control set to max, $C_L$ = 8pF | | 4 | | ns |
| **SERIALIZER PARALLEL INTERFACE** | | | | | | |
| PCLK_IN Frequency | $f_{IN}$ | | 6 | | 50 | MHz |
| PCLK_IN Duty Cycle | $t_{IDC}$ | | **40** | 50 | **60** | % |
| Parallel Input Setup Time | $t_{IS}$ | | **3.5** | | | ns |
| Parallel Input Hold Time | $t_{IH}$ | | **1.0** | | | ns |
| **DESERIALIZER PARALLEL INTERFACE** | | | | | | |
| PCLK_OUT Frequency | $f_{OUT}$ | | 6 | | 50 | MHz |
| PCLK_OUT Duty Cycle | $t_{ODC}$ | | | 50 | | % |
| PCLK_OUT Period Jitter (rms) | $t_{OJ}$ | Clock randomizer off | | 0.5 | | $\%t_{PCLK}$ |
| PCLK_OUT Spread Width | $t_{OSPRD}$ | Clock randomizer on | | ±20 | | $\%t_{PCLK}$ |
| PCLK_OUT to Parallel Data Outputs (includes Sync and DE pins) | $t_{DV}$ | Relative to PCLK_OUT, (Note 9) | **-1.0** | | **5.5** | ns |
| Deserializer Output Latency | $t_{CPD}$ | Inherent in the design | **4** | 9 | **14** | PCLK |
| **DESERIALIZER REFERENCE CLOCK (REF_CLK IS FED INTO PCLK_IN)** | | | | | | |
| REF_CLK Lock Time | $t_{PLL}$ | | | 100 | | µs |
| REF_CLK to PCLK_OUT Maximum Frequency Offset | | PCLK_OUT is the recovered clock | **1500** | 5000 | | ppm |
| **HIGH-SPEED TRANSMITTER** | | | | | | |
| HS Differential Output Voltage, Transition Bit | $VOD_{TR}$ | TXCN = 0x00 | **650** | 800 | **900** | $mV_{P-P}$ |
| | | TXCN = 0x0F | | 900 | | $mV_{P-P}$ |
| | | TXCN = 0xF0 | | 1100 | | $mV_{P-P}$ |
| | | TXCN = 0xFF | | 1300 | | $mV_{P-P}$ |
| HS Differential Output Voltage, Non-Transition Bit | $VOD_{NTR}$ | TXCN = 0x00 | **650** | 800 | **900** | $mV_{P-P}$ |
| | | TXCN = 0x0F | | 900 | | $mV_{P-P}$ |
| | | TXCN = 0xF0 | | 430 | | $mV_{P-P}$ |
| | | TXCN = 0xFF | | 600 | | $mV_{P-P}$ |
| HS Generated Output Common Mode Voltage | $V_{OCM}$ | | | 2.35 | | V |
| HS Common Mode Serializer-Deserializer Voltage Difference | $\Delta V_{CM}$ | | | 10 | **20** | mV |
| HS Differential Output Impedance | $R_{OUT}$ | | **80** | 100 | **120** | Ω |
| HS Output Latency | $t_{LPD}$ | Inherent in the design | **4** | 7 | **10** | PCLK |
| HS Output Rise and Fall Times | $t_R/t_F$ | 20% to 80% | | 150 | | ps |
| HS Differential Skew | $t_{SKEW}$ | | | <10 | | ps |
| HS Output Random Jitter | $t_{RJ}$ | PCLK_IN = 45MHz | | 6 | | $ps_{rms}$ |
| HS Output Deterministic Jitter | $t_{DJ}$ | PCLK_IN = 45MHz | | 25 | | $ps_{P-P}$ |

**Electrical Specifications** Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, $T_A$ = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| **HIGH SPEED RECEIVER** | | | | | | |
| HS Differential Input Voltage | $V_{ID}$ | | **75** | | | $mV_{P-P}$ |
| HS Generated Input Common Mode Voltage | $V_{ICM}$ | | | 2.32 | | V |
| HS Differential Input Impedance | $R_{IN}$ | | **80** | 100 | **120** | Ω |
| HS Maximum Jitter Tolerance | | | | 0.50 | | $UI_{P-P}$ |
| **$I^2C$** | | | | | | |
| $I^2C$ Clock Rate (on SCL) | $f_{I2C}$ | | | 100 | **400** | kHz |
| $I^2C$ Clock Pulse Width (HI or LO) | | | **1.3** | | | µs |
| $I^2C$ Clock Low to Data Out Valid | | | **0** | | **1** | µs |
| $I^2C$ Start/Stop Setup/Hold Time | | | **0.6** | | | µs |
| $I^2C$ Data in Setup Time | | | **100** | | | ns |
| $I^2C$ Data in Hold Time | | | **100** | | | ns |
| $I^2C$ Data out Hold Time | | | **100** | | | ms |

NOTES:

8. IDDIO is nominally 50µA and not included in this total as it is dominated by the loading of the parallel pins.
9. This parameter is the output data skew from the invalid edge of PCLK_OUT. The setup and hold time provided to a system is dependent on the PCLK frequency and is calculated as follows: 0.5 * $f_{IN}$ - $t_{DV}$.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

# Timing Diagrams

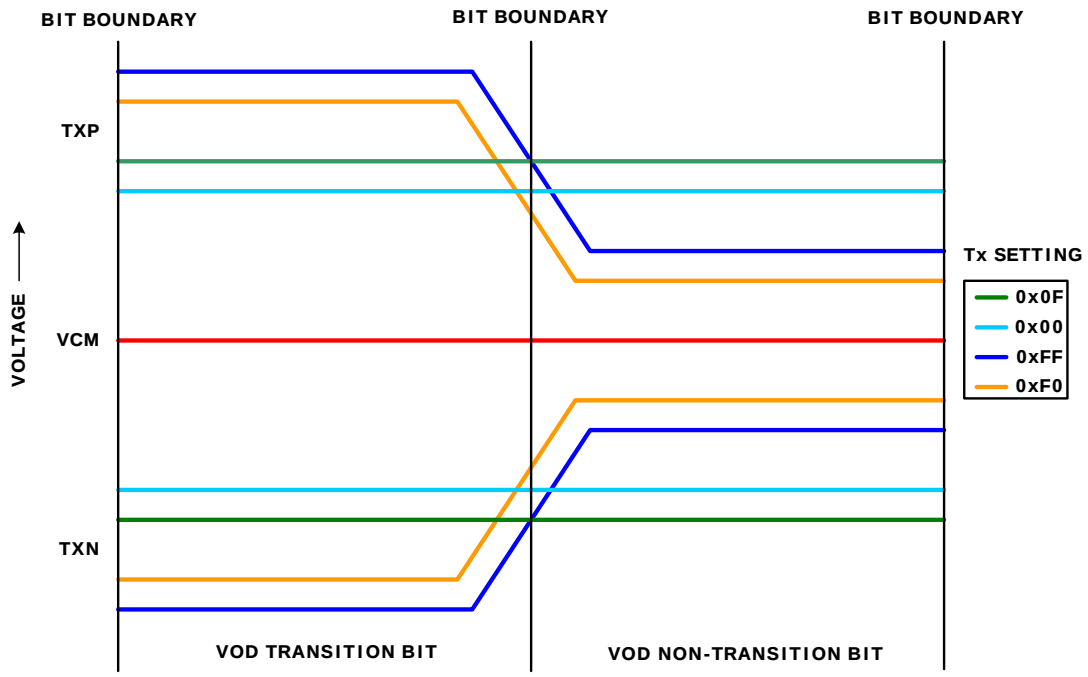



FIGURE 2. VOD vs TX SETTING

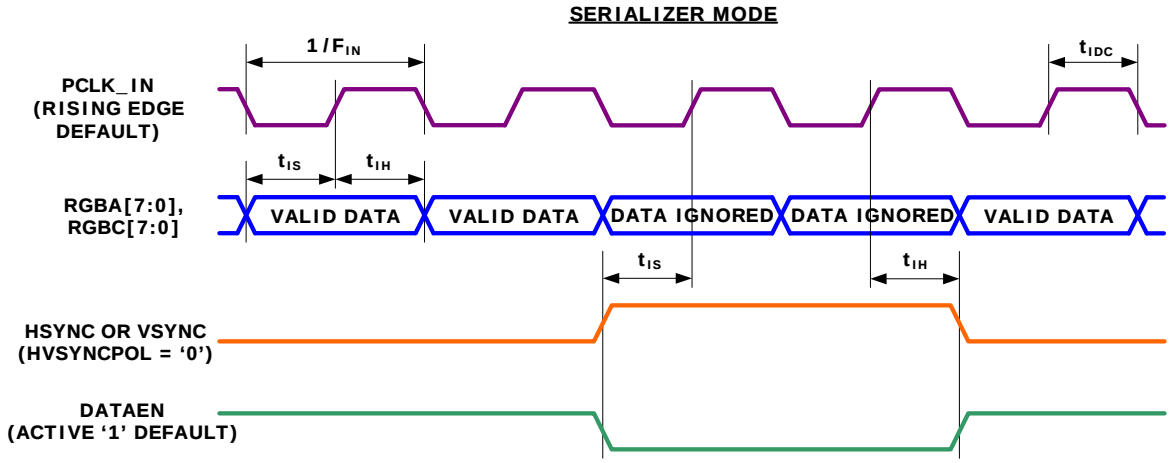



FIGURE 3. PARALLEL VIDEO INPUT TIMING

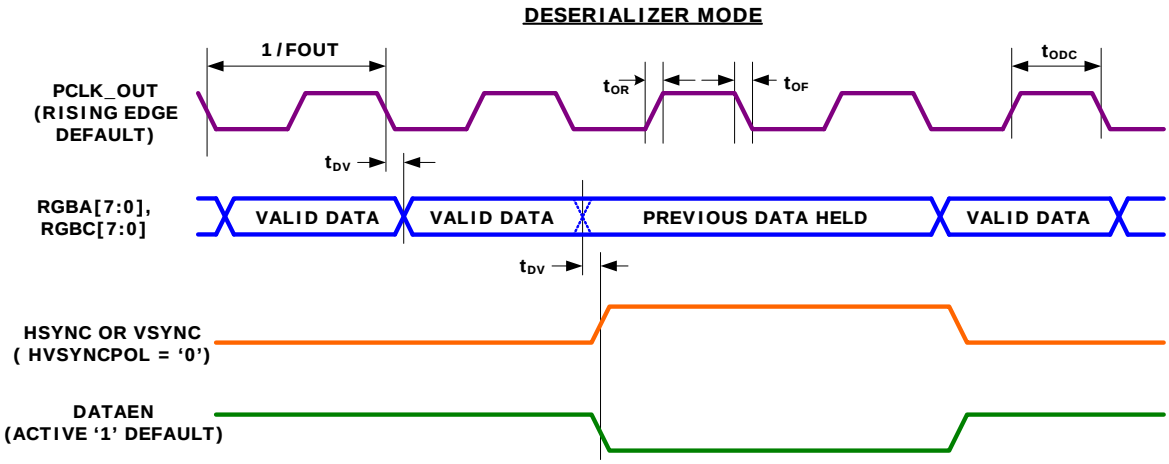



FIGURE 4. PARALLEL VIDEO OUTPUT TIMING

# Applications

## Detailed Description and Operation

A pair of ISL76321 SERDES transports 16-bit parallel video for the ISL76321 along with auxiliary data over a single 100Ω differential cable either to a display or from a camera. Auxiliary data is transferred in both directions every video frame. This feature can be used for remote configuration and telemetry.

The benefits include lower EMI, lower costs, greater reliability and space savings. The same device can be configured to be either a serializer or deserializer by setting one pin (VIDEO_TX), simplifying inventory. RGBA/C, VSYNC, HSYNC, and DATAEN pins are inputs in serializer mode and outputs in deserializer mode.

The video data presented to the serializer on the parallel LVCMOS bus is serialized into a high-speed differential signal. This differential signal is converted back to parallel video at the remote end by the deserializer. The Side Channel data (auxiliary data) is transferred between the SERDES pair during the first two lines of the vertical video blanking interval.

When the side-channel is enabled, which is the default, there will be a number of PCLK cycles uncertainty from frame-to-frame. This should not cause sync problems with most displays, as this occurs during the vertical front porch of the blanking period. When properly configured, the SERDES link supports end-to-end transport with fewer than one error in $10^{10}$ bits.

## Differential Signals and Termination

The ISL76321 serializes the 16-bit parallel data plus 3 sync signals at 20x the PCLK_IN frequency. The extra 2 bits per word come from the 8b/10b encoding scheme which helps create the highest quality serial link.

The high bit rate of the differential serial data requires special care in the layout of traces on PCBs, in the choice and assembly of connectors, and in the cables themselves.

PCB traces need to be adjacent, matched in length and drawn to result in a differential 100Ω controlled impedance. For best EMI performance, the cable should be low loss and have a differential 100Ω impedance. The maximum cable length for a functioning link is dependent on the PCLK_IN frequency, the cable loss and impedance, as well as the pre-emphasis and equalization settings. Functioning links of 25 meters are often possible at the maximum frequency.

SERIOP and SERION pins incorporate internal differential termination of the serial signal lines.

## SERIO Pin AC-Coupling

AC-coupling minimizes the effects of DC common mode voltage difference and local power supply variations between two SERDES. The serializer outputs DC balanced 8b/10b line code, which allows AC-coupling.

The AC-coupling capacitor on SERIO pins must be 27nF on the serializer board and 27nF on the deserializer board. The value of the AC-coupling capacitor is very critical since a value too small will attenuate the high-speed signal at a low clock rate. A value too big will slow down the turn around time for the side-channel. It is an advantage to have the pair of capacitors as closely matched as possible.

## Receiver Reference Clock (REF_CLK)

The reference clock (REF_CLK) for the PLL is fed into PCLK_IN pin. REF_CLK is used to recover the clock from the high-speed serial stream. REF_CLK is very sensitive to any instability. The following conditions must be met at all times after power is applied to the deserializer, or else the deserializer may need a manual reset:

- VDD must be applied and stable
- REF_CLK frequency must be within the limits specified
- REF_CLK amplitude must be stable

A simple 3.3V CMOS crystal oscillator can be used for REF_CLK

## Power Supply Sequencing

The 3.3V supply must be higher than the 1.8V supply at all times, including during power-up and power-down. To meet this requirement, the 3.3V supply must be powered up before the 1.8V supply.

For the deserializer, REF_CLK must not be applied before the device is fully powered up. Applying REF_CLK before power-up

may require the deserializer to be manually reset. A 10ms delay after the 1.8V supply is powered up guarantees normal operation.

## Power Supply Bypassing and Layout

The serializer and deserializer functions rely on the stable functioning of PLLs locked to local reference sources or locked to an incoming signal. It is important that the various supplies (VDD_P, VDD_AN, VDD_CDR, VDD_TX) be well bypassed over a wide range of frequencies, from below the typical loop bandwidth of the PLL to approaching the signal bit rate of the serial data. A combination of different values of capacitors from 1000pF to 5µF or more with low ESR characteristics is generally required.

The parallel LVCMOS VDD_IO supply is inherently less sensitive, but since the RGB and SYNC/DATAEN signals can all swing on the same clock edge, the current in these pins, and the corresponding GND pins, can undergo substantial current flow changes. Once again, a combination of different values of capacitors over a wide range, with low ESR characteristics, is desirable.

A set of arrangements of this type is shown in Figure 5, where each supply is bypassed with a ferrite-bead-based choke, and a range of capacitors. A “choke” is preferable to an “inductor” in this application, since a high-Q inductor will be likely to cause one or more resonances with the shunt capacitors, potentially causing problems at or near those frequencies, while a “lossy” choke will reflect a high impedance over a wide frequency range.

The higher value capacitor, in particular, needs to be chosen carefully, with special care regarding its ESR. Very good results can be obtained with multilayer ceramic capacitors (available from many suppliers) and generally in small outlines (such as the 1210 outline suggested in the schematic shown in Figure 5), which provide good bypass capabilities down to a few mΩ at 1MHz to 2MHz. Other capacitor technologies may also be suitable (perhaps niobium oxide), but “classic” electrolytic capacitors frequently have ESR values of above 1Ω, that nullify any decoupling effect above the 1kHz to 10kHz frequency range.

Capacitors of 0.1µF offer low impedance in the 10MHz to 20MHz region, and 1000pF capacitors in the 100MHz to 200MHz region. In general, one of the lower value capacitors should be used at each supply pin on the IC. Figure 5 shows the grounding of the various capacitors to the pin corresponding to the supply pin. Although all the ground supplies are tied together, the PCB layout should be arranged to emulate this arrangement (at least for the smaller value (high frequency) capacitors), as much as possible.

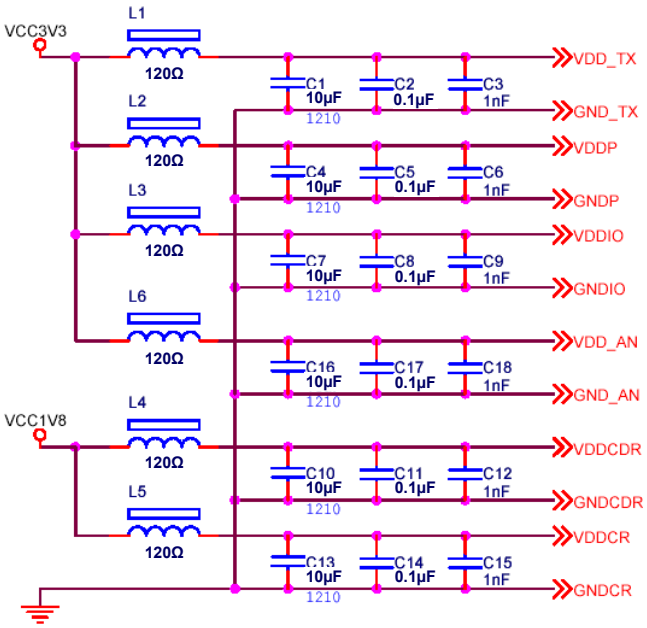



FIGURE 5. POWER SUPPLY BYPASSING

## I²C Interface

The I²C interface allows access to internal registers used to configure the SERDES and to obtain status information. A serializer must be assigned a different address than its deserializer counterpart if the side channel is used. The upper 5 bits are permanently set to 011 11 and the lower 2 bits determined by pins as follows:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | I2CA1 | I2CA0 | R/$\overline{W}$ |

Thus, 4 SERDES can reside on the same bus. By convention, when all address pins are tied low, the device address is referred to as 0x78.

SCL and SDA are open drain to allow multiple devices to share the bus. If not used, SCL and SDA should be tied to VDD_IO.

## Side Channel Interface

The Side Channel is a mechanism for transferring data between the two chips on each end of the link. This data is transferred during video blanking so none of the video bandwidth is used. It has three basic uses:

- Remote SERDES configuration
- Data exchanges between two processors
- Master Mode I²C commands to remote slaves

This interface allows the user to initialize registers, control and monitor both SERDES chips from a single microcontroller which can reside on either side of the serial link. This feature is used to automatically transport the remote side SERDES chip’s status back to a local register. The Side Channel needs to be enabled (the default) for this to work. In the case where there is a microcontroller on each side of the of the link, data can be buffered and exchanged between the two. Up to 224 bytes can be sent in each direction during each VSYNC active period.

## Master Mode

This is a mode activated by strapping the MASTER pin to a '1' on the ISL76321 on the remote side of the link from the microcontroller. This is a virtual extension of the $I^2C$ interface across the link that allows the local processor to read and write slave devices connected to the remote side SERDES $I^2C$ bus. No additional wires or components are needed other than the serial link. The $I^2C$ commands and data are transferred during video blanking causing no interruptions in the video data. In Master mode, the data is transported across the link by the Side Channel so the maximum throughput achievable would be the same. The SCL and SDA frequency is adjustable through the programming of a register. If a SERDES chip is configured as a master it is no longer available for communication by a local microcontroller. It is assumed that the SERDES is the only master.

## Exposed Pad

While it is not a required electrical connection, it is recommended that the exposed pad on the bottom of the package be soldered to the circuit board. This will ensure that the full power dissipation of the package can be utilized. The pad should be connected to ground and not left floating. For best thermal conductivity, 16 vias should connect the footprint for the exposed pad on the circuit board to the ground plane. This connection is not required for basic operation of the chip.

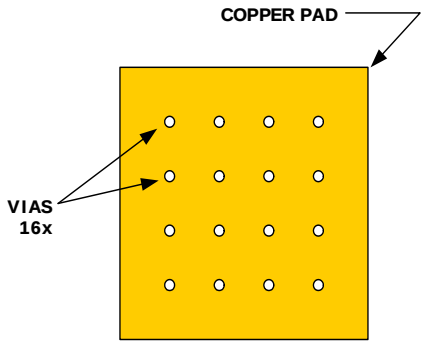



FIGURE 6. LAYOUT FOR THE EXPOSED PAD

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| May 1, 2015 | FN7803.2 | Updated AEC Q100 by adding a dash - now reading AEC-Q100 in Features on page 1<br>“Absolute Maximum Ratings” on page 6 - changed Charge Device Model from Charge Device Model (Tested per JESD22-C101C) to (Tested per AEC-Q100-011-B) |
| December 23, 2013 | FN7803.1 | Page 13<br>- 2nd line of the disclaimer changed from:<br>"Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted"<br>to:<br>"Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted" |
| January 31, 2011 | FN7803.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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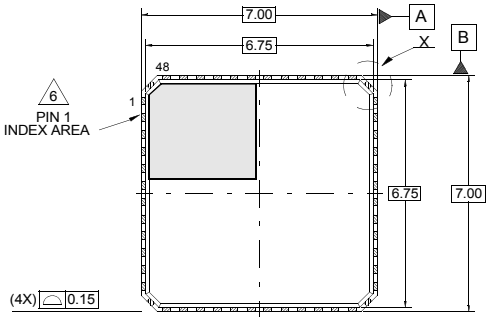
# Package Outline Drawing

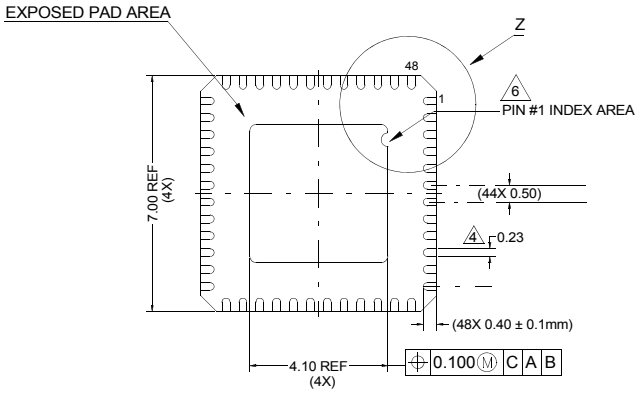
## L48.7x7C

**48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)**

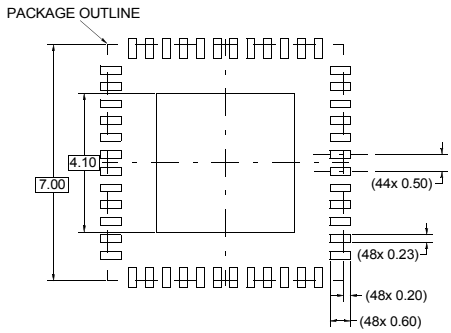
**Rev 0, 1/08**



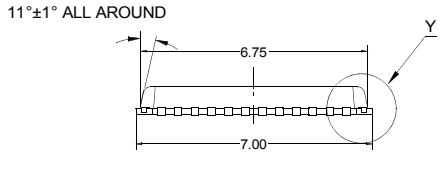

TOP VIEW



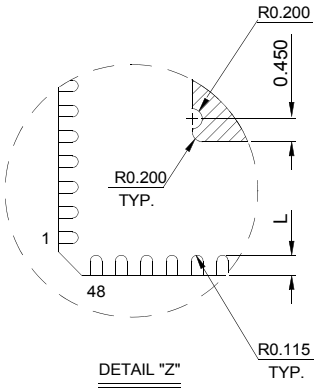

BOTTOM VIEW



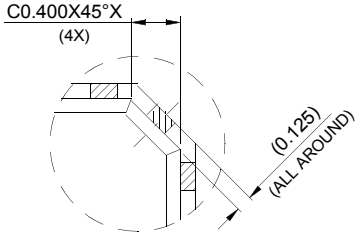

TYPICAL RECOMMENDED LAND PATTERN



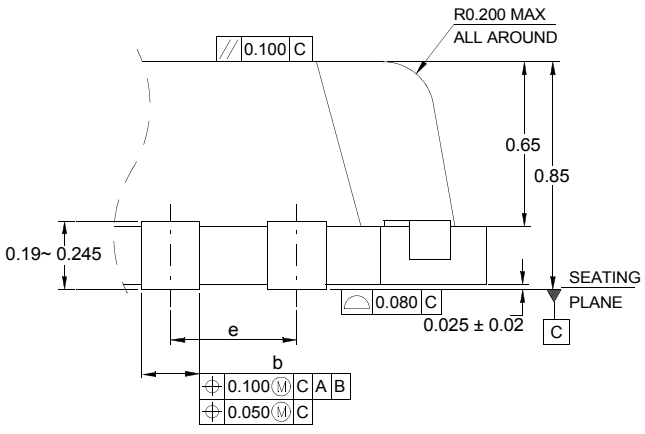

SIDE VIEW




DETAIL "Z"




DETAIL "X"




DETAIL "Y"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to JESD-MO220.
3. Unless otherwise specified, tolerance : Decimal ± 0.05, body tolerance ± 0.1
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.28mm from the terminal tip. Frame base metal thickness 0.203mm.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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