ISL78208

Wide V_{IN} Dual Standard Buck Regulator with 3A/3A Continuous Output Current

FN8354
Rev 1.00
July 29, 2014

The ISL78208 is a dual standard buck regulator capable of 3A per channel with continuous output current. With an input range of 4.5V to 28V, it provides a high frequency power solution for a variety of point of load applications.

The PWM controller in the ISL78208 drives an internal switching N-Channel power MOSFET and requires an external Schottky diode to generate the output voltage. The integrated power switch is optimized for excellent thermal performance up to 3A of output current. The PWM regulator switches at a default frequency of 500kHz and it can be user programmed or synchronized from 300kHz to 2MHz. The ISL78208 utilizes peak current mode control to provide flexibility in component selection and minimize solution size. The protection features include overcurrent, UVLO and thermal overload protection.

The ISL78208 is available in 5mmx5mm 32 Ld Wettable Flank Quad Flat Pb-free (WFQFN) package.

The ISL78208 is rated for the automotive temperature range (-40°C to +105°C).

Features

- Wide input voltage range from 4.5V to 28V
- Adjustable output voltage with continuous output current up to 3A
- Current mode control
- Adjustable switching frequency from 300kHz to 2MHz
- Independent power-good detection
- Selectable In-phase or out-of-phase PWM operation
- Independent, sequential, ratiometric or absolute tracking between outputs
- Internal 2ms Soft-start time
- Overcurrent/short circuit protection, thermal overload protection, UVLO
- Boot undervoltage detection
- Qualified for automotive applications
- Pb-Free (RoHS compliant)

Applications

- DSP and embedded processor power supply
- Infotainment system power

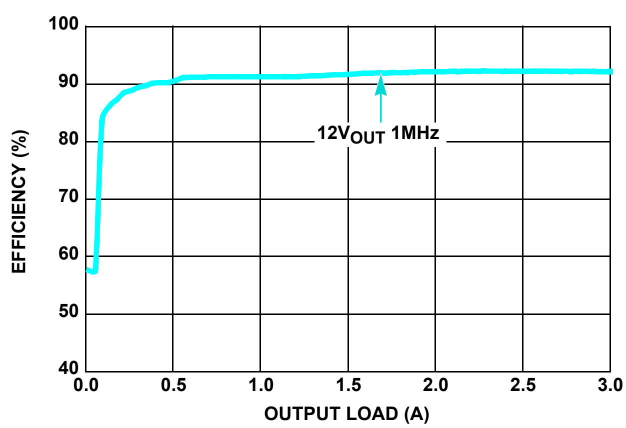
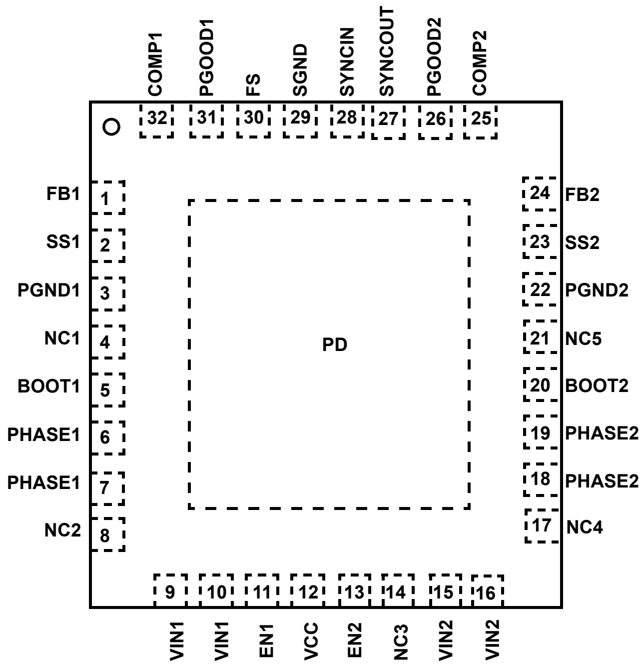


FIGURE 1. EFFICIENCY vs LOAD, V_{IN} = 28V, T_A = +25°C

Table of Contents

Pin Configuration

ISL78208
(32 LD WFQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
25, 32	COMP2, COMP1	COMP1/COMP2 is the output of the error amplifier.
1, 24	FB1, FB2	Feedback pin for the regulator. FB is the negative input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the PWM regulator's power-good and undervoltage protection circuits use FB1/2 to monitor the regulator output voltage.
2, 23	SS1, SS2	Soft-Start pins for each controller. The SS1/2 pins control the soft-start and sequence of their respective outputs. A single capacitor from the SS pin to ground determines the output ramp rate. See the "Output Tracking and Sequencing" on page 15 for soft-start and output tracking/sequencing details. If SS pins are tied to VCC, an internal soft-start of 2ms will be used. Maximum C_{SS} value is 50nF.
3, 22	PGND1, PGND2	Power ground connections. Connect directly to the system GND plane.
5, 20	BOOT1, BOOT2	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn on the internal N-Channel MOSFET. Connect an external capacitor from this pin to PHASE.
6, 7, 18, 19	PHASE1, PHASE2	Switch node output. It connects the source of the internal power MOSFET with the external output inductor and with the cathode of the external diode.
9, 10, 15, 16	VIN1, VIN2	The input supply for the power stage of the PWM regulator and the source for the internal linear regulator that provides bias for the IC. Place a minimum of 10µF ceramic capacitance from each VIN to GND and close to the IC for decoupling.
11, 13	EN1, EN2	PWM controller's enable inputs. The PWM controllers are held off when the pin is pulled to ground. When the voltage on this pin rises above 2V, the PWM controller is enabled. If EN1, EN2 pins are driven by an external signal, the minimum off-time for EN1, EN2 should be: $EN\_T\_off\ (\mu s) = 10\mu s \bullet C_{SS}/2.2nF$ where C_{SS} is the soft-start pin capacitor (nF). ISL78208 does not have debouncing to EN1, EN2 external signals.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	PIN DESCRIPTION
12	VCC	Output of the internal 5V linear regulator. Decouple to PGND with a minimum of 4.7µF ceramic capacitor. This pin is provided only for internal bias of ISL78208 (not to be loaded with current over 10mA).
27	SYNCOUT	Synchronization output. Provides a signal that is the inverse of the SYNCIN signal.
28	SYNCIN	Connect to an external signal for synchronization from 300kHz to 2MHz (negative edge trigger). SYNCIN is not allowed to be floating. When SYNCIN = logic 0, PHASE1 and PHASE2 are running at 180° out-of-phase. When SYNCIN = logic 1, PHASE1 and PHASE2 are running at 0° in-phase. When SYNCIN = an external clock, PHASE1 and PHASE2 are running at 180° out-of-phase. External SYNC frequency applied to the SYNCIN pin should be at least 2.4 times the internal switching frequency setting.
29	SGND	Signal ground connections. The exposed pad must be connected to SGND and soldered to the PCB. All voltage levels are measured with respect to this pin.
4, 8, 14, 17, 21	NC1, NC2, NC3, NC4, NC5	This is a no connection pin.
30	FS	Frequency selection pin. Tie to VCC for 500kHz switching frequency. Connect a resistor to GND for adjustable frequency from 300kHz to 2MHz.
26, 31	PGOOD2, PGOOD1	Open drain power-good output that is pulled to ground when the output voltage is below regulation limits or during the soft-start interval. There is an internal 5MΩ internal pull-up resistor.
EPAD	PD	The exposed pad must be connected to the system GND plane with as many vias as possible for proper electrical and thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78208ARZ	ISL7820 8ARZ	-40 to +105	32 Ld WFQFN	L32.5x5H

NOTES:

1. Add “-T*” suffix for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78208. For more information on MSL please see techbrief TB363.

Typical Application Schematics

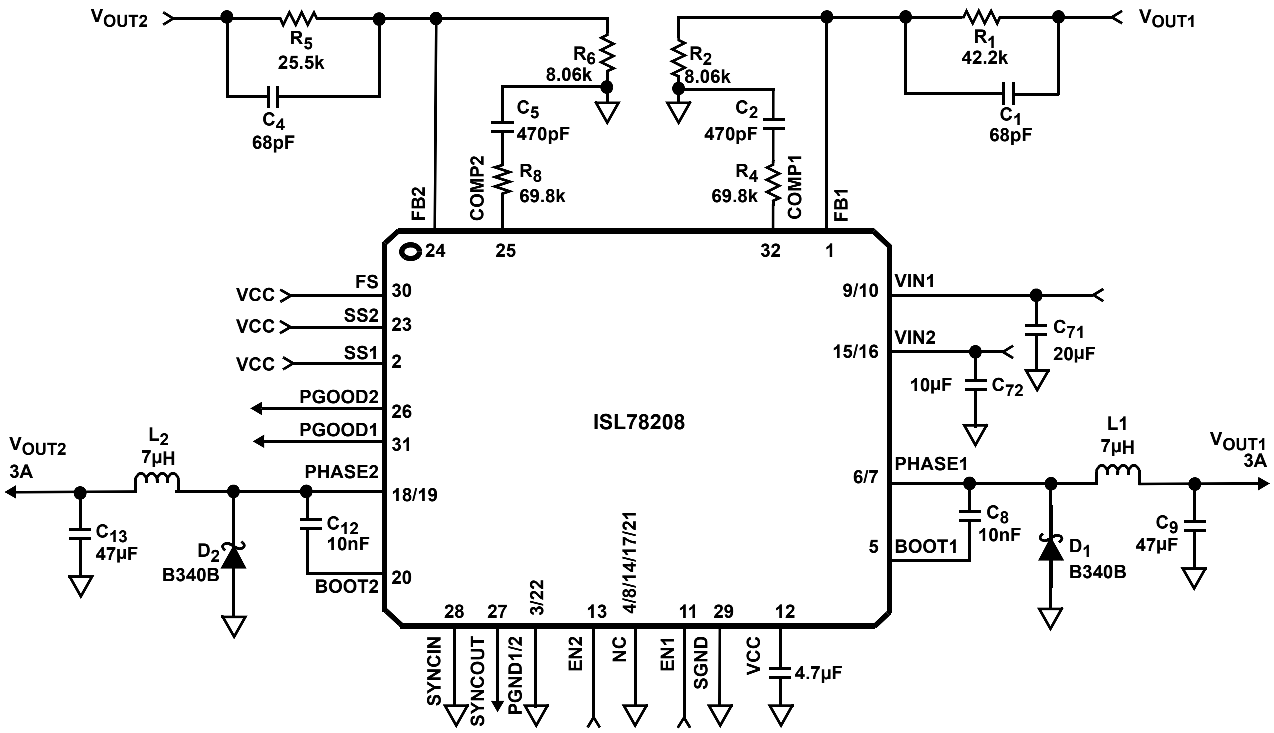


FIGURE 2. DUAL 3A OUTPUT (V_{IN} RANGE FROM 4.5V TO 28V)

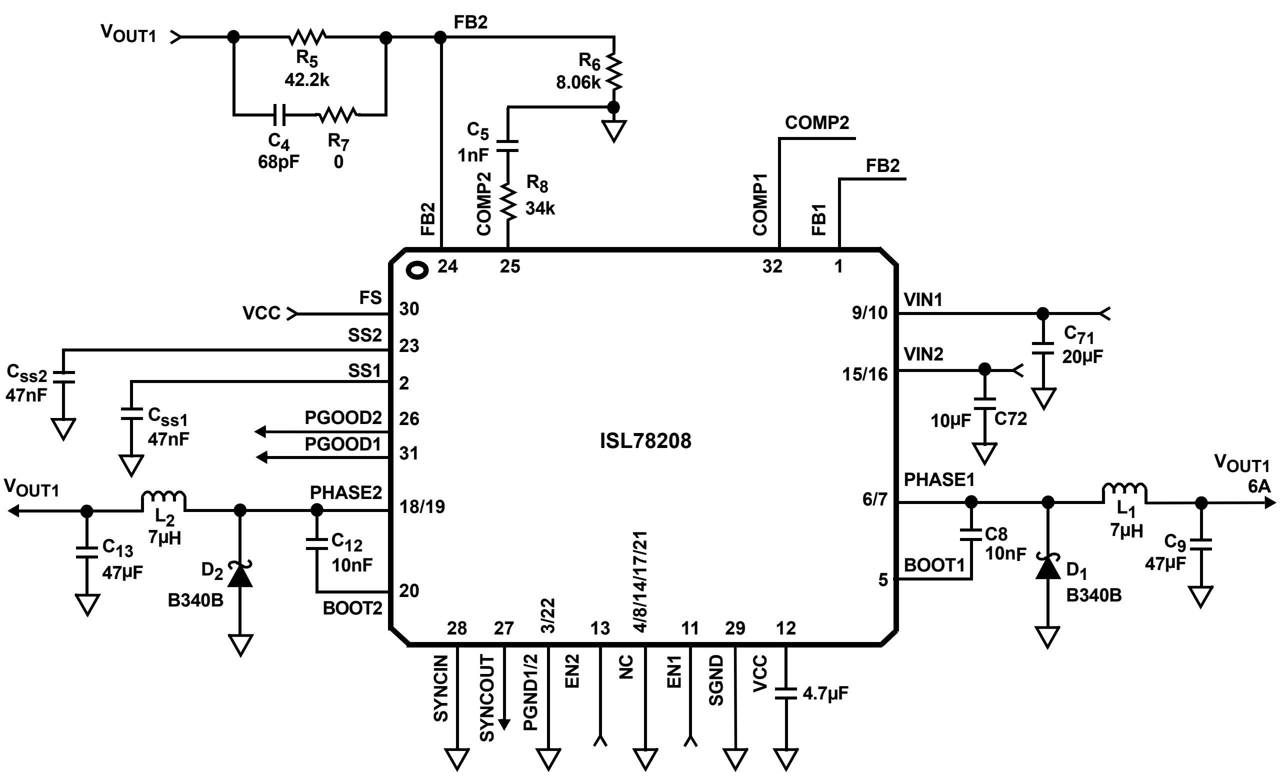
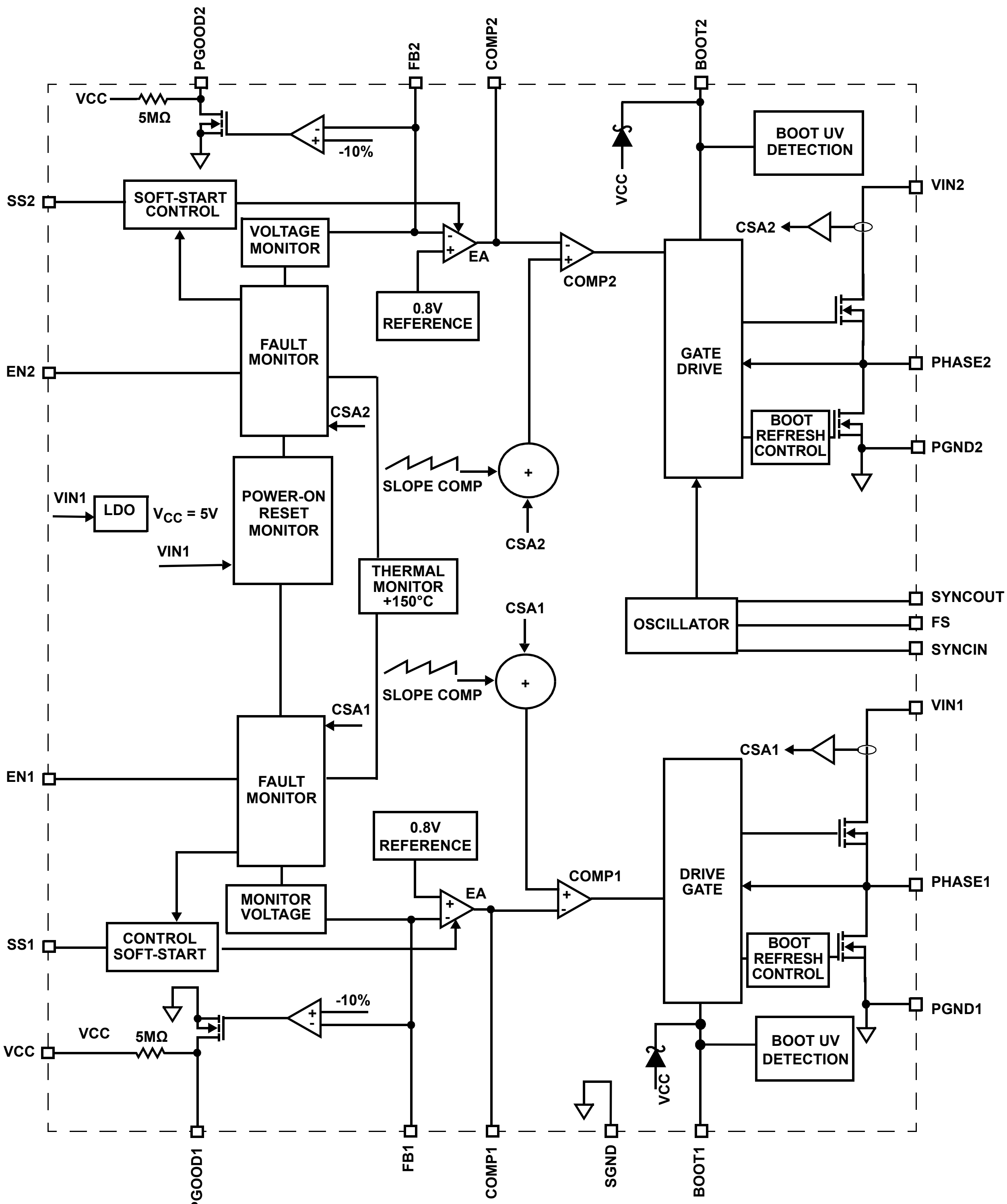


FIGURE 3. SINGLE 6A OUTPUT (V_{IN} RANGE FROM 4.5V TO 28V) CURRENT SHARING

Functional Block Diagram



Absolute Maximum Ratings

VIN1/2 to GND . . . . . -0.3V to +30V
PHASE1/2 to GND . . . . . -0.3V to +30V
BOOT1/2 to PHASE1/2 . . . . . -0.3V to +5.9V
FS to GND . . . . . -0.3V to +5.9V
SYNCIN to GND . . . . . -0.3V to +5.9V
FB1/2 to GND . . . . . -0.3V to +2.95V
EN1/2 to GND . . . . . -0.3V to +5.9V
PGOOD1/2 to GND . . . . . -0.3V to +5.9V
COMP1/2 to GND . . . . . -0.3V to +5.9V
VCC to GND Short Maximum Duration 1s
SYNCOUT to GND . . . . . -0.3V to +5.9V
SS1/2 to GND . . . . . -0.3V to +5.9V
ESD Rating
  Human Body Model (Tested per JESD22-A114) 4kV
  Charged Device Model (Tested per AEC-Q100-011) 2.2kV
  Machine Model (Tested per JESD22-A115) 300V
Latch Up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
WFQFN Package (Notes 4, 5)	30	1.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +105°C
Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -40°C to +105°C

Recommended Operating Conditions

Temperature . . . . . -40°C to +105°C
Supply Voltage . . . . . 4.5V to 28V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = -40°C to +105°C, V_{IN} = 4.5V to 28V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		**4.5**		**28**	V
V_{IN} Quiescent Supply Current	I_Q			1.2	**2.2**	mA
V_{IN} Shutdown Supply Current	I_{SD}	EN1/2 = 0V		20	**45**	µA
V_{CC} Voltage	V_{CC}	V_{IN} = 12V; I_{OUT} = 0mA	**4.5**	5.1	**5.6**	V
POWER-ON RESET						
V_{IN} POR Threshold		Rising Edge		3.9	**4.4**	V
		Falling Edge	**3.2**	3.7		V
OSCILLATOR						
Nominal Switching Frequency	F_{SW}	FS = VCC	**420**	500	**580**	kHz
		Resistor from FS to GND = 383kΩ		300		kHz
		Resistor from FS to GND = 40.2kΩ		2000		kHz
FS Voltage	V_{FS}	FS = 100kΩ	**780**	800	**820**	mV
Switching Frequency		SYNCIN = 600kHz		300		kHz
		1.2MHz ≤ SYNCIN ≤ 4MHz, +25°C	600		2000	kHz
		1.2MHz ≤ SYNCIN ≤ 4MHz, -40°C to +105°C	**600**		**1500**	
Minimum Off-Time	t_{OFF}			130		ns
ERROR AMPLIFIER						
Error Amplifier Transconductance Gain	gm		**125**	205	**285**	µA/V
FB1, FB2 Leakage Current		VFB = 0.8V		10	**100**	nA
Current Sense Amplifier Gain	R_T		**0.18**	0.21	**0.24**	V/A
Reference Voltage			**0.792**	0.8	**0.808**	V
Soft-Start Ramp Time		SS1/2 = VCC	**1.5**	2.5	**3.5**	ms

Electrical Specifications

T_A = -40°C to +105°C, V_{IN} = 4.5V to 28V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Soft-Start Charging Current	I_{SS}		**1.4**	2	**2.6**	µA
POWER-GOOD						
PG1, PG2 Trip Level PG to PGOOD1, PGOOD2		Rise		91	**94**	%
		Fall	**82.5**	85.5		%
PG1, PG2 Propagation Delay		Percentage of the soft-start time		10		%
PG1, PG2 Low Voltage		ISINK = 3mA		100	**300**	mV
ENABLE INPUT						
EN1, EN2 Leakage Current		EN1/2 = 0V/5V	**-1**		**1**	µA
EN1, EN2 Input Threshold Voltage		Low Level			**0.8**	V
		Float Level	**1.0**		**1.4**	V
		High Level	**2**			V
SYNC INPUT/OUTPUT						
SYNCIN Input Threshold		Falling Edge	**1.1**	1.4		V
		Rising Edge		1.6	**2.1**	V
		Hysteresis		200		mV
SYNCIN Leakage Current		SYNCIN = 0V/5V		10	**1000**	nA
SYNCIN Pulse Width			**100**			ns
SYNCOUT Phase-shift to SYNCIN		Measured from rising edge-to-rising edge, if duty cycle is 50%		180		°
SYNCOUT Frequency Range		T_A = +25°C	600		4000	kHz
		T_A = -40°C to +105°C	**600**		**3000**	
SYNCOUT Output Voltage High		ISYNCOUT = 3mA	**V_{CC} - 0.3**	V_{CC} -0.08		V
SYNCOUT Output Voltage Low				0.08	**0.3**	V
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		150		°C
	T_{HYS}	Hysteresis		20		°C
Overcurrent Protection Threshold		(Note 7)	**4.1**	5.1	**6.1**	A
OCP Blanking Time				60		ns
POWER MOSFET						
Highside	R_{HDS}	I_{PHASE} = 100mA		75	**150**	mΩ
Internal BOOT1, BOOT2 Refresh Lowside	R_{LDS}	I_{PHASE} = 100mA		1		Ω
PHASE Leakage Current		EN1/2 = PHASE1/2 = 0V			**300**	nA
PHASE Rise Time	t_{RISE}	V_{IN} = 25V		10		ns

NOTES:

6. Test Condition: V_{IN} = 28V, FB forced above regulation point (0.8V), no switching, and power MOSFET gate charging current not included.
7. Established by both current sense amplifier gain test and current sense amplifier output test @ I_L = 0A.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.

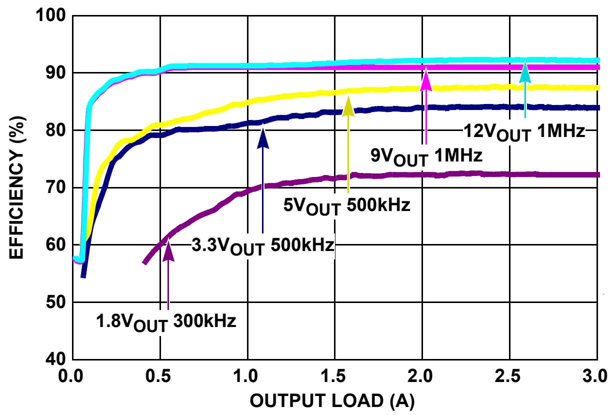


FIGURE 4. EFFICIENCY vs LOAD, T_A = +25°C, V_{IN} = 28V

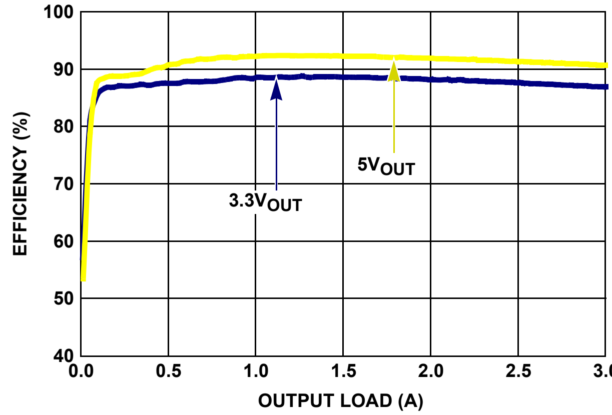


FIGURE 5. EFFICIENCY vs LOAD, T_A = +25°C, F_{SW} = 500kHz, V_{IN} = 12V

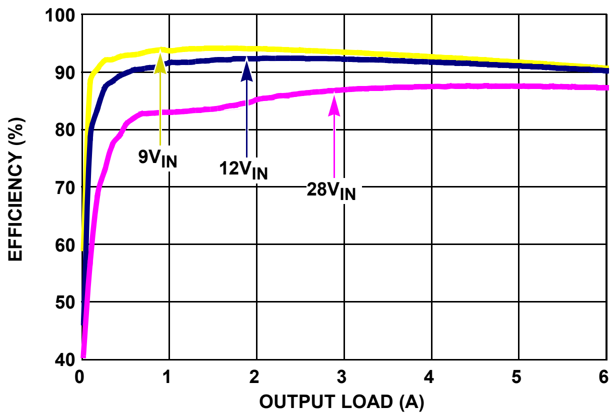


FIGURE 6. EFFICIENCY vs LOAD, T_A = +25°C, CURRENT SHARING 5V_{OUT}, F_{SW} = 500kHz

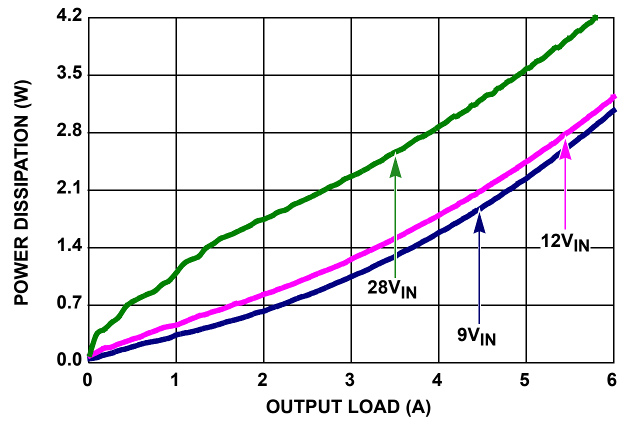


FIGURE 7. POWER DISSIPATION vs LOAD, T_A = +25°C, CURRENT SHARING 5V_{OUT}, F_{SW} = 500kHz

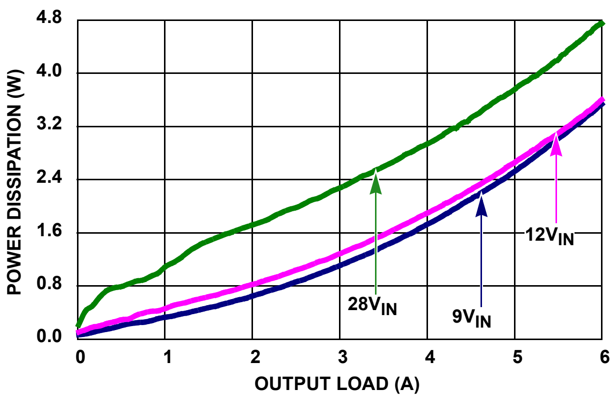


FIGURE 8. POWER DISSIPATION vs LOAD, T_A = +85°C, CURRENT SHARING 5V_{OUT}, F_{SW} = 500kHz

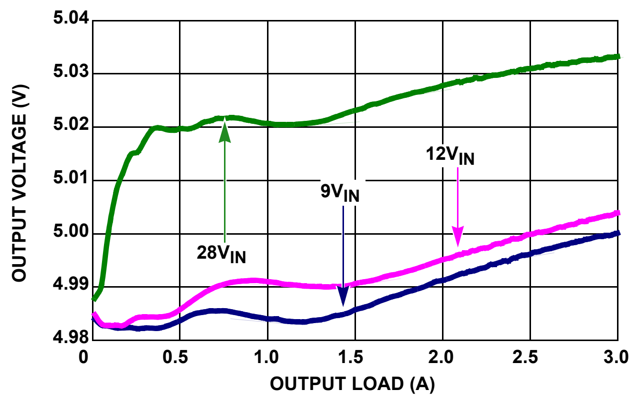


FIGURE 9. V_{OUT} REGULATION vs LOAD, CHANNEL 1, T_A = +25°C, 5V_{OUT}, F_{SW} = 500kHz

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Continued)

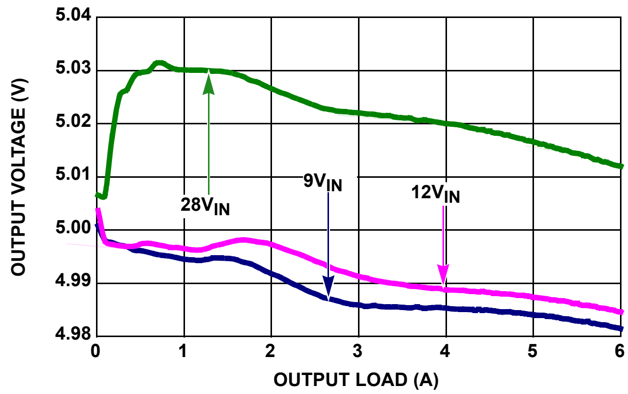


FIGURE 10. V_{OUT} REGULATION vs LOAD, CURRENT SHARING, T_A = +25°C, 5V_{OUT}, F_{SW} = 500kHz

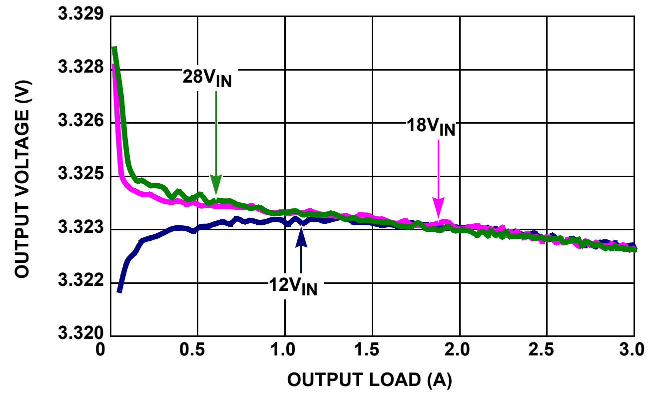


FIGURE 11. V_{OUT} REGULATION vs LOAD, CHANNEL 2, T_A = +25°C, 3.3V_{OUT}, F_{SW} = 500kHz

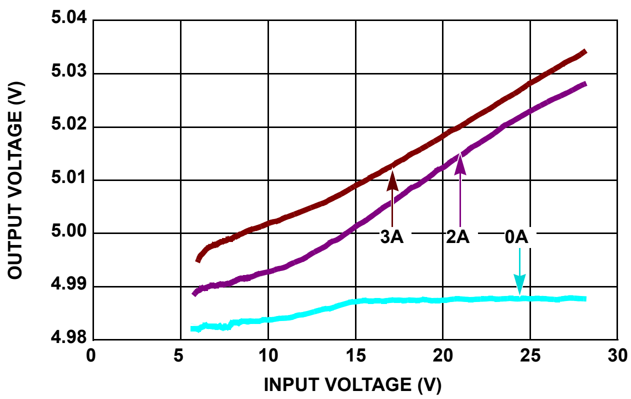


FIGURE 12. OUTPUT VOLTAGE REGULATION vs V_{IN}, CHANNEL 1, T_A = +25°C, 5V_{OUT}, F_{SW} = 500kHz

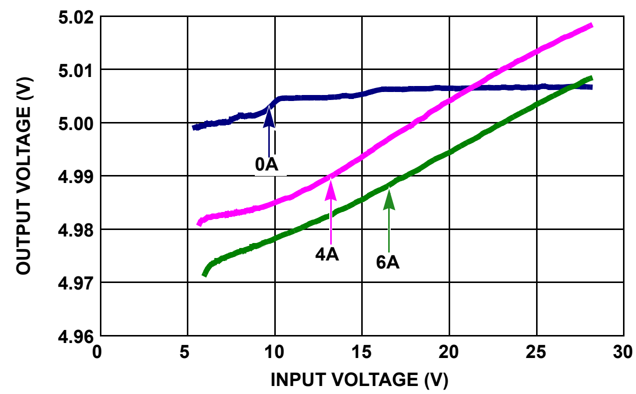


FIGURE 13. OUTPUT VOLTAGE REGULATION vs V_{IN}, CURRENT SHARING, T_A = +25°C, 5V_{OUT}, F_{SW} = 500kHz

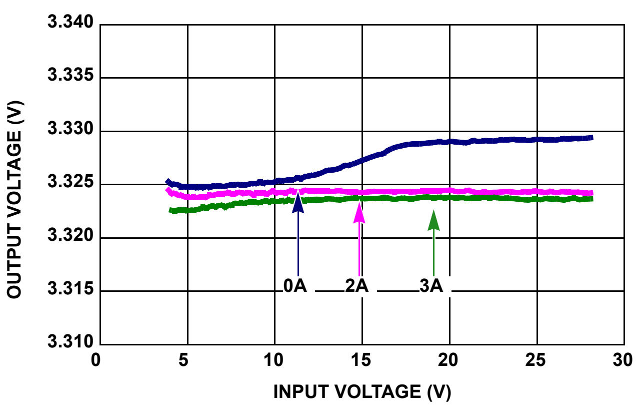


FIGURE 14. OUTPUT VOLTAGE REGULATION vs V_{IN}, CHANNEL 2, T_A = +25°C, 3.3V_{OUT}, F_{SW} = 500kHz

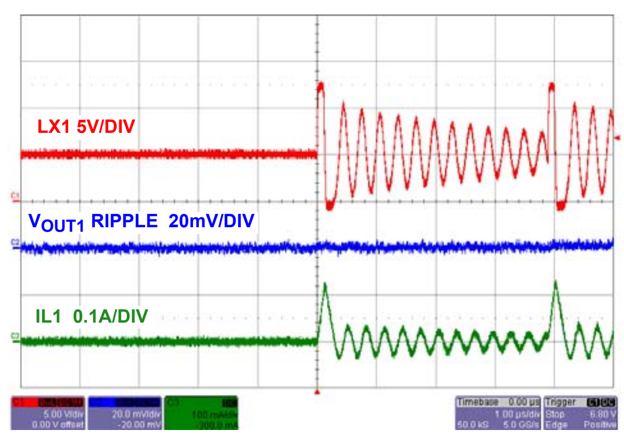


FIGURE 15. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Continued)

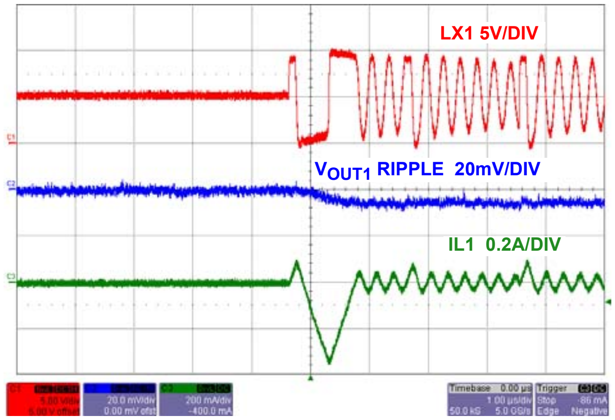


FIGURE 16. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 (V_{IN} = 9V)

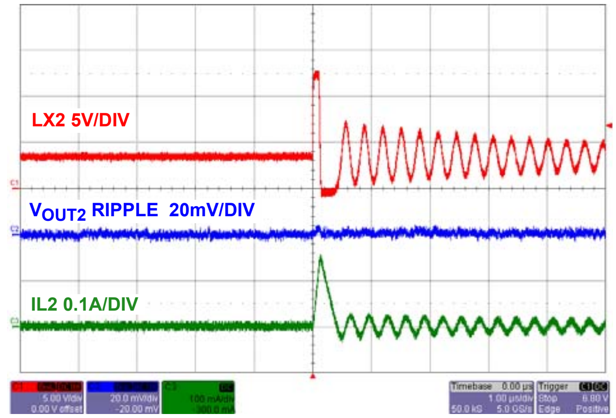


FIGURE 17. STEADY STATE OPERATION AT NO LOAD CHANNEL 2

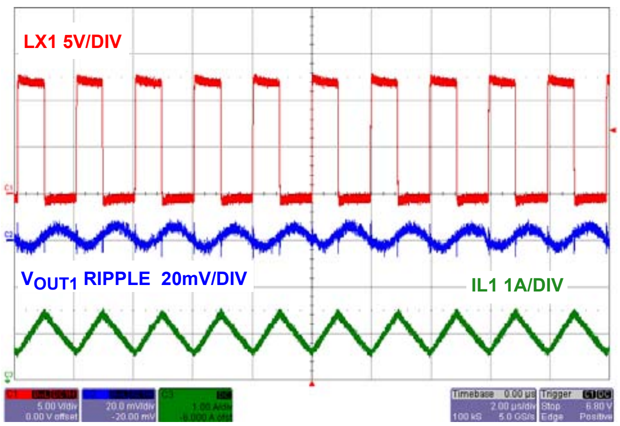


FIGURE 18. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

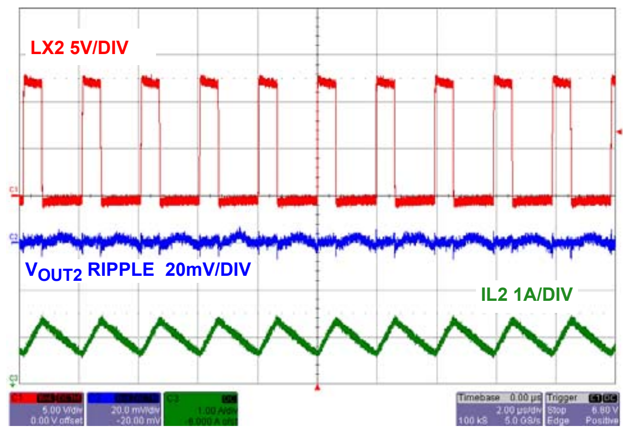


FIGURE 19. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

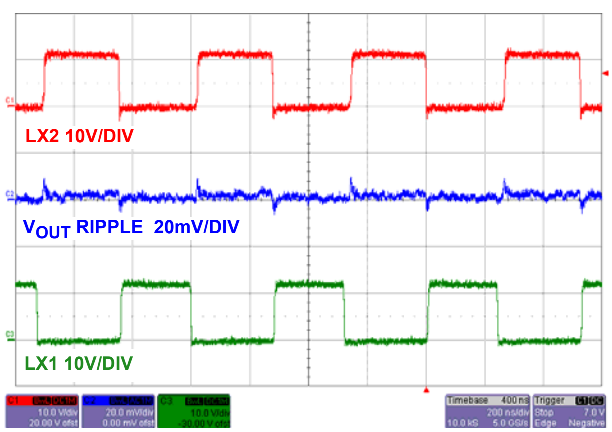


FIGURE 20. STEADY STATE OPERATION WITH FULL LOAD CURRENT SHARING

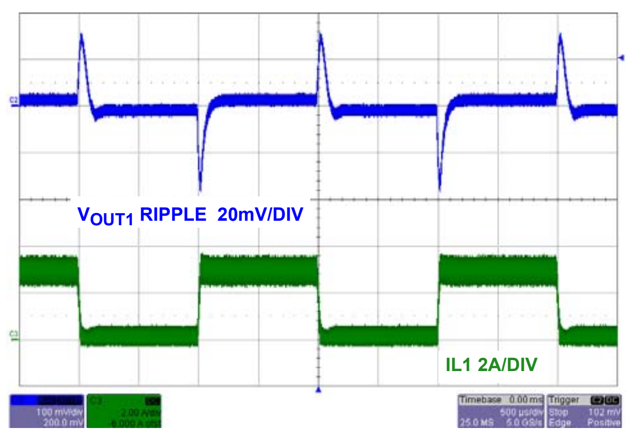


FIGURE 21. LOAD TRANSIENT CHANNEL 1

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Continued)

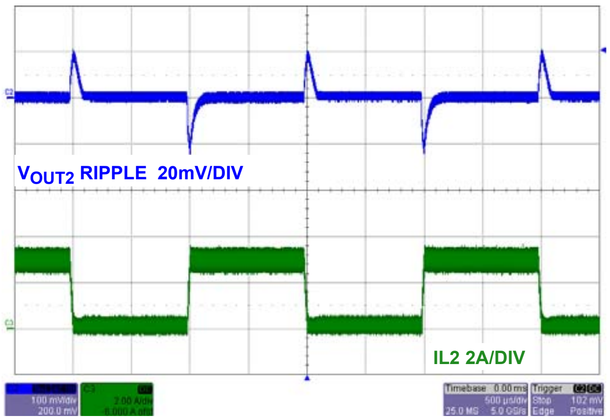


FIGURE 22. LOAD TRANSIENT CHANNEL 2

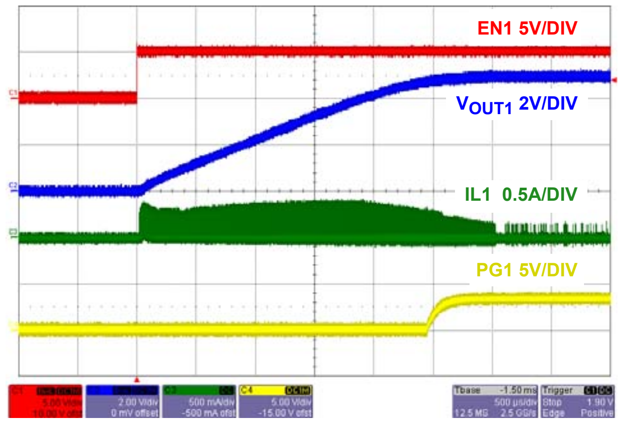


FIGURE 23. SOFT-START WITH NO LOAD CHANNEL 1

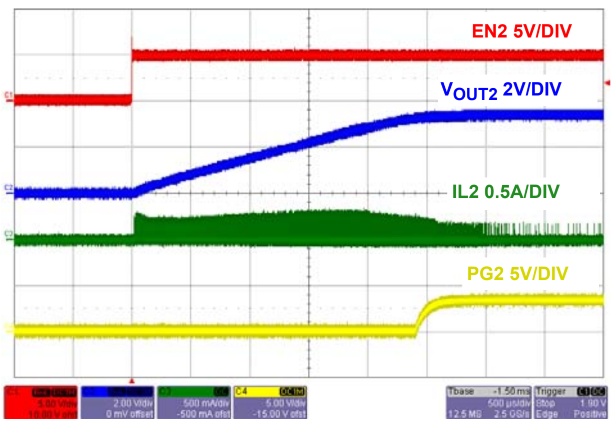


FIGURE 24. SOFT-START WITH NO LOAD CHANNEL 2

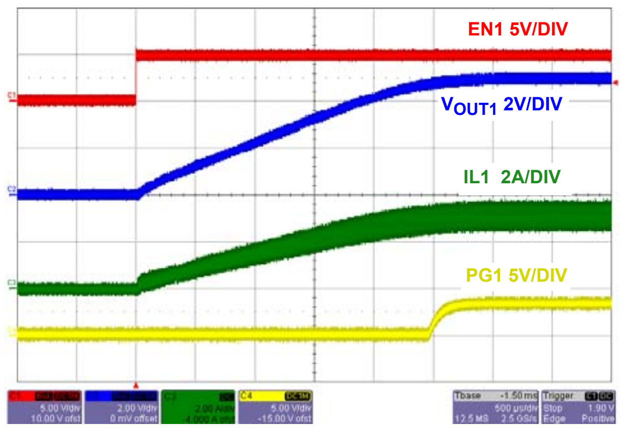


FIGURE 25. SOFT-START AT FULL LOAD CHANNEL 1

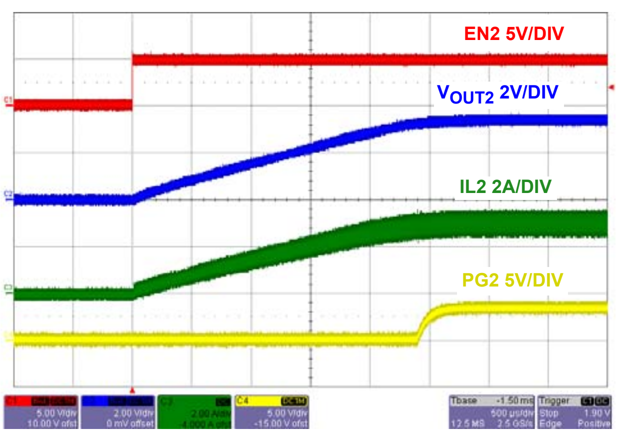


FIGURE 26. SOFT-START AT FULL LOAD CHANNEL 2

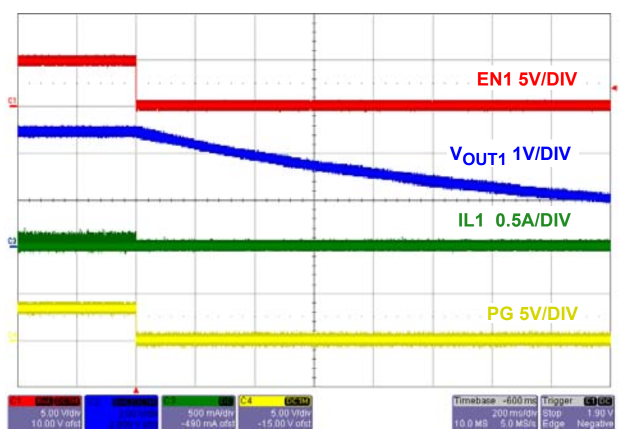


FIGURE 27. SHUTDOWN WITH NO LOAD CHANNEL 1

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

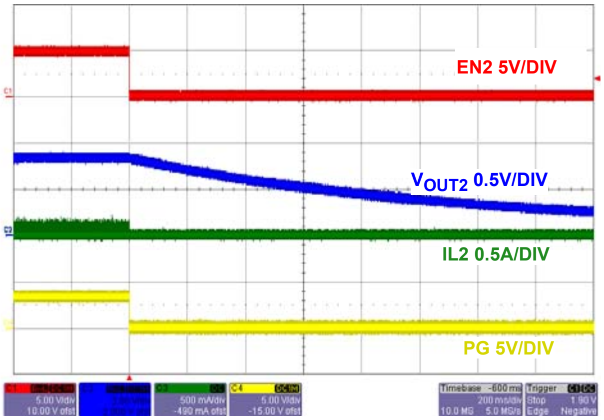


FIGURE 28. SHUTDOWN WITH NO LOAD CHANNEL 2

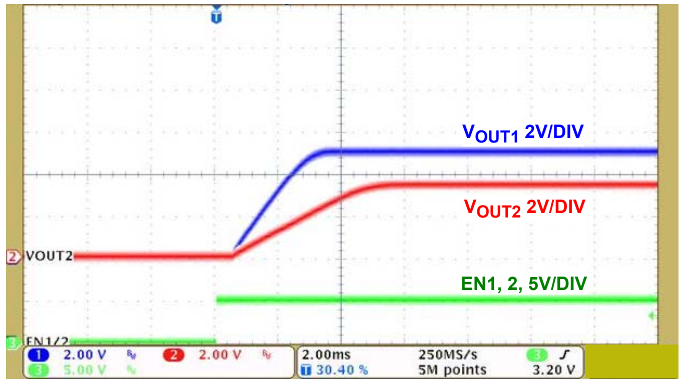


FIGURE 29. INDEPENDENT START-UP SEQUENCING AT NO LOAD

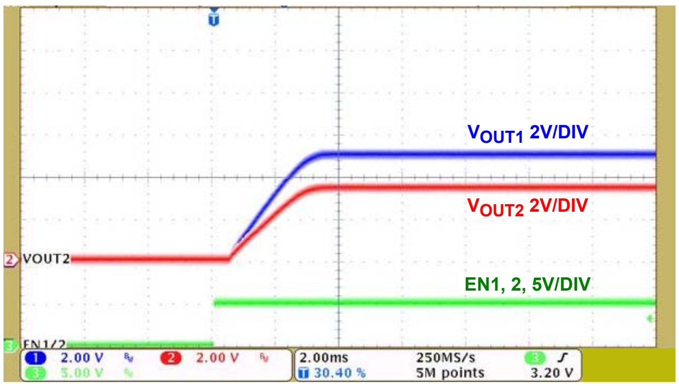


FIGURE 30. RATIOMETRIC START-UP SEQUENCING AT NO LOAD

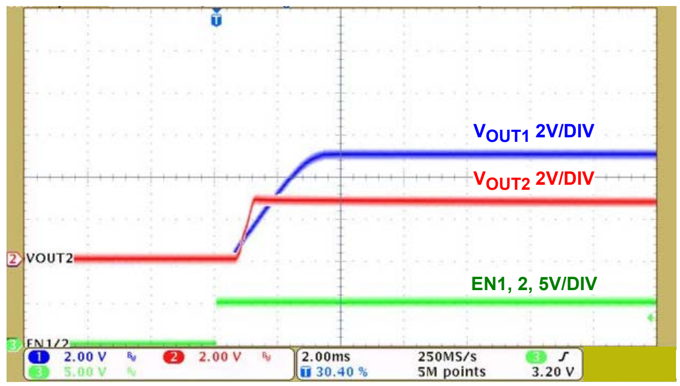


FIGURE 31. ABSOLUTE START-UP SEQUENCING AT NO LOAD

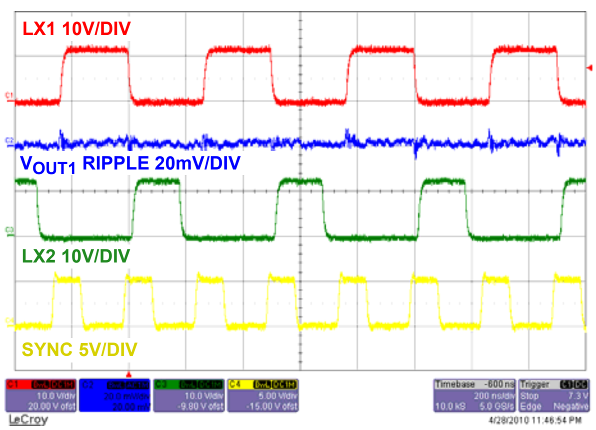


FIGURE 32. STEADY STATE OPERATION CHANNEL 1 AT FULL LOAD WITH SYNC FREQUENCY = 4MHz

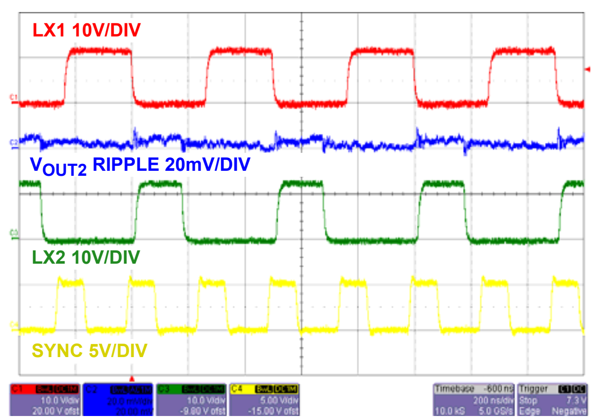


FIGURE 33. STEADY STATE OPERATION CHANNEL 2 AT FULL LOAD WITH SYNC FREQUENCY = 4MHz

Typical Performance Curves

Circuit of Figure 2. V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, I_{OUT1} = 3A, I_{OUT2} = 3A, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Continued)

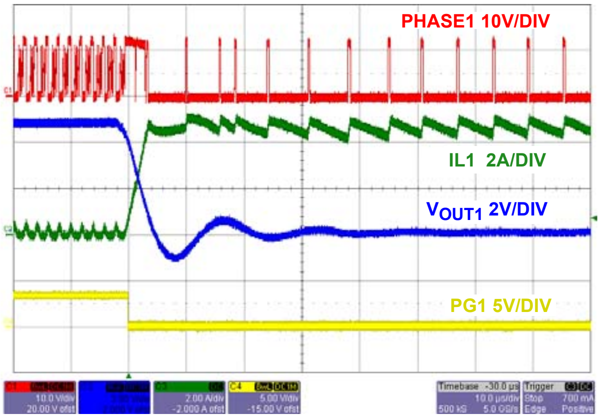


FIGURE 34. OUTPUT SHORT CIRCUIT CHANNEL 1

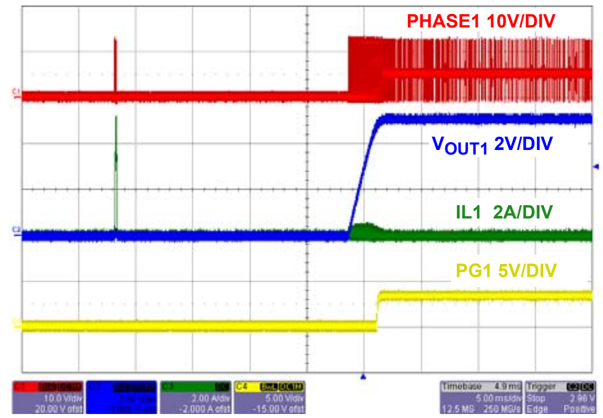


FIGURE 35. OUTPUT SHORT CIRCUIT HICCUP AND RECOVERY FOR CHANNEL 1

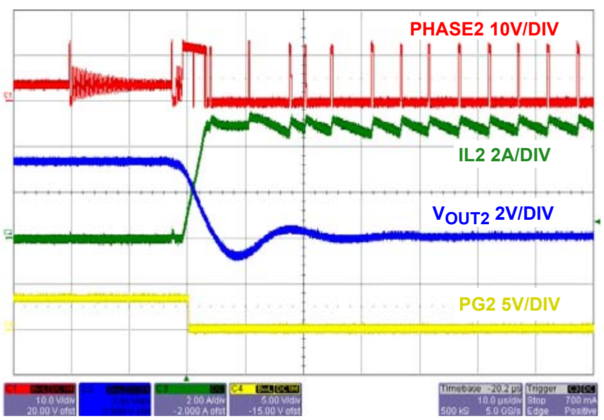


FIGURE 36. OUTPUT SHORT CIRCUIT CHANNEL 2

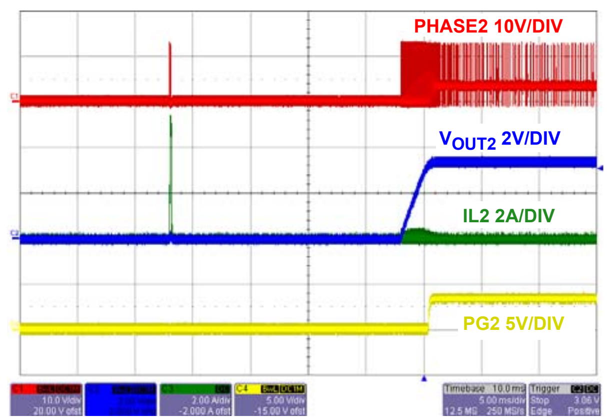


FIGURE 37. OUTPUT SHORT CIRCUIT HICCUP AND RECOVERY FOR CHANNEL 2

Detailed Description

The ISL78208 combines a standard buck PWM controller with an integrated switching MOSFET. The buck controller drives an internal N-Channel MOSFET and requires an external diode to deliver load current up to 3A. A Schottky diode is recommended for improved efficiency and performance over a standard diode. The standard buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +4.5V to +28V. The converter output can be regulated to as low as 0.8V. These features make the ISL78208 ideally suited for infotainment system power, and DSP and embedded processor power supply applications.

The ISL78208 employs a peak current mode control loop which simplifies feedback loop compensation and rejects input voltage variation. External feedback loop compensation allows flexibility in output filter component selection. The regulator switches at a default 500kHz and it can be adjusted from 300kHz to 2MHz with a resistor from FS to GND. The ISL78208 is also synchronizable from 300kHz to 2MHz.

Operation Initialization

The power-ON reset circuitry and enable inputs prevent false start-up of the PWM regulator output. Once all input criteria are met, the controller soft-starts the output voltage to the programmed level.

Power-On Reset and Undervoltage Lockout

The ISL78208 automatically initializes upon receipt of input power supply. The power-on reset (POR) function continually monitors VIN1 voltage. While below the POR threshold, the controller inhibits switching of the internal power MOSFET. Once exceeded, the controller initializes the internal soft-start circuitry. If VIN1 supply drops below their falling POR threshold during soft-start or operation, the buck regulator is disabled until the input voltage returns.

Enable and Disable

When EN1 and EN2 are pulled low, the device enters shutdown mode and the supply current drops to a typical value of 20µA. All internal power devices are held in a high-impedance state while in shutdown mode.

The EN pin enables the controller of the ISL78208. When the voltage on the EN pin exceeds its logic rising threshold, the controller initiates the 2ms soft-start function for the PWM regulator. If the voltage on the EN pin drops below the falling threshold, the buck regulator shuts down.

If EN1, EN2 pins are driven by an external signal, the minimum off-time for EN1, EN2 should be:

$$EN\_T\_off\ (\mu s) = 10\mu s \bullet C_{SS}/2.2nF \tag{EQ. 1}$$

where C_{SS} is the soft-start pin capacitor (nF). ISL78208 does not have debouncing to EN1, EN2 external signals.

Power-Good

PG is the open-drain output of a window comparator that continuously monitors the buck regulator output voltage via the FB pin. PG is actively held low when EN is low and during the buck regulator soft-start period. After the soft-start period terminates, PG becomes high impedance as long as the output voltage (monitored on the FB pin) is above 90% of the nominal regulation voltage set by FB. When V_{OUT} drops 10% below the nominal regulation voltage, the ISL78208 pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ internal pull-up resistor.

Output Voltage Selection

The regulator output voltages is easily programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; refer to Figure 38.

The output voltage programming resistor, R_2, depends on the value chosen for the feedback resistor, R_3, and the desired output voltage, V_{OUT}, of the regulator. Equation 2 describes the relationship between V_{OUT} and resistor values. R_3 is often chosen to be in the 1kΩ to 10kΩ range.

$$R_2 = (V_{OUT} - 0.8) \bullet R_3 / 0.8 \tag{EQ. 2}$$

If the desired output voltage is 0.8V, then R_3 is left unpopulated and R_2 is 0Ω.

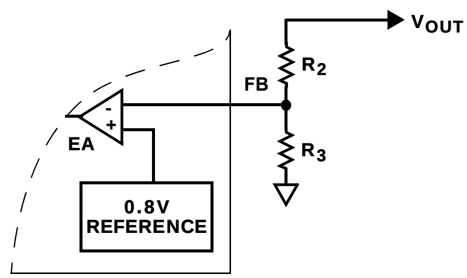


FIGURE 38. EXTERNAL RESISTOR DIVIDER

Output Tracking and Sequencing

Output tracking and sequencing between channels can be implemented by using the SS1 and SS2 pins. Figures 39, 40 and 41 show several configurations for output tracking/sequencing for a 5.0V and 3.3V application. Independent soft-start for each channel is shown in Figure 39 and measured in Figure 29. The output ramp-time for each channel (t_{SS}) is set by the soft-start capacitor (C_{SS}).

$$C_{SS}[\mu F] = 2.5 * t_{SS}(s) \tag{EQ. 3}$$

Maximum C_{SS} value is 50nF.

Ratiometric tracking is achieved in Figure 40 by using the same value for the soft-start capacitor on each channel; it is measured in Figure 30.

By connecting a feedback network from V_{OUT1} to the SS2 pin with the same ratio that sets V_{OUT2} voltage, absolute tracking shown in Figure 41 is implemented. The measurement is shown in Figure 31. If the output of Channel 1 is shorted to GND, it will enter overcurrent hiccup mode, SS2 will be pulled low through the added resistor between V_{OUT1} and SS2 and this will force Channel 2 into hiccup as well. If the output of Channel 2 is shorted to GND with VOUT1 in regulation, it will enter overcurrent hiccup mode with a very short hiccup waiting time. The reason is that VOUT1 is still in regulation and can pull-up SS2 very quickly via the resistor added between VOUT1 and SS2.

Figure 42 illustrates output sequencing. When EN1 is high and EN2 is floating, OUT1 comes up first and OUT2 won't start until OUT1 > 90% of its regulation point. If EN1 is floating and EN2 is high, OUT2 comes up first and OUT1 won't start until OUT2 > 90% of its regulation point. If EN1 = EN2 = high, OUT1 and OUT2 come up at the same time. Please refer to Table 1 for conditions related to Figure 42 (Output Sequencing).

TABLE 1. OUTPUT SEQUENCING

EN1	EN2	V_{OUT1}	V_{OUT2}	NOTE
High	Floating	First	After V_{OUT1} > 90%	
Floating	High	After V_{OUT2} > 90%	First	
High	High	Same time as V_{OUT2}	Same time as V_{OUT1}	
Floating	Floating			Not Allowed

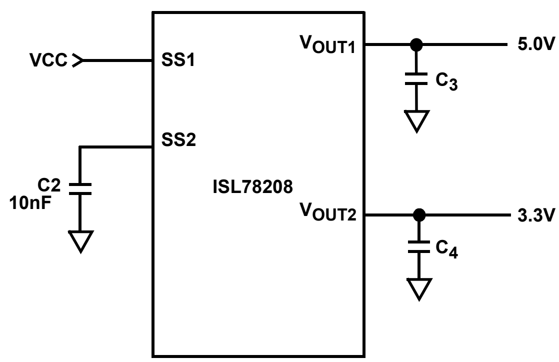


FIGURE 39. INDEPENDENT START-UP

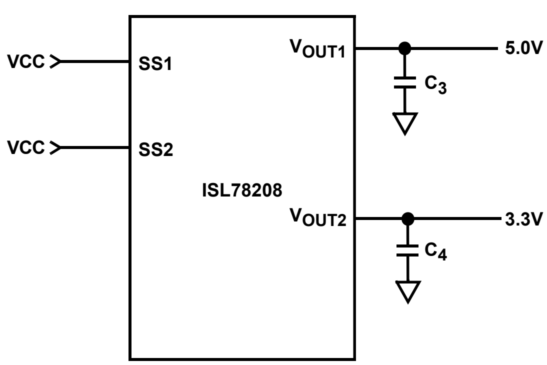


FIGURE 40. RATIOMETRIC START-UP

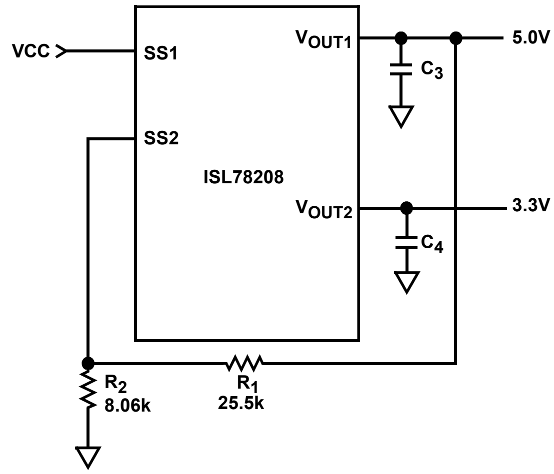


FIGURE 41. ABSOLUTE START-UP

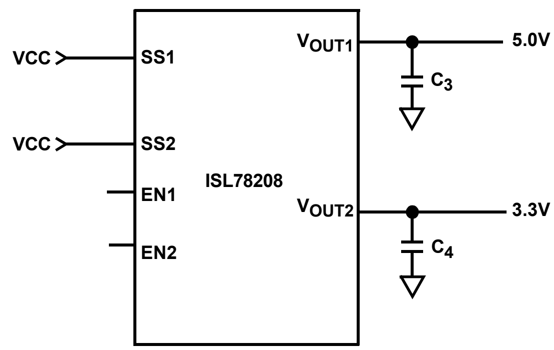


FIGURE 42. OUTPUT SEQUENCING

Protection Features

The ISL78208 limits the current in all on-chip power devices. Overcurrent protection limits the current on the two buck regulators and internal LDO for V_{CC}.

Buck Regulator Overcurrent Protection

During the PWM on-time, the current through the internal switching MOSFET is sampled and scaled through an internal pilot device. The sampled current is compared to a nominal 5A overcurrent limit. If the sampled current exceeds the overcurrent limit reference level, an internal overcurrent fault counter is set to 1 and an internal flag is set. The internal power MOSFET is immediately turned off and will not be turned on again until the next switching cycle.

The protection circuitry continues to monitor the current and turns off the internal MOSFET as described. If the overcurrent condition persists for 17 sequential clock cycles, the overcurrent fault counter overflows indicating an overcurrent fault condition exists. The regulator is shut down and power-good goes low.

The buck controller attempts to recover from the overcurrent condition after waiting 8 soft-start cycles. The internal overcurrent flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the overcurrent fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

Thermal Overload Protection

Thermal overload protection limits maximum junction temperature in the ISL78208. When the junction temperature (T_J) exceeds +150°C, a thermal sensor sends a signal to the fault monitor.

The fault monitor commands the buck regulator to shut down. When the junction temperature has decreased by 20°C, the regulator will attempt a normal soft-start sequence and return to normal operation. For continuous operation, the +125°C junction temperature rating should not be exceeded.

BOOT Undervoltage Protection

If the BOOT capacitor voltage falls below 2.5V, the BOOT undervoltage protection circuit will pull the phase pin low through a 1Ω switch for 400ns to recharge the capacitor. This operation may arise during long periods of no switching as in no load situations.

Application Guidelines

Operating Frequency

The ISL78208 operates at a default switching frequency of 500kHz if FS is tied to VCC. Tie a resistor from FS to GND to program the switching frequency from 300kHz to 2MHz, as shown in Equation 4.

$$R_{FS}[k\Omega] = 122k\Omega*(t - 0.17\mu s) \quad \text{(EQ. 4)}$$

Where:

t is the switching period in µs.

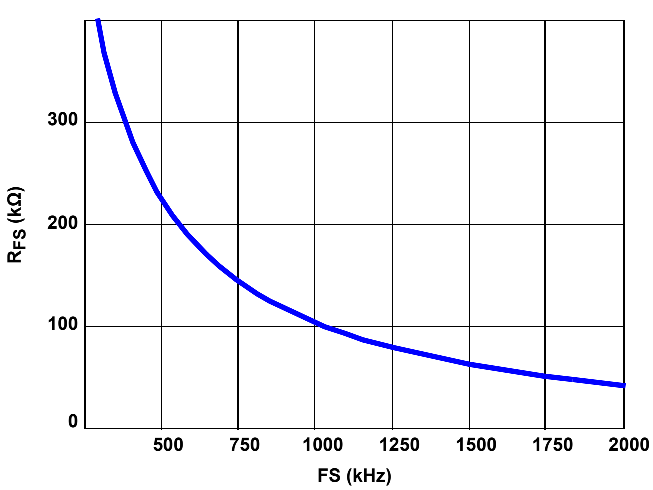


FIGURE 43. R_{FS} SELECTION vs FS

Synchronization Control

The frequency of operation can be synchronized up to 2MHz by an external signal applied to the SYNCIN pin. The falling edge on the SYNCIN triggers the rising edge of PHASE1/2. The switching frequency for each output is half of the SYNCIN frequency.

Output Inductor Selection

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% of total load current. The inductor value can then be calculated using Equation 5:

$$L = \frac{V_{IN} - V_{OUT}}{Fs \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 5)}$$

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it will not saturate in overcurrent conditions.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are 2 critical factors when considering output capacitance choice. The current mode control loop allows the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8*F_{SW}*C_{OUT}} \quad \text{(EQ. 6)}$$

where ΔI is the inductor's peak-to-peak ripple current, F_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I*ESR \quad \text{(EQ. 7)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. Equation 8 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}{}^2 * L}{V_{OUT}{}^2 * \left((V_{OUTMAX}/V_{OUT})^2 - 1\right)} \quad \text{(EQ. 8)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load. For an overshoot of 5%, the equation becomes Equation 9:

$$C_{OUT} = \frac{I_{OUT}{}^2 * L}{V_{OUT}{}^2 * (1.05^2 - 1)} \quad \text{(EQ. 9)}$$

The graph in Figure 44 shows the relationship of C_{OUT} and % overshoot at 3 different output voltages. L is assumed to be 7µH and I_{OUT} is 3A.

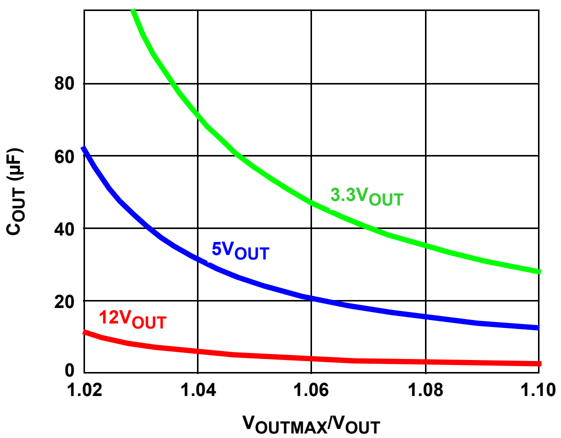


FIGURE 44. C_{OUT} vs OVERSHOOT V_{OUTMAX}/V_{OUT}

Current Sharing Configuration

In current sharing configuration, FB1 is connected to FB2, EN1 to EN2, COMP1 to COMP2 and V_{OUT1} to V_{OUT2} as shown in Figure 3. As a result, the equivalent gm doubles its single channel value. Since the two channels are out-of-phase, the frequency will be 2X the channel switching frequency. Ripple current cancellation will reduce the ripple current seen by the output capacitors and thus lower the ripple voltage. This results in the ability to use less capacitance than would be required by a single phase design of similar rating. Ripple current cancellation also reduces the ripple current seen at the input capacitors.

Input Capacitor Selection

To reduce the resulting input voltage ripple and to minimize EMI by forcing the very high frequency switching current into a tight local loop, an input capacitor is required. The input capacitor must have adequate ripple current rating, which can be approximated by the Equation 10.

If capacitors other than MLCC are used, attention must be paid to ripple and surge current ratings.

$$\frac{I_{RMS}}{Io} = \sqrt{D - D^2} \quad \text{(EQ. 10)}$$

where $D = V_O/V_{IN}$

The input ripple current is graphically represented in Figure 45.

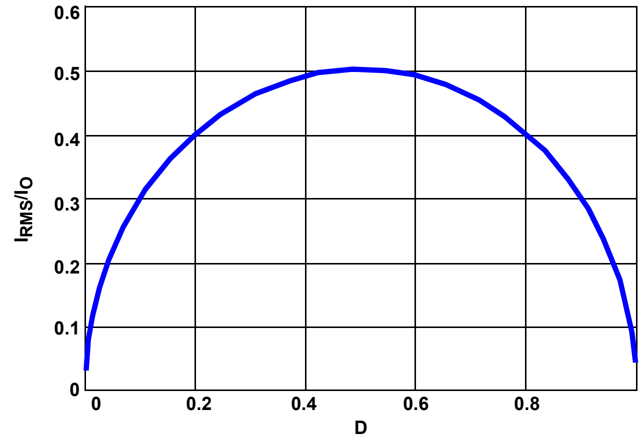


FIGURE 45. I_{RMS}/I_O vs DUTY CYCLE

A minimum of 10µF ceramic capacitance is required on each VIN pin. The capacitors must be as close to the IC as physically possible. Additional capacitance may be used.

Loop Compensation Design

ISL78208 uses a constant frequency current mode control architecture to achieve simplified loop compensation and fast loop transient response.

The compensator schematic is shown in Figure 47. As mentioned in the C_{OUT} selection, ISL78208 allows the usage of low ESR output capacitor. Choice of the loop bandwidth f_c is somewhat arbitrary but should not exceed 1/4 of the switching frequency. As a starting point, the lower of 100kHz or 1/6 of the switching frequency is reasonable. The following equations determine initial component values for the compensation, allowing the designer to make the selection with minimal effort. Further detail is provided in “Theory of Compensation” on page 19 to allow fine tuning of the compensator.

Compensation resistor R_1 is given by Equation 11:

$$R_1 = \frac{2\pi f_c V_o C_o R_T}{g_m V_{FB}} \quad \text{(EQ. 11)}$$

which when applied to ISL78208 becomes Equation 12:

$$R_1[k\Omega] = 0.008247 * f_c * V_o * C_o \quad \text{(EQ. 12)}$$

where C_o is the output capacitor value [µF], f_c = loop bandwidth [kHz] and V_o is the output voltage [V].

Compensation capacitors C_1 [nF], C_2 [pF] are given by Equation 13:

$$C_1 = \frac{C_o \times V_o \times (10)^3}{I_o \times R_1}, C_2 = \frac{C_o \times R_c \times (10)^6}{R_1} \quad \text{(EQ. 13)}$$

where Io [A] is the output load current, R_1 (Ω) and R_c (Ω) is the ESR of the output capacitor C_o.

Example: V_o = 5V, I_o = 3A, f_s = 500kHz, f_c = 50kHz, C_o = 47µF/R_c = 5mΩ, then the compensation resistance R_1 = 96kΩ.

The compensation capacitors are:

C_1 = 815pF, C_2 = 2.5pF (There is approximately 3pF parasitic capacitance from V_{COMP} to GND; therefore, C_2 is optional).

Theory of Compensation

The sensed current signal is injected into the voltage loop to achieve current mode control to simplify the loop compensation design. The inductor is not considered as a state variable for current mode control and the system becomes a single order system. It is much easier to design a compensator to stabilize the voltage loop than voltage mode control. Figure 46 shows the small signal model of the synchronous buck regulator.

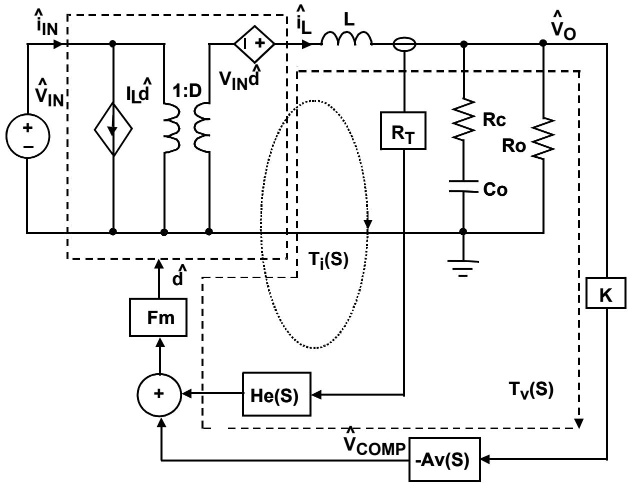


FIGURE 46. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

PWM Comparator Gain F_m

The PWM comparator gain F_m for peak current mode control is given by Equation 14:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \quad \text{(EQ. 14)}$$

Where S_e is the slew rate of the slope compensation and S_n is given by Equation 15.

$$S_n = R_t\frac{V_{in} - V_o}{L} \quad \text{(EQ. 15)}$$

Where:

R_T is trans-resistance, and is the product of the current sensing resistance and gain of the current amplifier in current loop.

CURRENT SAMPLING TRANSFER FUNCTION $H_e(S)$

In current loop, the current signal is sampled every switching cycle. Equation 16 shows the transfer function:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \quad \text{(EQ. 16)}$$

Where Q_n and ω_n are given by $Q_n = -\frac{2}{\pi}, = \omega_n = \pi f_s$.

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is calculated in Equation 17:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 17)}$$

Where $\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L}}, \omega_o = \frac{1}{\sqrt{LC_o}}$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 18:

$$F_2(S) = \frac{\hat{i}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_L}\frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 18)}$$

Where $\omega_z = \frac{1}{R_o C_o}$.

Current loop gain $T_i(S)$ is expressed as Equation 19:

$$T_i(S) = R_T F_m F_2(S) H_e(S) \quad \text{(EQ. 19)}$$

The voltage loop gain with open current loop is calculated in Equation 20:

$$T_v(S) = K F_m F_1(S) A_v(S) \quad \text{(EQ. 20)}$$

The voltage loop gain with current loop closed is given by Equation 21:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \quad \text{(EQ. 21)}$$

Where $K = \frac{V_{FB}}{V_o}$, V_{FB} is the feedback voltage of the voltage error amplifier. If $T_i(S)$>>1, then Equation 21 can be simplified as shown in Equation 22:

$$L_v(S) = \frac{V_{FB}}{V_o}\frac{R_o + R_L}{R_T}\frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}}\frac{A_v(S)}{H_e(S)}, \omega_p \approx \frac{1}{R_o C_o} \quad \text{(EQ. 22)}$$

From Equation 22, it is shown that the system is a single order system, which has a single pole located at ω_P before the half switching frequency. Therefore, a simple type II compensator can be easily used to stabilize the system.

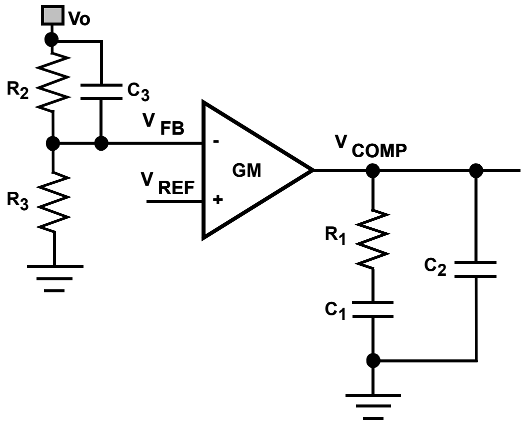


FIGURE 47. TYPE II COMPENSATOR

Figure 47 shows the type II compensator and its transfer function is expressed as Equation 23:

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{g_m}{C_1 + C_2} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp}}\right)} \quad \text{(EQ. 23)}$$

Where:

$$\omega_{cz1} = \frac{1}{R_1 C_1}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \omega_{cp} = \frac{C_1 + C_2}{R_1 C_1 C_2} \quad \text{(EQ. 24)}$$

the compensator design goal is:

High DC gain

Loop bandwidth f_c: $\left(\frac{1}{4} \text{to} \frac{1}{10}\right) f_s$

Gain margin: >10dB

Phase margin: 40°

The compensator design procedure is shown in Equation 25:

$$\text{Put compensator zero } \omega_{cz1} = (1 \text{to} 3) \frac{1}{R_O C_O} \quad \text{(EQ. 25)}$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower.

The loop gain $T_v(S)$ at crossover frequency of f_c has unity gain. Therefore, the compensator resistance R_1 is determined by Equation 26:

$$R_1 = \frac{2\pi f_c V_o C_o R_T}{g_m V_{FB}} \quad \text{(EQ. 26)}$$

where g_m is the trans-conductance of the voltage error amplifier, typically 200µA/V. Compensator capacitor C_1 is then given by Equation 27:

$$C_1 = \frac{1}{R_1 \omega_{cz}}, C_2 = \frac{1}{2\pi R_1 f_{esr}} \quad \text{(EQ. 27)}$$

Example: V_{IN} = 12V, V_o = 5V, I_o = 3A, f_s = 500kHz, C_o = 220µF/5mΩ, L = 5.6µH, g_m = 200µs, R_T = 0.21, V_{FB} = 0.8V, $S_e = 1.1 \times 10^5$V/s, $S_n = 3.4 \times 10^5$V/s, f_c = 80kHz, then compensator resistance R_1 = 72kΩ.

Put the compensator zero at 6.6kHz (~1.5x C_oR_o), and put the compensator pole at ESR zero, which is 1.45MHz. The compensator capacitors are:

C_1 = 470pF, C_2 = 3pF (There is approximately 3pF parasitic capacitance from V_{COMP} to GND; therefore, C_2 is optional).

Figure 48A shows the simulated voltage loop gain. It is shown that it has 80kHz loop bandwidth with 69° phase margin and 15dB gain margin. Optional addition phase boost can be added to the overall loop response by using C_3.

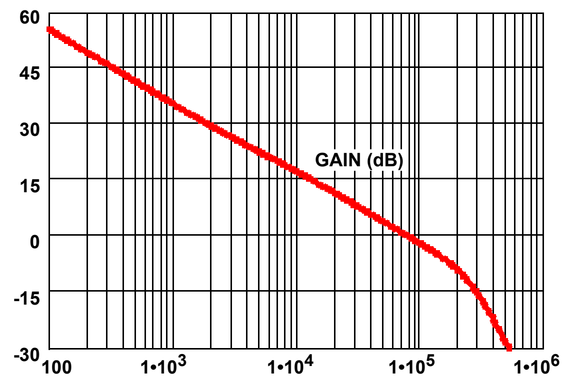


FIGURE 48A.

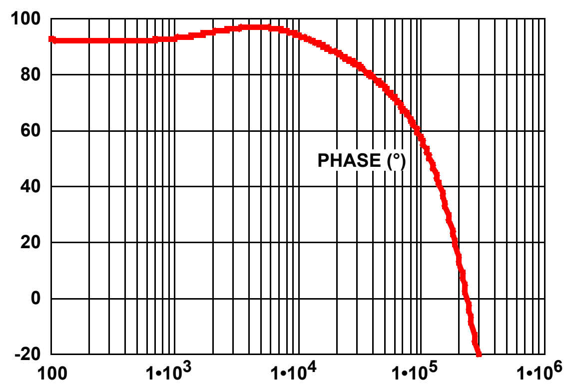


FIGURE 48B.

Rectifier Selection

Current circulates from ground to the junction of the external Schottky diode and the inductor when the high-side switch is off. As a consequence, the polarity of the switching node is negative with respect to ground. This voltage is approximately -0.5V (a Schottky diode drop) during the off-time. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor. The power dissipation when the Schottky diode conducts is expressed in Equation 28:

$$P_D[W] = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(EQ. 28)}$$

Where:

V_D is the voltage drop of the Schottky diode. Selection of the Schottky diode is critical in terms of the high temperature reverse bias leakage current which is very dependent on V_{IN} and exponentially increasing with temperature. Due to the nature of reverse bias leakage vs temperature, the diode should be carefully selected to operate in the worst case circuit conditions. Catastrophic failure is possible if the diode chosen experiences thermal runaway at elevated temperatures. Please refer to Application Note for diode selection.

Power Derating Characteristics

To prevent the ISL78208 from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 29:

$$T_{RISE} = (PD)(\theta_{JA}) \qquad \text{(EQ. 29)}$$

where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 30:

$$T_J = (T_A + T_{RISE}) \qquad \text{(EQ. 30)}$$

where T_A is the ambient temperature. For the WFQFN package, the θ_{JA} is +30°C/W.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C. When considering the thermal design, remember to consider the thermal needs of the rectifier diode.

The ISL78208 delivers full current at ambient temperatures up to +105°C if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level, depending on the Input Voltage/Output Voltage combination and the switching frequency. The device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level.

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently between 100kHz and 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the Schottky diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL78208 switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next, are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 49 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

In order to dissipate heat generated by the internal LDO and MOSFET, the ground pad should be connected to the internal ground plane through at least four vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the ISL78208 first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and Schottky diode and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

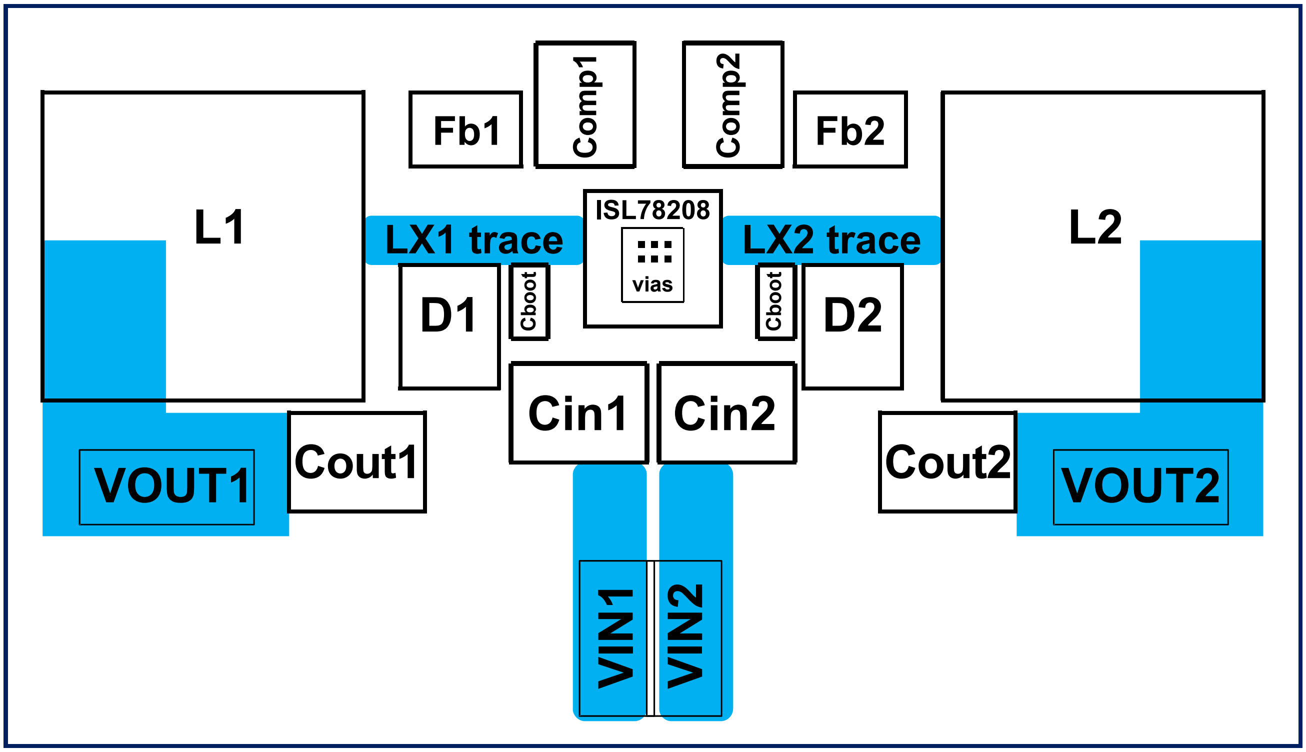


FIGURE 49. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 29, 2014	FN8354.1	Electrical Spec table on page 8 under "SYNCIN Input Threshold"; changed Rising Edge Max value from 1.9V to 2.1V.
July 12, 2013	FN8354.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

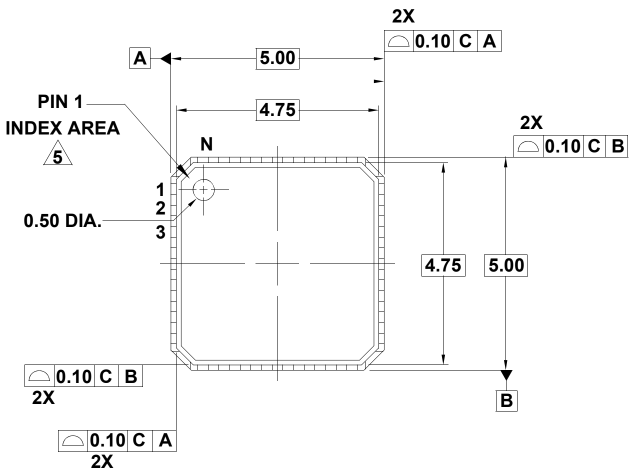
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

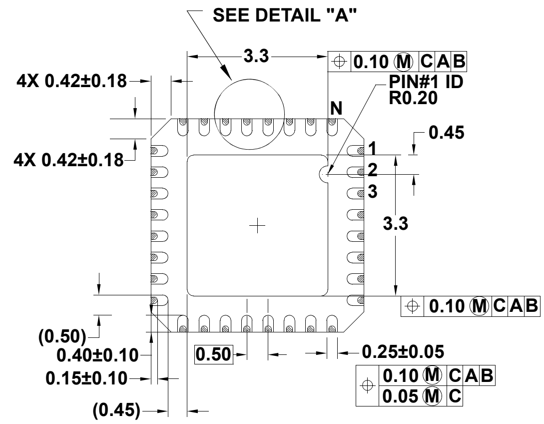
L32.5x5H

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETABLE FLANK)

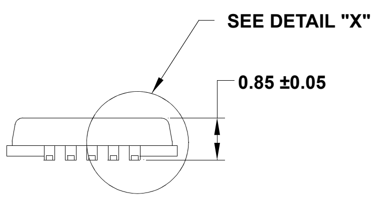
Rev 0, 4/12



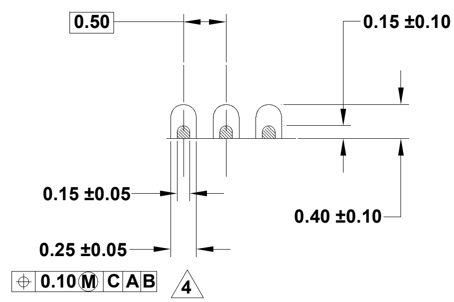
TOP VIEW



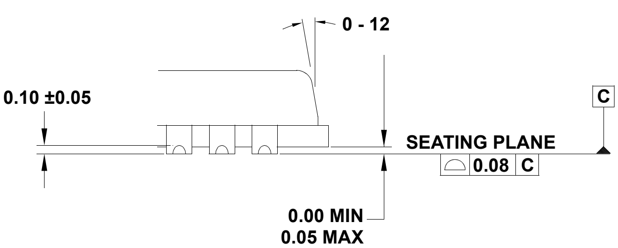
BOTTOM VIEW



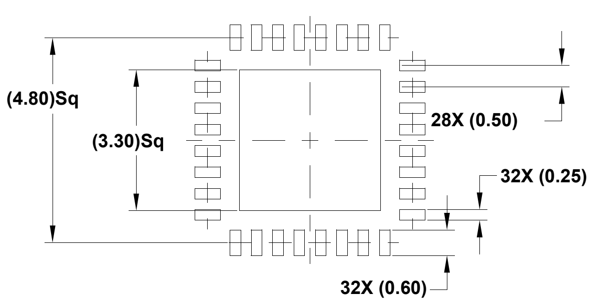
SIDE VIEW



DETAIL "A"



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC MO220