ISL8105, ISL8105A

+5V or +12V Single-Phase Synchronous Buck Converter PWM Controller with Integrated MOSFET Gate Drivers

FN6306
Rev 5.00
April 15, 2010

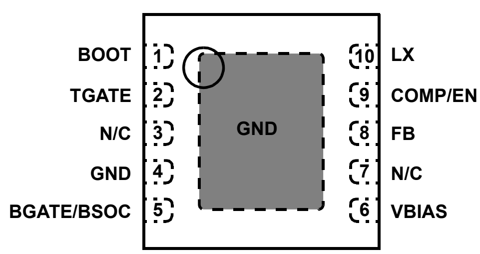
The ISL8105, ISL8105A is a simple single-phase PWM controller for a synchronous buck converter. It operates from +5V or +12V bias supply voltage. With integrated linear regulator, boot diode, and N-Channel MOSFET gate drivers, the ISL8105, ISL8105A reduces external component count and board space requirements. These make the IC suitable for a wide range of applications.

Utilizing voltage-mode control, the output voltage can be precisely regulated to as low as 0.6V. The 0.6V internal reference features a maximum tolerance of ±1.0% over the commercial temperature range, and ±1.5% over the industrial temperature range. Two fixed oscillator frequency versions are available; 300kHz (ISL8105 for high efficiency applications) and 600kHz (ISL8105A for fast transient applications).

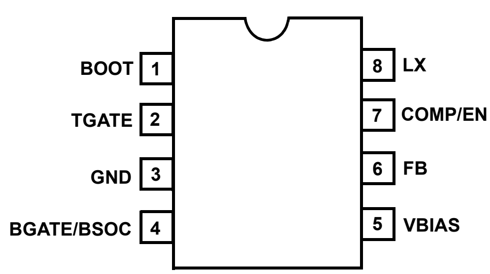
The ISL8105, ISL8105A features the capability of safe start-up with pre-biased load. It also provides overcurrent protection by monitoring the ON-resistance of the bottom-side MOSFET to inhibit PWM operation appropriately. During start-up interval, the resistor connected to BGATE/BSOC pin is employed to program overcurrent protection condition. This approach simplifies the implementation and does not deteriorate converter efficiency.

Pinouts

ISL8105, ISL8105A
(10 LD 3X3 DFN)
TOP VIEW



ISL8105, ISL8105A
(8 LD SOIC)
TOP VIEW



Features

- Operates from +5V or +12V Bias Supply Voltage
  - 1.0V to 12V Input Voltage Range (up to 20V possible with restrictions; see “Input Voltage Considerations” on page 9)
  - 0.6V to V_{IN} Output Voltage Range
- 0.6V Internal Reference Voltage
  - ±1.0% Tolerance Over the Commercial Temperature Range (0°C to +70°C)
  - ±1.5% Tolerance Over the Industrial Temperature Range (-40°C to +85°C).
- Integrated MOSFET Gate Drivers that Operate from V_{BIAS} (+5V to +12V)
  - Bootstrapped High-side Gate Driver with Integrated Boot Diode
  - Drives N-Channel MOSFETs
- Simple Voltage-Mode PWM Control
  - Traditional Dual Edge Modulation
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Cycle
- Fixed Operating Frequency
  - 300kHz for ISL8105
  - 600kHz for ISL8105A
- Fixed Internal Soft-Start with Pre-biased Load Capability
- Lossless, Programmable Overcurrent Protection
  - Uses Bottom-side MOSFET’s $r_{DS(ON)}$
- Enable/Disable Function Using COMP/EN Pin
- Output Current Sourcing and Sinking Currents
- Pb-Free (RoHS Compliant)

Applications

- 5V or 12V DC/DC Regulators
- Industrial Power Systems
- Telecom and Datacom Applications
- Test and Measurement Instruments
- Distributed DC/DC Power Architecture
- Point of Load Modules

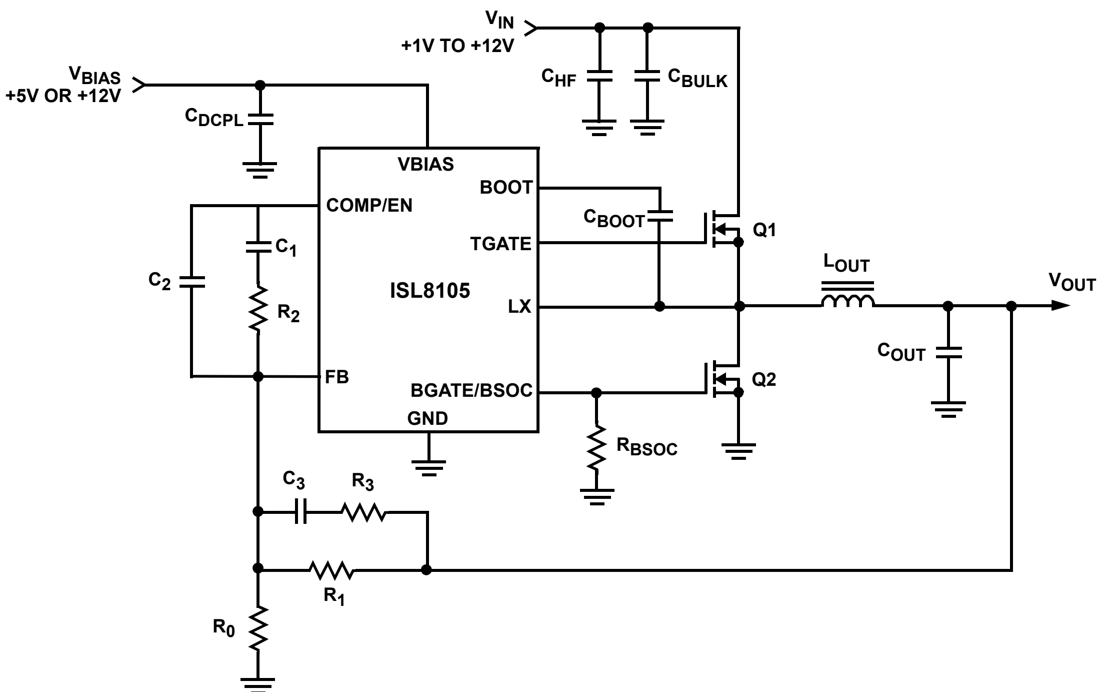
Ordering Information

PART NUMBER (Note)	PART MARKING	SWITCHING FREQUENCY (kHz)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8105CRZ*	5CRZ	300	0 to +70	10 Ld DFN	L10.3x3C
ISL8105IBZ*	8105 IBZ	300	-40 to +85	8 Ld SOIC	M8.15
ISL8105IRZ*	5IRZ	300	-40 to +85	10 Ld DFN	L10.3x3C
ISL8105ACRZ*	05AZ	600	0 to +70	10 Ld DFN	L10.3x3C
ISL8105AIBZ*	8105 AIBZ	600	-40 to +85	8 Ld SOIC	M8.15
ISL8105AIRZ*	5AIZ	600	-40 to +85	10 Ld DFN	L10.3x3C
ISL8105AEVAL1Z	Evaluation Board				

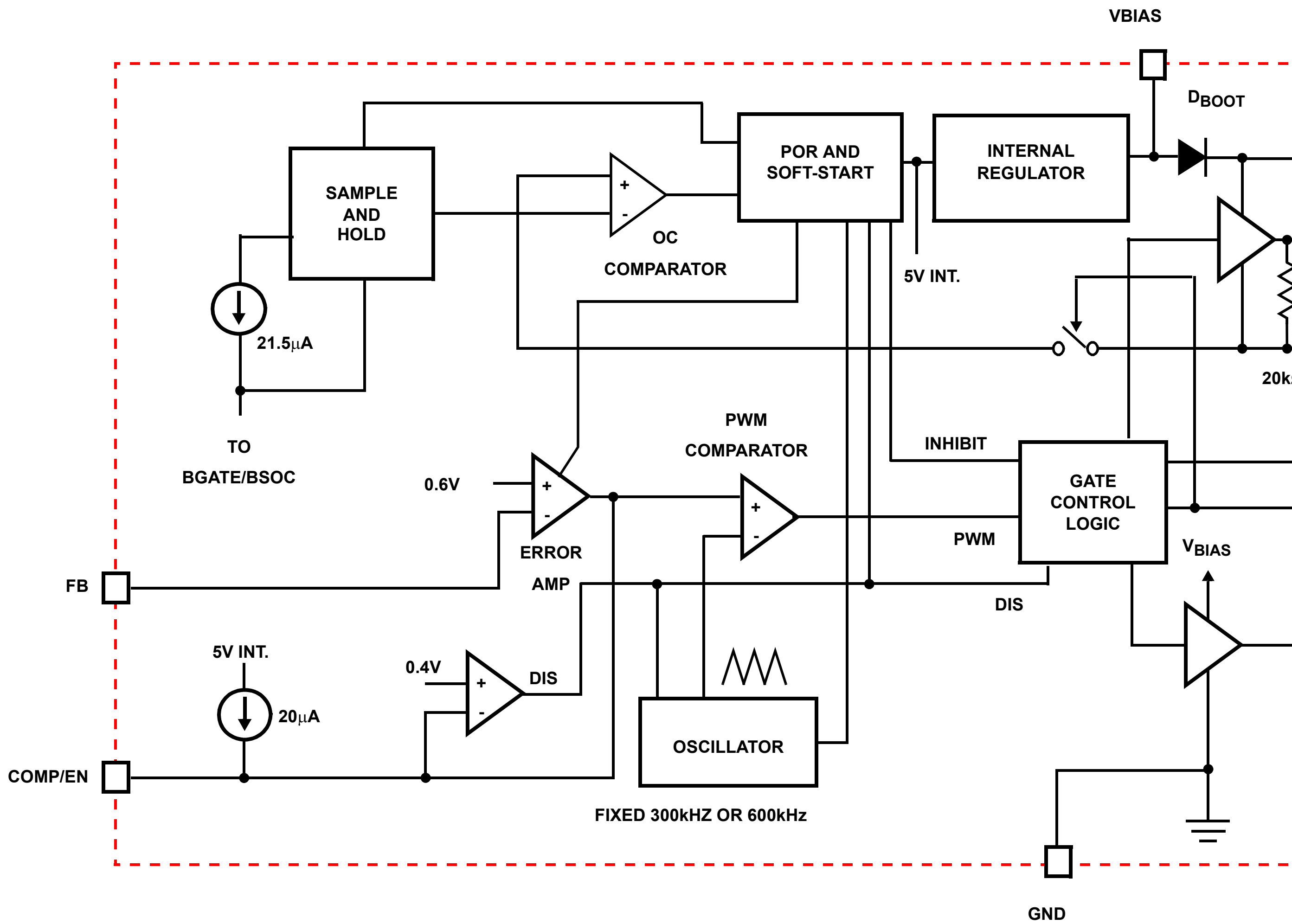
*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Diagram



Block Diagram



Absolute Maximum Ratings

Bias Voltage, V_{BIAS} . . . . GND - 0.3V to +15.0V
Boot Voltage, V_{BOOT} . . . . GND - 0.3V to +36.0V
TGATE Voltage, V_{TGATE} . . . . V_{LX} - 0.3V to V_{BOOT} + 0.3V
BGATE/BSOC Voltage, $V_{BGATE/BSOC}$ . . GND - 0.3 to V_{BIAS} + 0.3V
LX Voltage, V_{LX} . . . . GND - 0.3V to V_{BOOT} + 0.3V
Upper Driver Supply Voltage, V_{BOOT} - V_{LX} 15V
Clamp Voltage, V_{BOOT} - V_{BIAS} 24V
FB, COMP/EN Voltage . . . . GND - 0.3V to 6V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
DFN Package (Notes 1, 2)	44	5.5

Maximum Junction Temperature
(Plastic Package) . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Bias Voltage, V_{BIAS} . . . . . +5V ±10%, +12V ±20%, or 6.5V to 14.4V
Ambient Temperature Range
ISL8105C, ISL8105AC . . . . 0°C to +70°C
ISL8105I, ISL8105AI. . . . . -40°C to +85°C
Junction Temperature Range. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY CURRENTS						
Shutdown V_{BIAS} Supply Current	I_{VBIAS_S}	V_{BIAS} = 12V; Disabled	4	5.2	7	mA
DISABLE						
Disable Threshold (COMP/EN pin)	$V_{DISABLE}$		0.375	0.4	0.425	V
OSCILLATOR						
Nominal Frequency Range	f_{OSC}	ISL8105C	270	300	330	kHz
		ISL8105I	240	300	330	kHz
	f_{OSC}	ISL8105AC	540	600	660	kHz
		ISL8105AI	510	600	660	kHz
Ramp Amplitude (Note 3)	ΔV_{OSC}			1.5		V_{P-P}
POWER-ON RESET						
Rising V_{BIAS} Threshold	V_{POR_R}		3.9	4.1	4.3	V
V_{BIAS} POR Threshold Hysteresis	V_{POR_H}		0.30	0.35	0.40	V
REFERENCE						
Nominal Reference Voltage	V_{REF}			0.6		V
Reference Voltage Tolerance		ISL8105C (0°C to +70°C)	-1.0		+1.0	%
		ISL8105I (-40°C to +85°C)	-1.5		+1.5	%
ERROR AMPLIFIER						
DC Gain (Note 3)	$GAIN_{DC}$			96		dB
Unity Gain-Bandwidth (Note 3)	UGBW			20		MHz
Slew Rate (Note 3)	SR			9		V/µs
GATE DRIVERS						
TGATE Source Resistance	$R_{TG-SRCh}$	V_{BIAS} = 14.5V, 50mA Source Current		3.0		Ω

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TGATE Source Resistance	$R_{TG\text{-}SRCl}$	V_{BIAS} = 4.25V, 50mA Source Current		3.5		Ω
TGATE Sink Resistance	$R_{TG\text{-}SNKh}$	V_{BIAS} = 14.5V, 50mA Source Current		2.7		Ω
TGATE Sink Resistance	$R_{TG\text{-}SNKl}$	V_{BIAS} = 4.25V, 50mA Source Current		2.7		Ω
BGATE Source Resistance	$R_{BG\text{-}SRCh}$	V_{BIAS} = 14.5V, 50mA Source Current		2.4		Ω
BGATE Source Resistance	$R_{BG\text{-}SRCl}$	V_{BIAS} = 4.25V, 50mA Source Current		2.75		Ω
BGATE Sink Resistance	$R_{BG\text{-}SNKh}$	V_{BIAS} = 14.5V, 50mA Source Current		2.0		Ω
BGATE Sink Resistance	$R_{BG\text{-}SNKl}$	V_{BIAS} = 4.25V, 50mA Source Current		2.1		Ω
OVERCURRENT PROTECTION (OCP)						
BSOC Current Source	I_{BSOC}	ISL8105C; BGATE/BSOC Disabled	19.5	21.5	23.5	µA
		ISL8105I; BGATE/BSOC Disabled	18.0	21.5	23.5	µA

NOTE:

3. Limits established by characterization and are not production tested.

Functional Pin Description (SOIC, DFN)

BOOT (SOIC Pin 1, DFN Pin 1)

This pin provides ground referenced bias voltage to the top-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive an N-Channel MOSFET (equal to V_{BIAS} minus the on-chip BOOT diode voltage drop), with respect to LX.

TGATE (SOIC Pin 2, DFN Pin 2)

Connect this pin to the gate of top-side MOSFET; it provides the PWM-controlled gate drive. It is also monitored by the adaptive shoot-through protection circuitry to determine when the top-side MOSFET has turned off.

GND (SOIC Pin 3, DFN Pin 4)

This pin represents the signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available.

BGATE/BSOC (SOIC Pin 4, DFN Pin 5)

Connect this pin to the gate of the bottom-side MOSFET; it provides the PWM-controlled gate drive (from V_{BIAS}). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

During a short period of time following Power-On Reset (POR) or shut-down release, this pin is also used to determine the current limit threshold of the converter. Connect a resistor (R_{BSOC}) from this pin to GND. See “Overcurrent Protection (OCP)” on page 7 for equations. An overcurrent trip cycles the soft-start function, after two dummy soft-start time-outs. Some of the text describing the BGATE function may leave off the BSOC part of the name, when it is not relevant to the discussion.

VBIAS (SOIC Pin 5, DFN Pin 6)

This pin provides the bias supply for the ISL8105, as well as the bottom-side MOSFET's gate and the BOOT voltage for the top-side MOSFET's gate. An internal 5V regulator will supply bias if V_{BIAS} rises above 6.5V (but the BGATE/BSOC and BOOT will still be sourced by V_{BIAS}). Connect a well decoupled +5V or +12V supply to this pin.

FB (SOIC Pin 6, DFN Pin 8)

This pin is the inverting input of the internal error amplifier. Use FB, in combination with the COMP/EN pin, to compensate the voltage-control feedback loop of the converter. A resistor divider from the output to GND is used to set the regulation voltage.

COMP/EN (SOIC Pin 7, DFN Pin 9)

This is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. Use COMP/EN, in combination with the FB pin, to compensate the voltage-control feedback loop of the converter.

Pulling COMP/EN low ($V_{DISABLE}$ = 0.4V nominal) will disable (shut-down) the controller, which causes the oscillator to stop, the BGATE and TGATE outputs to be held low, and the soft-start circuitry to re-arm. The external pull-down device will initially need to overcome maximum of 5mA of COMP/EN output current. However, once the IC is disabled, the COMP output will also be disabled, so only a 20µA current source will continue to draw current.

When the pull-down device is released, the COMP/EN pin will start to rise at a rate determined by the 20µA charging up the capacitance on the COMP/EN pin. When the COMP/EN pin rises above the $V_{DISABLE}$ trip point, the ISL8105 will begin a new initialization and soft-start cycle.

LX (SOIC Pin 8, DFN Pin 10)

Connect this pin to the source of the top-side MOSFET and the drain of the bottom-side MOSFET. It is used as the sink for the TGATE driver and to monitor the voltage drop across the bottom-side MOSFET for overcurrent protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the top-side MOSFET has turned off.

N/C (DFN Only; Pin3, Pin 7)

These two pins in the DFN package are No Connect.

Functional Description

Initialization (POR and OCP Sampling)

Figure 1 shows a start-up waveform of ISL8105. The Power-ON-Reset (POR) function continually monitors the bias voltage at the VBIAS pin. Once the rising POR threshold is exceeded 4V (V_{POR} nominal), the POR function initiates the Overcurrent Protection (OCP) sample and hold operation (while COMP/EN is ~1V). When the sampling is complete, V_{OUT} begins the soft-start ramp.

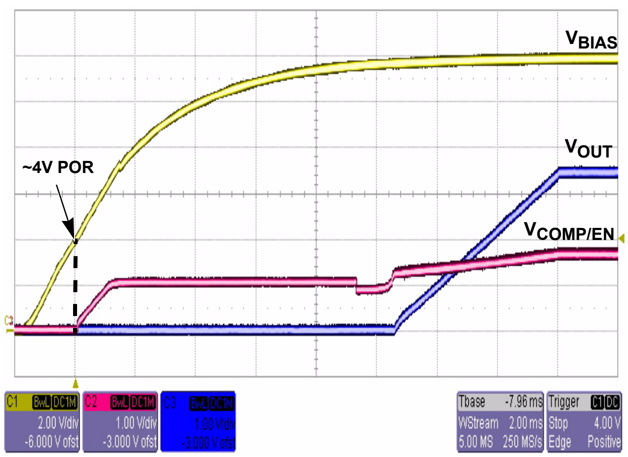


FIGURE 1. POR AND SOFT-START OPERATION

If the COMP/EN pin is held low during power-up, the initialization will be delayed until the COMP/EN is released and its voltage rises above the $V_{DISABLE}$ trip point.

Figure 2 shows a typical power-up sequence in more detail. The initialization starts at t_0, when either V_{BIAS} rises above V_{POR}, or the COMP/EN pin is released (after POR). The COMP/EN will be pulled up by an internal 20µA current source, but the timing will not begin until the COMP/EN exceeds the $V_{DISABLE}$ trip point (at t_1). The external capacitance of the disabling device, as well as the compensation capacitors, will determine how quickly the 20µA current source will charge the COMP/EN pin. With typical values, it should add a small delay compared to the soft-start times. The COMP/EN will continue to ramp to ~1V.

From t_1, there is a nominal 6.8ms delay, which allows the VBIAS pin to exceed 6.5V (if rising up towards 12V), so that the internal bias regulator can turn on cleanly. At the same time, the BGATE/BSOC pin is initialized by disabling the BGATE driver and drawing BSOC (nominal 21.5µA) through R_{BSOC}. This sets up a voltage that will represent the BSOC trip point. At t_2, there is a variable time period for the OCP sample and hold operation (0ms to 3.4ms nominal; the longer time occurs with the higher overcurrent setting). The sample and hold uses a digital counter and DAC to save the voltage, so the stored value does not degrade, for as long as the V_{BIAS} is above V_{POR}. See "Overcurrent Protection (OCP)" on page 7 for more details on the equations and variables. Upon the completion of sample and hold at t_3, the soft-start operation is initiated, and the output voltage ramps up between t_4 and t_5.

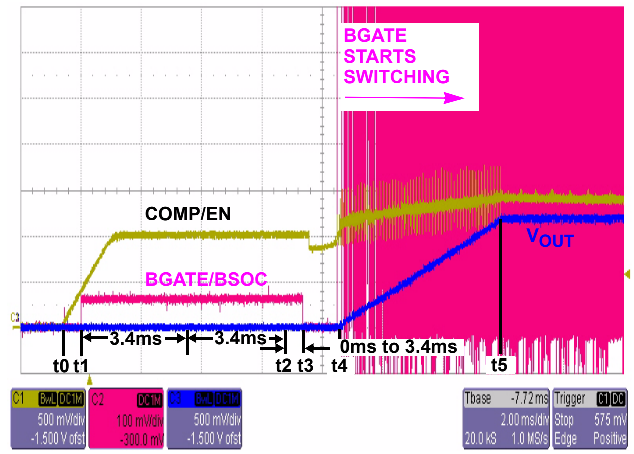


FIGURE 2. BGATE/BSOC AND SOFT-START OPERATION

Soft-Start and Pre-Biased Outputs

Functionally, the soft-start internally ramps the reference on the non-inverting terminal of the error amp from 0V to 0.6V in a nominal 6.8ms. The output voltage will thus follow the ramp, from zero to final value, in the same 6.8ms (the actual ramp seen on the V_{OUT} will be less than the nominal time), due to some initialization timing, between t_3 and t_4).

The ramp is created digitally, so there will be 64 small discrete steps. There is no simple way to change this ramp rate externally, and it is the same for either frequency version of the IC (300kHz or 600kHz).

After an initialization period (t_3 to t_4), the error amplifier (COMP/EN pin) is enabled, and begins to regulate the converter's output voltage during soft-start. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates LX pulses of increasing width that charge the output capacitors. When the internally generated soft-start voltage exceeds the reference voltage (0.6V), the soft-start is complete and the output should be in regulation at the expected voltage. This method provides a rapid and controlled output voltage rise; there is no large inrush current charging the output capacitors. The entire start-up sequence from POR typically takes up to 17ms; up

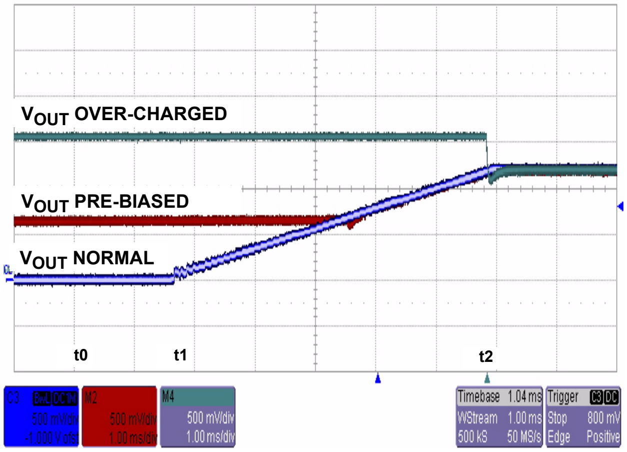


FIGURE 3. SOFT-START WITH PRE-BIAS

to 10.2ms for the delay and OCP sample and 6.8ms for the soft-start ramp.

Figure 3 shows the normal curve in blue; initialization begins at t_0, and the output ramps between t_1 and t_2. If the output is pre-biased to a voltage less than the expected value, as shown by the red curve, the ISL8105, ISL8105A will detect that condition. Neither MOSFET will turn on until the soft-start ramp voltage exceeds the output; V_{OUT} starts seamlessly ramping from there. If the output is pre-biased to a voltage above the expected value, as in the gray curve, neither MOSFET will turn on until the end of the soft-start, at which time it will pull the output voltage down to the final value. Any resistive load connected to the output will help pull down the voltage (at the RC rate of the R of the load and the C of the output capacitance).

If the V_{IN} for the synchronous buck converter is from a different supply that comes up after V_{BIAS}, the soft-start would go through its cycle, but with no output voltage ramp. When V_{IN} turns on, the output would follow the ramp of the V_{IN} from zero up to the final expected voltage (at close to 100% duty cycle, with COMP/EN pin >4V). If V_{IN} is too fast, there may be excessive inrush current charging the output capacitors (only the beginning of the ramp, from zero to V_{OUT} matters here). If this is not acceptable, then consider changing the sequencing of the power supplies, or sharing the same supply, or adding sequencing logic to the COMP/EN pin to delay the soft-start until the V_{IN} supply is ready (see “Input Voltage Considerations” on page 9).

If the IC is disabled after soft-start (by pulling COMP/EN pin low), and then enabled (by releasing the COMP/EN pin), then the full initialization (including OCP sample) will take place. However, there is no new OCP sampling during overcurrent retries. If the output is shorted to GND during soft-start, the OCP will handle it, as described in the next section.

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Overcurrent Protection (OCP)

The overcurrent function protects the converter from a shorted output by using the bottom-side MOSFET's on-resistance, $r_{DS(ON)}$, to monitor the current. A resistor (R_{BSOC}) programs the overcurrent trip level (see “Typical Application Diagram” on page 2). This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. If overcurrent is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (2 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely.

Following POR (and 6.8ms delay), the ISL8105, ISL8105A initiates the Overcurrent Protection sample and hold operation. The BGATE driver is disabled to allow an internal 21.5μA current source to develop a voltage across R_{BSOC}. The ISL8105, ISL8105A samples this voltage (which is referenced to the GND pin) at the BGATE/BSOC pin, and holds it in a counter and DAC combination. This sampled voltage is held internally as the Overcurrent Set Point, for as long as power is applied, or until a new sample is taken after coming out of a shut-down.

The actual monitoring of the bottom-side MOSFET's on-resistance starts 200ns (nominal) after the edge of the internal PWM logic signal (that creates the rising external BGATE signal). This is done to allow the gate transition noise and ringing on the LX pin to settle out before monitoring. The monitoring ends when the internal PWM edge (and thus BGATE) goes low. The OCP can be detected anywhere within the above window.

If the regulator is running at high TGATE duty cycles (around 75% for 600kHz or 87% for 300kHz operation), then the BGATE pulse width may not be wide enough for the OCP to properly sample the $r_{DS(ON)}$. For those cases, if the BGATE is too narrow (or not there at all) for 3 consecutive pulses, then the third pulse will be stretched and/or inserted to the 425ns minimum width. This allows for OCP monitoring every third pulse under this condition. This can introduce a small pulse-width error on the output voltage, which will be corrected on the next pulse; and the output ripple voltage will have an unusual 3-clock pattern, which may look like jitter. If the OCP is disabled (by choosing a too-high value of R_{BSOC}, or no resistor at all), then the pulse stretching feature is also disabled. Figure 4 illustrates the BGATE pulse width stretching, as the width gets smaller.

FIGURE 4. BGATE PULSE STRETCHING

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by Equation 1:

$$I_{PEAK} = \frac{2 \times I_{BSOC} \times R_{BSOC}}{r_{DS(ON)}} \quad \text{(EQ. 1)}$$

where I_{BSOC} is the internal BSOC current source (21.5µA typical). The scale factor of 2 doubles the trip point of the MOSFET voltage drop, compared to the setting on the R_{BSOC} resistor. The OC trip point varies in a system mainly due to the MOSFET's $r_{DS(ON)}$ variations (over process, current and temperature). To avoid overcurrent tripping in the normal operating load range, find the R_{BSOC} resistor from Equation 1 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{BSOC} from the specification table
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For an equation for the ripple current, see “Output Inductor Selection” on page 13.

The range of allowable voltages detected ($2 * I_{BSOC} * R_{BSOC}$) is 0mV to 475mV; but the practical range for typical MOSFETs is typically in the 20mV to 120mV ballpark (500Ω to 3000Ω). If the voltage drop across R_{BSOC} is set too low, that can cause almost continuous OCP tripping and retry. It would also be very sensitive to system noise and inrush current spikes, so it should be avoided. The maximum usable setting is around 0.2V across R_{BSOC} (0.4V across the MOSFET); values above that might disable the protection. Any voltage drop across R_{BSOC} that is greater than 0.3V (0.6V MOSFET trip point) will disable the OCP. The preferred method to disable OCP is simply to remove the resistor, which will be detected as no OCP.

Note that conditions during power-up or during a retry may look different than normal operation. During power-up in a 12V system, the IC starts operation just above 4V; if the supply ramp is slow, the soft-start ramp might be over well before 12V is reached. So with bottom-side gate drive voltages, the $r_{DS(ON)}$ of the MOSFETs will be higher during power-up, effectively lowering the OCP trip. In addition, the ripple current will likely be different at lower input voltage.

Another factor is the digital nature of the soft-start ramp. On each discrete voltage step, there is in effect a small load transient, and a current spike to charge the output capacitors. The height of the current spike is not controlled; it is affected by the step size of the output, the value of the output capacitors, as well as the IC error amp compensation. So it is possible to trip the overcurrent with inrush current, in addition to the normal load and ripple considerations.

Figure 5 shows the output response during a retry of an output shorted to GND. At time t_0, the output has been turned off, due to sensing an overcurrent condition. There are two internal soft-start delay cycles (t_1 and t_2) to allow the MOSFETs to cool down, to keep the average power dissipation in retry at an acceptable level. At time t_2, the output starts a normal soft-start cycle, and the output tries to ramp. If the short is still applied, and the current reaches the BSOC trip point any time during soft-start ramp period, the output will shut off and return to time t_0 for another delay cycle. Thus, the retry period is two dummy soft-start cycles plus one variable one (which depends on how long it takes to trip the sensor each time). Figure 5 also shows an example where the output gets about half-way up before shutting down; therefore, the retry (or hiccup) time will be around 17ms. The minimum should be nominally 13.6ms and the maximum 20.4ms. If the short condition is finally removed, the output should ramp up normally on the next t_2 cycle.

Starting up into a shorted load looks the same as a retry into that same shorted load. In both cases, OCP is always enabled during soft-start; once it trips, it will go into retry (hiccup) mode. The retry cycle will always have two dummy time-outs, plus whatever fraction of the real soft-start time passes before the detection and shutoff; at that point, the logic immediately starts a new two dummy cycle time-out.

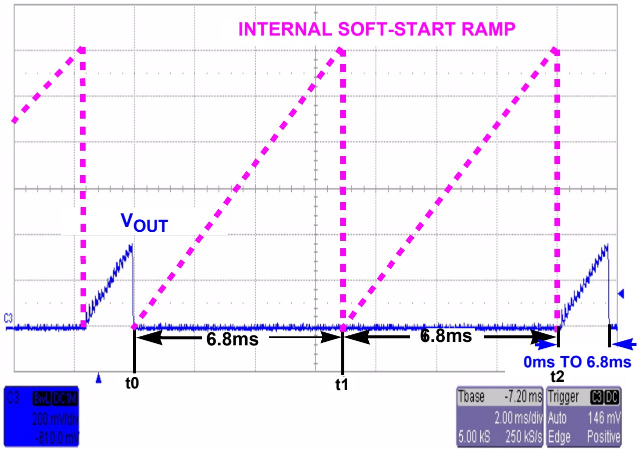


FIGURE 5. OVERCURRENT RETRY OPERATION

Output Voltage Selection

The output voltage can be programmed to any level between the 0.6V internal reference, up to the V_{BIAS} supply. The ISL8105, ISL8105A can run at near 100% duty cycle at zero load, but the $r_{DS(ON)}$ of the top-side MOSFET will effectively limit it to something less as the load current increases. In addition, the OCP (if enabled) will also limit the maximum effective duty cycle.

An external resistor divider is used to scale the output voltage relative to the internal reference voltage, and feed it back to the inverting input of the error amp. See “Typical Application Diagram” on page 2 for more detail; R_1 is the upper resistor; R_{OFFSET} (shortened to R_0 below) is the lower one. The recommended value for R_1 is 1kΩ to 5kΩ (±1% for accuracy) and then R_{OFFSET} is chosen according to Equations 2 and 3. Since R_1 is part of the compensation circuit (see “Feedback Compensation” on page 11), it is often easier to change R_{OFFSET} to change the output voltage; that way the compensation calculations do not need to be repeated. If V_{OUT} = 0.6V, then R_{OFFSET} can be left open. Output voltages less than 0.6V are not available.

$$V_{OUT} = 0.6V \bullet \frac{(R_1 + R_0)}{R_0} \qquad \text{(EQ. 2)}$$

$$R_0 = \frac{R_1 \bullet 0.6V}{V_{OUT} - 0.6V} \qquad \text{(EQ. 3)}$$

Input Voltage Considerations

The “Typical Application Diagram” on page 2 shows a standard configuration where V_{BIAS} is either 5V (±10%) or 12V (±20%); in each case, the gate drivers use the V_{BIAS} voltage for BGATE and BOOT/TGATE. In addition, V_{BIAS} is allowed to work anywhere from 6.5V up to the 14.4V maximum. **The V_{BIAS} range between 5.5V and 6.5V is <u>NOT</u> allowed for long-term reliability reasons,** but transitions through it to voltages above 6.5V are acceptable.

There is an internal 5V regulator for bias; it turns on between 5.5 and 6.5V. Some of the delay after POR is there to allow a typical power supply to ramp-up past 6.5V before the soft-start ramps begins. This prevents a disturbance on the output, due to the internal regulator turning on or off. If the transition is slow (not a step change), the disturbance should be minimal. So while the recommendation is to not have the output enabled during the transition through this region, it may be acceptable. The user should monitor the output for their application to see if there is any problem.

The V_{IN} to the top-side MOSFET can share the same supply as V_{BIAS} but can also run off a separate supply or other sources, such as outputs of other regulators. If V_{BIAS} powers up first, and the V_{IN} is not present by the time the initialization is done, then the soft-start will not be able to ramp the output, and the output will later follow part of the V_{IN} ramp when it is applied. If this is not desired, then change the sequencing of the supplies, or use the COMP/EN pin to disable V_{OUT} until both supplies are ready.

Figure 6 shows a simple sequencer for this situation. If V_{BIAS} powers up first, Q_1 will be off, and R_3 pulling to V_{BIAS} will turn Q_2 on, keeping the ISL8105, ISL8105A in shutdown. When V_{IN} turns on, the resistor divider R_1 and R_2 determines when Q_1 turns on, which will turn off Q_2 and release the shut-down. If V_{IN} powers up first, Q_1 will be on, turning Q_2 off; so the ISL8105, ISL8105A will start-up as soon as V_{BIAS} comes up. The $V_{DISABLE}$ trip point is 0.4V nominal, so a wide variety of NFET's or NPN's or even some logic IC's can be used as Q1 or Q_2; but Q_2 must be low leakage when off (open-drain or open-collector) so as not to interfere with the COMP output. Q_2 should also be placed near the COMP/EN pin.

The V_{IN} range can be as low as ~1V (for V_{OUT} as low as the 0.6V reference). It can be as high as 20V (for V_{OUT} just below V_{IN}). There are some restrictions for running high V_{IN} voltage.

The first consideration for high V_{IN} is the maximum BOOT voltage of 36V. The V_{IN} (as seen on LX) + V_{BIAS} (boot voltage - the diode drop) + any ringing (or other transients) on the BOOT pin must be less than 36V. If V_{IN} is 20V, that limits V_{BIAS} + ringing to 16V.

The second consideration for high V_{IN} is the maximum (BOOT - V_{BIAS}) voltage; this must be less than 24V. Since BOOT = V_{IN} + V_{BIAS} + ringing, that reduces to (V_{IN} + ringing)

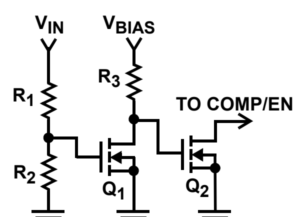


FIGURE 6. SEQUENCER CIRCUIT

must be <24V. So based on typical circuits, a 20V maximum V_{IN} is a good starting assumption; the user should verify the ringing in their particular application.

Another consideration for high V_{IN} is duty cycle. Very low duty cycles (such as 20V in to 1.0V out, for 5% duty cycle) require component selection compatible with that choice (such as low $r_{DS(ON)}$ bottom-side MOSFET, and a good LC output filter). At the other extreme (for example, 20V in to 12V out), the top-side MOSFET needs to be low $r_{DS(ON)}$. In addition, if the duty cycle gets too high, it can affect the overcurrent sample time. In all cases, the input and output capacitors and both MOSFETs must be rated for the voltages present.

Switching Frequency

The switching frequency is either a fixed 300kHz or 600kHz, depending on the part number chosen (ISL8105 is 300kHz; ISL8105A is 600kHz; the generic name "ISL8105" may apply to either in the rest of this document, except when choosing the frequency). However, all of the other timing mentioned (POR delay, OCP sample, soft-start, etc.) is independent of the clock frequency (unless otherwise noted).

BOOT Refresh

In the event that the TGATE is on for an extended period of time, the charge on the boot capacitor can start to sag, raising the $r_{DS(ON)}$ of the top-side MOSFET. The ISL8105 has a circuit that detects a long TGATE on-time (nominal 100µs), and forces the BGATE to go higher for one clock cycle, which will allow the boot capacitor some time to recharge. Separately, the OCP circuit has a BGATE pulse stretcher (to be sure the sample time is long enough), which can also help refresh the boot. But if OCP is disabled (no current sense resistor), the regular boot refresh circuit will still be active.

Current Sinking

The ISL8105 incorporates a MOSFET shoot-through protection method which allows a converter to sink current as well as source current. Care should be exercised when designing a converter with the ISL8105 when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the V_{IN} rail. If there is nowhere for this current to go, such as to other distributed loads on the V_{IN} rail, through a voltage limiting protection device, or other methods, the capacitance on the V_{IN} bus will absorb the current. This situation will allow voltage level of the V_{IN} rail (also LX) to increase. If the voltage level of the LX is increased to a level that exceeds the maximum voltage rating of the ISL8105, then the IC will experience an irreversible failure and the converter will no longer be operational. Ensuring that there is a path for the current to follow other than the capacitance on the rail will prevent this failure mode.

Application Guidelines

Layout Considerations

As in any high-frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

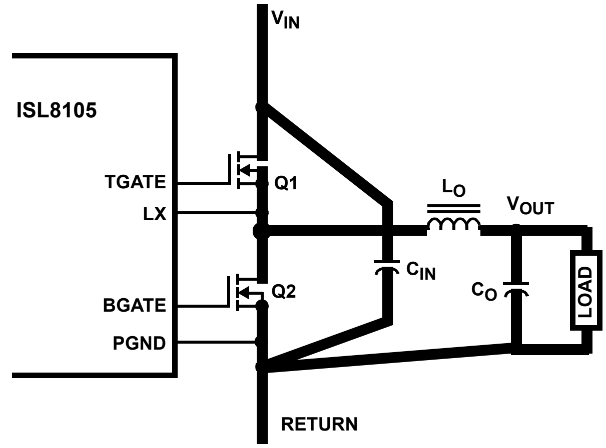


FIGURE 7. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 7 shows the critical power components of the converter. To minimize the voltage overshoot/undershoot, the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 8 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the ISL8105 within three inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the ISL8105 must be sized to handle up to 1A peak current.

Proper grounding of the IC is important for correct operation in noisy environments. The GND pin should be connected to a large copper fill under the IC which is subsequently connected to board ground at a quiet location on the board, typically found at an input or output bulk (electrolytic) capacitor.

Figure 8 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Locate the resistor, R_{BSOC}, close to the BGATE/BSOC pin as the internal BSOC current source is only 21.5µA.

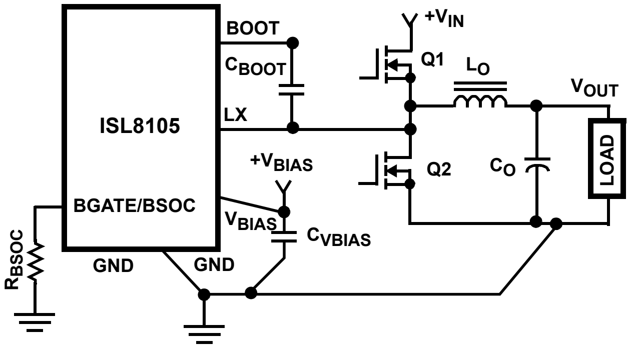


FIGURE 8. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Minimize the loop from any pulldown transistor connected to COMP/EN pin to reduce antenna effect. Provide local decoupling between VBIAS and GND pins as described earlier. Locate the capacitor, C_{BOOT}, as close as practical to the BOOT and LX pins. All components used for feedback compensation (not shown) should be located as close to the IC as practical.

Feedback Compensation

This section highlights the design considerations for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 9).

Figure 9 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable to the ISL8105 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, V_{REF}, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) triangle wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the LX node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, C and ESR represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR} \qquad \text{(EQ. 4)}$$

The compensation network consists of the error amplifier (internal to the ISL8105) and the external R_1 to R_3, C_1 to C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of f_{SW}) and adequate phase margin (better than +45°).

Phase margin is the difference between the closed loop phase at F_{0dB} and +180°.

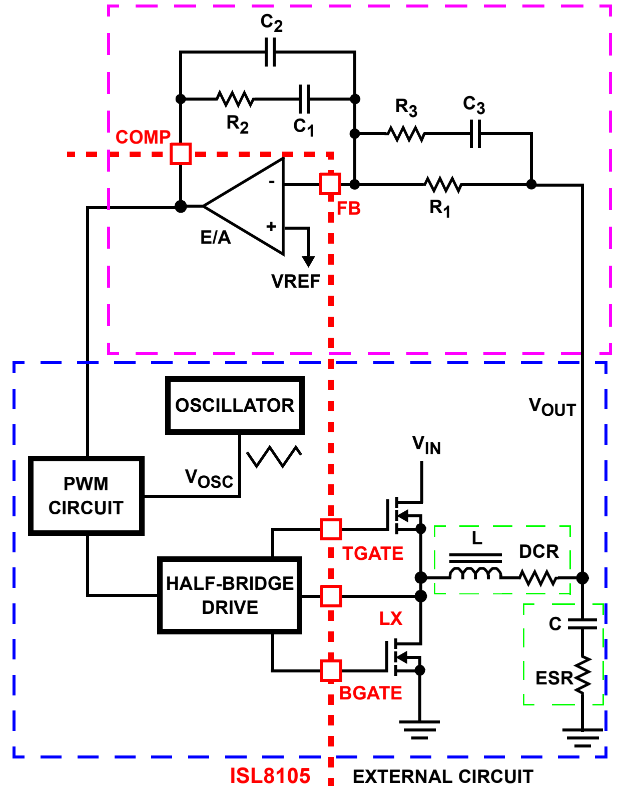


FIGURE 9. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Equations 5 through 8 that relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 9. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 10kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0). If setting the output voltage to be equal to the reference set voltage as shown in Figure 9, the design procedure can be followed as presented in Equation 5.

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 5)}$$

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \qquad \text{(EQ. 6)}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \qquad \text{(EQ. 7)}$$

4. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below f_{SW} (typically, 0.5 to 1.0 times f_{SW}). f_{SW} represents the regulator's switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in

frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{f_{SW}}{F_{LC}} - 1}$$
$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot f_{SW}} \qquad \text{(EQ. 8)}$$

It is recommended that a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The equations in Equation 9, describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j \qquad \text{(EQ. 9)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3} \qquad \text{(EQ. 10)}$$

Figure 10 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual modulator gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 10 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than +45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at

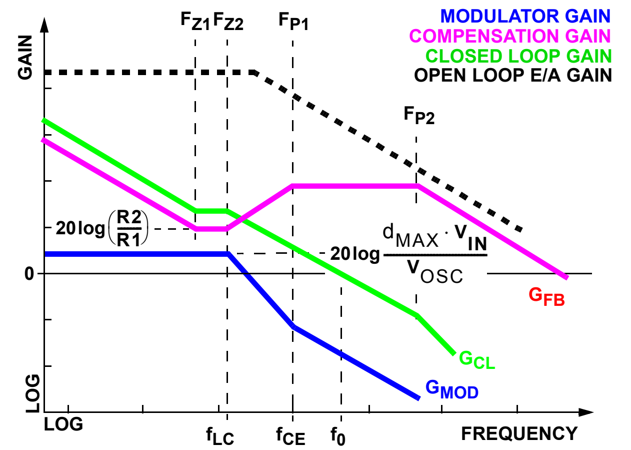


FIGURE 10. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, f_{SW}.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1.0mF ceramic capacitors in the 1206 surface-mount package. Follow on specifications have only increased the number and quality of required ceramic decoupling capacitors.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 11:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 11)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL8105 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 12 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 12)}$$

where:

I_{TRAN} is the transient load current step
t_{RISE} is the response time to the application of load
t_{FALL} is the response time to the removal of load

With a lower input source such as 1.8V or 3.3V, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

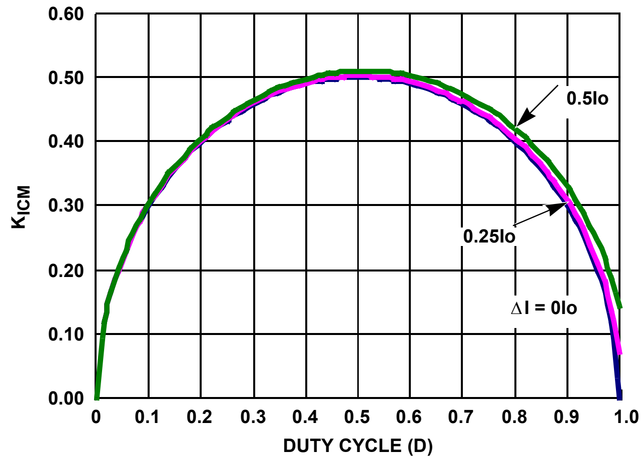


FIGURE 11. INPUT-CAPACITOR CURRENT MULTIPLIER FOR SINGLE-PHASE BUCK CONVERTER

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and a voltage rating of 1.5x is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately as shown in Equation 13..

$$I_{IN,RMS} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN}$$

OR (EQ. 13)

$$I_{IN,RMS} = K_{ICM} \bullet I_O$$

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series, available from AVX, and the 593D, available series from Sprague, are both surge current tested.

MOSFET Selection/Considerations

The ISL8105 requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the top and the bottom-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the top-side MOSFET realizes most of the switching losses. The bottom-side switch realizes most of the switching losses when the converter is sinking current (see Equation 14). These equations assume linear voltage current transitions and do not adequately model power loss due to the reverse recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL8105 and do not heat the MOSFETs. However, large gate charge increases the switching interval, t_{SW}, which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Losses while Sourcing Current

$$P_{TOP} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_S$$

$$P_{BOTTOM} = Io^2 \text{ x } r_{DS(ON)} \text{ x } (1 - D)$$

Losses while Sinking Current

$$P_{TOP} = Io^2 \text{ x } r_{DS(ON)} \text{ x } D$$

$$P_{BOTTOM} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_S \tag{EQ. 14}$$

Where:
D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the combined switch ON and OFF time, and
f_S is the switching frequency.

When operating with a 12V power supply for V_{BIAS} (or down to a minimum supply voltage of 6.5V), a wide variety of NMOSFETs can be used. Check the absolute maximum V_{GS} rating for both MOSFETs; it needs to be above the highest V_{BIAS} voltage allowed in the system; that usually means a 20V V_{GS} rating (which typically correlates with a 30V V_{DS} maximum rating). Low threshold transistors (around 1V or below) are not recommended for the reasons explained in the next paragraph.

For 5V-only operation, given the reduced available gate bias voltage (5V), logic-level transistors should be used for both N-MOSFETs. Look for $r_{DS(ON)}$ ratings at 4.5V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the ISL8105 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50ns or so.

Bootstrap Considerations

Figure 12 shows the top-side gate drive (BOOT pin) supplied by a bootstrap circuit from V_{BIAS}. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the LX pin. The supply is refreshed to a voltage of V_{BIAS} less the boot diode drop (V_D) each time the lower MOSFET, Q_2, turns on. Check that the voltage rating of the capacitor is above the maximum V_{BIAS} voltage in the system. A 16V rating should be sufficient for a 12V system. A value of 0.1µF is typical for many systems driving single MOSFETs.

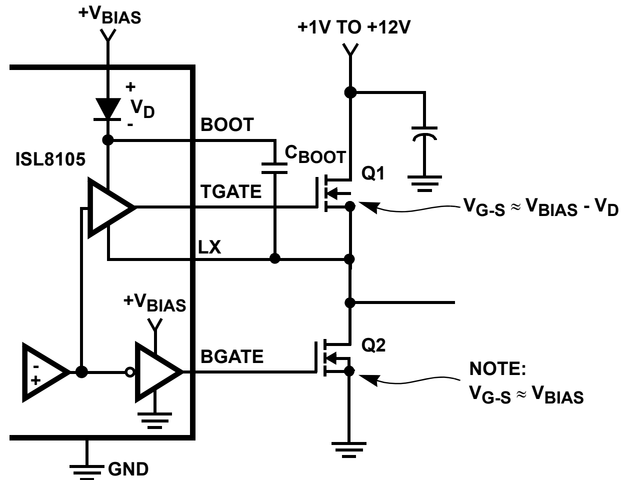


FIGURE 12. UPPER GATE DRIVE - BOOTSTRAP OPTION

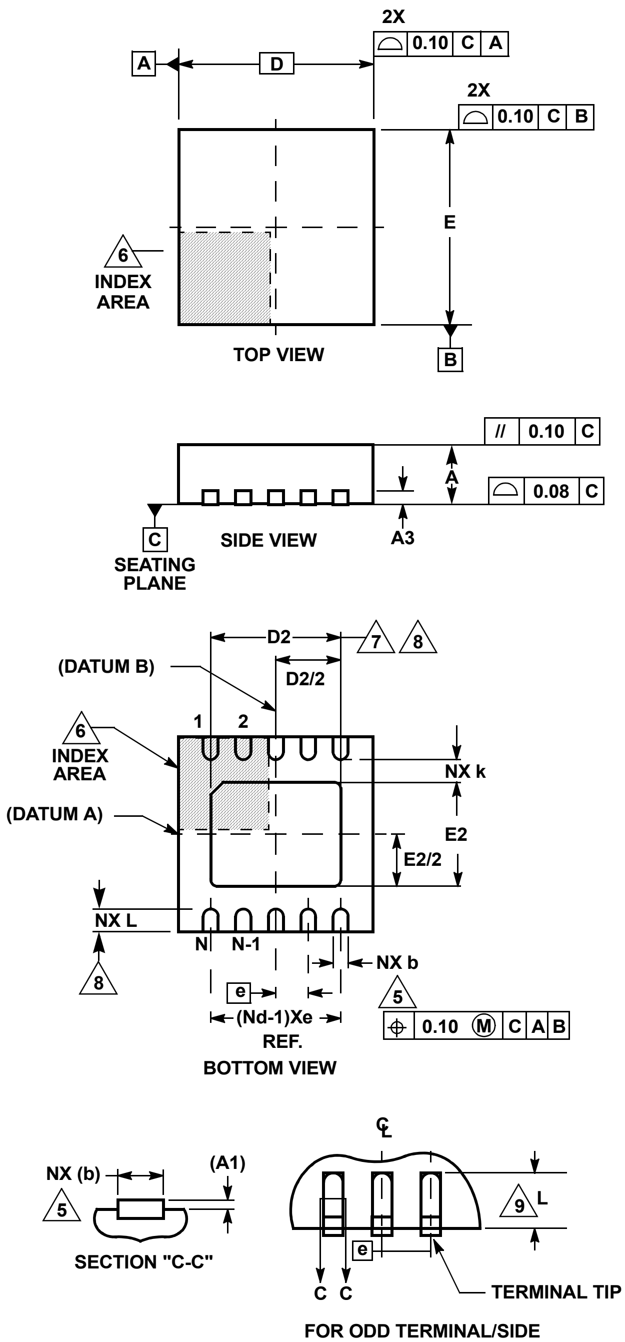
If V_{BIAS} is 12V, but V_{IN} is lower (such as 5V), then another option is to connect the BOOT pin to 12V and remove the BOOT capacitor (although, you may want to add a local capacitor from BOOT to GND). This will make the TGATE V_{GS} voltage equal to (12V - 5V = 7V). That should be high enough to drive most MOSFETs, and low enough to improve the efficiency slightly. Do **NOT** leave the BOOT pin open, and try to get the same effect by driving BOOT through V_{BIAS} and the internal diode; this path is not designed for the high current pulses that will result.

For low V_{BIAS} voltage applications where efficiency is very important, an external BOOT diode (in parallel with the internal one) may be considered. The external diode drop has to be lower than the internal one. The resulting higher V_{G-S} of the top-side FET will lower its $r_{DS(ON)}$. The modest gain in efficiency should be balanced against the extra cost and area of the external diode.

For information on the Application circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN1258.

http://www.intersil.com/data/an/AN1258.pdf

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

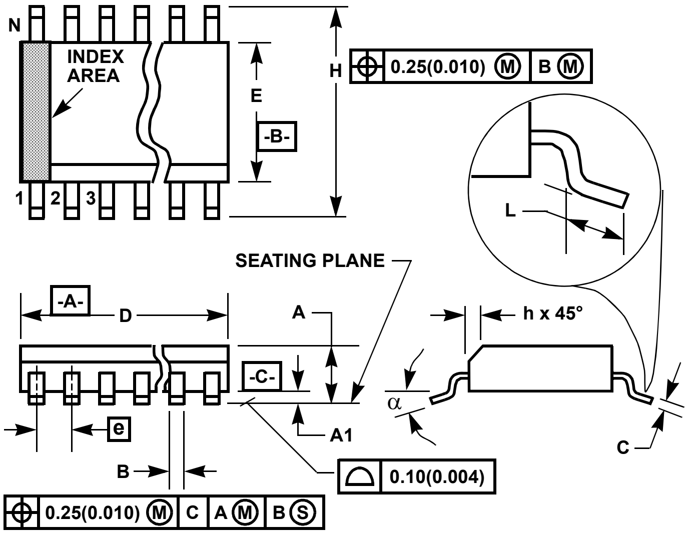
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	3.00 BSC			-
D2	2.33	2.38	2.43	7, 8
E	3.00 BSC			-
E2	1.59	1.64	1.69	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N	10			2
Nd	5			3

Rev. 1 4/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.