DATASHEET

ISL8200AM

Complete Current Share 10A DC/DC Power Module

FN8271
Rev.7.00
Apr 27, 2018

The ISL8200AM is a simple and easy to use high power, current-sharing DC/DC power module for datacom, telecom, and FPGA power hungry applications. All that is needed is the ISL8200AM, a few passive components, and one V_{OUT} setting resistor to have a complete 10A design ready for market.

The ease of use practically eliminates design and manufacturing risks while dramatically improving time to market.

Parallel up to six ISL8200AM modules to scale up to a 60A solution for more output current (see Figure 7 on page 10).

The simplicity of the ISL8200AM is in its "off-the-shelf", unassisted implementation compared to a discrete implementation. Patented current sharing in multiphase operation greatly reduces ripple currents, BOM cost, and complexity. For example, parallel two devices for 20A of current and up to six for 60A of current. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load, and temperature variations.

The ISL8200AM's thermally enhanced, compact QFN package operates at full load and over-temperature without requiring forced air cooling. The package is so thin it can even fit on the backside of the PCB. Easy access to all pins with few external components reduces the PCB design to a component layer and a simple ground layer.

Features

- Complete switch mode power supply in one package
- Patented current share architecture reduces layout sensitivity when modules are paralleled
- Programmable phase shift (1- to 6-phase)
- Extremely low profile (2.2mm height)
- Input voltage range +3V to +20V at 10A, current share up to 60A
- A single resistor sets V_{OUT} from +0.6V to +6V
- Output overvoltage, overcurrent, and over-temperature protection and undervoltage indication
- RoHS compliant

Applications

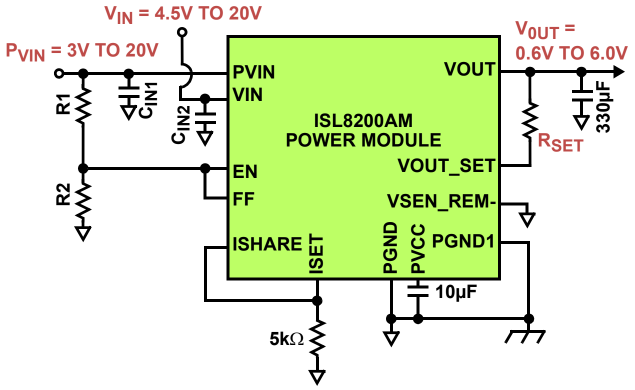
- Servers, telecom, and datacom applications
- Industrial and medical equipment
- Point of load regulation

Related Literature

For a full list of related documents, visit our website

- ISL8200AM product page

Complete Functional Schematic



NOTE: For input voltage higher than 4.5V, V_{IN} can be tied to P_{VIN} directly (see Figure 24 on page 13 for details).

FIGURE 1. COMPLETE 10A DESIGN, JUST SELECT R_{SET} FOR THE DESIRED V_{OUT}

ISL8200AM Package

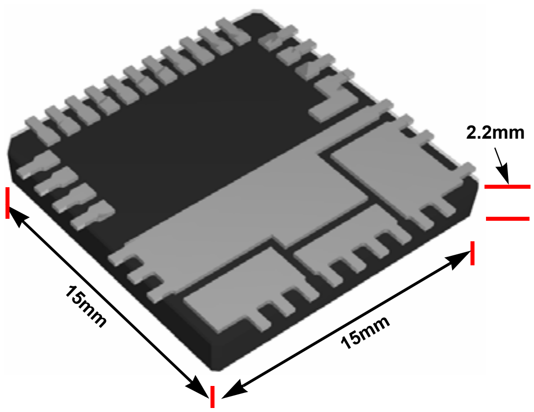


FIGURE 2. THE 2.2mm HEIGHT IS IDEAL FOR THE BACKSIDE OF PCB WHEN SPACE AND HEIGHT IS A PREMIUM

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8200AMIRZ	ISL8200AM	-40°C to +85°C	-	23 Ld QFN	L23.15x15
ISL8200AMIRZ-T	ISL8200AM	-40°C to +85°C	500	23 Ld QFN	L23.15x15
ISL8200AMMRZ	ISL8200AMM	-55°C to +125°C	-	23 Ld QFN	L23.15x15
ISL8200AMMRZ-T	ISL8200AMM	-55°C to +125°C	500	23 Ld QFN	L23.15x15
ISL8200AMEV1PHZ	Evaluation Board				

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3) termination finish which is compatible with both SnPb and Pb-free soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL8200AM product information page. For more information about MSL, see TB363.

Pinout Internal Circuit

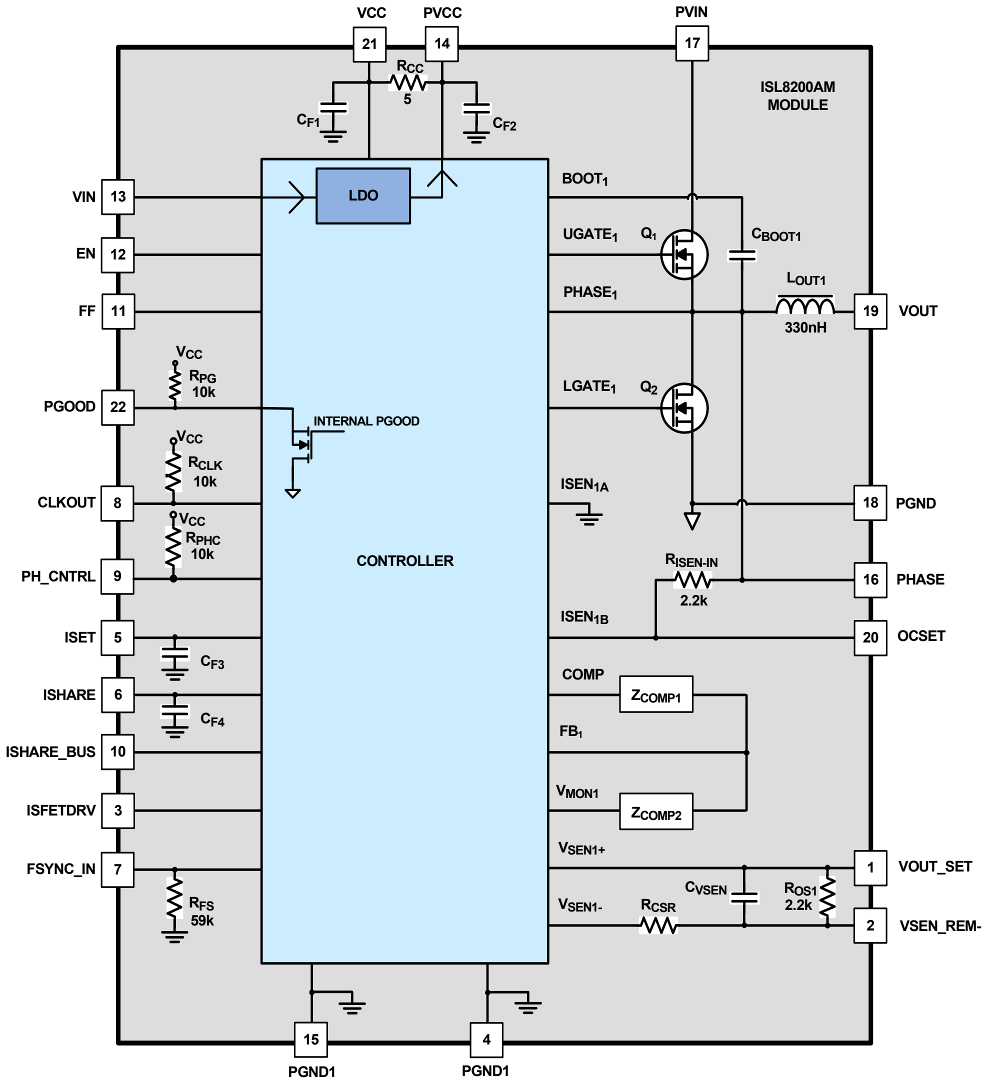
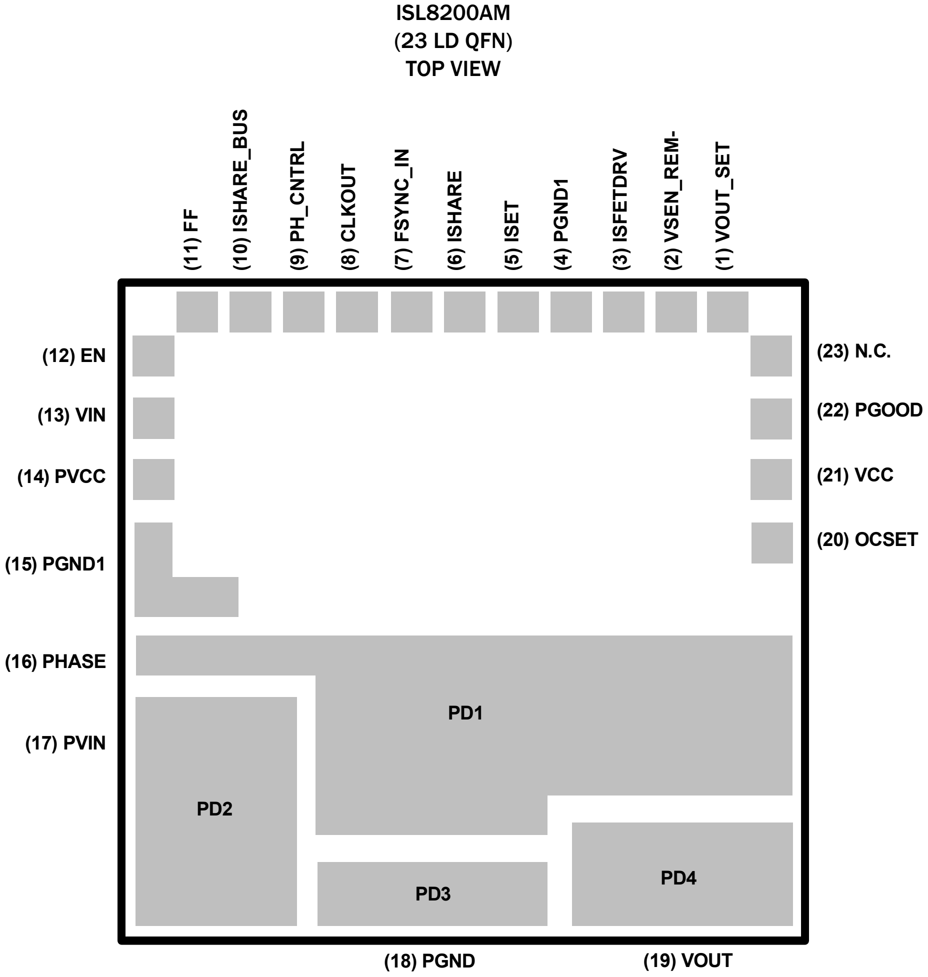


FIGURE 3. PINOUT INTERNAL CIRCUIT

Pin Configuration



Pin Descriptions

PIN #	PIN NAME	PIN DESCRIPTION
1	VOUT_SET	Analog voltage input. Used with V_{OUT} to program the regulator output voltage. The typical input impedance of VOUT_SET with respect to VSEN_REM- is 500kΩ. The typical voltage input is 0.6V.
2	VSEN_REM-	Analog voltage input. This pin is the negative input of standard unity gain operational amplifier for differential remote sense for the regulator, and should connect to the negative rail of the load/processor. Connect a resistor from this pin to the VOUT_SET pin for V_{OUT} trimming.
3	ISFETDRV	Digital output. This pin is used to drive an optional NFET, which will connect ISHARE with the system ISHARE bus upon completing a pre-bias start-up. The voltage output range is 0V to 5V.
4, 15	PGND1	Normal ground. All voltage levels are referenced to this pad. This pad provides a return path for the low-side MOSFET drivers and internal power circuitries as well as all analog signals. PGND and PGND1 should be connected together with a ground plane.
5	ISET	Analog current output. This pin sources a 15µA offset current plus Channel 1's average current. The voltage (VISET) set by an external resistor (RISET) represents the average current level of the local active module. For full-scale current, RISET should be ~10kΩ. The output current range is 15µA to 126µA typical. The ISET and ISHARE pins are used for current sharing purposes with multiple ISL8200AM modules. In the single module configuration, this pin can be tied to the ISHARE pin. In multiphase operation add an additional 10pF capacitor to the ISET line if noise is a concern.

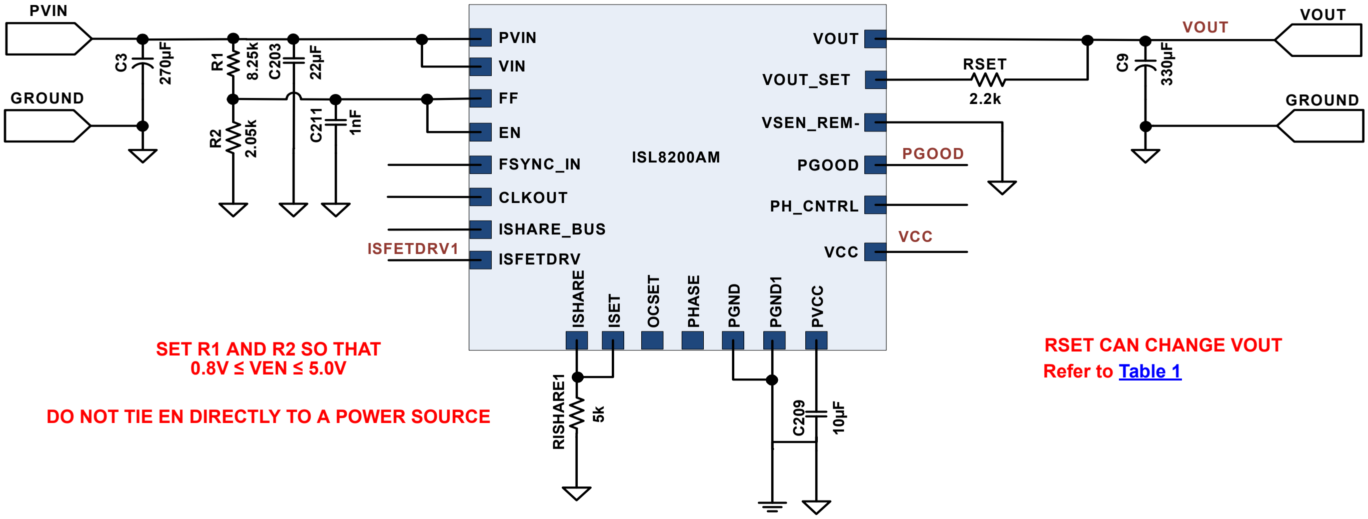
Pin Descriptions (Continued)

PIN #	PIN NAME	PIN DESCRIPTION
6	ISHARE	Analog current output. Cascaded system level overcurrent shutdown pin. Multi-module operation can be achieved by connecting the ISHARE pin of two or more modules together. The common current share bus sums each of the modules' average current contribution to the load to protect for an overcurrent condition at the load. The pin sources 15µA plus the average module's output current. The shared bus voltage (V_{ISHARE}) is developed across an external resistor (R_{ISHARE}). V_{ISHARE} represents the average current of all active channel(s) that are connected together. The ISHARE bus voltage is compared with each module's internal reference voltage set by each module's R_{ISET} resistor. This will generate an individual current share error signal in each cascaded controller. The share bus impedance R_{ISHARE} should be set as R_{ISET}/NCTRL, R_{ISET} divided by the number of active current sharing controllers. The output current from this pin generates a voltage across the external resistor. This voltage, V_{ISHARE}, is compared to an internal 1.2V threshold for average overcurrent protection. For full-scale current, R_{ISHARE} should be ~10kΩ. Typically 10kΩ is used for R_{SHARE} and R_{SET}. The output current range is 15µA to 126µA typical.
7	FSYNC_IN	Analog input control pin. An optional external resistor (RFS-ext) connected to this pin and ground will increase the oscillator switching frequency. The module has an internal 59kΩ resistor connected to the FSYNC_In pin for a default frequency of 700kHz. The internal oscillator will lock to an external frequency source when connected to a square waveform. The external source is typically the CLKOUT signal from another ISL8200AM or an external clock. The internal oscillator synchronizes with the leading positive edge of the input signal. The input voltage range for the external source is 0V to 5V square wave. When not synchronized to an external clock, a 100pF capacitor between FSYNC_IN and PGND1 is recommended.
8	CLKOUT	Digital voltage output. This pin provides a clock signal to synchronize with other ISL8200AM(s). When more than one ISL8200AM is in the system, the two independent regulators can be programmed through PH_CNTRL for different degrees of phase delay.
9	PH_CNTRL	Analog input. The voltage level on this pin is used to program the phase shift of the CLKOUT clock signal to synchronize with other module(s).
10	ISHARE_BUS	Open pin until the first PWM pulse is generated. Then, through an internal FET, this pin connects the module's ISHARE to the system's ISHARE bus after pre-bias is complete and soft-start is initiated.
11	FF	Analog voltage input. The voltage on this pin is fed into the controller, adjusting the sawtooth amplitude to generate the feed-forward function. The input voltage range is 0.8V to V_{CC}. Typically, FF is connected to EN.
12	EN	This is a double function pin: Analog input voltage - The input voltage to this pin is compared with a precision 0.8V reference and enables the digital soft-start. The input voltage range is 0V to V_{CC} or V_{IN} through a pull-up resistor maintaining a typical current of 5mA. Analog voltage output - This pin can be used as a voltage monitor for input bus undervoltage lockout. The hysteresis levels of the lockout can be programmed through this pin using a resistor divider network. Furthermore, during fault conditions (such as overvoltage, overcurrent, and over-temperature), this pin is used to communicate the information to other cascaded modules by pulling the wired OR low as it is an open drain. The output voltage range is 0V to V_{CC}.
13	VIN	Analog voltage input. This pin should be tied directly to the input rail when using the internal linear regulator. It provides power to the internal linear drive circuitry. When used with an external 5V supply, this pin should be tied directly to PVCC. The internal linear device is protected against the reversed bias generated by the remaining charge of the decoupling capacitor at VCC when losing the input rail. The input voltage range is 4.5V to 20V.
14	PVCC	Analog output. This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drives. Its operational voltage range is 4.5V to 5.6V. The decoupling ceramic capacitor in the PVCC pin is 10µF.
16	PHASE	Analog output. This pin is the phase node of the regulator. The output voltage range is 0V to 30V.
17	PVIN	Analog input. This input voltage is applied to the power FETs with the FETs ground being the PGND pin. It is recommended to place 22µF of input decoupling capacitance directly between the PVIN pin and the PGND pin as close as possible to the module. The input voltage range is 3V to 20V.
18	PGND	All voltage levels are referenced to this pad. This is the low-side MOSFET ground. PGND and PGND1 should be connected together with a ground plane.
19	VOUT	Output voltage from the module. The output voltage range is 0.6V to 6V.
20	OCSET	Analog input. This pin is used with the PHASE pin to set the current limit of the module. The input voltage range is 0V to 30V.
21	VCC	Analog input. This pin provides bias power for the analog circuitry. Its operational range is 4.5V to 5.6V. In 3.3V applications, VCC, PVCC, and VIN should be shorted to allow operation at the low end input as it relates to the V_{CC} falling threshold limit. This pin can be powered either by the internal linear regulator or by an external voltage source.
22	PGOOD	Analog output. This pin, pulled up to VCC using an internal 10kΩ resistor, provides a power-good signal when the output is within 9% of a nominal output regulation point with 4% hysteresis (13%/9%) and when soft-start is complete. An external pull-up is not required. PGOOD monitors the outputs (VMON1) of the internal differential amplifiers. The output voltage range is a 0V to V_{CC}.

Pin Descriptions (Continued)

PIN #	PIN NAME	PIN DESCRIPTION
23	N.C.	Not internally connected
PD1	Phase Thermal Pad	Used for both the PHASE pin (Pin 16) and for heat removal connecting to heat dissipation layers using vias. Connect this pad to a copper island on the PCB board with the same shape as the pad; this is electrically connected to PHASE Pin 16.
PD2	PV_{IN} Thermal Pad	Used for both the PVIN pin (Pin 17) and for heat removal connecting to heat dissipation layers using vias. Connect this pad to a copper island on the PCB board with the same shape as the pad; this is electrically connected to PVIN Pin 17.
PD3	PGND Thermal Pad	Used for both the PGND pin (Pin 18) and for heat removal connecting to heat dissipation layers using vias. Connect this pad to a copper island on the PCB board with the same shape as the pad; this is electrically connected to PGND Pin 18.
PD4	V_{OUT} Thermal Pad	Used for both the VOUT pin (Pin 19) and for heat removal connecting to heat dissipation layers using vias. Connect this pad to a copper island on the PCB board with the same shape as the pad; this is electrically connected to VOUT Pin 19.

Typical Application Circuits



SET R1 AND R2 SO THAT
0.8V ≤ VEN ≤ 5.0V

DO NOT TIE EN DIRECTLY TO A POWER SOURCE

RSET CAN CHANGE VOUT
Refer to Table 1

FIGURE 4. SINGLE PHASE 10A 1.2V OUTPUT CIRCUIT

Typical Application Circuits (continued)

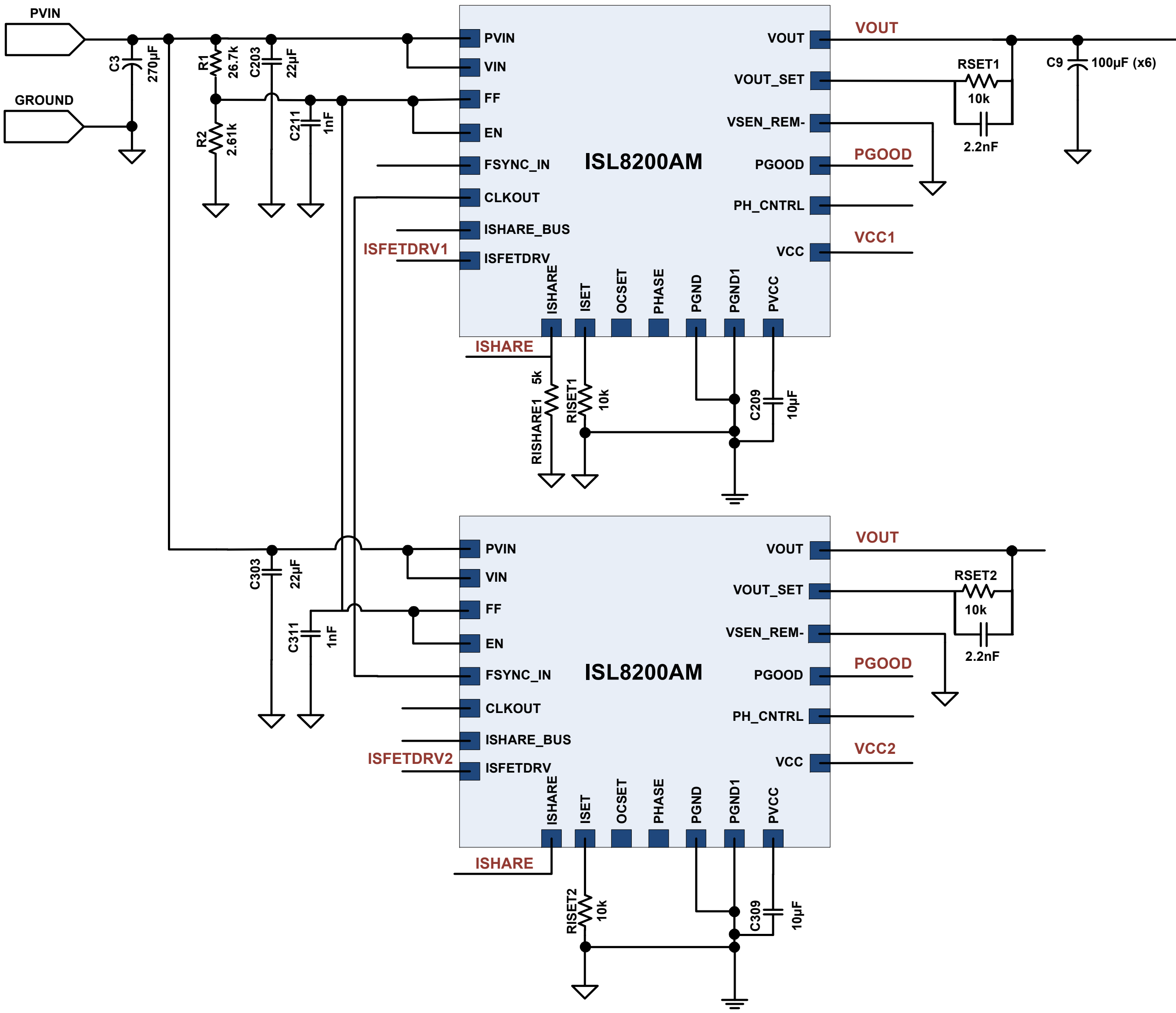


FIGURE 5. TWO PHASE 20A 3.3V OUTPUT CIRCUIT

Absolute Maximum Ratings

Input Voltage, PVIN, V_{IN}	-0.3V to +27V
Driver Bias Voltage, PVCC	-0.3V to +6.0V
Signal Bias Voltage, V_{CC}	-0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT}	-0.3V to +36V
Phase Voltage, V_{PHASE}	V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage,	
V_{BOOT} - V_{PHASE}	-0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage	-0.3V to V_{CC} + 0.3V
ESD Rating	
Human Body Model (Tested per JESD22-A114E)	2kV
Machine Model (Tested per JESD22-A115-A)	200V
Charge Device Model (Tested per JESD22-C101C)	1kV
Latch-up (Tested per JESD-78B; Class 2, Level A)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	13	2
Maximum Storage Temperature Range	-55°C to +150°C	
Typical Reflow Profile	See Figure 42 on page 21	

Recommended Operating Conditions

Input Voltage	
P_{VIN}	3V to 20V
V_{IN}	4.5V to 20V
Driver Bias Voltage, PVCC	4.5V to 5.6V
Signal Bias Voltage, V_{CC}	4.5V to 5.6V
Boot to Phase Voltage	
V_{BOOT} - V_{PHASE}	<6V
ISL8200AMIRZ Ambient Temperature Range	-40°C to +85°C
ISL8200AMIRZ Junction Temperature Range	-40°C to +125°C
ISL8200AMMRZ Ambient Temperature Range	-55°C to +125°C
ISL8200AMMRZ Junction Temperature Range	-55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board (for example, 4-layer type without thermal vias. See TB379) per JEDEC standards except that the top and bottom layers assume solid plains.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Boldface limits apply across the operating temperature range, -40°C to +85°C for ISL8200AMIRZ and -55°C to +125°C for ISL8200AMMRZ.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 6)	MAX (Note 7)	UNIT
V_{CC} SUPPLY CURRENT						
Nominal Supply V_{IN} Current	I_{Q_VIN}	PVIN = V_{IN} = 20V; No Load; f_{SW} = 700kHz		36		mA
Nominal Supply V_{IN} Current	I_{Q_VIN}	PVIN = V_{IN} = 4.5V; No Load; f_{SW} = 700kHz		27		mA
Shutdown Supply V_{CC} Current	I_{VCC}	EN = 0V, V_{CC} = 2.97V		9		mA
INTERNAL LINEAR REGULATOR						
Maximum Current	I_{PVCC}	PVCC = 4V to 5.6V		320		mA
Saturated Equivalent Impedance	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)		1		Ω
PVCC Voltage Level (Note 8)	PVCC	I_{PVCC} = 0mA, V_{IN} = 12V, ISL8200AMIRZ	**5.15**	5.4	**5.60**	V
POWER-ON RESET (Note 8)						
Rising VCC Threshold		ISL8200AMIRZ		2.85	**2.97**	V
		ISL8200AMMRZ		2.85	**2.98**	
Falling V_{CC} Threshold				2.65	**2.75**	V
Rising PV_{CC} Threshold				2.85	**2.97**	V
Falling PV_{CC} Threshold				2.65	**2.75**	V
System Soft-start Delay	t_{SS_DLY}	After PLL, V_{CC}, and PVCC PORs, and EN above their thresholds		384		Cycles
ENABLE (Note 8)						
Turn-On Threshold Voltage			**0.75**	0.8	**0.86**	V
Hysteresis Sink Current	I_{EN_HYS}	ISL8200AMIRZ	**21**	30	**35**	µA
		ISL8200AMMRZ	**19**	30	**35**	µA
Undervoltage Lockout Hysteresis	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.6		V

Electrical Specifications

Boldface limits apply across the operating temperature range, -40°C to +85°C for ISL8200AMIRZ and -55°C to +125°C for ISL8200AMMRZ. (Continued)

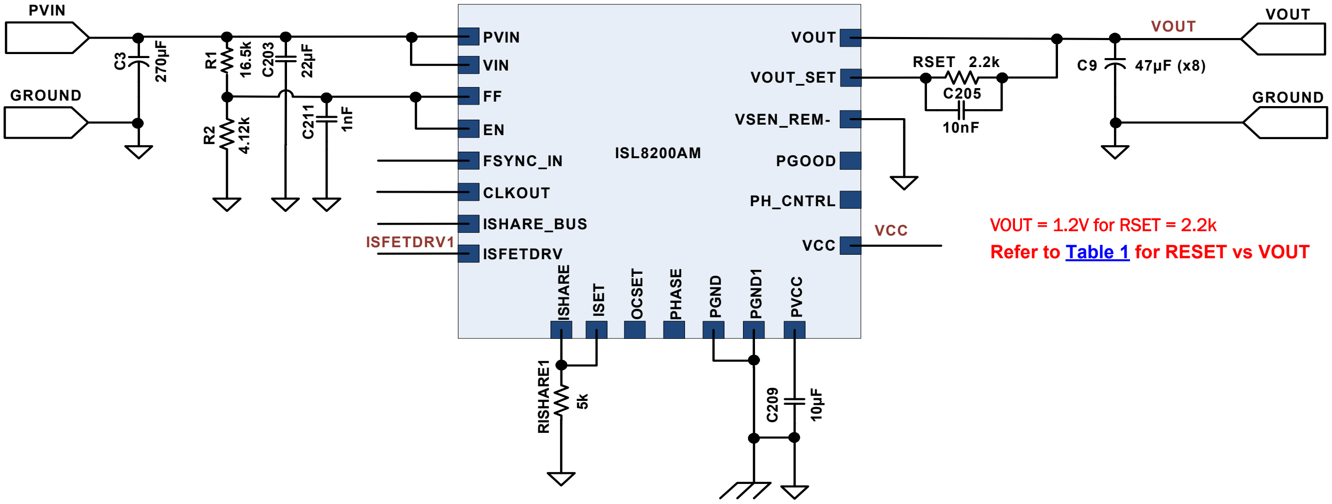
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 6)	MAX (Note 7)	UNIT
Sink Current	I_{EN_SINK}	VEN = 1V, ISL8200AMIRZ	**15.4**			mA
		VEN = 1V, ISL8200AMMRZ	**10**			mA
Sink Impedance	R_{EN_SINK}	VEN = 1V			**64**	Ω
OSCILLATOR						
Oscillator Frequency	FOSC	R_{FS} = 59kΩ; Figure 35		700		kHz
Total Variation (Note 8)		V_{CC} = 5V; ISL8200AMIRZ	**-9**		**+9**	%
		V_{CC} = 5V; ISL8200AMMRZ	**-12**		**-12**	%
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP (Note 7)						
Synchronization Frequency		V_{CC} = 5.4V	FOSC		**1500**	kHz
PLL Locking Time		V_{CC} = 5.4V; f_{SW} = 700kHz, ISL8200AMIRZ		210		µs
Input Signal Duty Cycle Range			**10**		**90**	%
PWM (Note 8)						
Minimum PWM OFF Time	t_{MIN_OFF}	ISL8200AMIRZ	**310**	345	**410**	ns
		ISL8200AMMRZ	**310**	345	**425**	ns
Current Sampling Blanking Time	$t_{BLANKING}$			175		ns
OUTPUT CHARACTERISTICS						
Output Continuous Current Range	$I_{OUT(DC)}$	PVIN = V_{IN} = 12V, V_{OUT} = 1.2V	0		10	A
Line Regulation Accuracy	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} = 1.2V, I_{OUT} = 0A, PVIN = V_{IN} = 3.5V to 20V		0.15		%
		V_{OUT} = 1.2V, I_{OUT} = 10A, PVIN = V_{IN} = 5V to 20V		0.15		%
Load Regulation Accuracy	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 0A to 10A, V_{OUT} = 1.2V, PVIN = V_{IN} = 12V		0.1		%
Output Ripple Voltage	ΔV_{OUT}	I_{OUT} = 10A, V_{OUT} = 1.2V, PVIN = V_{IN} = 12V		27		mV_{P-P}
		I_{OUT} = 0A, V_{OUT} = 1.2V, PVIN = V_{IN} = 12V		19		mV_{P-P}
DYNAMIC CHARACTERISTICS						
Voltage Change for Positive Load Step	ΔV_{OUT-DP}	I_{OUT} = 0A to 5A. Current slew rate = 2.5A/µs, PVIN = V_{IN} = 12V, V_{OUT} = 1.2V		45		mV_{P-P}
Voltage Change for Negative Load Step	ΔV_{OUT-DN}	I_{OUT} = 5A to 0A. Current slew rate = 2.5A/µs, PVIN = V_{IN} = 12V, V_{OUT} = 1.2V		55		mV_{P-P}
REFERENCE (Note 8)						
Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF}			0.6		V
		ISL8200AMIRZ	**-0.75**		**0.75**	%
		ISL8200AMMRZ	**-0.95**		**0.95**	%
DIFFERENTIAL AMPLIFIER (Note 8)						
DC Gain	UG_DA	Unity Gain Amplifier		0		dB
Unity Gain Bandwidth	UGBW_DA			5		MHz
V_{SEN+} Pins Input Current	I_{VSEN+}	ISL8200AMIRZ	**0.2**	1.16	**2.5**	µA
Maximum Source Current for Current Sharing	I_{VSEN1-}	VSEN1- source current for current sharing when parallel multiple modules each of which has its own voltage loop		350		µA
Input Impedance	$R_{VSEN+\_to\_VSEN-}$	V_{VSEN+}/I_{VSEN+}, V_{VSEN+} = 0.6V, ISL8200AMIRZ		-500		kΩ
Output Voltage Swing			0		**V_{CC} - 1.8**	V
Input Common Mode Range		ISL8200AMIRZ	**-0.2**		**V_{CC} - 1.8**	V
Disable Threshold	V_{VSEN-}	V_{MON1} = Tri-state		V_{CC} - 0.4		V

Electrical Specifications **Boldface limits apply across the operating temperature range, -40°C to +85°C for ISL8200AMIRZ and -55°C to +125°C for ISL8200AMMRZ. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 6)	MAX (Note 7)	UNIT
OVERCURRENT PROTECTION (Note 8)						
Channel Overcurrent Limit	I_{SOURCE}	V_{CC} = 5V; ISL8200AMIRZ	**89**	111	**129**	µA
		V_{CC} = 5V; ISL8200AMMRZ	**84**	111	**129**	µA
Share Pin OC Threshold	V_{OC_ISHARE}	Comparator offset included	**1.16**	1.20	**1.22**	V
CURRENT SHARE						
External Current Share Accuracy		Up to three phases; ISL8200AMIRZ		±10		%
POWER GOOD MONITOR (Note 8)						
Undervoltage Falling Trip Point	V_{UVF}	Percentage below reference point	**-15**	-13	**-11**	%
Undervoltage Rising Hysteresis	V_{UVR_HYS}	Percentage above UV trip point		4		%
Overvoltage Rising Trip Point	V_{OVR}	Percentage above reference point	**11**	13	**15**	%
Overvoltage Falling Hysteresis	V_{OVF_HYS}	Percentage below OV trip point		4		%
PGOOD Low Output Voltage		I_{PGOOD} = 2mA			**0.35**	V
Sinking Impedance		I_{PGOOD} = 2mA			**70**	Ω
Maximum Sinking Current		V_{PGOOD} < 0.8V		10		mA
OVERVOLTAGE PROTECTION (Note 8)						
OV Latching Trip Point		EN = UGATE = LATCH Low, LGATE = High	**118**	120	**122**	%
OV Non-latching Trip Point		EN = Low, UGATE = Low, LGATE = High		113		%
LGATE Release Trip Point		EN = Low/HIGH, UGATE = Low, LGATE = Low		87		%
OVER-TEMPERATURE PROTECTION CONTROLLER JUNCTION TEMPERATURE						
Over-temperature Trip				150		°C
Over-temperature Release Threshold				125		°C
INTERNAL COMPONENT VALUES						
Internal Resistor Between PVCC and VCC pin	R_{CC}			5		Ω
Internal Resistor Between PHASE and OCSET Pins	$R_{ISEN\text{-}IN}$			2.2k		Ω
Internal Resistor Between FSYNC_IN and PGND1 Pins	R_{FS}			59k		Ω
Internal Resistor Between PGOOD and VCC Pins	R_{PG}			10k		Ω
Internal Resistor Between CLKOUT and VCC Pins	R_{CLK}			10k		Ω
Internal Resistor Between PH_CNTRL and VCC Pins	R_{PHC}			10k		Ω
Internal Resistor Between VOUT_SET and VSEN_REM- pin	R_{OS1}			2.2k		Ω

NOTES:

6. Parameters with TYP limits are not production tested, unless otherwise specified.
7. Parameters with MIN and/or MAX limits are 100% tested for internal IC prior to module assembly, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.



VOUT = 1.2V for RSET = 2.2k

Refer to Table 1 for RESET vs VOUT

FIGURE 6. TEST CIRCUIT FOR ALL PERFORMANCE AND DERATING GRAPHS

Typical Performance Characteristics

Efficiency Performance

T_A = +25°C, P_{VIN} = V_{IN}, C_{IN} = 220µFx1, 10µF/ceramic x 2, C_{OUT} = 47µF/ceramic x 8.

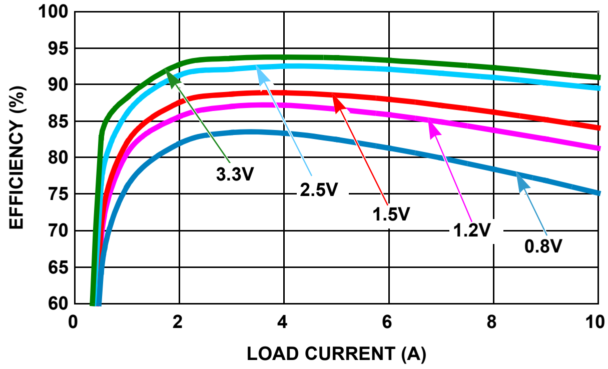


FIGURE 7. EFFICIENCY vs LOAD CURRENT ($5V_{IN}$)

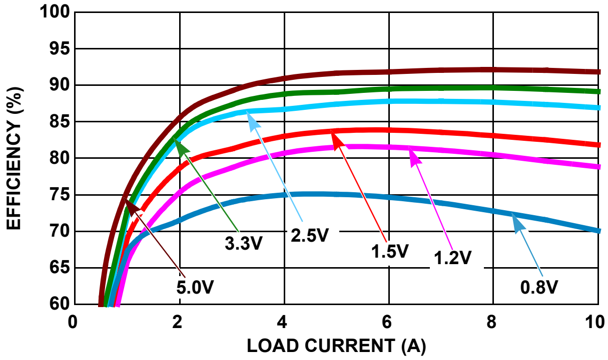


FIGURE 8. EFFICIENCY vs LOAD CURRENT ($12V_{IN}$)

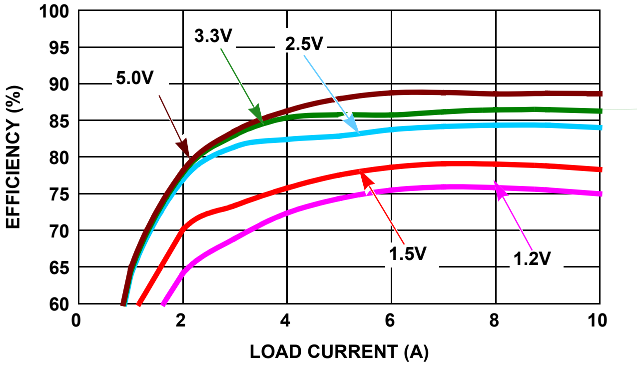


FIGURE 9. EFFICIENCY vs LOAD CURRENT ($20V_{IN}$)

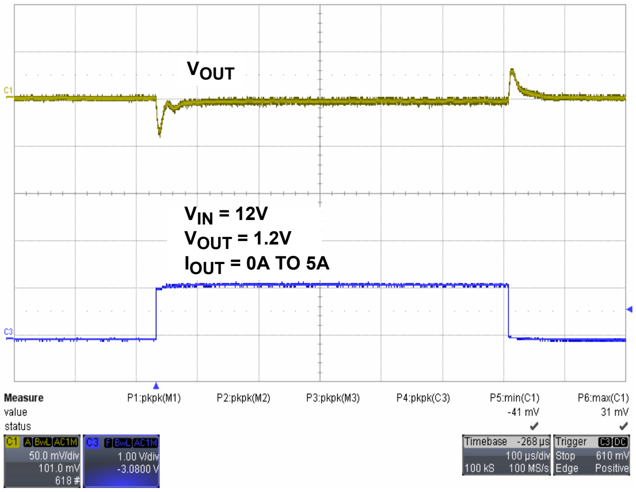


FIGURE 10. 1.2V TRANSIENT RESPONSE

Transient Response Performance

T_A = +25°C, P_{VIN} = V_{IN} = 12V, C_{IN} = 220µFx1, 10µF/ceramic x 2, C_{OUT} = 47µF/ceramic x 8, I_{OUT} = 0A to 5A, current slew rate = 2.5A/µs.

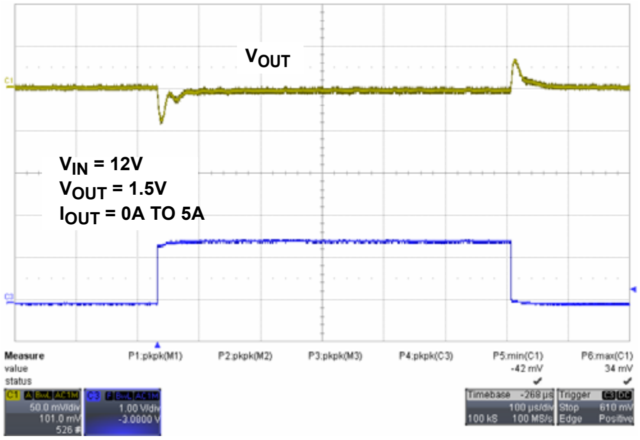


FIGURE 11. 1.5V TRANSIENT RESPONSE

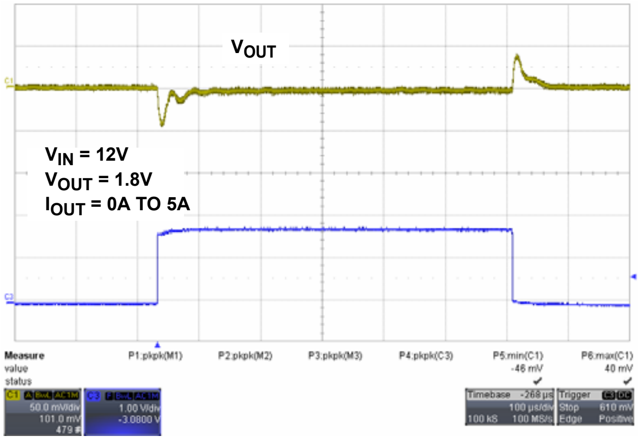


FIGURE 12. 1.8V TRANSIENT RESPONSE

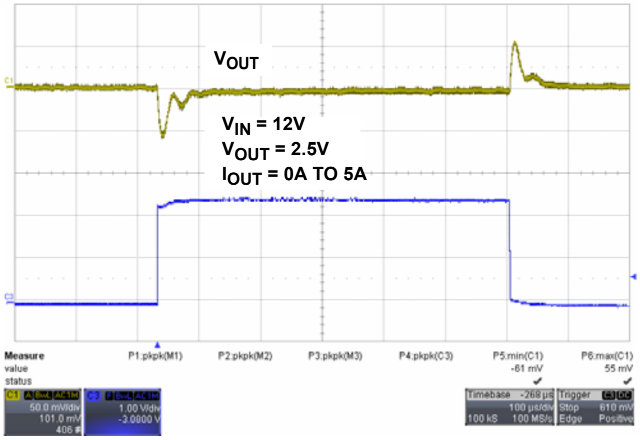


FIGURE 13. 2.5V TRANSIENT RESPONSE

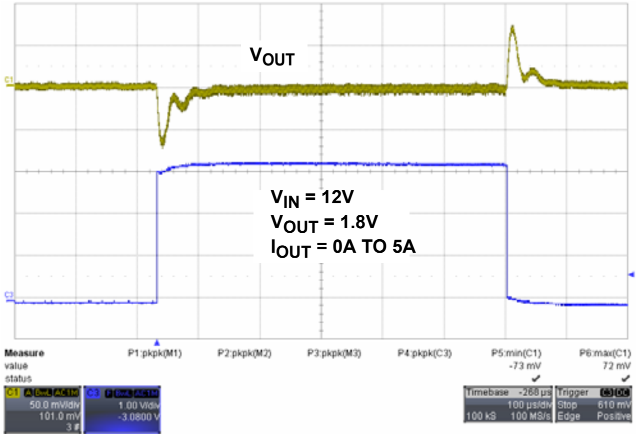


FIGURE 14. 3.3V TRANSIENT RESPONSE

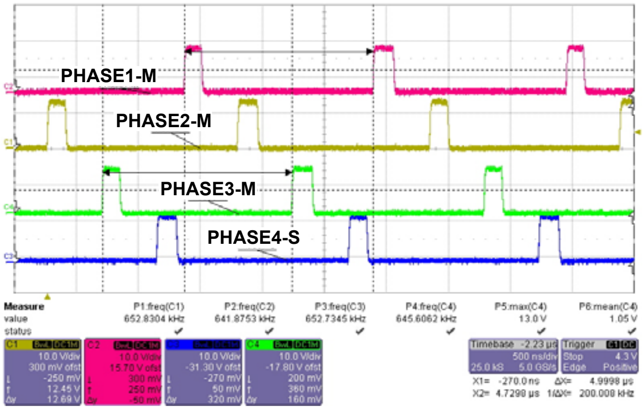


FIGURE 15. FOUR MODULE CLOCK SYNC (V_{IN} = 12V)

Current Ripple Performance

T_A = +25°C, P_{VIN} = V_{IN} = 12V, C_{IN} = 220µFx1, 10µF/ceramic x 2, C_{OUT} = 100µF/ceramic x 6 I_{OUT} = No Load, 5, 10A.

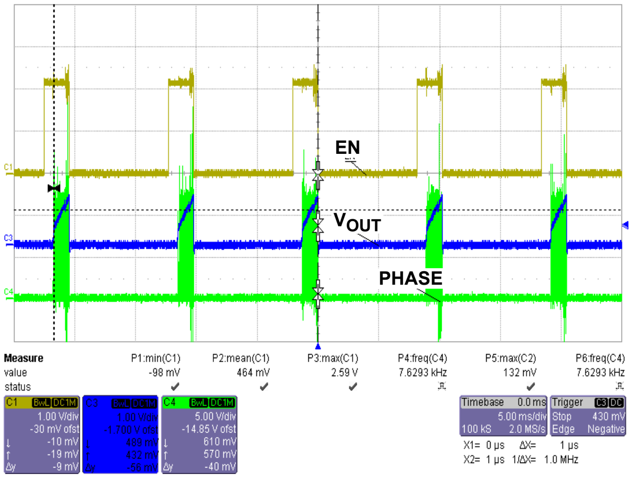


FIGURE 16. OVERCURRENT PROTECTION

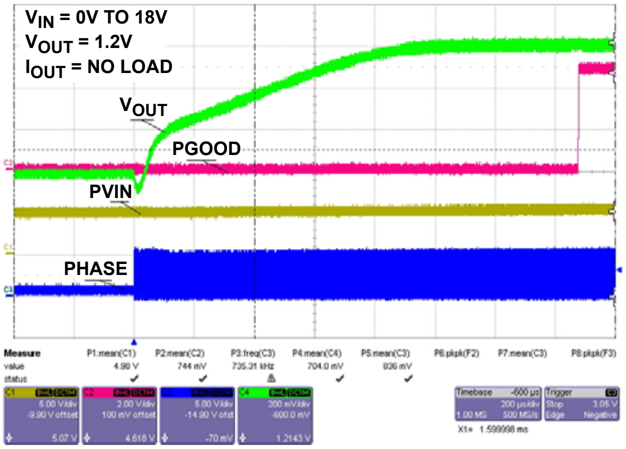


FIGURE 17. 50% PRE-BIAS START-UP

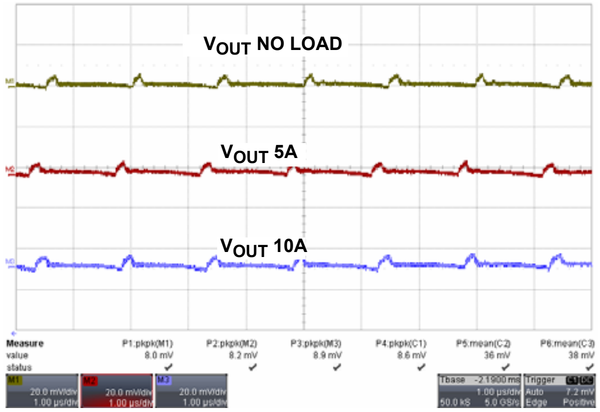


FIGURE 18. 1.2V OUTPUT RIPPLE

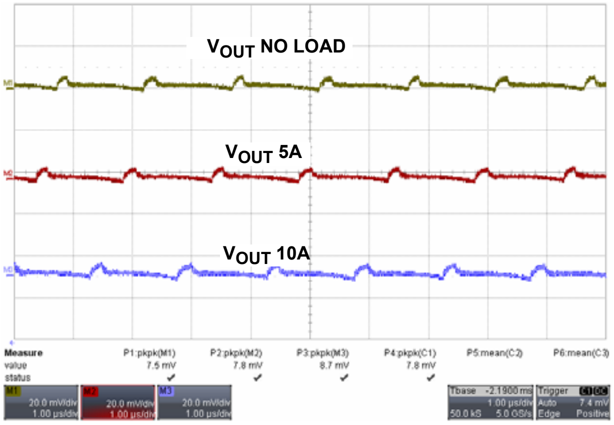


FIGURE 19. 1.5V OUTPUT RIPPLE

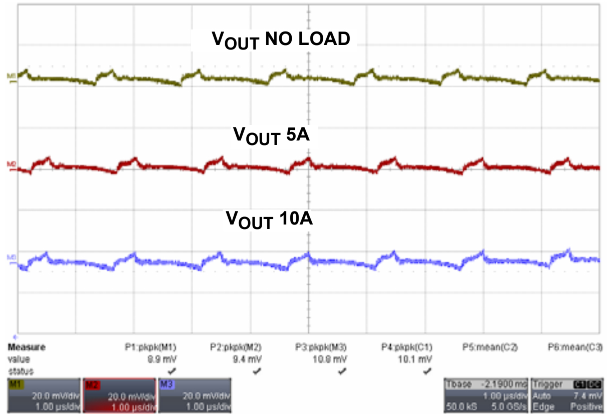


FIGURE 20. 2.5V OUTPUT RIPPLE

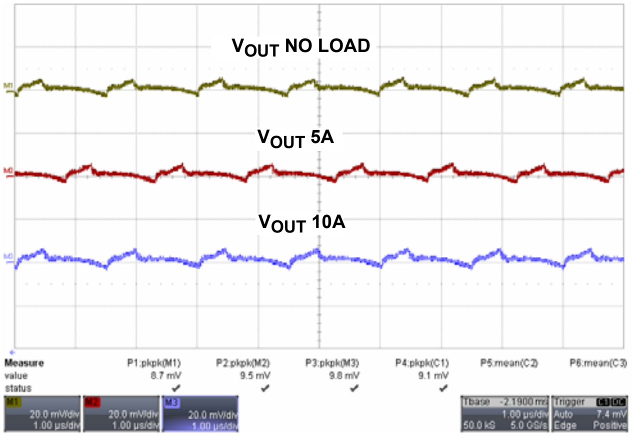


FIGURE 21. 3.3V OUTPUT RIPPLE

Applications Information

Programming the Output Voltage (R_{SET})

The ISL8200AM has an internal 0.6V ±0.7% reference voltage. Programming the output voltage requires a dividing resistor (R_{SET}) between the VOUT_SET pin and the V_{OUT} regulation point. The output voltage can be calculated as shown in Equation 1:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{SET}}{R_{OS}}\right) \quad \text{(EQ. 1)}$$

Note: The ISL8200AM has integrated 2.2kΩ resistances into the module dividing resistor for the bottom side (R_{OS}). The resistances for different output voltages in single-phase operation are listed in Table 1.

TABLE 1. V_{OUT} - R_{SET}

V_{OUT} (V)	0.6	0.8	1.0	1.2
R_{SET} (Ω)	0	732	1.47k	2.2k

V_{OUT} (V)	1.5	1.8	2.0	2.5
R_{SET} (Ω)	3.32k	4.42k	5.11k	6.98k

V_{OUT} (V)	3.3	5.0	6.0
R_{SET} (Ω)	10k	16.2k	20k

The output voltage accuracy can be improved by maintaining the impedance at V_{OUTSET} (internal V_{SEN1+}) at or below 1kΩ effective impedance. Note: The impedance between V_{SEN1+} and V_{SEN1-} is about 500kΩ.

The module has a minimum input voltage at a given output voltage, which needs to be a minimum of 1.43 times the output voltage if operating at f_{SW} = 700kHz switching frequency. This is due to the minimum PWM OFF time ($t_{MIN\text{-}OFF}$).

The equations to determine the minimum P_{VIN} to support the required V_{OUT} are given by Equations 2 and 3; it is recommended to add 0.5V to the result to account for temperature variations.

$$PV_{IN\_MIN} = \frac{V_{OUT} \times t_{SW}}{t_{SW} - t_{MIN\_OFF}} \quad \text{(EQ. 2)}$$

t_{SW} = switching period = $1/f_{SW}$

for the 700kHz switching frequency = 1428ns

$$PV_{IN\_MIN} = 1.43 \times V_{OUT} \quad \text{(EQ. 3)}$$

For 3.3V input voltage operation, the V_{IN} voltage is recommended to be 5V for sufficient gate drive voltage. This can be accomplished by using a voltage greater than or equal to 5V on V_{IN}, or directly connecting the 5V source to both V_{IN} and PVCC.

V_{IN} is the input to the internal LDO that powers the control circuitry while PVCC is the output of the aforementioned LDO. P_{VIN} is the power input to the power stage. Figure 22 shows a scenario in which the power stage is running at 3.3V and the control circuitry is running at 5V; keep in mind that the PVCC pin is also at 5V to ensure that the LDO is not functioning. Figure 23 shows a setup in which both the control circuitry and the power stage is at a 5V rail. It is imperative to not cross 5.5V in this setup as that is the voltage limit on the PVCC pin. Figure 24 is a more general setup and can accommodate V_{IN} ranges up to 20V; PVCC is not tied to V_{IN} and hence the control circuitry is powered by the internal LDO.

The circuit shown in Figure 25 ensures proper start-up by injecting current into the ISHARE line until all phases are ready to start regulating.

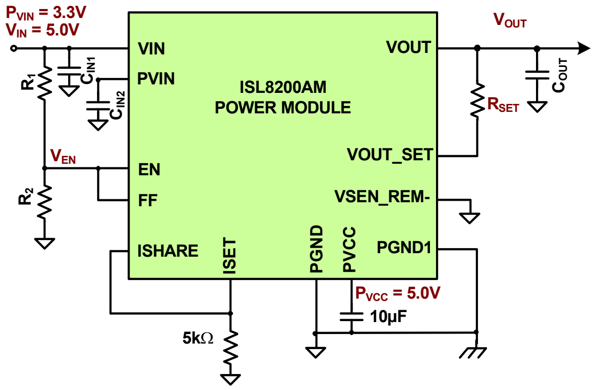


FIGURE 22. 3.3V OPERATION

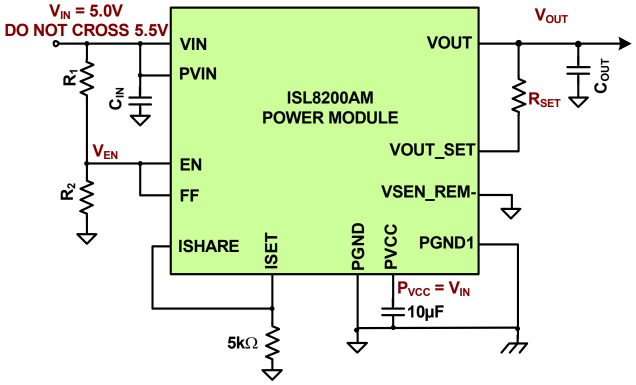


FIGURE 23. 5V OPERATION

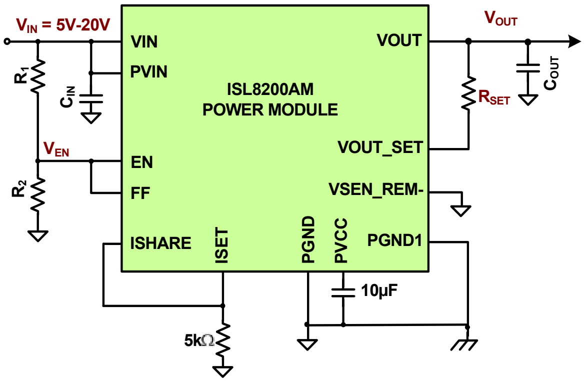


FIGURE 24. 5V TO 20V OPERATION

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, but consideration should be taken for the higher surge current during power-up. The ISL8200AM provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 4:

$$C_{IN(MIN)} = I_O \bullet \frac{D \bullet (1-D)}{V_{P\text{-}P(MAX)} \bullet f_{SW}} \qquad \text{(EQ. 4)}$$

where:

$C_{IN(MIN)}$ is the minimum input capacitance (μF) required.

I_O is the output current (A).

D is the duty cycle (V_O/V_{IN}).

$V_{P\text{-}P(MAX)}$ is the maximum peak-to-peak voltage (V).

f_{SW} is the switching frequency (Hz).

In addition to the bulk capacitance, some low Equivalent Series Inductance (ESL) ceramic capacitance is recommended to decouple between the drain terminal of the high-side MOSFET and the source terminal of the low-side MOSFET. This is used to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

The ISL8200AM is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (C_{OUT}) with low enough Equivalent Series Resistance (ESR); the recommended ESR is <10mΩ. When the total ESR is below 4mΩ, a capacitor (C_{FF}) between 2.2nF to 10nF is recommended; C_{FF} is placed in parallel with RSET, in between the VOUT and VOUT_SET pin. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor, or a ceramic capacitor. The typical capacitance is 330μF and decoupled ceramic output capacitors are used per phase. The internally optimized loop compensation provides sufficient stability margins for all ceramic capacitor applications with a recommended total value of 300μF per phase. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spike is required.

Using Multiple Phases

The ISL8200AM can be easily connected in parallel with other ISL8200AM modules and current share providing an additional 10A per phase. For two phases, simply follow the schematic shown in Figure 5 on page 6. A rough summary shows that the modules share VIN, VOUT, and GND and have their ISHARE pins tied together with a 10kΩ resistor to ground (per phase). When using three phases or more, it is recommended that you add the following circuitry (see Figure 25) to ensure proper start-up. The circuit shown in Figure 25 ensures proper start-up by injecting current into the ISHARE line until all phases are ready to start regulating. For additional phases, the RC time constant, using R_{INC} and C_G, might have to be adjusted to increase the turn on time of the PFET (QSHR). For three to four phases, these are the values: R_{INC} = 243k, R_{PH1} = 15k, Q_{SHR} = Small Signal PFET, C_G = 22nF.

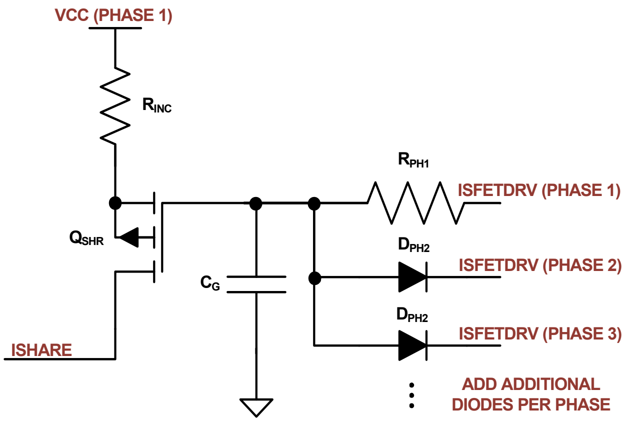


FIGURE 25. START-UP CIRCUITRY

Functional Description

Initialization

The ISL8200AM requires VCC and PVCC to be biased by a single supply. Power-On Reset (POR) circuits continually monitor the bias voltages (PVCC and VCC) and the voltage at the EN pin. The POR function initiates soft-start operation 384 clock cycles after the EN pin voltage is pulled above 0.8V, all input supplies exceed their POR thresholds, and the PLL locking time expires. The enable pin can be used as a voltage monitor and to set desired hysteresis with an internal 30μA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is especially designed for applications that require higher input rail POR for better undervoltage protection. For example, in 12V applications, R_{UP} = 53.6k and R_{DOWN} = 5.23k will set the turn-on threshold (V_{EN_RTH}) to 10.6V and turn-off threshold (V_{EN_FTH}) to 9V, with 1.6V hysteresis (V_{EN_HYS}). These numbers are explained in Figure 30 on page 15.

During shutdown or fault conditions, the soft-start is quickly reset while UGATE and LGATE immediately change state (<100ns) upon the input dropping below POR.

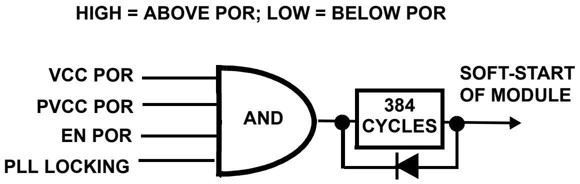


FIGURE 26. SOFT-START INITIALIZATION LOGIC

Soft-start

The ISL8200AM has an internal digital precharged soft-start circuitry, which has a rise time inversely proportional to the switching frequency and is determined by a digital counter that increments with every pulse of the phase clock. The full soft-start time from 0V to 0.6V can be estimated by Equation 5.

$$t_{SS} = \frac{2560}{f_{SW}} \qquad \text{(EQ. 5)}$$

The ISL8200AM can work under a precharged output. The PWM outputs will not be fed to the drivers until the first PWM pulse is seen. The low-side MOSFET is held low for the first clock cycle to provide charge for the bootstrap capacitor. If the precharged output voltage is greater than the final target level but less than the 113% setpoint, switching will not start until the output voltage is reduced to the target voltage and the first PWM pulse is generated. The maximum allowable precharged level is 113%. If the precharged level is above 113% but below 120%, the output will hiccup between 113% (LGATE turns on) and 87% (LGATE turns off) while EN is pulled low. If the precharged load voltage is above 120% of the targeted output voltage, then the controller will be latched off and not be able to power-up.

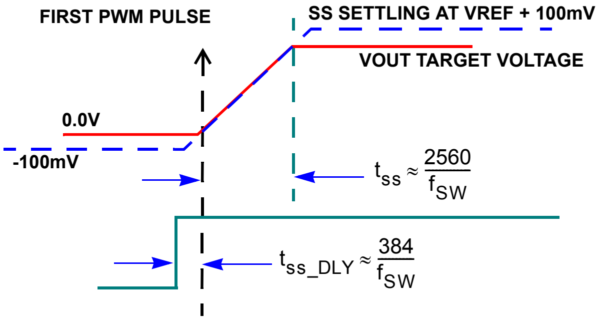


FIGURE 27. SOFT-START WITH V_{OUT} = 0V

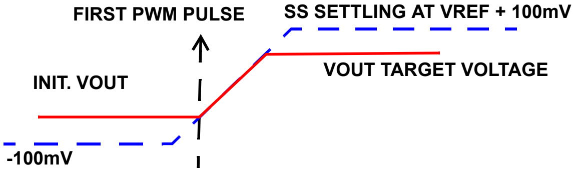


FIGURE 28. SOFT-START WITH V_{OUT} < TARGET VOLTAGE

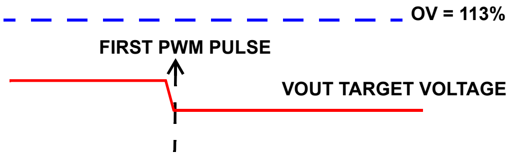
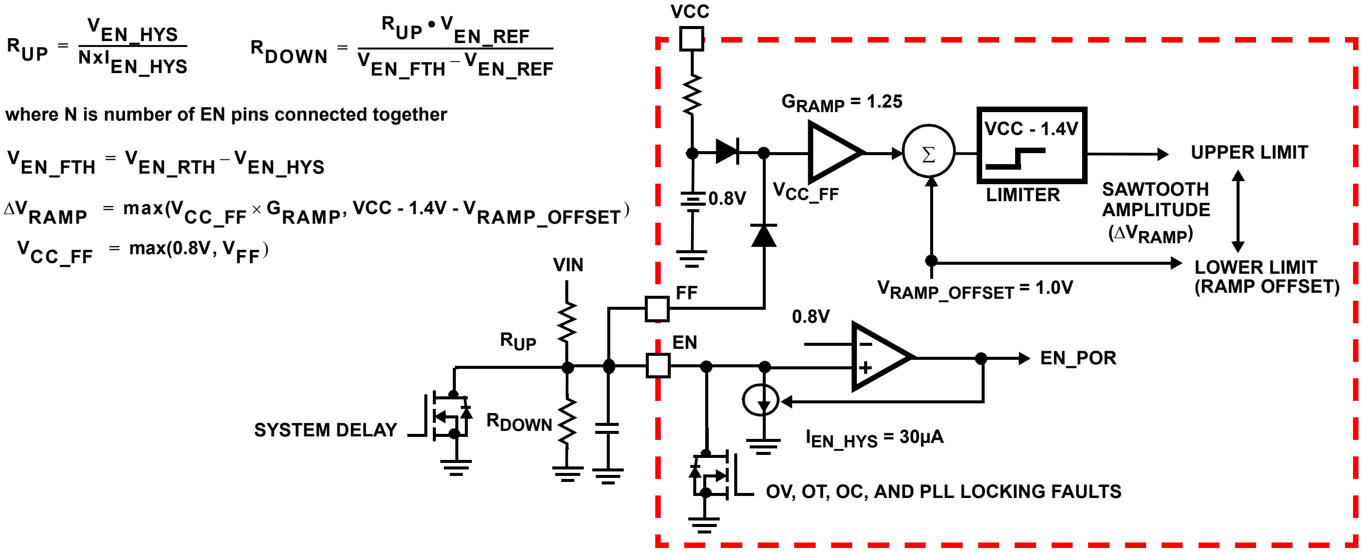


FIGURE 29. SOFT-START WITH V_{OUT} BELOW OV BUT ABOVE FINAL TARGET VOLTAGE

Voltage Feedforward

The voltage applied to the FF pin is fed to adjust the sawtooth amplitude of the channel. The amplitude the sawtooth is set to is 1.25 times the corresponding FF voltage when the module is enabled. This configuration helps to maintain a constant gain ($G_M = V_{IN} \bullet D_{MAX}/\Delta V_{RAMP}$) and input voltage to achieve optimum loop response over a wide input voltage range. The sawtooth ramp offset voltage is 1V (equal to 0.8V*1.25), and the peak of the sawtooth is limited to V_{CC} - 1.4V. With V_{CC} = 5.4V, the ramp has a maximum peak-to-peak amplitude of V_{CC} - 2.4V (equal to 3V); so the feed-forward voltage effective range is typically 3 times as the ramp amplitude ranges from 1V to 3V.

A 384 cycle delay is added after the system reaches its rising POR and prior to the soft-start. The RC timing at the FF pin should be sufficiently small to ensure that the input bus reaches its static state and the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. A 1nF capacitor is recommended as a starting value for typical applications. The voltage on the FF pin needs to be above 0.8V prior to soft-start and during PWM switching to ensure reliable regulation. In a typical application, the FF pin can be shorted to the EN pin.



$$R_{UP} = \frac{V_{EN\_HYS}}{N \times I_{EN\_HYS}} \qquad R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

where N is number of EN pins connected together

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

$$\Delta V_{RAMP} = \max(V_{CC\_FF} \times G_{RAMP}, VCC - 1.4V - V_{RAMP\_OFFSET})$$

$$V_{CC\_FF} = \max(0.8V, V_{FF})$$

FIGURE 30. SIMPLIFIED ENABLE AND VOLTAGE FEEDFORWARD CIRCUIT

Power-good

The power-good comparators monitor the voltage on the internal VMON1 pin. The trip points are shown in Figure 31. PGOOD will not be asserted until after the completion of the soft-start cycle. PGOOD pulls low upon both ENs disabling it if the internal VMON1 pin's voltage is out of the threshold window. PGOOD will not be asserted until after the completion of the soft-start cycle. PGOOD will not pull low until the fault is present for three consecutive clock cycles.

The UV indication is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to some reason (cases when EN is not pulled low) other than OV, OC, OT, and PLL faults, PGOOD will be pulled low.

Current Share

The IAVG_CS is the current of the module. ISHARE and ISET pins source a copy of IAVG_CS with 15µA offset. That is, the full scale will be 126µA.

The share bus voltage (V_{ISHARE}) set by an external resistor ($R_{ISHARE} = R_{ISET}/NCTRL$) represents the average current of all active modules. The voltage (V_{ISET}) set by R_{ISET} represents the average current of the corresponding module and is compared with the share bus (V_{ISHARE}). The current share error signal (ICSH_ER) is then fed into the current correction block to adjust each module's PWM pulse accordingly. The current share function provides at least 10% overall accuracy between ICs, up to three phases. The current share bus works for up to six phases. Figure 5 on page 6 further illustrates the current sharing aspects of the ISL8200AM.

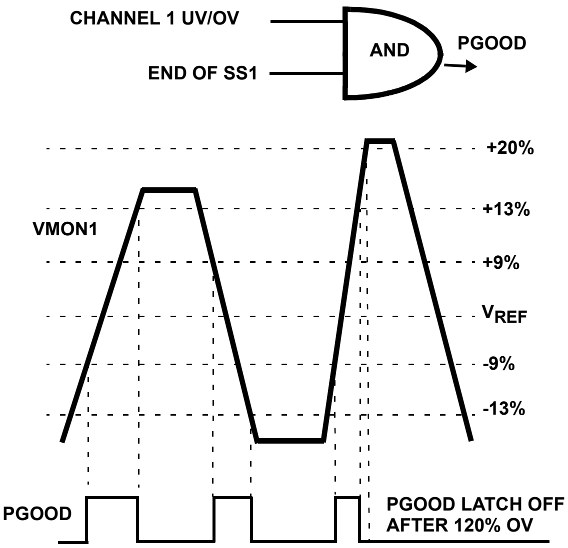


FIGURE 31. POWER-GOOD THRESHOLD WINDOW

When only one module is in the system, the ISET and ISHARE pins can be shorted together and grounded through a single resistor to ensure zero share error. A resistor value of 5k (paralleling 10k on ISET and ISHARE) will allow operation up to the OCP level.

Overvoltage Protection (OVP)

The OVP indication circuitry monitors the voltage on the internal VMON1 pin.

The OVP is active from the beginning of soft-start. An overvoltage (OV) condition (>120%) latches the IC off (the high-side MOSFET to latch off permanently; the low-side MOSFET turns on immediately at the time of OV trip and then turns off permanently after the output voltage drops below 87%). The EN and PGOOD are also latched low at an OV event. The latch condition can be reset only by recycling VCC.

There is another non-latch OVP (113% of target level). At the condition of EN low and an output over 113% OV, the lower side MOSFET will turn on until the output drops below 87%. This is to protect the overall power trains if a single-channel in a multimodule system detects an OV. The low-side MOSFET always turns on at the conditions of EN = LOW and an output voltage above 113% (all EN pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (multimodule mode), all cascaded modules can latch off simultaneously through the EN pins (EN pins are tied together in multiphase mode), and each IC shares the same sink current to reduce the stress and eliminate the bouncing among phases.

Over-temperature Protection (OTP)

When the junction temperature of the IC is greater than +150°C (typically), the EN pin will be pulled low to inform other cascaded channels through their EN pins. All connected ENs stay low and release after the IC's junction temperature drops below +125°C (typically), a +25°C hysteresis (typically).

Overcurrent Protection (OCP)

The OCP function is enabled at start-up. The load current sampling ICS1 is sensed by sampling the voltage across Q2 MOSFET $r_{DS(ON)}$ during turn on through the resistor between OCSET and PHASE pin. IC1 is compared with the Channel Overcurrent Limit '111µA OCP' comparator, and waits seven cycles before an OCP condition is declared. The module's output current (ICS1) plus a fixed internal 15µA offset forms a voltage (V_{ISHARE}) across the external resistor, R_{ISHARE}. V_{ISHARE} is compared with a precision internal 1.2V threshold for a second method to detect the OCP condition.

Multi-module operation can be achieved by connecting the ISHARE pin of two or more modules together. In multi-module operation the voltage on the ISHARE pin correlates to the average current of all active channels. The output current of each module in multi-module operation is compared to a precise 1.2V threshold to determine the overcurrent condition. Additionally, each module has an overcurrent trip point of 111µA with 7-cycle delay. Note that it is not necessary for the R_{ISHARE} to be scaled to trip at the same level as the 111µA OCP comparator. Typically the ISHARE pin average current protection level should be higher than the phase current protection level.

With an internal $R_{ISEN\text{-}IN}$ of 2.2kΩ, the OCP level is set to the default value. To lower the OCP level, an external $R_{ISEN\text{-}EX}$ is connected between the OCSET and PHASE pins. The relationships between the external $R_{ISEN\text{-}EX}$ values and the typical output current $I_{OUT(MAX)}$ OCP levels for ISL8200AM are shown in Figures 32 through 34. Note that the OCP level shown in these graphs is the average output current and not the inductor ripple current.

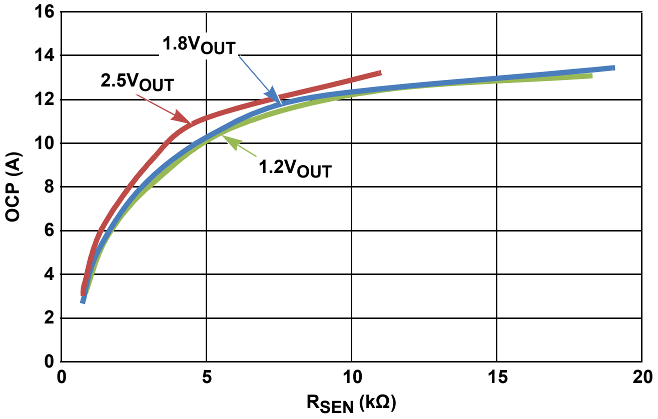


FIGURE 32. $5V_{IN}$

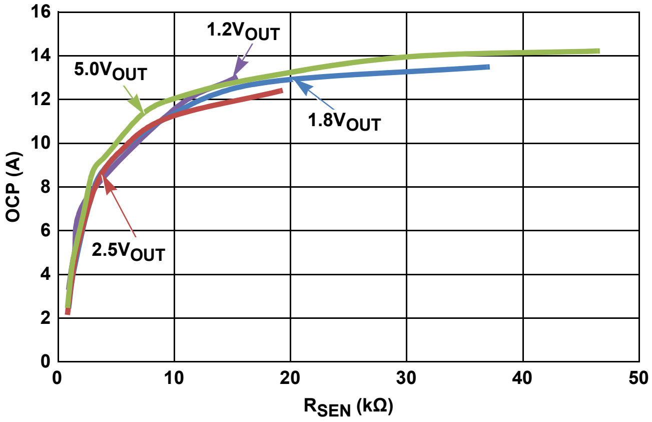


FIGURE 33. $12V_{IN}$

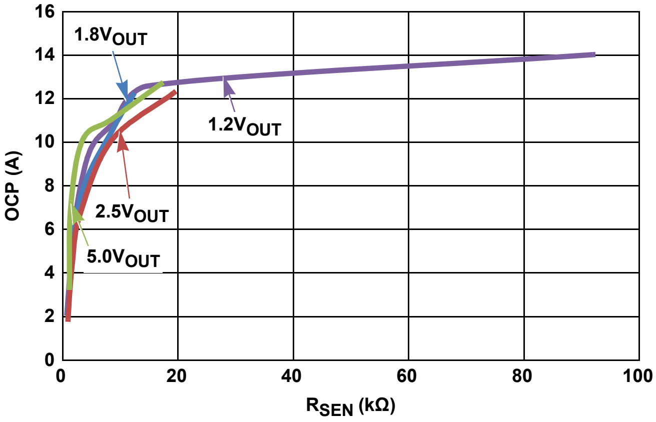


FIGURE 34. $20V_{IN}$

In a high input voltage, high output voltage application, such as 20V input to 5V output, the inductor ripple becomes excessive due to the fixed internal inductor value. In such applications, the output current will be limited from the rating to approximately 70% of the module's rated current.

When OCP is triggered, the controller pulls EN low immediately to turn off UGATE and LGATE.

For overload and hard short conditions, the overcurrent protection reduces the regulator RMS output current to much less than a full load by putting the controller into hiccup mode. A delay time, equal to three soft-start intervals, is entered to allow the disturbance to be cleared out. After the delay time, the controller then initiates a soft-start interval. If the output voltage comes up and returns to the regulation, PGOOD transitions high. If the OC trip is exceeded during the soft-start interval, the controller pulls EN low again. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed.

Fault Handshake

In a multi-module system with the EN pins wired-OR together, all modules can immediately turn off at one time when a fault condition occurs in one or more modules. A fault pulls the EN pin low, disabling all the modules and therefore not creating current bounce. Thus, no single channel is overstressed when a fault occurs.

Because the EN pins are pulled down under fault conditions, the pull-up resistor (R_{UP}) should be scaled to sink no more than 5mA current from EN pin. Essentially, the EN pins cannot be directly connected to VCC.

Oscillator

The oscillator is a sawtooth waveform, providing for leading edge modulation with 350ns minimum dead time. The oscillator (sawtooth) waveform has a DC offset of 1.0V. Each channel's peak-to-peak of the ramp amplitude is set to be proportional to the voltage applied to its corresponding FF pin.

Frequency Synchronization and Phase Lock Loop

The FSYNC_IN pin has two primary capabilities: fixed frequency operation and synchronized frequency operation. By tying a resistor (RFS) to PGND1 from the FSYNC_IN pin, the switching frequency can be set at any frequency between 700kHz and 1.5MHz. The ISL8200AM has an integrated 59kΩ resistor between FSYNC_IN and PGND1, which sets the default frequency to 700kHz. The frequency setting curve shown in Figure 35 is provided to assist in selecting an externally connected resistor RFS-ext between FSYNC_IN and PGND1 to increase the switching frequency.

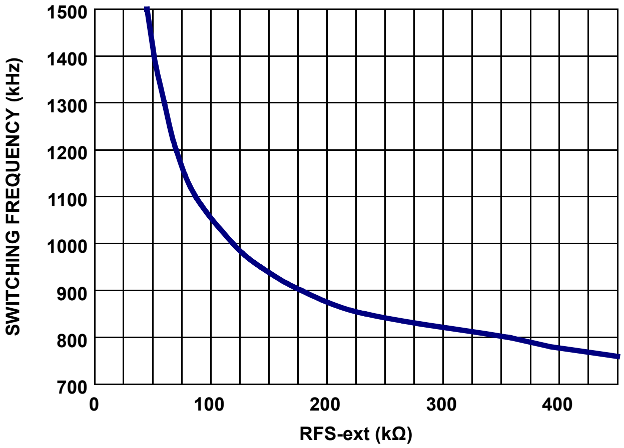


FIGURE 35. RFS-ext vs SWITCHING FREQUENCY

By connecting the FSYNC_IN pin to an external square pulse waveform (such as the CLKOUT signal, typically 50% duty cycle from another ISL8200AM), the ISL8200AM will synchronize its switching frequency to the fundamental frequency of the input waveform. The voltage range on the FSYNC_IN pin is $V_{CC}/2$ to V_{CC}. The Frequency Synchronization feature will synchronize the leading edge of the CLKOUT signal with the falling edge of Channel 1's PWM clock signal. CLKOUT is not available until the PLL locks.

The locking time is typically 210µs for f_{SW} = 700kHz. EN is not released for a soft-start cycle until FSYNC_IN is stabilized and the PLL is in locking. It is recommended to connect all EN pins together in multiphase configuration.

The loss of a synchronization signal for 13 clock cycles causes the IC to be disabled until the PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding FSYNC_IN low will disable the IC.

Setting Relative Phase-shift on CLKOUT

Depending upon the voltage level at PH_CNTRL, set by the V_{CC} resistor divider output, the ISL8200AM operates with CLKOUT phase shifted, as shown in Table 2. The phase shift is latched as V_{CC} raises above POR so it cannot be changed on the fly.

TABLE 2.

DECODING PH_CNTRL RANGE	PHASE FOR CLKOUT WRT CHANNEL 1	REQUIRED PH_CNTRL
<29% of V_{CC}	-60°	15% V_{CC}
29% to 45% of V_{CC}	90°	37% V_{CC}
45% to 62% of V_{CC}	120°	53% V_{CC}
62% to V_{CC}	180°	V_{CC}

Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary, which are illustrated in Figures 36 and 37.

- The ground connection between PGND1 (Pin 15) and PGND (Pin 18) should be a solid ground plane under the module.
- Place a high frequency ceramic capacitor between (1) PVIN and PGND (Pin 18) and (2) a 10µF between PVCC and PGND1 (Pin 15) as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (PVIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Keep the trace connection to the feedback resistor short.
- Use remote sensed traces to the regulation point to achieve a tight output voltage regulation, and keep them in parallel. Route a trace from VSEN_REM- to a location near the load ground, and a trace from feedback resistor to the point-of-load where the tight output voltage is desired.
- Avoid routing any sensitive signal traces, such as the VOUT and VSENREM- sensing point near the PHASE pin or any other noise-prone areas.
- FSYNC_IN is a sensitive pin. If it is not used for receiving an external synchronization signal, then keep the trace connecting to the pin short. A bypass capacitor value of 100pF, connecting between FSYNC_IN pin and GND1, can help to bypass the noise sensitivity on the pin.

The recommended layout considerations for operating multiple modules in parallel follows the single-phase guidelines as well as these additional points:

- Orient VOUT toward the load on the same layer and connect with thick direct copper etch directly to minimize the loss.
- Place modules such that Pins 1 to 11 point away from power pads (PD1-4) so that signal busses (EN, ISHARE, CLKOUT-to-FSYNCIN) can be routed without going under the module. Run them along the perimeter as in Figure 37.
- Keep remote sensing traces separate, and connect only at the regulation point. Four separate traces for VSEN_REM- and RFBT (which stands for remote feedback) as the example shows in Figure 37.

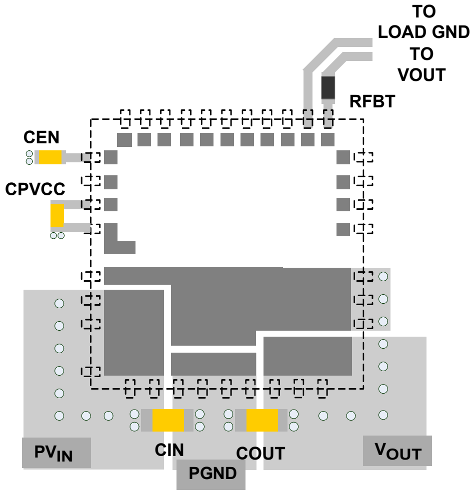


FIGURE 36. RECOMMENDED LAYOUT FOR SINGLE PHASE SETUP

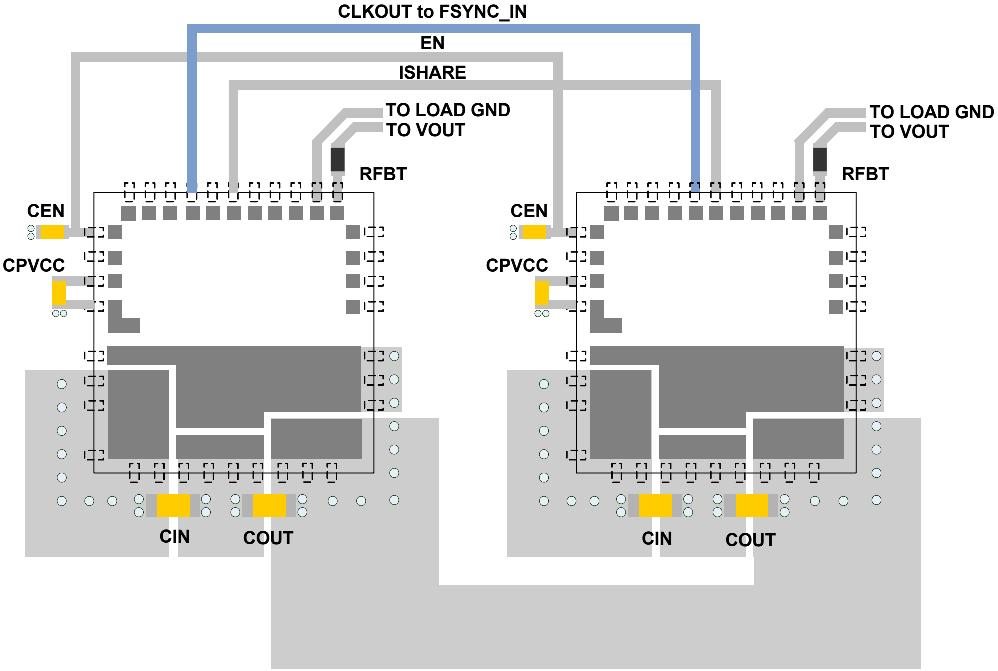


FIGURE 37. RECOMMENDED LAYOUT FOR DUAL PHASE SETUP

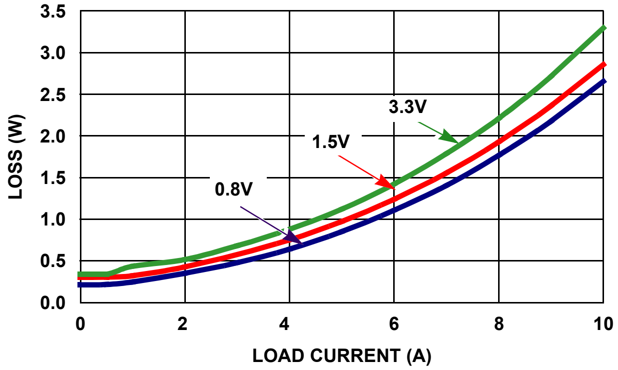


FIGURE 38. POWER LOSS vs LOAD CURRENT ($5V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

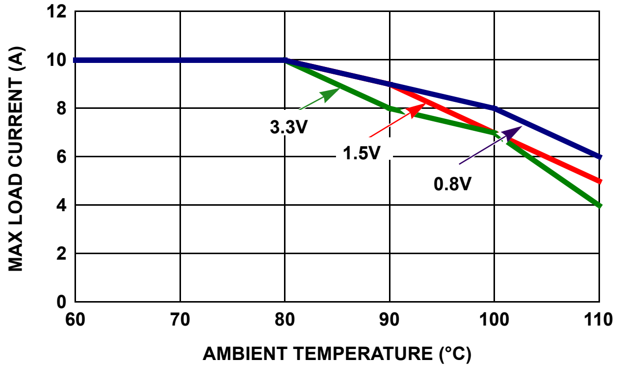


FIGURE 39. DERATING CURVE ($5V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

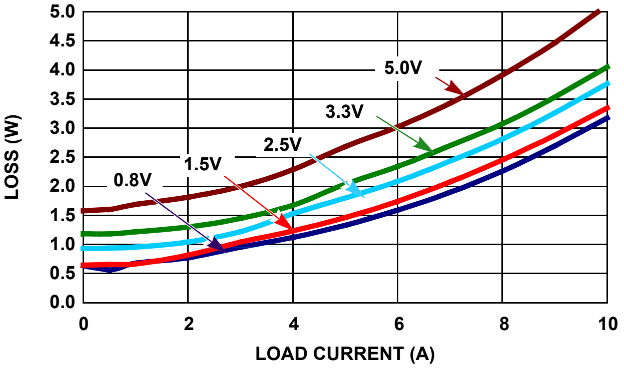


FIGURE 40. POWER LOSS vs LOAD CURRENT ($12V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

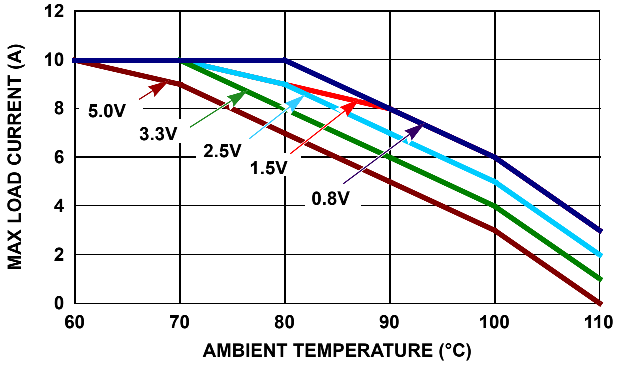


FIGURE 41. DERATING CURVE ($12V_{IN}$) 0 LFM FOR VARIOUS OUTPUT VOLTAGES

Thermal Considerations

Empirical power loss curves, shown in Figures 38 to 41, along with θ_{JA} from thermal modeling analysis can be used to evaluate the module's thermal requirements. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

Package Description

The structure of the ISL8200AM belongs to the Quad Flat-pack No-lead package (QFN). This kind of package has advantages such as good thermal and electrical conductivity, low weight, and small size. The QFN package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8200AM contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8200AM is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multiple component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing L23.15x15 on page 23. The module has a small size of 15mmx15mmx2.2mm. Figure 42 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to their application.

PCB Layout Pattern Design

The bottom of the ISL8200AM is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing L23.15x15 on page 23. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and I/O termination dimensions, except for the PCB lands being a slightly extended distance of 0.2mm (0.4mm max) longer than the QFN terminations, which allows for solder filleting around the periphery of the package. This ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be from 0.3mm to 0.33mm in diameter with the barrel plated with 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing L23.15x15 on page 24. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) QFN.

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 42 is provided as a guideline to be customized for varying manufacturing practices and applications.

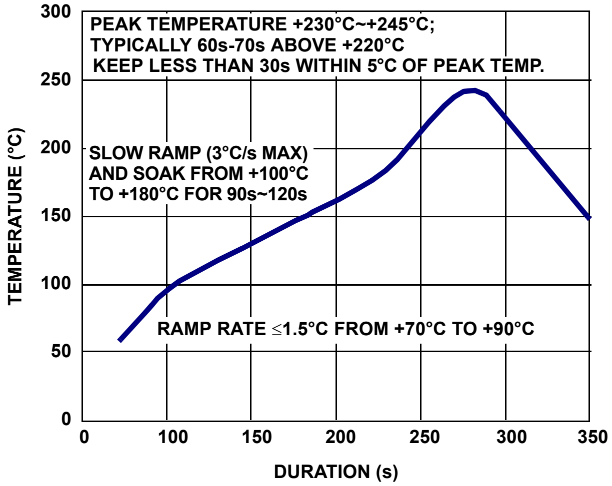


FIGURE 42. TYPICAL REFLOW PROFILE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Apr 27, 2018	FN8271.7	Updated Ordering Information table by adding tape and reel parts to table, updating brand of ISL8200AMM parts, updating Note 1 and its reference location, and added tape and reel quantity column. Removed About Intersil section and updated disclaimer.
May 12, 2017	FN8271.6	Added ISL8200AMMZ device in ordering information table. Updated Note 2. Added ISL8200AMMZ parameters in electrical specification table. Corrected syntax and grammar errors in “Initialization” on page 14, “Overvoltage Protection (OVP)” on page 16, and “Fault Handshake” on page 17. Applied header/footer template.
Jul 30, 2015	FN8271.5	On page 1, in Features, changed “Input Voltage Range +4.5V to +20V at 10A” to “Input Voltage Range +3.0V to +20V at 10A” Updated Graphic on page 1 Added Evaluation Board ISL8200AMEV1PHZ to Ordering Information on page 2. Added Note 8 to Electrical Spec Table on page 9.
Mar 7, 2013	FN8271.4	Features on page 1 Input Voltage Range updated from 3V to 20V to 4.5V to 20V.
Jan 24, 2013	FN8271.3	Made correction in Abs Max Ratings Table under Recommended Operating Conditions on page 7 by separating in the Input Voltage PVIN and VIN. PVIN is 3V to 20V and V_{IN} 4.5V to 20V.
Jan 2, 2013		Abs Max Ratings Table under Recommended Operating Conditions on page 7 changed Input Voltage, PVIN, V_{IN} from 3V to 20V to 4.5 to 20V.
Oct 8, 2012		Pin Description Table on page 4 changed in Description column operational voltage range for PVCC and VCC from “4.5V to 5.5V” to “4.5 to 5.6” Abs Max Ratings Table under Recommended Operating Conditions on page 7 changed Driver Bias Voltage, PVCC and Signal Bias Voltage, VCC from “3V to 5.6V” to “4.5V to 5.6V”
Sep 13, 2012	FN8271.2	Initial Release.

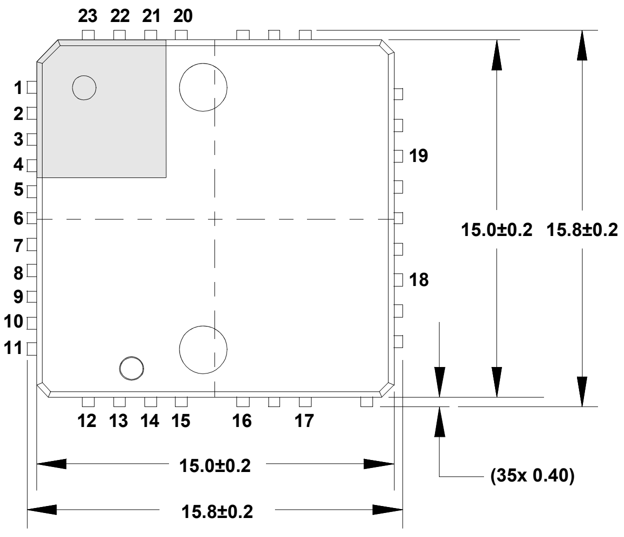
Package Outline Drawing

L23.15x15

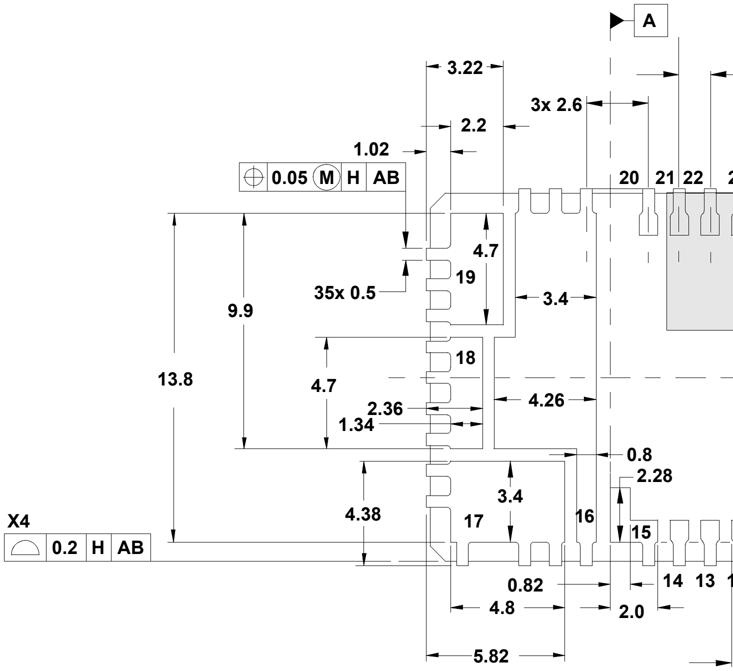
23 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

Rev 3, 10/10

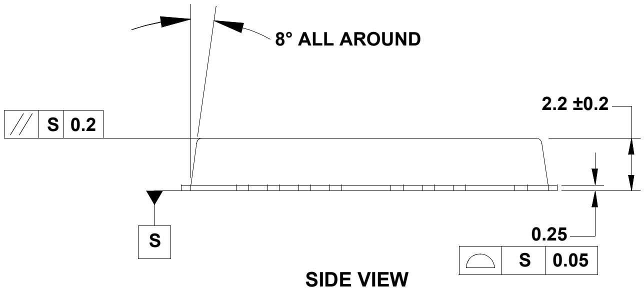
For the most recent packa



TOP VIEW



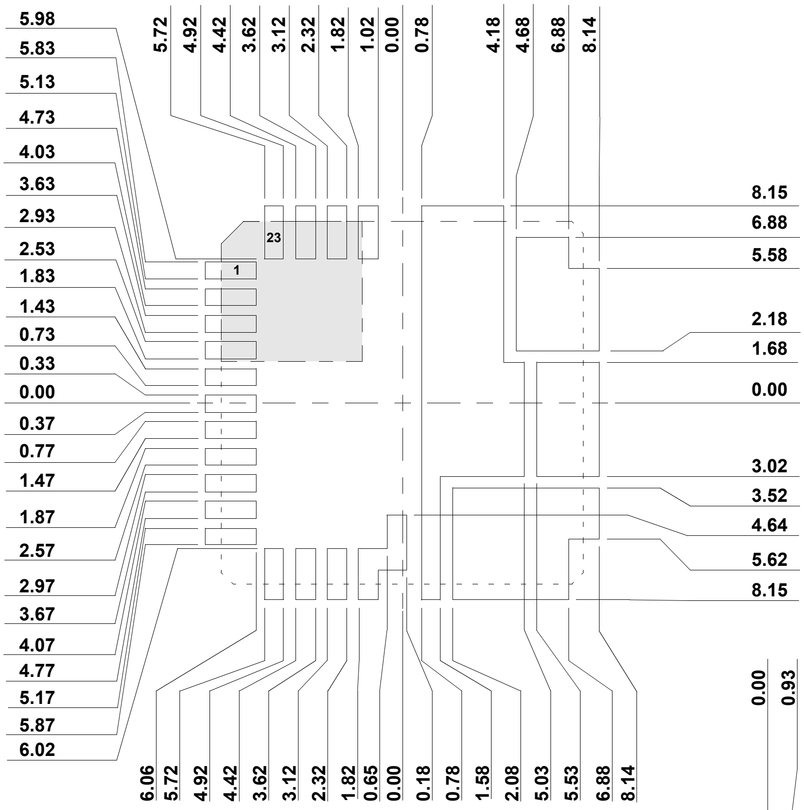
BOTTOM VIEW



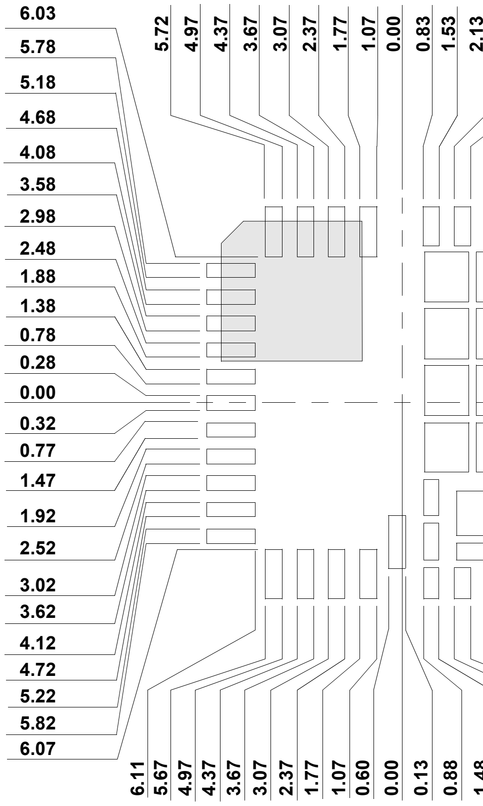
SIDE VIEW

NOTES:

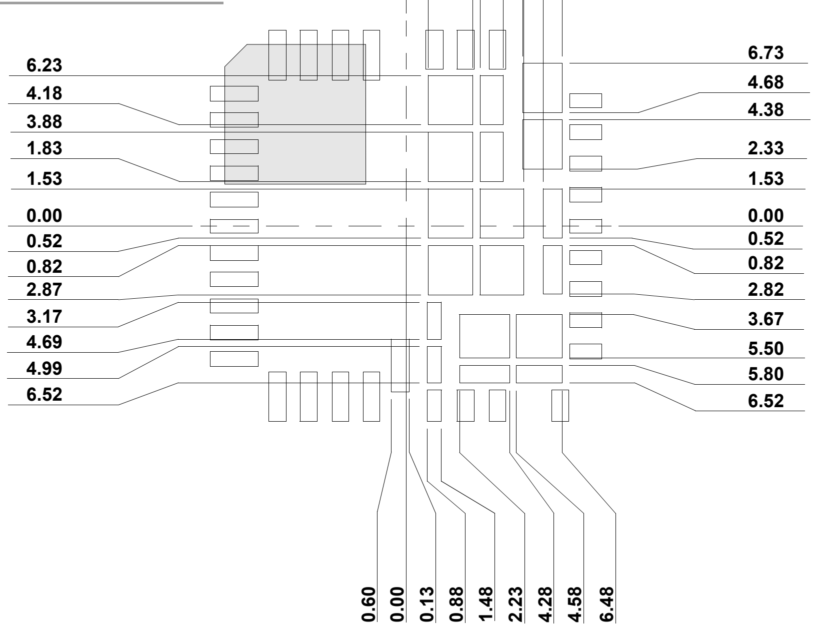
1. Dimensions are in millimeters.
2. Unless otherwise specified, tole
   Body Tolerance ±0.2mm
3. The configuration of the pin #1 i
   located within the zone indicate
   either a mold or mark feature.



TYPICAL RECOMMENDED LAND PATTERN



STENCIL PATTERN WITH SQ



STENCIL PATTERN WITH SQUARE PADS-2

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(Rev.4.0-1 November 2017)

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