

## ISL8212M

15A High Efficiency Step-Down Power Module

FN8990  
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The [ISL8212M](#) power module is a single channel, synchronous step-down, non-isolated complete power supply featuring the proprietary Renesas R4™ Technology. The module supports a wide 4.5V to 16.5V input voltage range and a wide 0.5V to 5V output range capable of delivering up to 15A of continuous current, and is optimized for high power density. Integrated LDOs provide module bias voltage, allowing for single supply operation.

The proprietary Renesas R4 control scheme has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. An efficiency enhancing PFM mode greatly improves light-load efficiency. The ISL8212M allows for easy R4 loop optimization, resulting in fast transient performance across a wide range of applications, including all ceramic output filters.

The power module integrates all power and most passive components and requires only a few external components to operate. A set of optional external resistors provides very flexible configuration options (such as frequency,  $V_{OUT}$ , and AV gain). The ISL8212M also features remote voltage sensing and completely eliminates any potential difference between remote and local grounds, improving regulation and protection accuracy. A programmable soft-start reduces the inrush current from the input supply. A precision enable input and power-good (PGOOD) flag are available to coordinate the start-up of the ISL8212M with other voltage rails, which is especially useful for power sequencing. Excellent efficiency and low thermal resistance permit full power operation without heatsinks.

Input Undervoltage Lockout (UVLO), over-temperature, overcurrent, output overvoltage, and output prebias start-up protections ensure safe operations under abnormal operating conditions.

The ISL8212M is available in a compact RoHS compliant thermally-enhanced 12mmx11mmx5.3mm HDA package.

### Applications

- Servers, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- Graphics cards
- General purpose power for ASIC, FPGA, DSP, and memory

### Features

- [R4](#) Technology
  - Linear control loop for optimal transient response
  - Variable frequency and duty cycle control during load transient for fastest possible response
  - Inherent voltage feed-forward for wide range input
- Input voltage range: 4.5V to 16.5V
- Output voltage range: 0.5V to 5V
- ±1.5% load and line regulation with remote sense
- Supports all ceramic solutions
- Integrated LDOs for single input rail solution
- 256 output voltage levels with a configuration pin
- Seven switching frequency options from 300kHz to 1MHz
- PFM operation option for improved light-load efficiency
- Start-up into precharged load
- Power-good monitor for soft-start and fault detection
- Comprehensive fault protection for high system reliability
  - Over-temperature protection
  - Output overcurrent and short-circuit protection
  - Output overvoltage and undervoltage protection
  - Open remote sense protection
  - Input UVLO and power sequence as well as fault reset
- Thermally enhanced 12mmx11mmx5.3mm HDA package

### Related Literature

For a full list of related documents, visit our website:

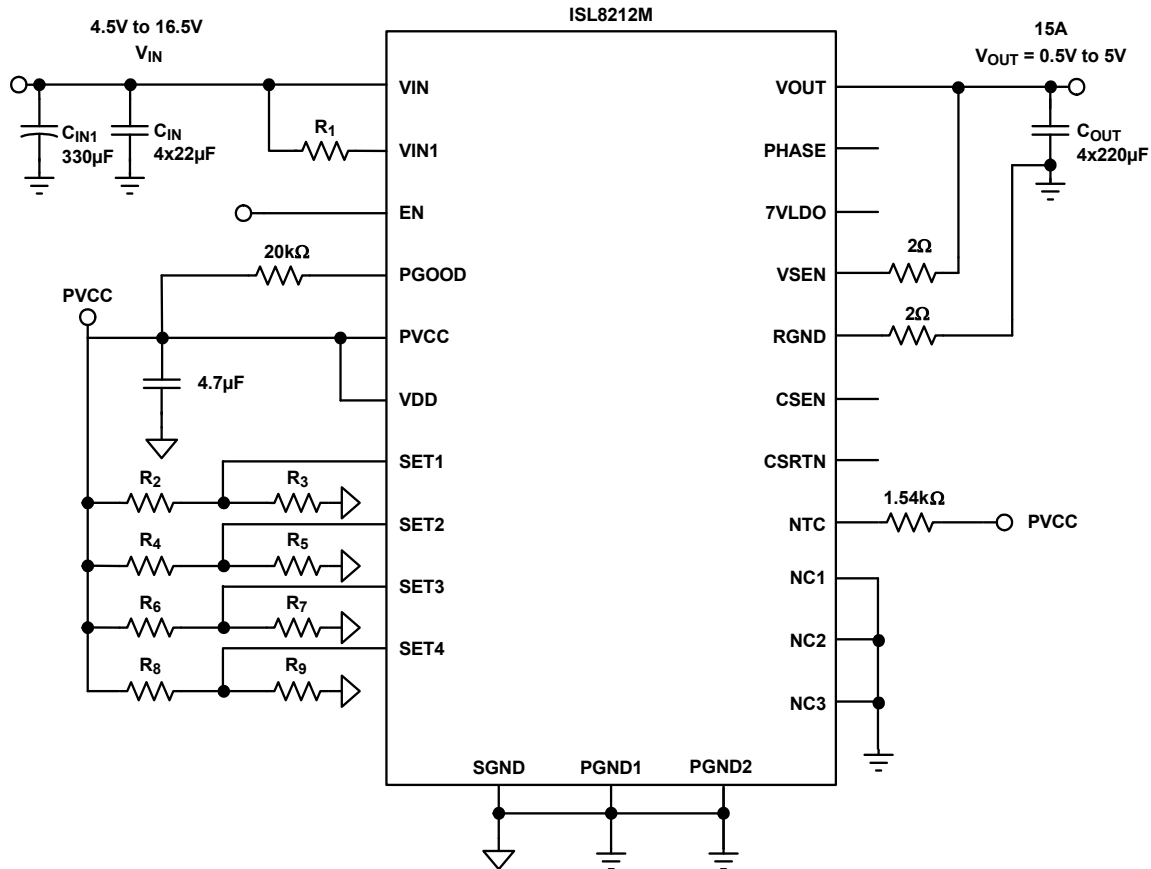
- [ISL8212M](#) device page

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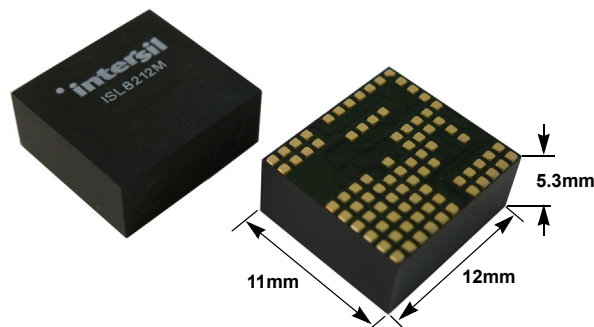
## 1. Overview

### 1.1 Typical Application Circuit



- For  $V_{OUT} = 3.3V$ , minimum  $V_{IN}$  is 5.5V; for  $V_{OUT} = 5V$ , minimum  $V_{IN}$  is 8V.
- $R_1$ : see [Table 2 on page 7](#).
- $R_2$  and  $R_3$ : to set output voltage, see [Table 4 on page 22](#) for typical  $V_{OUT}$ .
- $R_4$  and  $R_5$ : to set PFM/PWM mode and temperature compensation, see [Table 5 on page 22](#).
- $R_6$  and  $R_7$ : to set  $f_{SW}$ , AV gain, OCP hiccup/latch off, and ultrasonic PWM enable, see [Table 6 on page 23](#).
- $R_8$  and  $R_9$ : to set soft start, RR impedance, and AV gain multiplier (1x or 2x), see [Table 7 on page 23](#).
- $R_2$  to  $R_9$ , see [Table 2](#) for typical output voltage selections.

Figure 1. Typical Application Circuit 5V Input Applications



## 1.2 Block Diagram

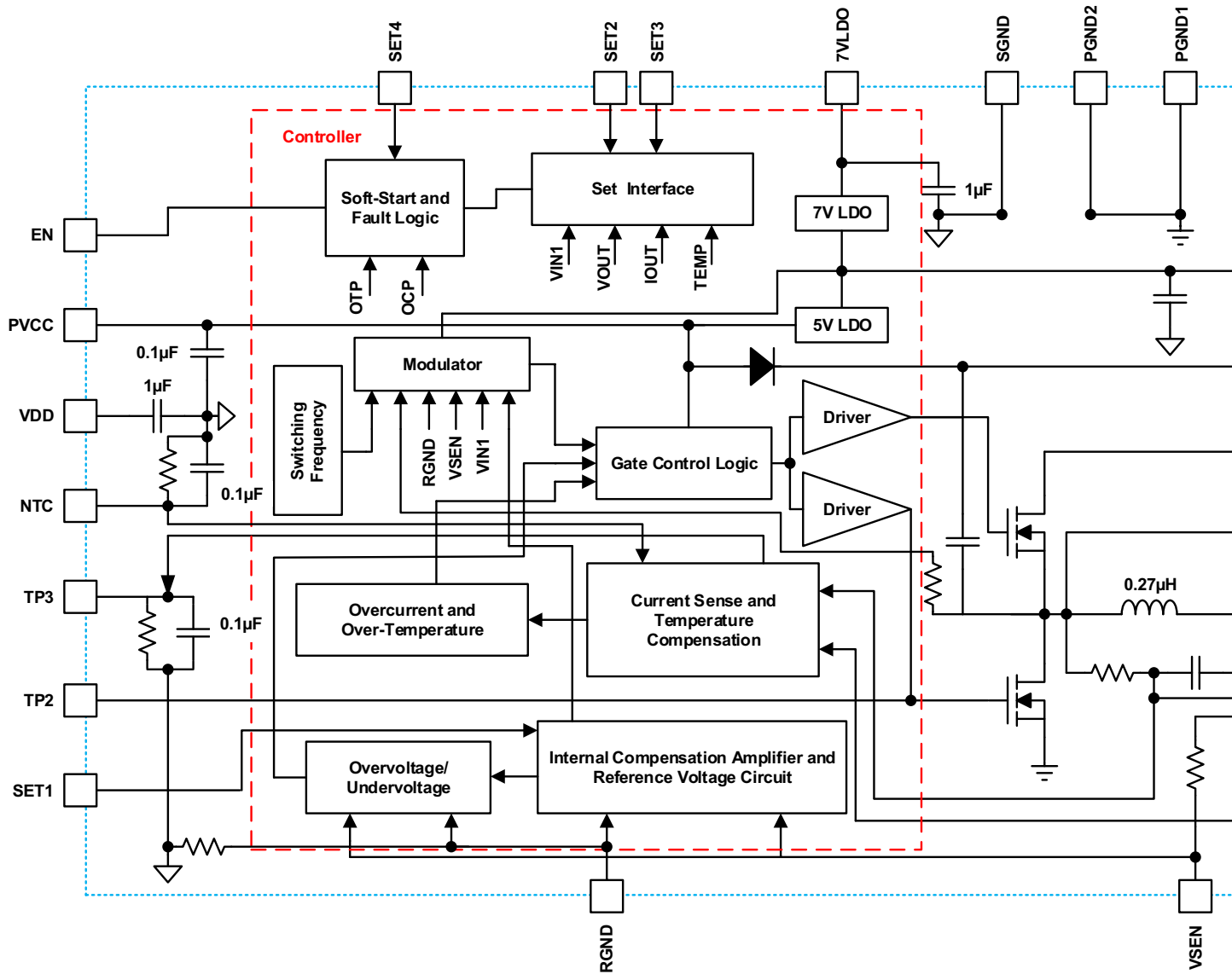


Figure 2. Block Diagram

### 1.3 Ordering Information

| Part Number<br>(Notes 2, 3) | Part Marking     | Temp Range (°C) | Tape and Reel<br>(Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|-----------------------------|------------------|-----------------|-----------------------------------|--------------------------|-------------|
| ISL8212MFRZ                 | ISL8212M         | -40 to +125     | -                                 | 83 Ld 12x11 HDA Module   | Y83.12x11   |
| ISL8212MFRZ-T               | ISL8212M         | -40 to +125     | 720                               | 83 Ld 12x11 HDA Module   | Y83.12x11   |
| ISL8212MFRZ-T1              | ISL8212M         | -40 to +125     | 100                               | 83 Ld 12x11 HDA Module   | Y83.12x11   |
| ISL8212MEVAL1Z              | Evaluation Board |                 |                                   |                          |             |

## Notes:

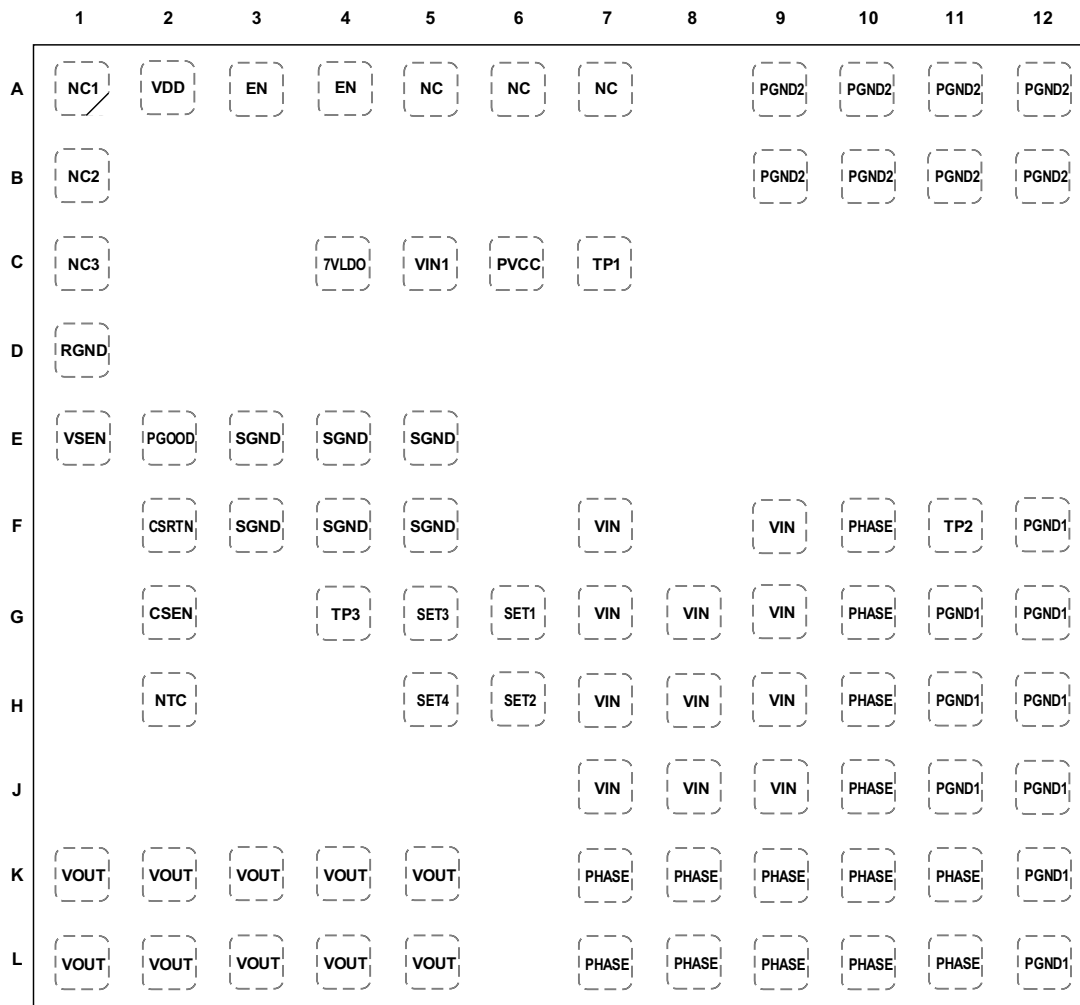
1. See [TB347](#) for details about reel specifications.
2. These plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the [ISL8212M](#) device page. For more information about MSL, see [TB363](#).

**Table 1. Key Differences Between Family of Parts**

| Parameters                        | ISL8282M | ISL8280M | ISL8212M | ISL8210M |
|-----------------------------------|----------|----------|----------|----------|
| Load Current (A)                  | 15       | 10       | 15       | 10       |
| Minimum $V_{IN}$ (V)              | 4.5      | 4.5      | 4.5      | 4.5      |
| Maximum $V_{IN}$ (V)              | 16.5     | 16.5     | 16.5     | 16.5     |
| Minimum $V_{OUT}$ (min) (V)       | 0.5      | 0.5      | 0.5      | 0.5      |
| Maximum $V_{OUT}$ (V)             | 5        | 5        | 5        | 5        |
| Peak efficiency (%)               | 95.2     | 95.2     | 95.2     | 95.2     |
| POR                               | Yes      | Yes      | Yes      | Yes      |
| Minimum Switching Frequency (kHz) | 255      | 255      | 255      | 255      |
| Maximum Switching Frequency (kHz) | 1130     | 1130     | 1130     | 1130     |
| Control Type                      | R4       | R4       | R4       | R4       |
| Sync Capability                   | No       | No       | No       | No       |
| Load Sharing                      | No       | No       | No       | No       |
| PMBus                             | Yes      | Yes      | No       | No       |

## 1.4 Pin Configuration

83 Ld 12x11 HDA  
Top View



## 1.5 Functional Pin Descriptions

| Pin Number   | Symbol | Description   |
|--|--------|---|
| A5, A6, A7   | NC     | No connection pads. The pads dissipate the inductor heat and provide good thermal performance. Do not connect to any other circuits.  |
| A9, A10, A11, A12, B9, B10, B11, B12                           | PGND2  | Power ground. The pads are connected to the source of the low-side MOSFET inside the module and remove heat from the module.  |
| F7, F9, G7, G8, G9, H7, H8, H9, J7, J8, J9                     | VIN    | Power input. Connect the pads directly to an input rail in the range of 4.5V to 16.5V. Connect the input ceramic capacitors between VIN and PGND1 as close as possible to the module.         |
| F10, G10, H10, J10, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11 | PHASE  | Phase node connection. The pads are connected to the source of high-side MOSFET, the drain of low-side MOSFET, output filter inductor, and return path for the UGATE high-side MOSFET driver. |
| F12, G11, G12, H11, H12, J11, J12, K12, L12                    | PGND1  | Power ground. The pads are the sources of the lower MOSFET inside the module and should be connected to the (-) terminals of the external input capacitors and output capacitors.             |
| K1, K2, K3, K4, K5, L1, L2, L3, L4, L5                         | VOUT   | Regulated power module output. Apply the output load between VOUT and PGND1.  |

| Pin Number             | Symbol | Description  |
|------------------------|--------|--|
| A1                     | NC1    | Connected to power ground.   |
| A2                     | VDD    | Logic bias supply. Connect this pin externally to the PVCC rail.   |
| A3, A4                 | EN     | Precision enable input. Pulling EN above the rising threshold voltage initiates the soft-start sequence. Pulling EN below the falling threshold voltage suspends module operation.   |
| B1                     | NC2    | Connected to power ground.   |
| C1                     | NC3    | Connected to power ground.   |
| C4                     | 7V LDO | 7V LDO used to bias the current sensing amplifier.   |
| C5                     | VIN1   | Input voltage pin for the R4 loop (5V) and LDO (7V). Place a high quality low ESR ceramic capacitor (1.0 $\mu$ F, X7R) in close proximity to the pin.  |
| C6                     | PVCC   | Output of the 5V LDO that biases internal control circuits and MOSFET drivers of the ISL8212M. Place a high quality low ESR capacitor (4.7 $\mu$ F X7R) in close proximity to this pin.  |
| C7                     | TP1    | Test pad, leave this pin open.   |
| D1                     | RGND   | Monitors the negative rail of the module output. Connect to ground at the point of regulation.   |
| E1                     | VSEN   | Monitors the positive rail of the module output. Connect to the point of regulation.   |
| E2                     | PGOOD  | Open-drain indicator output. The PGOOD signal is asserted when the output voltage is within $\pm 12.5\%$ of the nominal set output voltage and deasserted when the output voltage is outside of the stated range or the EN pin is pulled low.  |
| E3, E4, E5, F3, F4, F5 | SGND   | Signal ground pads. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. Tie SGND to a solid low noise GND plane.  |
| F2                     | CSRTN  | This pin monitors the negative flow of output current for overcurrent protection and telemetry.  |
| F11                    | TP2    | Test pad, leave this pin open.   |
| G2                     | CSEN   | Monitors the positive flow of output current for overcurrent protection  |
| G4                     | TP3    | Test pad, leave this pin open.   |
| G5                     | SET3   | Programming pin for ultrasonic PFM operation, fault behavior, switching frequency, and R4 (AV) control loop gain.  |
| G6                     | SET1   | Programming pin for output voltage.  |
| H2                     | NTC    | Input pin for the temperature measurement. An NTC thermistor and a decoupling capacitor inside the module are connected between this pin and SGND. Connect this pin through a resistor (1.54k $\Omega$ ) to a VDD pad externally. The voltage at this pin is inversely proportional to the module temperature. |
| H5                     | SET4   | Programming pin for modulator (R4) RR impedance and output slew rate during Soft-Start (SS). It also sets the AV gain multiplier to 1x or 2x and determines the AV gain on SET3.   |
| H6                     | SET2   | Programming pin for PWM/PFM mode and temperature compensation.   |

Table 2. ISL8212M Design Guide Matrix of Typical Applications

| V <sub>OUT</sub> (V) | V <sub>IN</sub> (V) | Frequency (kHz) | AV Gain | RR ( $\Omega$ ) | TCOMP ( $^{\circ}$ C) | R <sub>1</sub> ( $\Omega$ ) |
|----------------------|---------------------|-----------------|---------|-----------------|-----------------------|-----------------------------|
| 0.5                  | 5                   | 400             | 49      | 200k            | 5                     | 0                           |
|                      | 10                  |                 |         |                 |                       |                             |
|                      | 12                  |                 |         |                 |                       |                             |
|                      | 15                  |                 |         |                 |                       |                             |
| 0.6                  | 5                   | 400             | 49      | 200k            | 5                     | 0                           |
|                      | 10                  |                 |         |                 |                       |                             |
|                      | 12                  |                 |         |                 |                       |                             |
|                      | 15                  |                 |         |                 |                       |                             |

Table 2. ISL8212M Design Guide Matrix of Typical Applications (Continued)

| V <sub>OUT</sub> (V) | V <sub>IN</sub> (V) | Frequency (kHz) | AV Gain | RR (Ω) | TCOMP (°C) | R <sub>1</sub> (Ω)             |
|----------------------|---------------------|-----------------|---------|--------|------------|--------------------------------|
| 0.75                 | 5                   | 400             | 49      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 0.9                  | 5                   | 400             | 49      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 1                    | 5                   | 400             | 49      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 1.2                  | 5                   | 400             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 1.5                  | 5                   | 500             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 1.8                  | 5                   | 500             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 2.5                  | 5                   | 600             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 0                              |
|                      | 12                  |                 |         |        |            | 0                              |
|                      | 15                  |                 |         |        |            | 0                              |
| 3.3                  | 5.5                 | 700             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |
|                      | 12                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |
|                      | 15                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |
| 5                    | 8                   | 850             | 26      | 200k   | 5          | 0                              |
|                      | 10                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |
|                      | 12                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |
|                      | 15                  |                 |         |        |            | 121 ( <a href="#">Note 4</a> ) |

Note:

4. A 121Ω resistor is needed only when OCP behavior is set to Retry.



## 2. Specifications

### 2.1 Absolute Maximum Ratings

| Parameter  | Minimum       | Maximum               | Unit |
|--|---------------|-----------------------|------|
| VDD, PVCC, VSEN  | -0.3          | 7                     | V    |
| Module Input Voltage, VIN                                | -0.3          | 20                    | V    |
| Module Input Voltage, VIN1                               | -0.3          | 20                    | V    |
| 7VLDO  | -0.3          | 7.75                  | V    |
| BOOT Voltage (V <sub>BOOT-GND</sub> )                    | -0.3          | 30                    | V    |
| BOOT to PHASE Voltage (V <sub>BOOT-PHASE</sub> ) (DC)    | -0.3          | 7                     | V    |
| BOOT to PHASE Voltage (V <sub>BOOT-PHASE</sub> ) (<10ns) | -0.3          | 9                     | V    |
| PHASE Voltage  | -0.3          | 25                    | V    |
| PHASE Voltage (<20ns Pulse Width, 10μJ)                  | -9            | 25                    | V    |
| All Other Pins   | -0.3 to GND   | V <sub>DD</sub> + 0.3 | V    |
| ESD Rating   | Value         |                       | Unit |
| Human Body Model (Tested per JS-001-2017)                | 2             |                       | kV   |
| Charged Device Model (Tested per JS-002-2014)            | 750           |                       | V    |
| Machine Model (Tested per JESD22-A115C)                  | 200           |                       | V    |
| Latch-Up (Tested per JESD78E; Class 2, Level A)          | 100 at +125°C |                       | mA   |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

| Thermal Resistance (Typical)                    | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|----------------------|----------------------|
| 83 Ld HDA Module ( <a href="#">Notes 5, 6</a> ) | 16.8                 | 5.6                  |

Notes:

- $\theta_{JA}$  is measured in free air with the module mounted on a 6-layer thermal test board 3x3 inches in size with significant coverage of 2oz Cu on all layers, with numerous vias.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

| Parameter                  | Minimum                                  | Maximum | Unit |
|----------------------------|--|---------|------|
| Junction Temperature Range | -55                                      | +150    | °C   |
| Storage Temperature Range  | -65                                      | +150    | °C   |
| Pb-Free Reflow Profile     | See <a href="#">Figure 48 on page 38</a> |         |      |

### 2.3 Recommended Operating Conditions

| Parameter   | Minimum | Maximum | Unit |
|---|---------|---------|------|
| Junction Temperature Range  | -40     | +125    | °C   |
| Application Input Voltage, V <sub>IN</sub> , <a href="#">Figure 1</a> | 4.5     | 16.5    | V    |
| Output Voltage, V <sub>OUT</sub> , <a href="#">Figure 1</a>           | 0.5     | 5       | V    |
| Output Current, I <sub>OUT</sub> , <a href="#">Figure 1</a>           | 0       | 15      | A    |

## 2.4 Electrical Specifications

All typical specifications  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 12$ ,  $V_{IN1} = 12\text{V}$ ,  $V_{OUT} = 1\text{V}$ . **Boldface limits apply across the junction temperature range,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  (Note 7), unless otherwise stated.**

| Parameter  | Symbol                        | Test Conditions   | Min<br>(Note 7) | Typ  | Max<br>(Note 7) | Unit              |
|--|-------------------------------|---|-----------------|------|-----------------|-------------------|
| <b><math>V_{IN}</math> Supply</b>                                |                               |   |                 |      |                 |                   |
| Input Voltage Range  | $V_{IN}$                      |   | <b>4.5</b>      |      | <b>16.5</b>     | V                 |
| <b><math>V_{IN}</math> Supply Current</b>                        |                               |   |                 |      |                 |                   |
| Input Supply Current in PFM mode Operation                       | $I_{S(PFM)}$                  | PFM mode, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1\text{V}$ , $I_{OUT} = 0\text{A}$   |                 | 0.2  |                 | mA                |
| Input Supply Current in PWM mode Operation                       | $I_{S(PWM)}$                  | PWM mode, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1\text{V}$ , $I_{OUT} = 0\text{A}$   |                 | 35   |                 | mA                |
| Input Supply Current in PWM mode Operation                       | $I_{S(PWM)}$                  | PWM mode, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1\text{V}$ , $I_{OUT} = 15\text{A}$  |                 | 1.49 |                 | A                 |
| Input Supply Current in Shutdown                                 | $I_{S(SHUTDOWN)}$             | Shutdown  |                 | 0.05 |                 | $\mu\text{A}$     |
| <b><math>V_{IN1}</math> Supply Current</b>                       |                               |   |                 |      |                 |                   |
| Shutdown Current   | $I_{VIN1Q}$                   | EN = 0, PGOOD is floating, $V_{IN1} = 12\text{V}$   |                 | 14.5 | <b>17</b>       | mA                |
| Operating Current  | $I_{VIN1OP}$                  | PGOOD is floating, $V_{IN1} = 12\text{V}$   |                 | 19   | <b>25</b>       | mA                |
| <b><math>V_{DD}</math> and <math>V_{IN}</math> POR Threshold</b> |                               |   |                 |      |                 |                   |
| $V_{DD}$ , PVCC Rising POR Threshold Voltage                     |                               |   |                 | 4.2  | <b>4.35</b>     | V                 |
| $V_{DD}$ , PVCC Falling POR Threshold Voltage                    |                               |   | <b>3.8</b>      | 3.95 | <b>4.15</b>     | V                 |
| $V_{IN}$ , 7VLDO Rising POR Threshold Voltage                    |                               |   |                 | 4.2  | <b>4.35</b>     | V                 |
| $V_{IN}$ , 7VLDO Falling POR Threshold Voltage                   |                               |   | <b>3.8</b>      | 3.95 | <b>4.15</b>     | V                 |
| <b>Output Regulation</b>   |                               |   |                 |      |                 |                   |
| Output Continuous Current Range                                  | $I_{OUT}$                     | (Note 9)  | <b>0</b>        |      | <b>15</b>       | A                 |
| Output Voltage Range   | $V_{OUT\_RANGE}$              |   | <b>0.5</b>      |      | <b>5</b>        | V                 |
| Output Voltage Set-Point Accuracy                                |                               | $0.5\text{V} \leq V_{OUT} < 0.75\text{V}$ , Total variation with line, load, and temperature ( $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ ) | <b>-12.5</b>    |      | <b>12.5</b>     | mV                |
| Output Voltage Set-Point Accuracy                                |                               | $0.75\text{V} \leq V_{OUT} < 0.9\text{V}$ , Total variation with line, load, and temperature ( $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ ) | <b>-15</b>      |      | <b>15</b>       | mV                |
| Output Voltage Set-Point Accuracy                                |                               | $0.9\text{V} \leq V_{OUT} \leq 5\text{V}$ , Total variation with line, load, and temperature ( $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ ) | <b>-1.5</b>     |      | <b>1.5</b>      | %                 |
| Line Regulation  | $\Delta V_{OUT}/V_{OUT\_SET}$ | $V_{OUT} = 1\text{V}$ , $V_{IN}$ from 4.5V to 16.5V, $I_L = 0\text{A}$  | <b>-1.2</b>     |      | <b>1.2</b>      | %                 |
|  |                               | $V_{OUT} = 1.8\text{V}$ , $V_{IN}$ from 4.5V to 16.5V, $I_L = 0\text{A}$  | <b>-1.2</b>     |      | <b>1.2</b>      | %                 |
| Load Regulation  | $\Delta V_{OUT}/V_{OUT\_SET}$ | From 0A to 15A, $V_{IN} = 5\text{V}/12\text{V}$ , $V_{OUT} = 1\text{V}$   | <b>-1.2</b>     |      | <b>1.2</b>      | %                 |
|  |                               | From 0A to 15A, $V_{IN} = 5\text{V}/12\text{V}$ , $V_{OUT} = 1.8\text{V}$   | <b>-1.2</b>     |      | <b>1.2</b>      | %                 |
| Output Ripple Voltage  | $V_{OUT(AC)}$                 | $V_{IN} = 12\text{V}$ , $V_{OUT} = 1\text{V}$ , $I_{OUT} = 15\text{A}$ , 4x220 $\mu\text{F}$ ceramic capacitor  |                 | 8    |                 | mV <sub>P-P</sub> |

All typical specifications  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 12$ ,  $V_{IN1} = 12\text{V}$ ,  $V_{OUT} = 1\text{V}$ . **Boldface limits apply across the junction temperature range,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  (Note 7), unless otherwise stated. (Continued)**

| Parameter                              | Symbol        | Test Conditions   | Min<br>(Note 7) | Typ   | Max<br>(Note 7) | Unit                    |
|--|---------------|---|-----------------|-------|-----------------|-------------------------|
| <b>Dynamic Characteristics</b>         |               |   |                 |       |                 |                         |
| Voltage Change of Positive Load Step   | $V_{OUT\_DP}$ | Current slew rate = $2.5\text{A}/\mu\text{s}$ , $V_{IN} = 12\text{V}$ ,<br>4x220 $\mu\text{F}$ ceramic capacitor<br>$V_{OUT} = 1\text{V}$ , $I_{OUT}$ from 0A to 7.5A |                 | 10    |                 | mV                      |
| Voltage Change of Negative Load Step   | $V_{OUT\_DN}$ | Current slew rate = $2.5\text{A}/\mu\text{s}$ , $V_{IN} = 12\text{V}$ ,<br>4x220 $\mu\text{F}$ ceramic capacitor<br>$V_{OUT} = 1\text{V}$ , $I_{OUT}$ from 7.5A to 0A |                 | 10    |                 | mV                      |
| <b>Enable Input</b>                    |               |   |                 |       |                 |                         |
| EN High Threshold Voltage              | $V_{ENTHR}$   |   | <b>0.81</b>     | 0.84  | <b>0.87</b>     | V                       |
| EN Low Threshold Voltage               | $V_{ENTHF}$   |   | <b>0.71</b>     | 0.76  | <b>0.81</b>     | V                       |
| <b>Channel Frequency</b>               |               |   |                 |       |                 |                         |
| 300kHz Configuration                   |               | PWM Mode  | <b>255</b>      | 300   | <b>340</b>      | kHz                     |
| 400kHz Configuration                   |               |   | <b>340</b>      | 400   | <b>455</b>      | kHz                     |
| 500kHz Configuration                   |               |   | <b>425</b>      | 500   | <b>565</b>      | kHz                     |
| 600kHz Configuration                   |               |   | <b>510</b>      | 600   | <b>680</b>      | kHz                     |
| 700kHz Configuration                   |               |   | <b>600</b>      | 700   | <b>790</b>      | kHz                     |
| 850kHz Configuration                   |               |   | <b>720</b>      | 850   | <b>960</b>      | kHz                     |
| 1000kHz Configuration                  |               |   | <b>855</b>      | 1000  | <b>1130</b>     | kHz                     |
| <b>Soft-Start</b>                      |               |   |                 |       |                 |                         |
| SS Rate = $0.157\text{mV}/\mu\text{s}$ |               |   | <b>0.125</b>    | 0.157 | <b>0.18</b>     | $\text{mV}/\mu\text{s}$ |
| SS Rate = $0.315\text{mV}/\mu\text{s}$ |               |   | <b>0.25</b>     | 0.315 | <b>0.37</b>     | $\text{mV}/\mu\text{s}$ |
| SS Rate = $0.625\text{mV}/\mu\text{s}$ |               |   | <b>0.52</b>     | 0.625 | <b>0.7</b>      | $\text{mV}/\mu\text{s}$ |
| SS Rate = $1.25\text{mV}/\mu\text{s}$  |               |   | <b>1</b>        | 1.25  | <b>1.4</b>      | $\text{mV}/\mu\text{s}$ |
| SS Rate = $2.5\text{mV}/\mu\text{s}$   |               |   | <b>2</b>        | 2.5   | <b>2.8</b>      | $\text{mV}/\mu\text{s}$ |
| SS Rate = $5\text{mV}/\mu\text{s}$     |               |   | <b>4.1</b>      | 5     | <b>5.6</b>      | $\text{mV}/\mu\text{s}$ |
| SS Rate = $10\text{mV}/\mu\text{s}$    |               |   | <b>8.4</b>      | 10    | <b>10.9</b>     | $\text{mV}/\mu\text{s}$ |
| Soft-Start Delay from Enable High      |               | Excluding 5.5ms POR timeout   | <b>140</b>      | 200   | <b>260</b>      | $\mu\text{s}$           |
| <b>Remote Sense</b>                    |               |   |                 |       |                 |                         |
| Bias Current of VSEN and RGND Pins     |               |   |                 |       | <b>250</b>      | $\mu\text{A}$           |
| Maximum Differential Input Voltage     |               |   | <b>5.8</b>      |       |                 | V                       |
| <b>Power-Good</b>                      |               |   |                 |       |                 |                         |
| PGOOD Pull-Down Impedance              | $R_{PG}$      | PGOOD = 5mA sink  |                 | 10    | <b>50</b>       | $\Omega$                |
| PGOOD Leakage Current                  | $I_{PG}$      | PGOOD = 5V  |                 |       | <b>1</b>        | $\mu\text{A}$           |
| <b>LDOs</b>                            |               |   |                 |       |                 |                         |
| 5V LDO Regulation                      |               | $V_{IN} = 12\text{V}$ , 5V LDO load = 50mA  | <b>4.8</b>      | 5     | <b>5.15</b>     | V                       |
| 5V LDO Regulation                      |               | $V_{IN} = 4.75\text{V}$ , 5V LDO load = 50mA  | <b>4.15</b>     |       |                 | V                       |
| 5V LDO Maximum Load Capability         |               |   | <b>100</b>      |       |                 | mA                      |
| 7V LDO Regulation                      |               | 7V LDO 250 $\mu\text{A}$ load   | <b>7.15</b>     | 7.4   | <b>7.5</b>      | V                       |
| 7V Dropout                             |               | $V_{IN} = 4.75\text{V}$ , 7V LDO 250 $\mu\text{A}$ load   | <b>4.3</b>      |       |                 | V                       |
| 7V LDO Current Capability              |               | Not recommended for external use  | <b>2</b>        |       |                 | mA                      |

All typical specifications  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 12$ ,  $V_{IN1} = 12\text{V}$ ,  $V_{OUT} = 1\text{V}$ . **Boldface limits apply across the junction temperature range,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  (Note 7), unless otherwise stated. (Continued)**

| Parameter                                 | Symbol      | Test Conditions  | Min<br>(Note 7) | Typ   | Max<br>(Note 7) | Unit        |
|---|-------------|--|-----------------|-------|-----------------|-------------|
| <b>Current Sense</b>                      |             |  |                 |       |                 |             |
| OCP                                       | $I_{OCP}$   | $V_{IN} = 12\text{V}$ , $V_{OUT} = 1\text{V}$          | <b>15</b>       | 18.8  |                 | A           |
| Maximum Common-Mode Input Voltage         |             | $7\text{VLDO} = 7.4\text{V}$                           | <b>5.7</b>      |       |                 | V           |
|   |             | $V_{DD} = \text{PV}_{CC} = 7\text{VLDO} = 4.5\text{V}$ | <b>2.8</b>      |       |                 | V           |
| <b>Fault Protection</b>                   |             |  |                 |       |                 |             |
| UVP Threshold Voltage                     |             | $0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$            | <b>67</b>       | 74    | <b>88</b>       | $\%V_{OUT}$ |
|   |             | $0.7\text{V} \leq V_{OUT} < 1\text{V}$                 | <b>68</b>       | 74    | <b>85</b>       | $\%V_{OUT}$ |
|   |             | $1\text{V} \leq V_{OUT} < 1.5\text{V}$                 | <b>68</b>       | 74    | <b>82</b>       | $\%V_{OUT}$ |
|   |             | $1.5\text{V} \leq V_{OUT} \leq 5\text{V}$              | <b>68</b>       | 74    | <b>80</b>       | $\%V_{OUT}$ |
| Start-Up OVP Threshold Voltage            |             | $0\text{V} \leq V_{OUT} \leq 1.08\text{V}$             | <b>1.1</b>      | 1.15  | <b>1.25</b>     | V           |
|   |             | $1.08\text{V} < V_{OUT} \leq 1.55\text{V}$             | <b>1.58</b>     | 1.65  | <b>1.75</b>     | V           |
|   |             | $1.55\text{V} < V_{OUT} \leq 1.85\text{V}$             | <b>1.88</b>     | 1.95  | <b>2.05</b>     | V           |
|   |             | $1.85\text{V} < V_{OUT} \leq 2.08\text{V}$             | <b>2.09</b>     | 2.15  | <b>2.25</b>     | V           |
|   |             | $2.08\text{V} < V_{OUT} \leq 2.53\text{V}$             | <b>2.56</b>     | 2.65  | <b>2.75</b>     | V           |
|   |             | $2.53\text{V} < V_{OUT} \leq 3.33\text{V}$             | <b>3.36</b>     | 3.45  | <b>3.6</b>      | V           |
|   |             | $3.33\text{V} < V_{OUT} \leq 5\text{V}$                | <b>5.52</b>     | 5.65  | <b>5.85</b>     | V           |
| Start-Up OVP Hysteresis                   |             |  |                 | 100   |                 | mV          |
| OVP Rising Threshold Voltage              | $V_{OVRTH}$ | $0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$            | <b>111</b>      | 120   | <b>136</b>      | $\%V_{OUT}$ |
|   |             | $0.7\text{V} \leq V_{OUT} < 1\text{V}$                 | <b>113</b>      | 120   | <b>132</b>      | $\%V_{OUT}$ |
|   |             | $1\text{V} \leq V_{OUT} < 1.5\text{V}$                 | <b>114</b>      | 120   | <b>128</b>      | $\%V_{OUT}$ |
|   |             | $1.5\text{V} \leq V_{OUT} \leq 5\text{V}$              | <b>114</b>      | 120   | <b>127</b>      | $\%V_{OUT}$ |
| OVP Falling Threshold Voltage             | $V_{OVFTH}$ | $0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$            | <b>93</b>       | 100   | <b>115</b>      | $\%V_{OUT}$ |
|   |             | $0.7\text{V} \leq V_{OUT} < 1\text{V}$                 | <b>95</b>       | 100   | <b>111</b>      | $\%V_{OUT}$ |
|   |             | $1\text{V} \leq V_{OUT} < 1.5\text{V}$                 | <b>96</b>       | 100   | <b>109</b>      | $\%V_{OUT}$ |
|   |             | $1.5\text{V} \leq V_{OUT} \leq 5\text{V}$              | <b>96</b>       | 100   | <b>108</b>      | $\%V_{OUT}$ |
| Over-Temperature Shutdown Threshold       |             | $22.31\%V_{DD}$ ( $\sim +136^\circ\text{C}$ )          | <b>20</b>       | 22.31 | <b>26</b>       | $\%V_{DD}$  |
| Over-Temperature Shutdown Reset Threshold |             | $27.79\%V_{DD}$ ( $\sim +122^\circ\text{C}$ )          | <b>25</b>       | 27.79 | <b>30</b>       | $\%V_{DD}$  |

Notes:

- The ISL8212M is tested under pulsed-load conditions such that  $T_J \approx T_A$ .
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- See output current derating curves for different  $V_{OUT}$  and  $T_A$  located in "[Derating Curves](#)" on page 18.
- See [Table 2 on page 7](#).

### 3. Typical Performance Curves

#### 3.1 Efficiency Performance

Operating conditions:  $T_A=25^{\circ}\text{C}$ , no air flow, PWM mode. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 7](#).

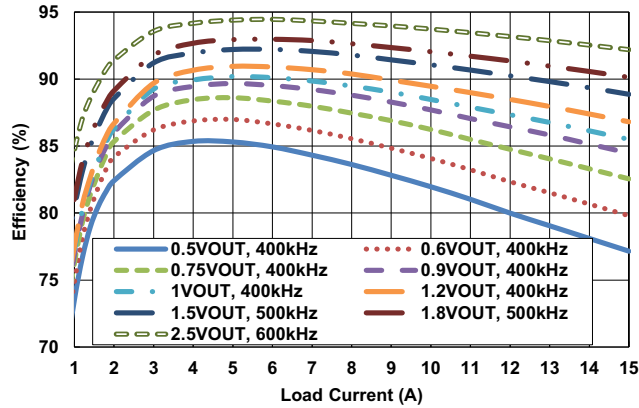


Figure 3. Efficiency vs Load Current at 5V<sub>IN</sub> (PWM)

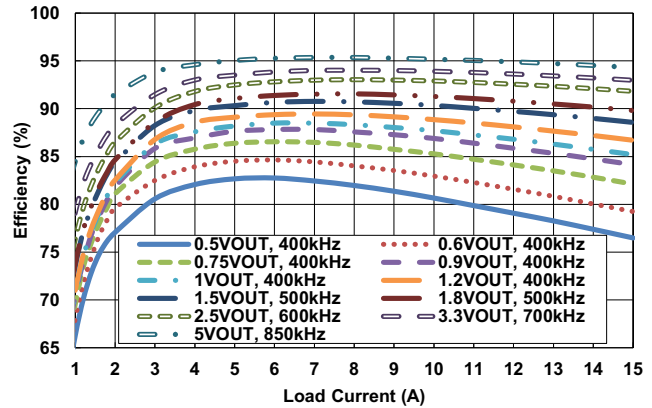


Figure 4. Efficiency vs Load Current at 8V<sub>IN</sub> (PWM)

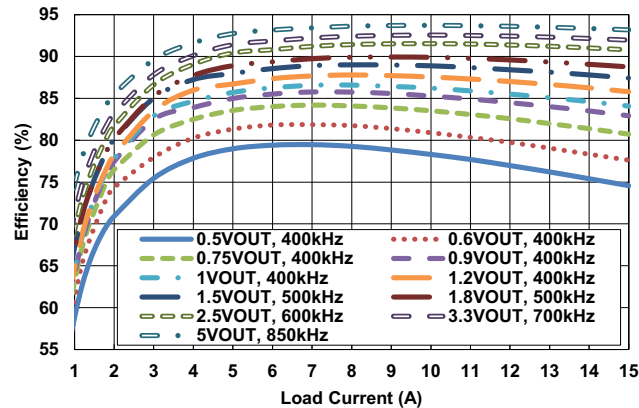


Figure 5. Efficiency vs Load Current at 12V<sub>IN</sub> (PWM)

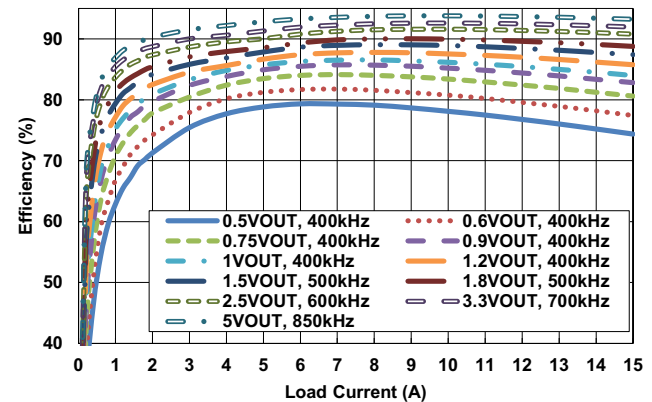


Figure 6. Efficiency vs Load Current at 12V<sub>IN</sub> (PFM)

### 3.2 Output Voltage Ripple

Operating conditions:  $T_A = +25^\circ\text{C}$ , no air flow, PWM mode,  $C_{OUT} = 4 \times 220\mu\text{F}$  Ceramic,  $RR = 200\text{k}\Omega$ . Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 7](#).

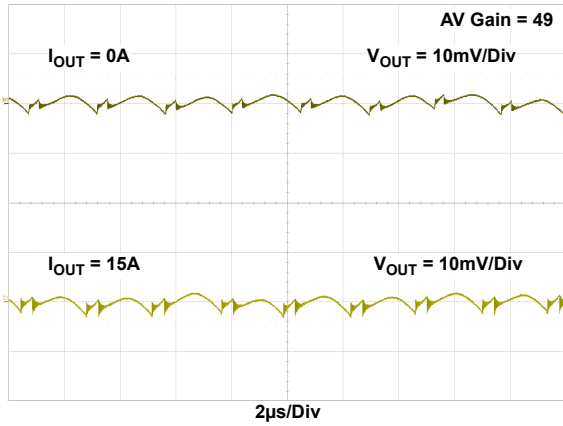


Figure 7. Output Ripple at  $5V_{IN}$  and  $0.75V_{OUT}$ , 400kHz

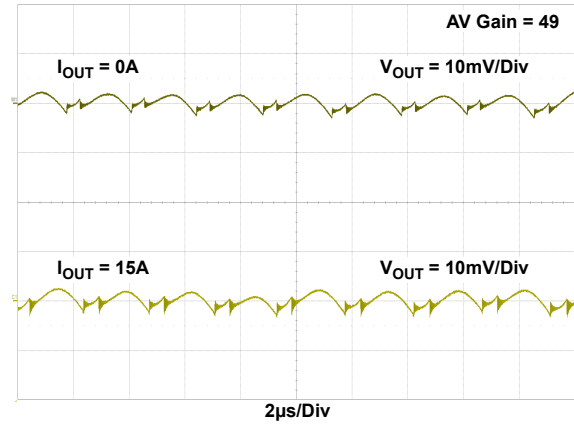


Figure 8. Output Ripple at  $5V_{IN}$  and  $1V_{OUT}$ , 400kHz

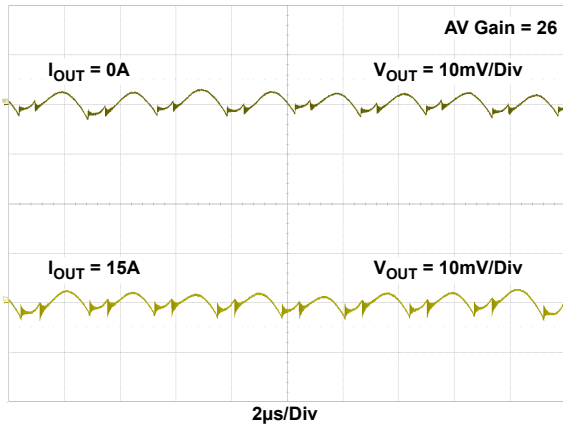


Figure 9. Output Ripple at  $5V_{IN}$  and  $1.2V_{OUT}$ , 400kHz

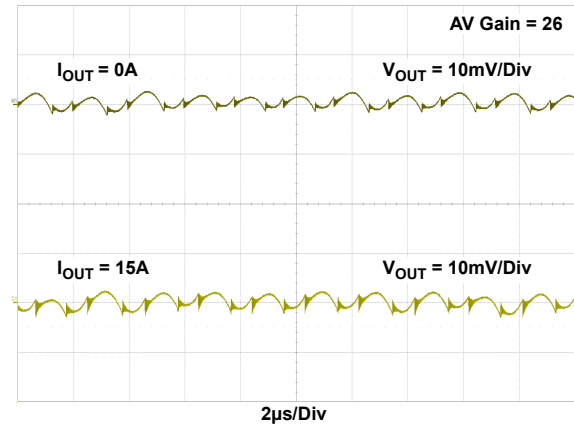


Figure 10. Output Ripple at  $5V_{IN}$  and  $1.8V_{OUT}$ , 500kHz

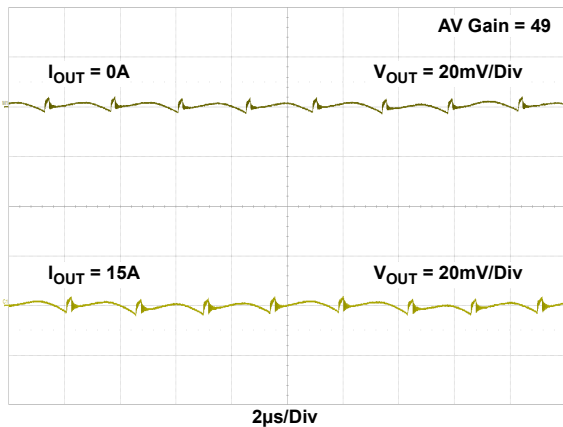


Figure 11. Output Ripple at  $12V_{IN}$  and  $0.75V_{OUT}$ , 400kHz

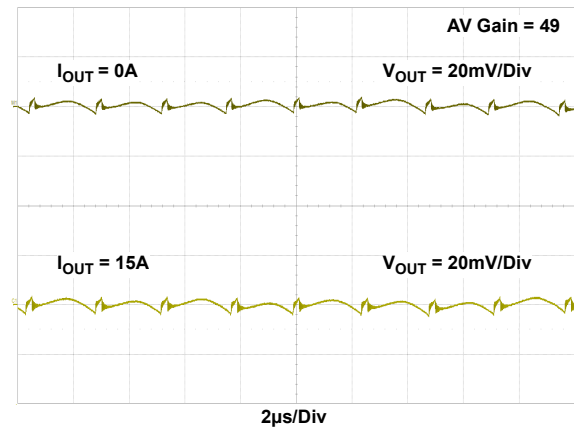


Figure 12. Output Ripple at  $12V_{IN}$  and  $1V_{OUT}$ , 400kHz

Operating conditions:  $T_A = +25^\circ\text{C}$ , no air flow, PWM mode,  $C_{OUT} = 4 \times 220\mu\text{F}$  Ceramic,  $RR = 200\text{k}\Omega$ . Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 7](#). (Continued)

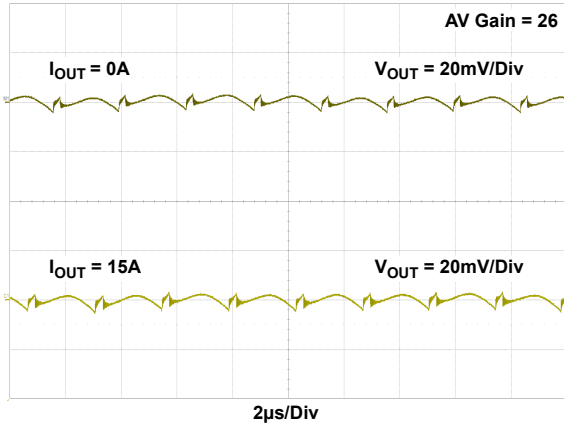


Figure 13. Output Ripple at  $12V_{IN}$  and  $1.2V_{OUT}$ , 400kHz

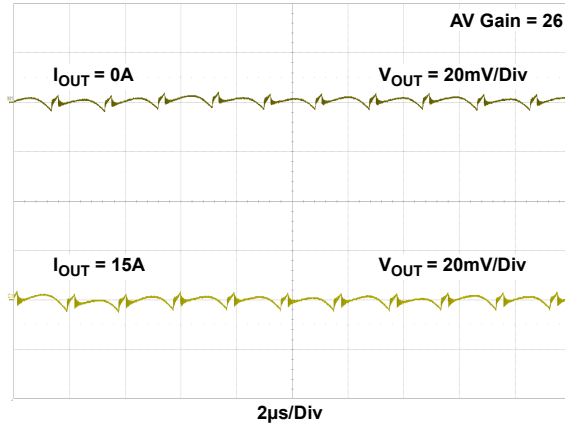


Figure 14. Output Ripple at  $12V_{IN}$  and  $1.5V_{OUT}$ , 500kHz

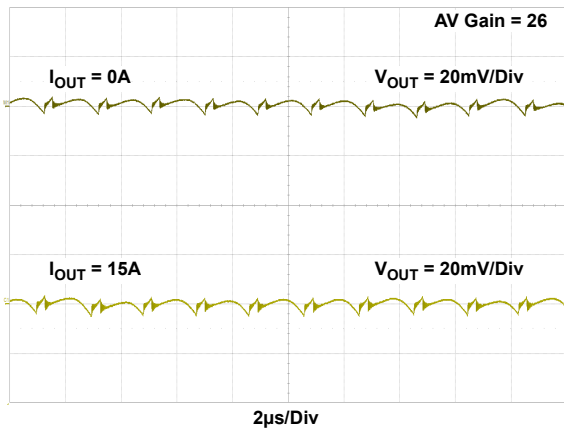


Figure 15. Output Ripple at  $12V_{IN}$  and  $1.8V_{OUT}$ , 500kHz

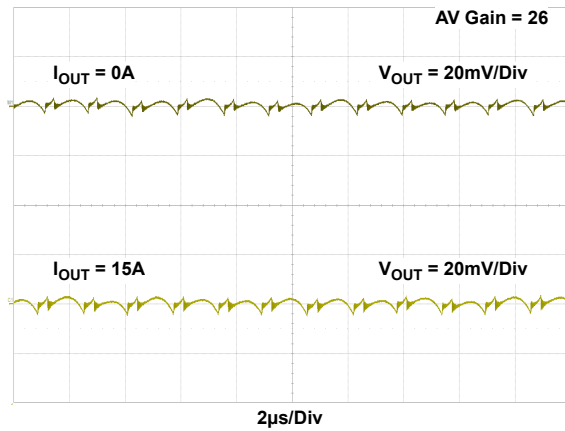


Figure 16. Output Ripple at  $12V_{IN}$  and  $2.5V_{OUT}$ , 600kHz

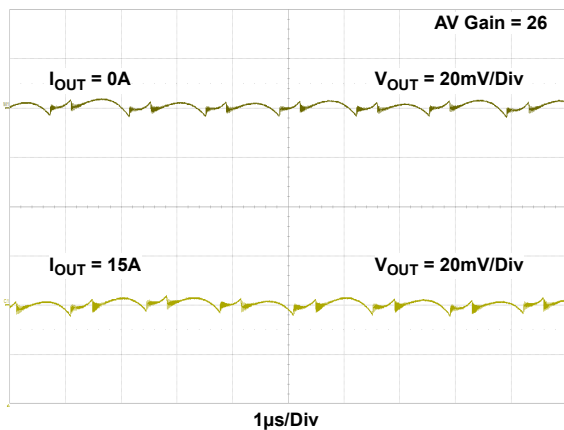


Figure 17. Output Ripple at  $12V_{IN}$  and  $3.3V_{OUT}$ , 700kHz

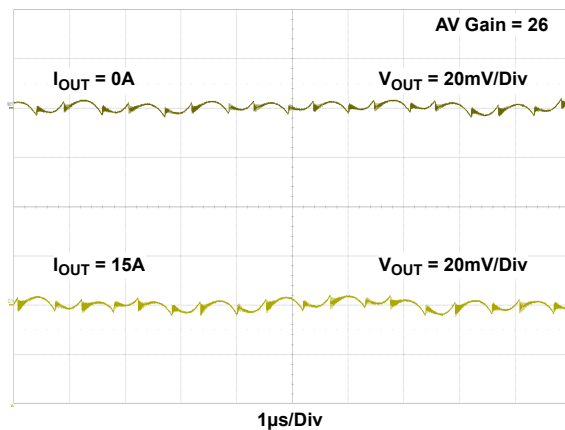


Figure 18. Output Ripple at  $12V_{IN}$  and  $5V_{OUT}$ , 850kHz

### 3.3 Load Transient Response Performance

Operating conditions:  $T_A = +25^\circ\text{C}$ , no air flow,  $V_{IN} = 12\text{V}$ , PWM mode,  $C_{OUT} = 4 \times 220\mu\text{F}$  Ceramic, 0A to 7.5A step load at  $7.5\text{A}/\mu\text{s}$  slew rate,  $RR = 200\text{k}\Omega$ . Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 7](#).

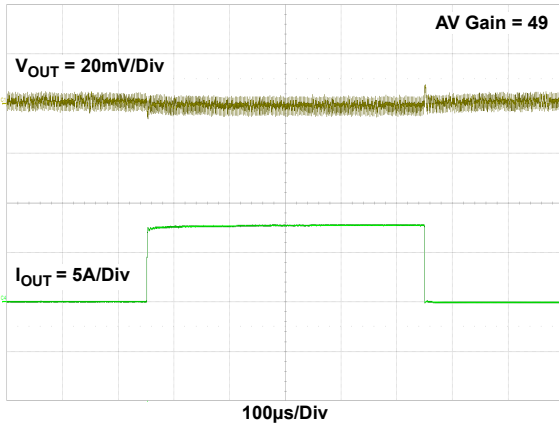


Figure 19. Load Transient Response at  $0.75V_{OUT}$ , 400kHz

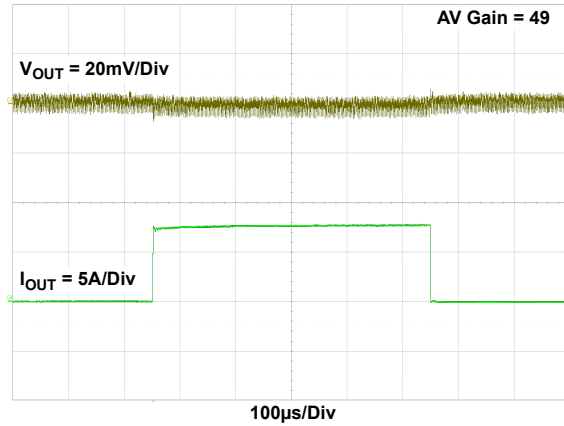


Figure 20. Load Transient Response at  $1V_{OUT}$ , 400kHz

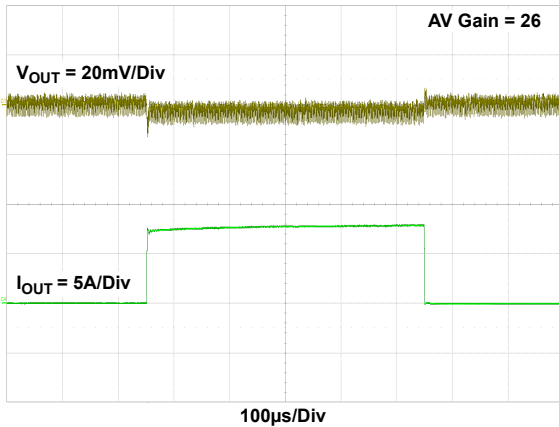


Figure 21. Load Transient Response at  $1.8V_{OUT}$ , 500kHz

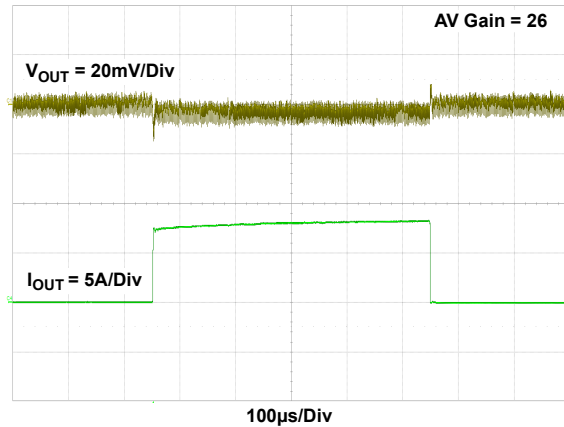


Figure 22. Load Transient Response at  $2.5V_{OUT}$ , 600kHz

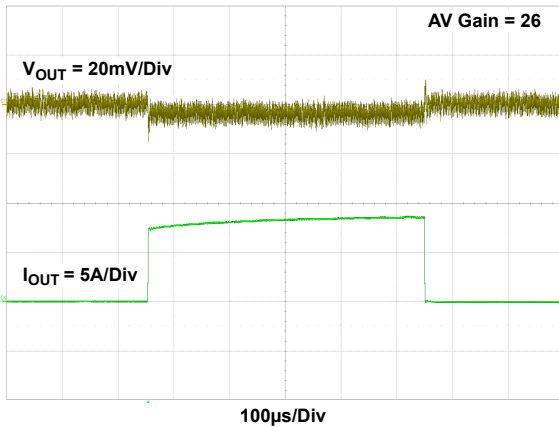


Figure 23. Load Transient Response at  $3.3V_{OUT}$ , 700kHz

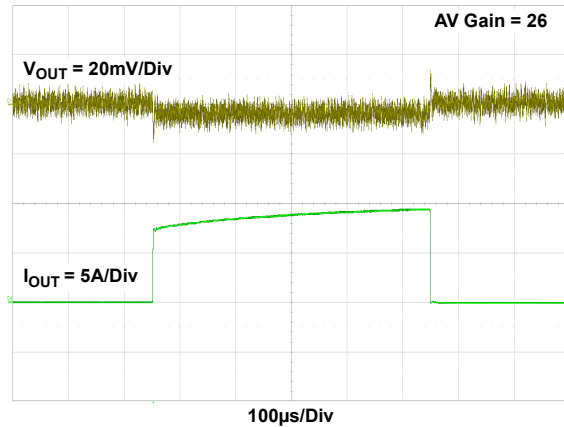


Figure 24. Load Transient Response at  $5V_{OUT}$ , 850kHz



### 3.4 Start-Up and Shutdown

Operating conditions:  $T_A = +25^\circ\text{C}$ , no air flow,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1\text{V}$ , PWM mode. Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 7](#).

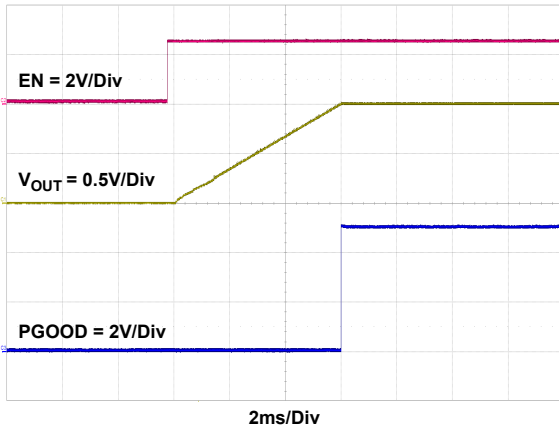


Figure 25. Start-Up Waveform,  $I_{OUT} = 0\text{A}$

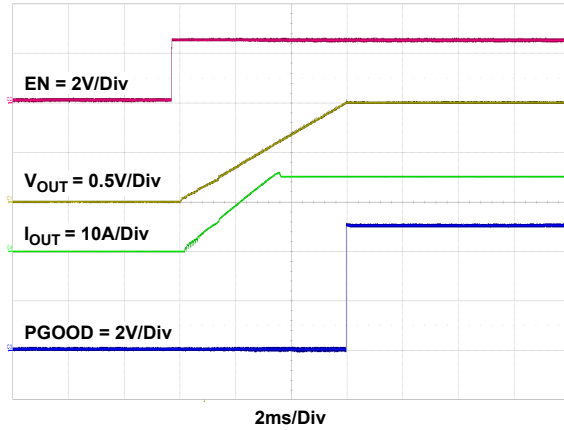


Figure 26. Start-Up Waveform,  $I_{OUT} = 15\text{A}$

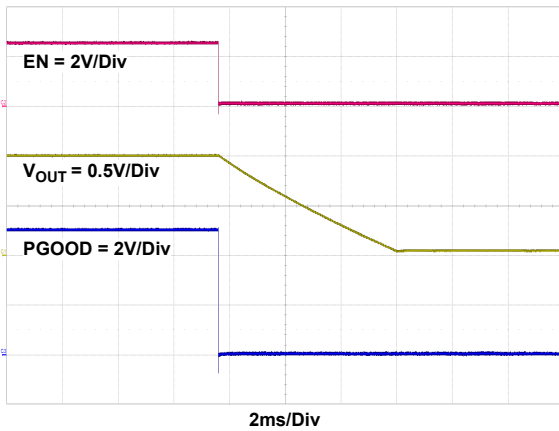


Figure 27. Shutdown Waveform,  $I_{OUT} = 0\text{A}$

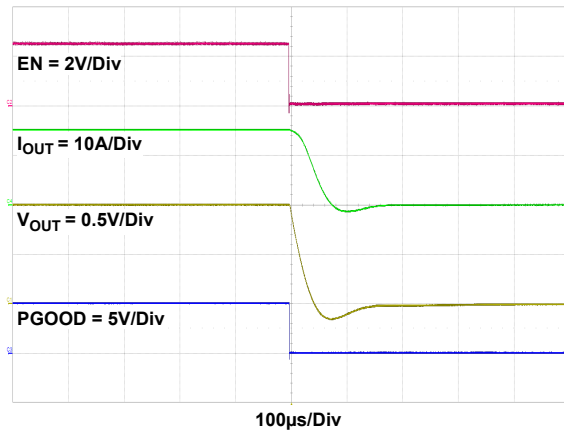


Figure 28. Shutdown Waveform,  $I_{OUT} = 15\text{A}$

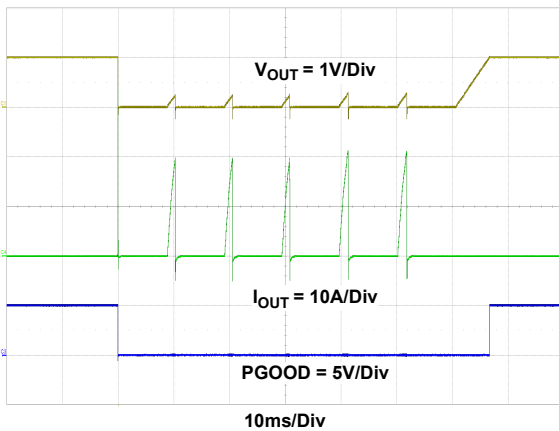


Figure 29. OCP Response; Output Short-Circuited from No Load to Ground and Released,  $I_{OUT} = 0\text{A}$

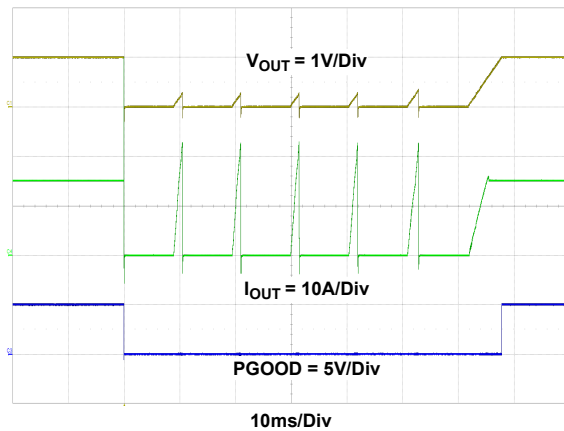


Figure 30. OCP Response; Output Short-Circuited from No Load to Ground and Released,  $I_{OUT} = 15\text{A}$

### 3.5 Derating Curves

Operating conditions:  $V_{IN} = 12V$ , PWM mode. All of the following curves were plotted at  $T_J = +125^{\circ}C$ . The derating curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 7](#).

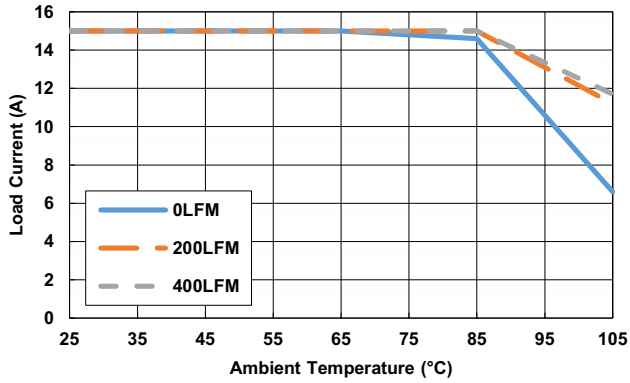


Figure 31. 0.6V<sub>OUT</sub>

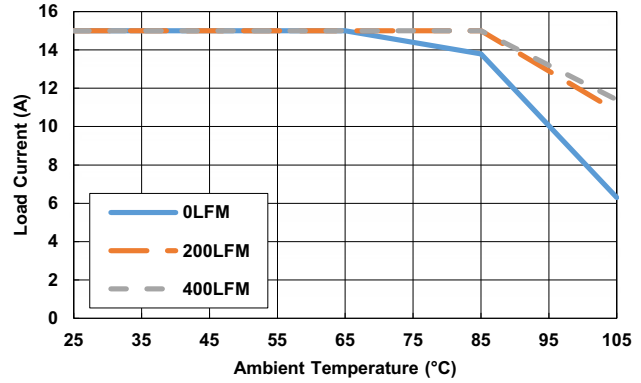


Figure 32. 0.8V<sub>OUT</sub>

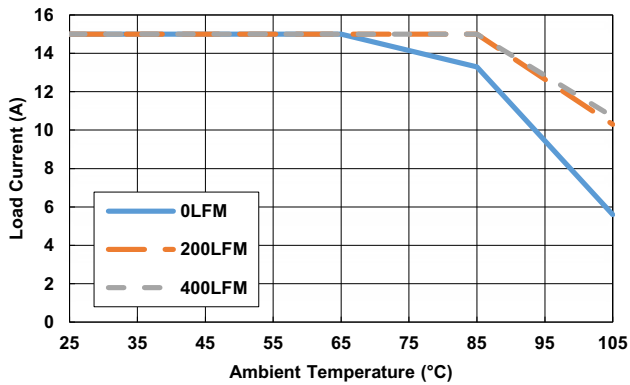


Figure 33. 1V<sub>OUT</sub>

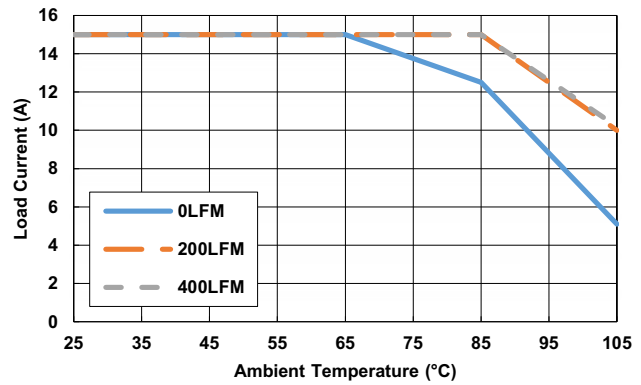


Figure 34. 1.2V<sub>OUT</sub>

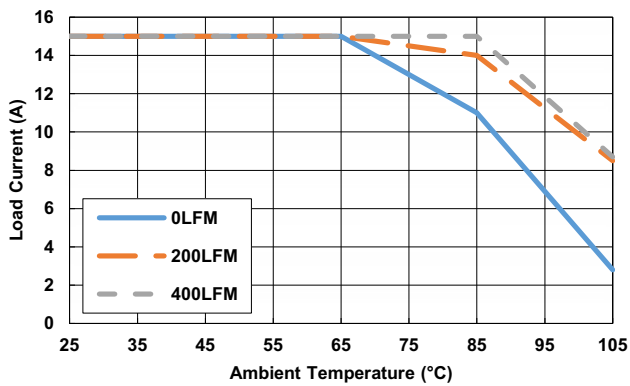


Figure 35. 1.8V<sub>OUT</sub>

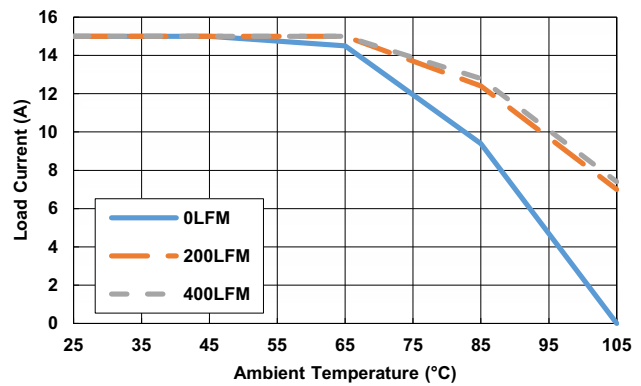


Figure 36. 2.5V<sub>OUT</sub>

Operating conditions:  $V_{IN} = 12V$ , PWM mode. All of the following curves were plotted at  $T_J = +125^{\circ}C$ . The derating curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 7](#). (Continued)

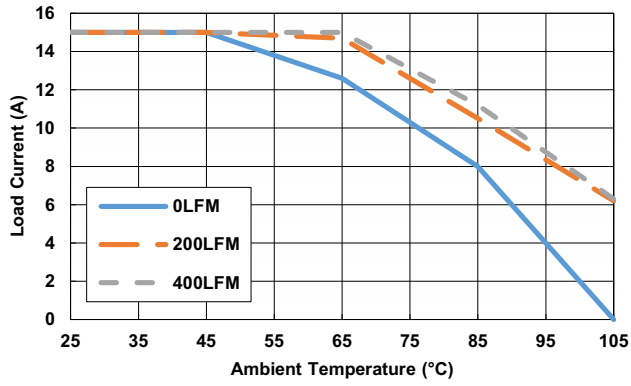


Figure 37. 3.3V<sub>OUT</sub>

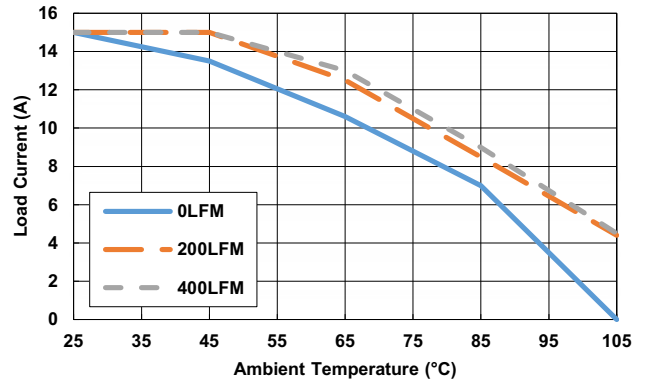


Figure 38. 5V<sub>OUT</sub>

## 4. Operating the ISL8212M

The following sections describe the operation of the ISL8212M.

### 4.1 Configuring Internal Bias and LDO

The ISL8212M has four bias pins: VIN1, 7VLDO, PVCC, and VDD. The PVCC and 7VLDO voltage rails are 5V LDO and 7V LDO supplied by VIN1, respectively, while the VDD pin needs to connect to the PVCC rail externally to be biased.

### 4.2 Enabling and Disabling the ISL8212M

The module is enabled until the 7VLDO, PVCC, VDD, VIN1, and EN pins increase above their respective rising threshold voltages and the typical 5.5ms timeout expires (worst case = 6.5ms). The module becomes disabled when the 7VLDO, PVCC, VDD, VIN, or EN pins drop below their respective falling POR threshold voltages.

The precision threshold EN pin allows you to set a precision input UVLO level with an external resistor divider, as shown in [Figure 39](#).

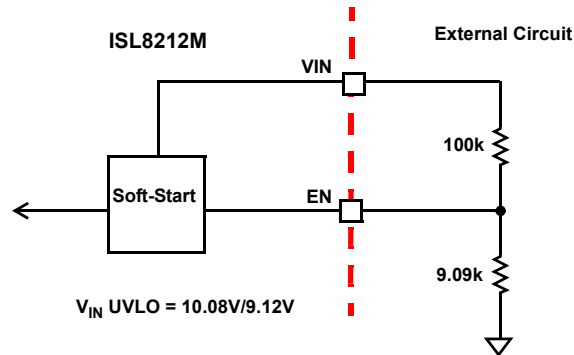


Figure 39. Input UVP Configuration

For 5V input applications or wide range input applications, the EN pin can directly connect to VDD, as shown in [Figure 40](#). If an external enable control signal is available and is an open-drain signal, a pull-up impedance (100k or higher) can be used to connect the pull-up resistor to VDD.

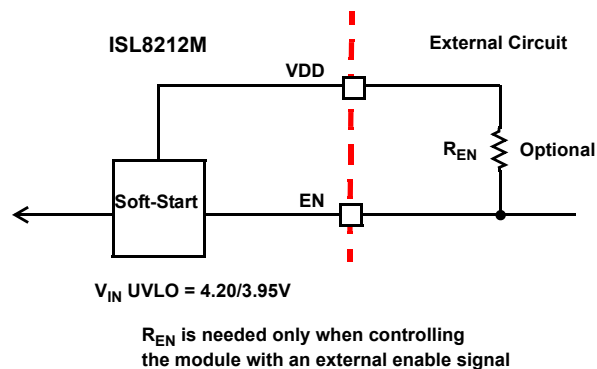


Figure 40. 5V Input or Wide Range Input Configuration

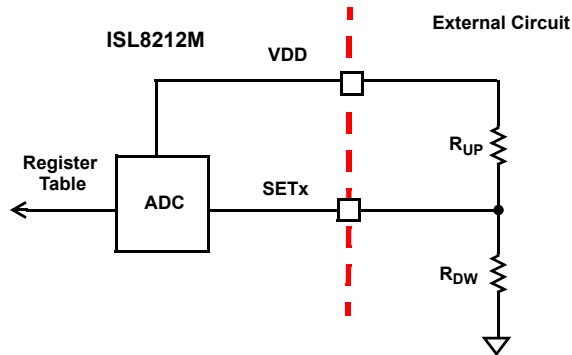
### 4.3 Setting Up Resistors

The ISL8212M offers four setting up pins (SETx) to customize module specifications. The details of these pins are summarized in [Table 3](#), followed by a detailed description of resistor reader operation.

**Table 3. Definition of SET Pins**

| Pin  | Name                     | Description   |
|------|--------------------------|---|
| SET1 | Output Voltage           | Sets the 256 output voltage options: 0V, 0.5V to 5V (see <a href="#">Table 9</a> ). |
| SET2 | PWM/PFM                  | Enables PFM mode or forced PWM.   |
|      | Temperature Compensation | Adjusts NTC temperature compensation: OFF, +5°C, +15°C, +30°C.                      |
|      | Not Used                 | Not used  |
| SET3 | uSPFM                    | Ultrasonic (25kHz clamp) PFM enable.  |
|      | Fault Behavior           | OCP fault behavior:<br>Latch, Infinite 9ms retry.                                   |
|      | FSW                      | Sets/Selects the switching frequency ( $f_{SW}$ ).                                  |
|      | AV Gain                  | Sets/Selects the error amplifier gain (AV).   |
| SET4 | RAMP_RATE                | Sets/Selects the soft-start ramp rate.  |
|      | RR                       | Sets/Selects the RR impedance for R4 loop.  |
|      | AVMLTI                   | Sets/Selects the AV Gain Multiplier (1x or 2x).                                     |
|      | Not Used                 | Not used  |

Renesas has developed a high resolution ADC using a patented technique with a simple 1%, 100ppm/K or better temperature coefficient resistor divider. Renesas recommends using the same type of resistor in the design so the ADC has similar change over temperature. The divider is compared to the internal divider off VDD and SGND nodes and therefore must refer to the VDD and SGND pins, not through any RC decoupling network.



**Figure 41. Simplified Resistor Divider ADC**

[Tables 4](#) through [7](#) show the  $R_{UP}$  and  $R_{DW}$  values of each pin for a specific system design with some tie-high and tie-low options that enable easy programming with reduced resistors. You can use the tie-high and tie-low options to validate the module operation during In-Circuit Test (ICT) for 0V output voltage option.

**Note:** More options are described in the [ISL8212MEVAL1Z User's Manual](#) and the case of 10kΩ tie-high or tie-low is equivalent to 0Ω tie-high or tie-low.

Table 4. SET1 Resistor Reader Example

| $R_{UP}$ (k $\Omega$ ) | $R_{DW}$ (k $\Omega$ ) | $V_{OUT}$ (V) |
|------------------------|------------------------|---------------|
| 499                    | Open                   | 0.000         |
| 49.9                   | 12.4                   | 0.5           |
| 23.2                   | 17.8                   | 0.594         |
| 22.1                   | 18.2                   | 0.602         |
| 97.6                   | 27.4                   | 0.742         |
| 90.9                   | 28.7                   | 0.75          |
| 82.5                   | 28.7                   | 0.758         |
| Open                   | 34.8                   | 0.898         |
| 34                     | 57.6                   | 0.906         |
| 133                    | 46.4                   | 0.992         |
| Open                   | 75                     | 1.000         |
| 118                    | 49.9                   | 1.008         |
| 45.3                   | 150                    | 1.195         |
| Open                   | 499                    | 1.203         |
| 221                    | 113                    | 1.492         |
| 21.5                   | Open                   | 1.500         |
| 200                    | 121                    | 1.508         |
| 34.8                   | Open                   | 1.797         |
| 196                    | 226                    | 1.805         |
| 576                    | 200                    | 2.492         |
| 52.3                   | Open                   | 2.500         |
| 499                    | 210                    | 2.508         |
| 105                    | Open                   | 3.297         |
| 249                    | 357                    | 3.305         |
| 374                    | 422                    | 4.992         |
| 147                    | Open                   | 5.000         |
| 348                    | 464                    | 5.008         |

Table 5. SET2 Resistor Reader Example

| $R_{UP}$ (k $\Omega$ ) | $R_{DW}$ (k $\Omega$ ) | PWM/PFM  | Temp Comp |
|------------------------|------------------------|----------|-----------|
| Open                   | 0                      | Enabled  | 30        |
| Open                   | 21.5                   | Enabled  | 15        |
| Open                   | 34.8                   | Enabled  | 5         |
| Open                   | 52.3                   | Enabled  | OFF       |
| Open                   | 75                     | Disabled | 30        |
| Open                   | 105                    | Disabled | 15        |
| Open                   | 147                    | Disabled | 5         |
| Open                   | 499                    | Disabled | OFF       |

Table 6. SET3 Resistor Reader Example

| R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) | Ultrasonic PFM | OCP and Short-Circuit Behavior | f <sub>SW</sub> (kHz) | AV Gain |    |
|----------------------|----------------------|----------------|--------------------------------|-----------------------|---------|----|
|                      |                      |                |                                |                       | 1x      | 2x |
| 25.5                 | 16.5                 | Disabled       | Retry                          | 400                   | 24.5    | 49 |
| 88.7                 | 57.6                 | Disabled       | Latch                          | 400                   | 24.5    | 49 |
| 374                  | 243                  | Enabled        | Latch                          | 400                   | 24.5    | 49 |
| 191                  | 124                  | Enabled        | Retry                          | 400                   | 24.5    | 49 |
| 23.2                 | 17.8                 | Disabled       | Retry                          | 400                   | 13      | 26 |
| 80.6                 | 61.9                 | Disabled       | Latch                          | 400                   | 13      | 26 |
| 340                  | 261                  | Enabled        | Latch                          | 400                   | 13      | 26 |
| 174                  | 133                  | Enabled        | Retry                          | 400                   | 13      | 26 |
| 16.9                 | 24.3                 | Disabled       | Retry                          | 500                   | 13      | 26 |
| 59                   | 84.5                 | Disabled       | Latch                          | 500                   | 13      | 26 |
| 249                  | 357                  | Enabled        | Latch                          | 500                   | 13      | 26 |
| 127                  | 182                  | Enabled        | Retry                          | 500                   | 13      | 26 |
| 13.3                 | 39.2                 | Disabled       | Retry                          | 600                   | 13      | 26 |
| 46.4                 | 137                  | Disabled       | Latch                          | 600                   | 13      | 26 |
| 196                  | 576                  | Enabled        | Latch                          | 600                   | 13      | 26 |
| 100                  | 294                  | Enabled        | Retry                          | 600                   | 13      | 26 |
| 76.8                 | 29.4                 | Disabled       | Retry                          | 700                   | 13      | 26 |
| 187                  | 71.5                 | Disabled       | Latch                          | 700                   | 13      | 26 |
| 715                  | 274                  | Enabled        | Latch                          | 700                   | 13      | 26 |
| 374                  | 143                  | Enabled        | Retry                          | 700                   | 13      | 26 |
| 49.9                 | 38.3                 | Disabled       | Retry                          | 850                   | 13      | 26 |
| 121                  | 93.1                 | Disabled       | Latch                          | 850                   | 13      | 26 |
| 464                  | 357                  | Enabled        | Latch                          | 850                   | 13      | 26 |
| 243                  | 187                  | Enabled        | Retry                          | 850                   | 13      | 26 |

Table 7. SET 4 Resistor Reader Example

| R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) | SS Rate (mV/μs) | RR (kΩ) | AV MULTI |
|----------------------|----------------------|-----------------|---------|----------|
| Open                 | 0                    | 1.25            | 200     | 1        |
| Open                 | 20                   | 2.5             | 200     | 1        |
| Open                 | 34.8                 | 5               | 200     | 1        |
| Open                 | 52.3                 | 10              | 200     | 1        |
| Open                 | 105                  | 0.157           | 200     | 1        |
| Open                 | 147                  | 0.315           | 200     | 1        |
| Open                 | 499                  | 0.625           | 200     | 1        |
| 31.6                 | 14.7                 | 1.25            | 200     | 2        |
| 68.1                 | 31.6                 | 2.5             | 200     | 2        |
| 110                  | 51.1                 | 5               | 200     | 2        |
| 165                  | 76.8                 | 10              | 200     | 2        |
| 332                  | 154                  | 0.157           | 200     | 2        |

**Table 7. SET 4 Resistor Reader Example (Continued)**

| R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) | SS Rate (mV/μs) | RR (kΩ) | AV MULTI |
|----------------------|----------------------|-----------------|---------|----------|
| 464                  | 215                  | 0.315           | 200     | 2        |
| 634                  | 294                  | 0.625           | 200     | 2        |
| 0                    | Open                 | 1.25            | 800     | 2        |
| 20                   | Open                 | 2.5             | 800     | 2        |
| 34.8                 | Open                 | 5               | 800     | 2        |
| 52.3                 | Open                 | 10              | 800     | 2        |
| 105                  | Open                 | 0.157           | 800     | 2        |
| 147                  | Open                 | 0.315           | 800     | 2        |
| 499                  | Open                 | 0.625           | 800     | 2        |

#### 4.4 Soft-Starting

The ISL8212M begins the soft-start ramp after the following two conditions are met.

- 5.5ms (worst case = 6.5ms) time out after bias supply (VDD, PVCC, 7VLDO) above POR threshold
- A fixed 200μs delay after EN pin above its 0.84V threshold

The output voltage reaches the output voltage at a fixed slew rate set by the SET4 pin. The ramp time can be calculated based on [Equation 1](#).

$$(EQ. 1) \quad t_{ss} = \frac{V_{OUT}}{RAMP\_RATE} (\mu s)$$

The ISL8212M supports precharged start-up. It initiates the first PWM pulse until the internal reference (DAC) reaches the pre-charged level at the RAMP\_RATE programmed by SET4. When the precharged level is below V<sub>OUT</sub>, the output walks up to the V<sub>OUT</sub> at RAMP\_RATE and releases PGOOD when soft-start finishes. When the precharged output is above V<sub>OUT</sub> but below OVP, it walks down to V<sub>OUT</sub> at RAMP\_RATE and releases PGOOD. The ramp time is defined in [Equation 2 on page 24](#), and is clearly longer than a normal start-up.

$$(EQ. 2) \quad t_{D2} = \frac{V_{PRECHARGED}}{RAMP\_RATE} + \frac{V_{PRECHARGED} - V_{OUT}}{RAMP\_RATE} (\mu s)$$

If the boot capacitor voltage is high enough, the ISL8212M is able to handle up to 5.5V precharged load. However, it is hard to ensure high boot voltage for all precharged loads. If the precharged load is above 2.5V and the precharged start-up time is long, the boot capacitor is discharged to “PVCC - V<sub>OUT</sub> - V<sub>D</sub>” by the high-side drive circuits’ standby current. For a 4V precharged load, the boot capacitor can be discharged to less than 1V, which is insufficient to turn on the high-side MOSFET. In this case, Renesas recommends letting the output drop below 2.5V with an external bleed resistor before soft-start, or using a high RAMP\_RATE to reduce the start-up time.

#### 4.5 Output Voltage Programming

The SET1 pin is used for output voltage set up, which offers 256 options: 0V and 0.5V to 5.5V, as shown in [Table 8](#). The most popular output voltage levels are summarized in [Table 4 on page 22](#). 0V output voltage is considered “OFF”; the driver is in tri-state and the internal DAC sets to 0V.

**Table 8. Output Voltage Set Up**

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 0                    | 499                  | OPEN                 |
| 0.5                  | 49.9                 | 12.4                 |
| 0.508                | 45.3                 | 12.7                 |
| 0.516                | 42.2                 | 13.3                 |



Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 0.523                | 38.3                 | 13.3                 |
| 0.531                | 35.7                 | 13.7                 |
| 0.539                | 34                   | 14.3                 |
| 0.547                | 31.6                 | 14.7                 |
| 0.555                | 29.4                 | 15                   |
| 0.562                | 28                   | 15.4                 |
| 0.57                 | 26.7                 | 16.2                 |
| 0.578                | 25.5                 | 16.5                 |
| 0.586                | 24.3                 | 17.4                 |
| 0.594                | 23.2                 | 17.8                 |
| 0.602                | 22.1                 | 18.2                 |
| 0.609                | 21                   | 19.1                 |
| 0.617                | 20                   | 19.6                 |
| 0.625                | 19.6                 | 20.5                 |
| 0.633                | 18.7                 | 21.5                 |
| 0.641                | 18.2                 | 22.6                 |
| 0.648                | 17.4                 | 23.2                 |
| 0.656                | 16.9                 | 24.3                 |
| 0.664                | 16.5                 | 26.1                 |
| 0.672                | 15.8                 | 26.7                 |
| 0.68                 | 15.4                 | 28.7                 |
| 0.688                | 15                   | 30.1                 |
| 0.695                | 14.7                 | 32.4                 |
| 0.703                | 14                   | 34                   |
| 0.711                | 13.7                 | 36.5                 |
| 0.719                | 13.3                 | 39.2                 |
| 0.727                | 13                   | 43.2                 |
| 0.734                | 107                  | 26.7                 |
| 0.742                | 97.6                 | 27.4                 |
| 0.75                 | 90.9                 | 28.7                 |
| 0.758                | 82.5                 | 28.7                 |
| 0.766                | 76.8                 | 29.4                 |
| 0.773                | 71.5                 | 30.1                 |
| 0.781                | 68.1                 | 31.6                 |
| 0.789                | 63.4                 | 32.4                 |
| 0.797                | OPEN                 | 10                   |
| 0.805                | 57.6                 | 34.8                 |
| 0.812                | 54.9                 | 35.7                 |
| 0.82                 | 52.3                 | 37.4                 |
| 0.828                | 49.9                 | 38.3                 |
| 0.836                | 47.5                 | 39.2                 |

Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 0.844                | 45.3                 | 41.2                 |
| 0.852                | OPEN                 | 21.5                 |
| 0.859                | 42.2                 | 44.2                 |
| 0.867                | 40.2                 | 45.3                 |
| 0.875                | 39.2                 | 48.7                 |
| 0.883                | 37.4                 | 49.9                 |
| 0.891                | 36.5                 | 52.3                 |
| 0.898                | OPEN                 | 34.8                 |
| 0.906                | 34                   | 57.6                 |
| 0.914                | 33.2                 | 61.9                 |
| 0.922                | 32.4                 | 66.5                 |
| 0.93                 | 30.9                 | 68.1                 |
| 0.938                | 30.1                 | 73.2                 |
| 0.945                | 29.4                 | 78.7                 |
| 0.953                | OPEN                 | 52.3                 |
| 0.961                | 28                   | 93.1                 |
| 0.969                | 174                  | 43.2                 |
| 0.977                | 158                  | 44.2                 |
| 0.984                | 147                  | 46.4                 |
| 0.992                | 133                  | 46.4                 |
| 1                    | OPEN                 | 75                   |
| 1.008                | 118                  | 49.9                 |
| 1.016                | 110                  | 51.1                 |
| 1.023                | 102                  | 52.3                 |
| 1.031                | 97.6                 | 53.6                 |
| 1.039                | 93.1                 | 56.2                 |
| 1.047                | OPEN                 | 105                  |
| 1.055                | 84.5                 | 60.4                 |
| 1.062                | 80.6                 | 61.9                 |
| 1.07                 | 76.8                 | 63.4                 |
| 1.078                | 73.2                 | 66.5                 |
| 1.086                | 69.8                 | 68.1                 |
| 1.094                | 68.1                 | 71.5                 |
| 1.102                | OPEN                 | 147                  |
| 1.109                | 63.4                 | 78.7                 |
| 1.117                | 60.4                 | 80.6                 |
| 1.125                | 59                   | 84.5                 |
| 1.133                | 57.6                 | 90.9                 |
| 1.141                | 54.9                 | 93.1                 |
| 1.148                | 53.6                 | 100                  |
| 1.156                | 52.3                 | 105                  |

Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 1.164                | 49.9                 | 110                  |
| 1.172                | 48.7                 | 118                  |
| 1.18                 | 47.5                 | 127                  |
| 1.188                | 46.4                 | 137                  |
| 1.195                | 45.3                 | 150                  |
| 1.203                | OPEN                 | 499                  |
| 1.211                | 237                  | 66.5                 |
| 1.219                | 221                  | 69.8                 |
| 1.227                | 200                  | 69.8                 |
| 1.234                | 187                  | 71.5                 |
| 1.242                | 178                  | 75                   |
| 1.25                 | 165                  | 76.8                 |
| 1.258                | 154                  | 78.7                 |
| 1.266                | 147                  | 80.6                 |
| 1.273                | 140                  | 84.5                 |
| 1.281                | 133                  | 86.6                 |
| 1.289                | 127                  | 90.9                 |
| 1.297                | 121                  | 93.1                 |
| 1.305                | 115                  | 95.3                 |
| 1.312                | 110                  | 100                  |
| 1.32                 | 105                  | 102                  |
| 1.328                | 102                  | 107                  |
| 1.336                | 97.6                 | 110                  |
| 1.344                | 95.3                 | 118                  |
| 1.352                | 10                   | OPEN                 |
| 1.359                | 88.7                 | 127                  |
| 1.367                | 86.6                 | 137                  |
| 1.375                | 82.5                 | 140                  |
| 1.383                | 80.6                 | 150                  |
| 1.391                | 78.7                 | 162                  |
| 1.398                | 75                   | 165                  |
| 1.406                | 73.2                 | 178                  |
| 1.414                | 71.5                 | 191                  |
| 1.422                | 69.8                 | 205                  |
| 1.43                 | 68.1                 | 226                  |
| 1.438                | 374                  | 93.1                 |
| 1.445                | 340                  | 95.3                 |
| 1.453                | 316                  | 100                  |
| 1.461                | 287                  | 100                  |
| 1.469                | 267                  | 102                  |
| 1.477                | 255                  | 107                  |

Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 1.484                | 237                  | 110                  |
| 1.492                | 221                  | 113                  |
| 1.5                  | 21.5                 | OPEN                 |
| 1.508                | 200                  | 121                  |
| 1.516                | 191                  | 124                  |
| 1.523                | 182                  | 130                  |
| 1.531                | 174                  | 133                  |
| 1.539                | 165                  | 137                  |
| 1.547                | 158                  | 143                  |
| 1.555                | 150                  | 147                  |
| 1.562                | 147                  | 154                  |
| 1.57                 | 140                  | 158                  |
| 1.578                | 137                  | 169                  |
| 1.586                | 130                  | 174                  |
| 1.594                | 127                  | 182                  |
| 1.602                | 124                  | 196                  |
| 1.609                | 118                  | 200                  |
| 1.617                | 115                  | 215                  |
| 1.625                | 113                  | 232                  |
| 1.633                | 110                  | 243                  |
| 1.641                | 105                  | 255                  |
| 1.648                | 102                  | 274                  |
| 1.656                | 100                  | 294                  |
| 1.664                | 97.6                 | 324                  |
| 1.672                | 523                  | 130                  |
| 1.68                 | 475                  | 133                  |
| 1.688                | 442                  | 140                  |
| 1.695                | 402                  | 140                  |
| 1.703                | 374                  | 143                  |
| 1.711                | 357                  | 150                  |
| 1.719                | 332                  | 154                  |
| 1.727                | 309                  | 158                  |
| 1.734                | 294                  | 162                  |
| 1.742                | 280                  | 169                  |
| 1.75                 | 267                  | 174                  |
| 1.758                | 255                  | 182                  |
| 1.766                | 243                  | 187                  |
| 1.773                | 232                  | 191                  |
| 1.781                | 221                  | 200                  |
| 1.789                | 210                  | 205                  |
| 1.797                | 34.8                 | OPEN                 |

Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 1.805                | 196                  | 226                  |
| 1.812                | 191                  | 237                  |
| 1.82                 | 182                  | 243                  |
| 1.828                | 178                  | 255                  |
| 1.836                | 174                  | 274                  |
| 1.914                | 165                  | 280                  |
| 1.992                | 162                  | 301                  |
| 2.07                 | 158                  | 324                  |
| 2.148                | 154                  | 340                  |
| 2.227                | 147                  | 357                  |
| 2.305                | 143                  | 383                  |
| 2.383                | 140                  | 412                  |
| 2.461                | 137                  | 453                  |
| 2.469                | 732                  | 182                  |
| 2.477                | 665                  | 187                  |
| 2.484                | 619                  | 196                  |
| 2.492                | 576                  | 200                  |
| 2.5                  | 52.3                 | OPEN                 |
| 2.508                | 499                  | 210                  |
| 2.516                | 464                  | 215                  |
| 2.523                | 432                  | 221                  |
| 2.602                | 412                  | 226                  |
| 2.68                 | 392                  | 237                  |
| 2.758                | 374                  | 243                  |
| 2.836                | 357                  | 255                  |
| 2.914                | 340                  | 261                  |
| 2.992                | 324                  | 267                  |
| 3                    | 75                   | OPEN                 |
| 3.07                 | 309                  | 280                  |
| 3.148                | 301                  | 294                  |
| 3.227                | 287                  | 301                  |
| 3.281                | 274                  | 309                  |
| 3.289                | 267                  | 332                  |
| 3.297                | 105                  | OPEN                 |
| 3.305                | 249                  | 357                  |
| 3.312                | 243                  | 383                  |
| 3.32                 | 232                  | 392                  |
| 3.328                | 226                  | 422                  |
| 3.406                | 221                  | 453                  |
| 3.484                | 215                  | 475                  |
| 3.562                | 205                  | 499                  |

Table 8. Output Voltage Set Up (Continued)

| V <sub>OUT</sub> (V) | R <sub>UP</sub> (kΩ) | R <sub>DW</sub> (kΩ) |
|----------------------|----------------------|----------------------|
| 3.641                | 200                  | 536                  |
| 3.719                | 196                  | 576                  |
| 3.797                | 191                  | 634                  |
| 3.875                | 1000                 | 249                  |
| 3.953                | 909                  | 255                  |
| 4.031                | 845                  | 267                  |
| 4.109                | 768                  | 267                  |
| 4.188                | 715                  | 274                  |
| 4.266                | 665                  | 280                  |
| 4.344                | 634                  | 294                  |
| 4.422                | 590                  | 301                  |
| 4.5                  | 562                  | 309                  |
| 4.578                | 536                  | 324                  |
| 4.656                | 511                  | 332                  |
| 4.734                | 487                  | 348                  |
| 4.812                | 464                  | 357                  |
| 4.891                | 442                  | 365                  |
| 4.969                | 422                  | 383                  |
| 4.977                | 402                  | 392                  |
| 4.984                | 392                  | 412                  |
| 4.992                | 374                  | 422                  |
| 5                    | 147                  | OPEN                 |
| 5.008                | 348                  | 464                  |
| 5.016                | 340                  | 487                  |
| 5.023                | 324                  | 511                  |
| 5.031                | 316                  | 536                  |
| 5.109                | 309                  | 576                  |
| 5.188                | 301                  | 604                  |
| 5.266                | 287                  | 634                  |
| 5.344                | 280                  | 681                  |
| 5.422                | 274                  | 732                  |
| 5.492                | 267                  | 787                  |
| 5.5                  | 261                  | 866                  |

As shown in [Table 8](#), one step is  $2^{-7} = 7.8125\text{mV}$  and some selections are higher than one step from adjacent codes. However, the resolution is  $\pm 7.8125\text{mV}$  around the popular voltage regulation points, as in [Table 4 on page 22](#), for fine-tuning. For finer than  $7.8125\text{mV}$  tuning, place a large ratio resistor divider on the VSEN pin between the output (V<sub>OUT</sub>) and RGND for positive offset or VDD for negative offset, as shown in [Figure 42 on page 31](#).

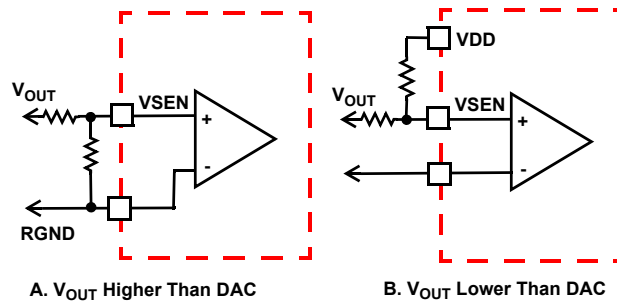


Figure 42. External Programmable Regulation

### 4.6 Thermal Monitoring and Compensation

The thermal monitoring block diagram is shown in [Figure 43](#). Inside the module, a 10kΩ NTC resistor (P/N: NCP15XH103J03RC from Murata,  $\beta = 3380$ ) is placed close to the power stage to sense the operational temperature, and a 1.54kΩ pull-up resistor,  $R_{TM}$ , forms the voltage dividers for the NTC pin. As the power stage temperature increases, the NTC resistance reduces, resulting in the reduced voltage at the NTC pin.

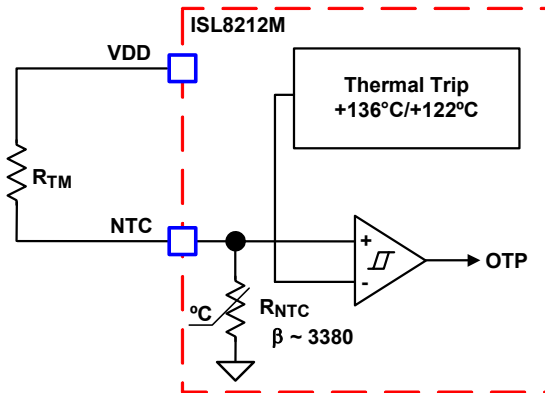


Figure 43. Block Diagram of Thermal Monitoring and Protection

[Figure 44 on page 31](#) shows the TM voltage over the temperature. Renesas recommends using a 1.54kΩ resistor for accurate temperature compensation because the internal thermal digital code is based on that component.

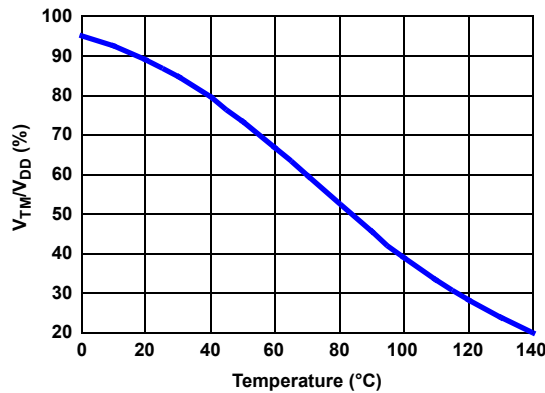
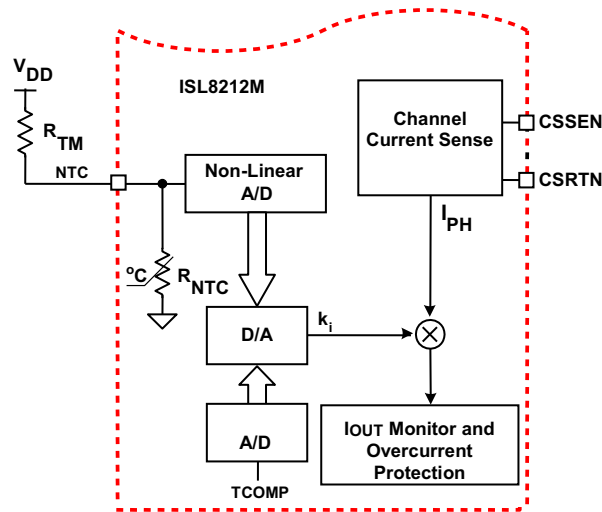


Figure 44. Ratio of TM Voltage to NTC Temperature with Recommended Parts

Because the voltage across the inductor DCR is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR, which is about +0.385%/°C. To obtain the correct

current information, the ISL8212M uses the voltage at the NTC pin and TCOMP register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in [Figure 45](#).



**Figure 45. Block Diagram of Integrated Temperature Compensation**

Based on the  $V_{DD}$  voltage, the ISL8212M converts the NTC pin voltage to a digital signal for temperature compensation. With the nonlinear A/D converter of the ISL8212M, the NTC digital signal is linearly proportional to the NTC temperature.

Because the NTC is not directly attached to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The TCOMP can be used to correct the temperature difference between NTC and the current sense component.

The ISL8212M multiplexes the TCOMP value with the NTC digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated current signal is used for  $I_{OUT}$  and overcurrent protection functions. The four different TCOMP options that can be set by resistor dividers connected to the SET2 pin are:

- +5°C
- +15°C
- +30°C
- OFF

Renesas recommends using +5°C as the TCOMP.

## 4.7 Fault Protection

The ISL8212M provides high system reliability with many fault protections, as summarized in [Table 9](#).

**Table 9. Fault Protection Summary**

| Fault        | Description   | Fault Action                                   |
|--------------|---|--|
| Input UVLO   | VIN pin UVLO; or set by the EN pin with an external divider for higher level. See <a href="#">Figures 39</a> and <a href="#">40</a> . | Shut down and recover when $V_{IN} > UVLO$     |
| Bias UVLO    | $V_{DD}$ , PVCC, 7VLD0 UVLO   | Shut down and recover when Bias > UVLO         |
| Start-Up OVP | Higher than $V_{OUT}$ . See <a href="#">“Electrical Specifications” on page 10</a> .  | Latch OFF, reset by VDD or toggling the EN pin |
| Output OVP   | Rising = 116%; Falling = 100%   |  |
| Output UVP   | 74% of $V_{OUT}$ . Latch OFF  |  |



**Table 9. Fault Protection Summary (Continued)**

| Fault                            | Description   | Fault Action   |
|----------------------------------|---|--|
| Short-Circuit and OCP Protection | Peak load current = 18.8A typical   | Latch OFF (reset by VDD or toggling the EN pin), or retry every 9ms    |
| OTP                              | Rising = 22.31%V <sub>DD</sub> (~+136°C)<br>Falling = 27.79%V <sub>DD</sub> (~+122°C) | Shut down above +136°C and recover when temperature drops below +122°C |

Input UVLO and OTP faults respond to the current state with hysteresis, while output OVP and output UVP faults are latch events. Output OCP and output short-circuit faults can be latch or retry events depending on the SET3 setting. All fault latch events can be reset by VDD cycling or toggling the EN pin. The OCP retry event has a hiccup time of 9ms and the module can be recovered when the fault is removed.

#### 4.7.1 Overvoltage Protection

The Overvoltage Protection (OVP) fault detection circuit triggers when the voltage between V<sub>SEN+</sub> and V<sub>SEN-</sub> is above the rising overvoltage threshold. When an OVP fault is declared, the module is latched off and PGOOD is asserted low. The fault remains latched and can be reset by VDD cycling or toggling the EN pin.

Although the module has latched off in response to an OVP fault, the Low-Side Gate Driver (LGATE) retains the ability to toggle the low-side MOSFET on and off in response to the output voltage transverse the OVP rising and falling thresholds. The LGATE turns on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE turns off the low-side MOSFET when the sensed output voltage is lower than the falling overvoltage threshold (typically 100%). If the output voltage rises again, the LGATE turns on the low-side MOSFET again when the output voltage is above the rising overvoltage threshold (typically 120%). By doing so, the IC protects the load when there is a consistent overvoltage condition.

In addition to normal operation OVP, 5.5ms (typical, worst 6.5ms) after all rails (VDD, PVCC, 7VLDO, VIN) POR and before the end of soft-start, the start-up OVP circuits are enabled to protect against OVP event. See [“Electrical Specifications” on page 10](#).

#### 4.7.2 Undervoltage Protection

The Undervoltage Protection (UVP) fault detection circuit triggers if the output voltage is below the undervoltage threshold (typically 74% of DAC). When an UVP fault is declared, the module is latched off, forcing the LGATE and High-Side Gate Driver (UGATE) outputs low, and the PGOOD pin is asserted low. The fault remains latched and can be reset by VDD cycling or toggling the EN pin.

#### 4.7.3 Overcurrent and Short-Circuit Protection

Inductor DCR sensing is used for current sense and senses current continuously for fast response. The current sense amplifier uses the CSEN and CSRTN inputs to reproduce a signal proportional to the inductor current, I<sub>L</sub>. The sense current is proportional to the inductor current and is used for overcurrent protection.

The Overcurrent Protection (OCP) is triggered when the load current is 18.8A typically. OCP protects inductor saturation from a short-circuit event and provides a more robust power train and system protection. When an OCP or short-circuit fault is declared, the module is latched off, forcing both the high-side and low-side gate driver outputs low, or it retries with a hiccup time of 9ms. The fault response is programmable by SET3. However, the latched off event can be reset by VDD cycling or toggling the EN pin.

#### 4.7.4 Over-Temperature Protection

An NTC inside the module senses the inductor temperature for both over-temperature and current sense temperature compensation. The NTC is connected to the NTC pin and SGND pad, and it results in lower NTC pin voltage at higher temperature. A comparator with hysteresis compares the NTC pin voltage to the threshold set. At +136°C (typical), Over-Temperature Protection (OTP) is triggered, and ISL8212M operation is disabled. When the sensed temperature is around +122.4°C, the ISL8212M resumes normal operation. When an OTP fault is declared, the module forces the LGATE and UGATE outputs low.

#### 4.8 PGOOD Monitor

The PGOOD pin indicates when the module is capable of supplying regulated voltage. If there is a fault condition of a rail's (VDD, PVCC, 7VLDO, or VIN) UVLO, output Overcurrent (OCP), output Overvoltage (OVP), output Undervoltage (UVP), or Over-Temperature (OTP), PGOOD is asserted low. Note that the PGOOD pin is an undefined impedance with insufficient  $V_{DD}$  (typically <2.5V).

#### 4.9 PFM Mode Operation

In PFM mode, programmable by SET2, the switching frequency is dramatically reduced to minimize the switching loss and significantly improve light-load efficiency. The ISL8212M can enter and exit PFM mode seamlessly as load changes. For high  $V_{OUT}$  applications, the LGATE might not turn on long enough to charge the boot capacitor in PFM mode with 0A load. Renesas recommends enabling the ISL8212M's ultrasonic PFM feature (by SET3), which maintains the LGATE switching frequency above 20kHz and keeps the boot capacitor charged for immediate load apply events. Alternatively, maintaining a minimum load can enhance the boot capacitor charge.

## 5. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of the ISL8212M power module. The ISL8212M switches at a very high frequency. Therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Current transition speed from one MOSFET to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, generate EMI, and increase MOSFET voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes. Use the ISL8212MEVAL1Z as a example and reference for the PCB layout.

- Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense and PGOOD signals.
- Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND, as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to avoid any parasitic inductances and resistances. An illustrative layout example is shown in [Figures 46](#) and [47](#).
- Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers.
- Do not oversize the copper planes for the PHASE planes. Because the PHASE planes are subjected to very high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE plane.
- Place the PVCC and VIN1 bypass capacitors underneath the PVCC and VIN1 pins and connect their grounds to the SGND. For the external pin-strap resistor dividers connected to SET1, SET2, SET3, and SET4, connect the low side dividers' ground to the SGND. If a local decoupling capacitor is used to bias these resistor dividers, place the decoupling capacitor close to the dividers and connect the capacitor's ground to the SGND. An illustrative layout example is shown in [Figure 47](#).
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as PHASE. Place 2Ω resistors close to VSEN and RGND, respectively, to dampen the noise on the traces.

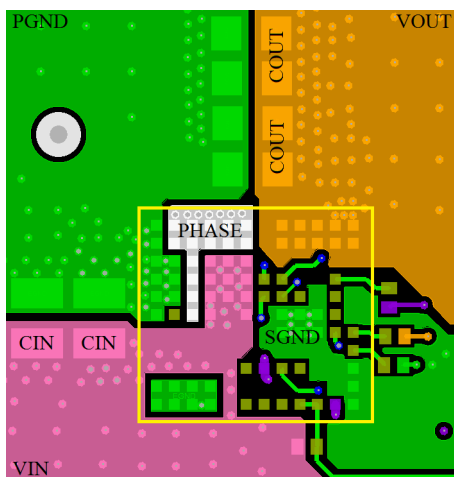


Figure 46. Layout Example - Top Layer

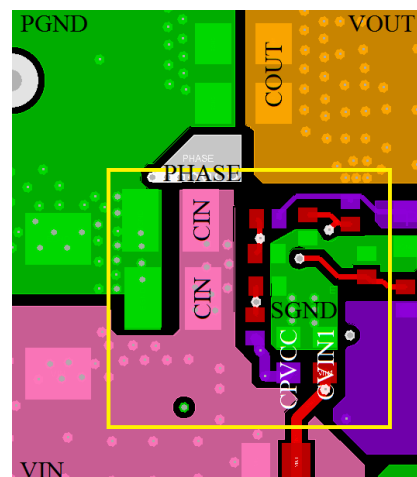


Figure 47. Layout Example - Bottom Layer

## 6. Thermal Considerations

Use the experimental power loss and  $\theta_{JA}$  from the thermal modeling analysis to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. The derating curves are derived based on tests of the ISL8212M evaluation board, which is a 6-layer board 3 x 3 inches in size with 2oz Cu on all layers and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

## 7. Package Description

The structure of the ISL8212M belongs to the High Density Array (HDA) no-lead package. The HDA package has advantages such as good thermal and electrical conductivity, low weight, and small size and is applicable for surface mounting technology that is being more readily used in the industry. The ISL8212M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8212M is a copper leadframe based package with exposed copper thermal pads that have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline, typical Printed Circuit Board (PCB) layout pattern design, and typical stencil pattern design are shown in [“Package Outline Drawing” on page 40](#). The module has a small size of 12mm x 11mm x 5.3mm.

### 7.1 PCB Layout Pattern Design

The bottom of the ISL8212M is a leadframe footprint attached to the PCB by surface mounting process. The PCB layout pattern is shown in [“Package Outline Drawing” on page 40](#). The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

### 7.2 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s). Place the grid under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, increasing the number of vias eventually yields diminishing returns. Use as many vias as practical for the thermal land size and your board design rules allow.

### 7.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50 $\mu$ m to 75 $\mu$ m (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the [“Package Outline Drawing” on page 40](#). Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a “brick like” paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

## 7.4 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in [Figure 48](#) is provided as a guideline, which can be adapted for varying manufacturing practices and applications.

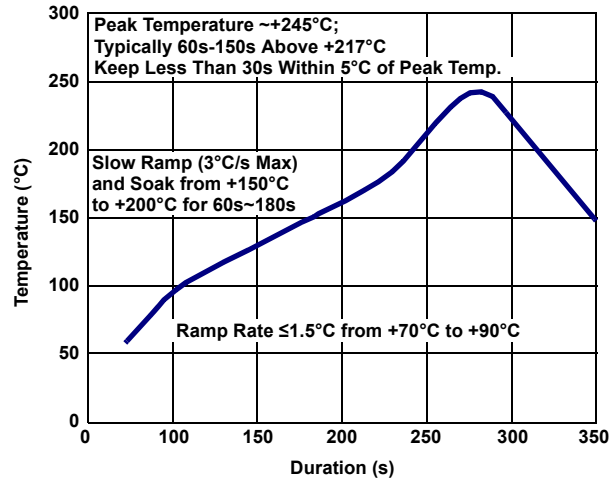


Figure 48. Typical Reflow Profile

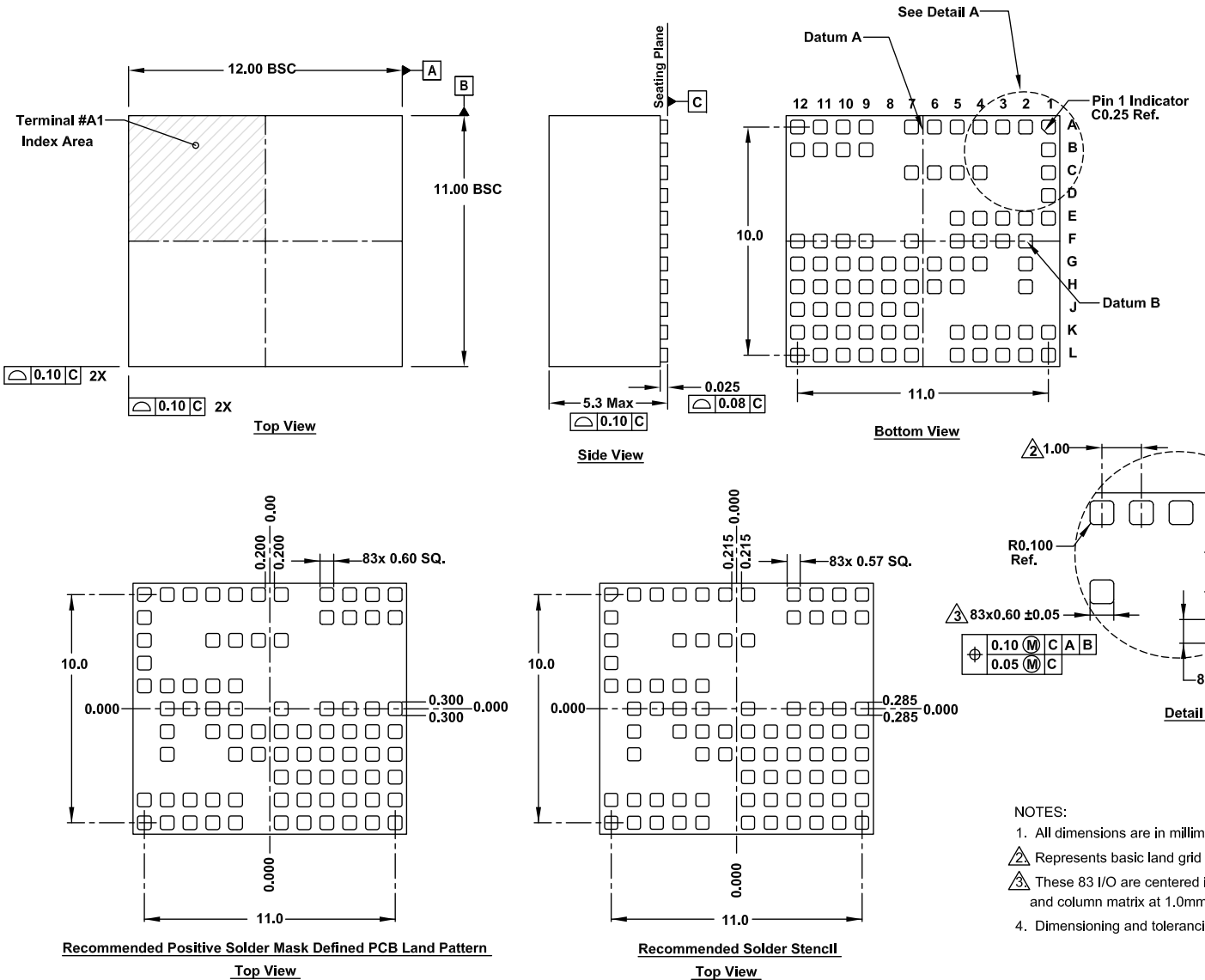
## 8. Revision History

| Rev. | Date         | Description   |
|------|--------------|---|
| 1.00 | Feb 15, 2019 | <p>Changed "R4 gain" to "AV gain" throughout document.</p> <p>Updated typical application diagram on page 3.</p> <p>Changed "power supply" to "power module" on page 6.</p> <p>Updated Note 5 on page 9.</p> <p>Updated Figure 41 on page 20.</p> <p>Changed "regulator specifications" to "module specifications" on page 21.</p> <p>Added information about tie options on page 21.</p> <p>Added information about recommended resistors on page 31.</p> <p>Clarified information about NTC attachment on page 32.</p> <p>Corrected VDD and EN pin names on page 33.</p> <p>Changed "ISL8212M based DC/DC converter" to "ISL8212M power module" on page 35.</p> <p>Updated first item in Layout Guidelines on page 35.</p> <p>Updated Figures 46 and 47 on page 35.</p> <p>Correct setting pin names on page 35.</p> <p>Corrected information about board size on page 36.</p> <p>Updated disclaimer.</p> |
| 0.00 | Dec 14, 2018 | Initial release.  |

## 9. Package Outline Drawing

Y83.12x11  
83 I/O 12mmx11mmx5.3mm HDA Module  
Rev 0, 3/18

For the most recent package outline





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[MP2148GQD-18-P](#)