## ISL8225MEVAL4Z

User's Manual: Evaluation Board

Industrial Analog and Power

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User's Manual

## ISL8225MEVAL4Z

## Evaluation Board

The ISL8225M is a complete, dual step-down switching mode DC/DC power module. The dual outputs can easily be paralleled for single-output, high current use. It is easy to apply this high-power, current sharing DC/DC power module to power-hungry datacom, telecom, and FPGA applications. All that is needed to have a complete, dual 15A design ready for use are the ISL8225M, a few passive components, and $V_{\text {OUT }}$ setting resistors.

The simplicity of the ISL8225M is its off-the-shelf, unassisted implementation. Patented current sharing in multiphase operation greatly reduces ripple currents, BOM costs, and complexity. The ISL8225M has a thermally enhanced, compact 17 mmx 17 mmx 7.5 mm QFN package that operates at full load and over-temperature without requiring forced-air cooling. Easy access to all pins, with few external components, reduces PCB design to a component layer and a simple ground layer.

This ISL8225MEVAL4Z evaluation board is designed for dual 15A output applications. Optionally, this board can easily be converted for 30A single output use. Multiple ISL8225MEVAL4Z boards can be cascadable through the SYNC and CLKOUT pins to operate with phase shifting, for paralleling or multiple output use. The input voltage of this board is 4.5 V to 20 V and the default outputs on this board are set at 1.2 V and 1.5 V .

## Key Features

- Full encapsulated dual step down switching power supply
- Up to 100 W output
- Dual 15A or single 30A output
- 4.5 V to 20 V input range
- 0.6 V to 7.5 V output range
- $1.5 \%$ output voltage accuracy
- Up to $95 \%$ conversion efficiency


## Specifications

This board is configured and optimized for the following operating conditions:

- $\mathrm{V}_{\mathrm{IN}}=4.5 \mathrm{~V}$ to $20 \mathrm{~V}, \mathrm{~V}_{\mathrm{O} 1}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{O} 2}=1.5 \mathrm{~V}$
- $\mathrm{I}_{\mathrm{O} 1}=15 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=15 \mathrm{~A}$
- $\mathrm{f}_{\mathrm{SW}}=500 \mathrm{kHz}$


## Ordering information

| Part Number | Description |
| :--- | :--- |
| ISL8225MEVAL4Z | Dual 15A/Optional 30A Cascadable Evaluation Board |

## Related Literature

For a full list of related documents, visit our website:

- ISL8225M device page


## Related Resources

- Evaluation Board Video


Figure 1. ISL8225MEVAL4Z Board

## 1. Functional Description

### 1.1 Recommended Equipment

- 0 V to 20 V power supply with at least 5A source current capability
- Electronic load capable of sinking current up to 30A
- Digital Multimeters (DMMs)
- 100 MHz quad-trace oscilloscope


### 1.2 High Output Voltage Operation

The ISL8225MEVAL4Z is designed for output voltage below 5.5 V . For an output voltage higher than 6 V , see the "ISL8225M Design Guide Matrix" table in the ISL8225M datasheet for selections of output capacitors, input capacitors, and switching frequency. The maximum load capability of each phase is 10 A for 6.5 V output and 7 A for 7.5 V output.

### 1.3 Quick Start

For dual output operation, the inputs are BA7 (VIN1), BA8 (GND), BA3 (VIN2), and BA4 (GND). The outputs are BA5 (VOUT1), BA6 (GND), BA1 (VOUT2), and BA2 (GND).
For paralleled single output operation, the inputs are BA7 (VIN1) and BA8 (GND). The outputs are BA5 (VOUT1) and BA6 (GND) with BA5 and BA1 shorted.

### 1.3.1 Dual Output Mode

1. Connect a power supply capable of sourcing at least 5 A to the inputs BA7 (VIN1), BA8 (GND), BA3 (VIN2), and BA4 (GND) of the ISL8225MEVAL4Z, with a voltage between 4.5 V to 20 V . VIN1 and VIN2 can be different with $\mathrm{R}_{18}$ and $\mathrm{R}_{19}$ open.
2. Connect an electronic load or the device to be powered to the outputs BA5 (VOUT1) and BA6 (GND), BA1 (VOUT2) and BA2 (GND) of the board. All connections, especially the low voltage, high current $\mathrm{V}_{\text {OUT }}$ lines, should be able to carry the load current and should be made as short as possible.
3. Make sure that the setup is connected correctly. Turn on the power supply. If the board is working properly, the green LED illuminates; if not, the red LED illuminates (recheck the wire/jumper connections in this case). Measure the output voltages, which should be $\mathrm{V}_{\text {OUT1 }}$ at 1.2 V and $\mathrm{V}_{\text {OUT2 }}$ at 1.5 V
4. For different output voltages, board resistors can be exchanged to provide the needed $\mathrm{V}_{\text {OUT }}$. See Table 1 for $R_{2} / R_{4}$ resistor values, which can produce different output voltages.
For $12 \mathrm{~V} \mathrm{~V}_{\mathrm{IN}}$ and $\mathrm{V}_{\text {OUT }}$ more than 1.5 V , the switching frequency needs to be adjusted, as shown in Table 1. The resistor $\mathrm{R}_{\text {FSET }}$ can be adjusted for the desired frequency. No frequency adjustments are necessary for $\mathrm{V}_{\mathrm{OUT}}$ below 1.5 V . For $5 \mathrm{~V} \mathrm{~V}_{\text {IN }}$, the frequency does not need to be adjusted and the module default frequency can be used at any allowed $\mathrm{V}_{\text {OUT. }}$. If the output voltage is set to more than 1.8 V , the output current needs to be derated to allow for safe operation. See the derating curves in the ISL8225M datasheet.

Table 1. Value of Bottom Resistor (Top Resistor $R_{1}, R_{3}=1 \mathrm{k} \Omega$ ) and Frequency Selection for Different Output Voltages

| $\mathbf{V}_{\text {OUT }}(\mathbf{V})$ | $\mathbf{R}_{\mathbf{2}} / \mathbf{R}_{\mathbf{4}} \mathbf{( \Omega )}$ | Frequency (kHz) | $\mathbf{R}_{\mathbf{F S E T}}(\mathbf{\Omega} \mathbf{( \mathbf { V } \mathbf { I N }} \mathbf{= 1 2 V )}$ |
| :---: | :---: | :---: | :---: |
| 1.0 | 1500 | DEFAULT | OPEN |
| 1.2 | 1000 | DEFAULT | OPEN |
| 1.5 | 665 | DEFAULT | OPEN |
| 2.5 | 316 | 650 | 249 k |
| 3.3 | 221 | 800 | 124 k |
| 5.0 | 137 | 950 | 82.5 k |
| 5.5 | 121 | 950 | 82.5 k |

Table 1. Value of Bottom Resistor (Top Resistor $R_{1}, R_{3}=1 k \Omega$ ) and Frequency Selection for Different Output Voltages (Continued)

| $\mathbf{V}_{\text {OUT }}(\mathbf{V})$ | $\mathbf{R}_{\mathbf{2}} / \mathbf{R}_{\mathbf{4}} \mathbf{( \Omega )}$ | Frequency $\mathbf{( k H z )}$ | $\mathbf{R}_{\mathbf{F S E T}}(\mathbf{\Omega})(\mathbf{V} \mathbf{I N} \mathbf{= 1 2 V )}$ |
| :---: | :---: | :---: | :---: |
| 6.5 | 102 | 750 | 147 k |
| 7.5 | 86.6 | 750 | 147 k |

### 1.3.2 Optional Paralleled Single Output Mode

1. To set up the parallel mode, short JP1 (ENC), JP2 (VMON), and JP3 (COMP) with a jumper. To set up $180^{\circ}$ interleaving phase between two channels, short the MODE pin and GND pin of JP6 with a jumper.
2. Remove $R_{9}$ and $R_{13}$. Change $R_{14}$ to $0 \Omega$. Change $R_{18}$ and $R_{19}$ to $0 \Omega$. Short $V_{\text {OUT1 }}$ to $V_{\text {OUT2 }}$ using short wires or copper straps. Add $C_{2}$ for a 470 pF capacitor.
3. Connect a power supply capable of sourcing at least 5A to the ISL8225MEVAL4Z's inputs, BA7 (VIN1), BA8 (GND), BA3 (VIN2), and BA4 (GND), with a voltage between 4.5V to 20V. VIN1 and VIN2 need to be shorted together.
4. Connect an electronic load or the device to be powered to the board's outputs, BA5 (VOUT1) and BA6 (GND). All connections, especially the low voltage, high current $\mathrm{V}_{\mathrm{OUT}}$ lines, should be able to carry the load current and should be made as short as possible.
5. Make sure the setup is connected correctly prior to applying any power to the board. Adjust the power supply to 12 V and turn on the input power supply. If the board is working properly, the green LED illuminates; if not, the red LED illuminates (recheck the wire/jumper connections in this case). Measure the output voltages, $\mathrm{V}_{\text {OUT1 }}$, which should be at 1.2 V .
6. Apply any load that is less than 30A for normal steady state operation. See Table 1 to change the output voltage by changing resistor $\mathrm{R}_{2}$.

Table 2. Board Configuration for Single Output 30A Application

|  | ENC | VMON | MODE | COMP | $\mathbf{R}_{\mathbf{9}}$ | $\mathbf{R}_{\mathbf{1 3}}$ | $\mathbf{R}_{\mathbf{1 4}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dual | OPEN | OPEN | OPEN | OPEN | 0 | 0 | OPEN |
| Single | ON | ON | ON | ON | OPEN | OPEN | 0 |

### 1.3.3 Optional Cascadable Mode

Cascadable mode is needed when multiple evaluation boards are used for paralleling or multiple output use. To evaluate the parallel features, Renesas recommends using the ISL8225MEVAL2Z 6-phase evaluation board for an easy and efficient setup (see AN1789 "ISL8225MEVAL2Z Evaluation Board User Guide"). Otherwise, complete the following steps:

1. To generate CLKOUT at a shifted phase clock signal, disable the control loop of $\mathrm{V}_{\text {OUT2 }}$ by connecting VSEN2to VCC.
2. Program the MODE and VSEN2+ pin voltages to set the CLKOUT signal and the shifted degrees between two phases on the board (see Table 3 on page 6).
3. Use a coaxial cable to connect CLKOUT (J5) to SYNC (J2) of the next evaluation board, which can be programmed for parallel or dual output use.
4. If the second board is programed for parallel use, the ISHARE pins of the first and second boards need to be tied together. Using two twisted wires, short two different jumpers of JP7 (ISHARE/SGND) on two evaluation boards. Add 1 nF capacitors of $\mathrm{C}_{14}$ for different boards to decouple the noise.
5. If the third board is used in cascadable mode, the second board can only be used in the parallel mode to generate the CLKOUT signal for the SYNC pin on the third board.
6. Follow the instructions from Steps 1 through 5 for more cascadable boards.

## 2. PCB Layout Guidelines

The evaluation board size is $114.3 \mathrm{mmx76.2mm}$. It is a 4-layer board that contains 2 -oz copper on all layers. The board can be used as a dual 15A reference design. See "ISL8225MEVAL4Z Board Layout" on page 9. The board is made of FR4 material and all components, including the solder attachment, are Pb-free.

### 2.1 Thermal Considerations and Current Derating

For high current applications, board layout is very critical to make the module operate safely and deliver maximum allowable power. To carry large currents, the board layout needs to be designed carefully to maximize thermal performance. For best thermal performance, select enough trace width, copper weight, and the proper connectors.

This evaluation board is designed for running dual 15A at room temperature without additional cooling systems needed. However, if the output voltage is increased or the board is operated at elevated temperatures, the available current is derated. See the derated current curves in the ISL8225M datasheet to determine the output current available.

For layout of designs using the ISL8225M, the thermal performance can be improved by adhering to the following design tips:

- Use the top and bottom layers to carry the large current. VOUT1, VOUT2, Phase 1, Phase 2, PGND, VIN1, and VIN2 should have large, solid planes. Place enough thermal vias to connect the power planes in different layers under and around the module.
- The Phase 1 and Phase 2 pads are switching nodes that generate switching noise. Keep these pads under the module. For noise-sensitive applications, Renesas recommends keeping phase pads only on the top and inner layers of the PCB; do not place phase pads exposed to the outside on the bottom layer of the PCB. To improve the thermal performance, the phase pads can be extended in the inner layer, as shown in Phase 1 and Phase 2 pads on layer 2 (Figure 5 on page 9) for this dual 15A evaluation board. Make sure that layer 1 and layer 3 have the GND layers cover the extended areas of the phase pads at layer 2 to avoid noise coupling.
- Place the modules evenly on the board and leave enough space between modules. If the board space is limited, try to put the modules with low power loss closely together (such as low $\mathrm{V}_{\mathrm{OUT}}$ or $\mathrm{I}_{\mathrm{OUT}}$ ) while still separating the module with high power loss.
- If the ambient temperature is high or the board space is limited, airflow is needed to dissipate more heat from the modules. A heatsink can also be applied to the top side of the module to further improve the thermal performance (heatsink recommendation: Aavid Thermalloy, part number 375424B00034G, www.aavid.com).

Table 3. ISL8225M Operation Modes

| 1ST Module ( $\mathrm{=}$ Input; $\mathrm{O}=$ Output; $/ \mathrm{O}=$ Input and Output, Bi-Direction) |  |  |  |  |  |  |  |  |  | Modes of Operation |  | Output (See Description For Details) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Mode | $\begin{array}{\|c} \text { EN1/ } \\ \text { FF1 } \\ \text { (I) } \end{array}$ | $\begin{array}{\|l} \hline \text { EN2/ } \\ \hline \text { FF2 } \\ \text { (I) } \end{array}$ | VSEN2- <br> (I) | Mode (I) | VSEN2+ <br> (I) | CLKOUT /REFIN WRT 1st (I OR O) | VMON2 (Notes 2, $\underline{3}, 4)$ | VMON1 of 2nd Module (Notes 2, $3,4)$ | 2nd Channel WRT 1st (O) (Note 1) | Operation Mode of 2nd Module | Operation <br> Mode <br> of 3rd <br> Module |  |
| 1 | 0 | 0 | - | - | - | - | - | - |  | - | - | Disabled |
| 2A | 0 | 1 | Active | Active | Active | - | Active | - | VMON1 = <br> VMON2 to Keep PGOOD Valid | - | - | Single Phase |
| 2B | 1 | 0 | - | - | - | - | - | - | VMON1 = <br> VMON2 to Keep PGOOD Valid | - | - | Single Phase |
| 3A | 1 | 1 | $<\mathrm{V}_{\text {CC }}-0.7 \mathrm{~V}$ | Active | Active | $\begin{aligned} & 29 \% \text { to } \\ & 45 \% \text { of } \\ & \mathrm{V}_{\mathrm{Cc}}(\mathrm{I}) \\ & \hline \end{aligned}$ | Active | - | $0^{\circ}$ | - | - | Dual Regulator |

Table 3. ISL8225M Operation Modes (Continued)

| 1ST Module ( $\mathrm{I}=$ Input; $\mathrm{O}=$ Output; $/ \mathrm{O}=$ Input and Output, Bi-Direction) |  |  |  |  |  |  |  |  |  | Modes of Operation |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Mode | $\begin{array}{\|c\|} \hline \text { EN1/ } \\ \hline \text { FF1 } \\ \text { (I) } \\ \hline \end{array}$ | $\begin{array}{\|c\|c\|} \hline \text { EN2I } \\ \text { FF2 } \\ \text { (I) } \\ \hline \end{array}$ | VSEN2- <br> (I) | Mode (I) | VSEN2+ <br> (I) | CLKOUT /REFIN WRT 1st (I OR O) | $\left.\begin{array}{\|c\|} \text { VMON2 } \\ (\text { Notes } 2, \\ \underline{3}, \underline{4}) \end{array} \right\rvert\,$ | VMON1 of 2nd Module (Notes 2, 3, 4) | 2nd Channel WRT 1st (O) (Note 1) | Operation Mode of 2nd Module | Operation Mode of 3rd Module | Output (See Description For Details) |
| 3B | 1 | 1 | $<V_{\text {CC }}-0.7 \mathrm{~V}$ | Active | Active | $45 \%$ to 62\% of $\mathrm{V}_{\mathrm{CC}}(\mathrm{I})$ | Active | - | $90^{\circ}$ | - | - | Dual Regulator |
| 3 C | 1 | 1 | $<\mathrm{V}_{\text {CC }}-0.7 \mathrm{~V}$ | Active | Active | $\begin{gathered} >62 \% \text { of } \\ \mathrm{V}_{\mathrm{CC}}(\mathrm{I}) \end{gathered}$ | Active | - | $180^{\circ}$ | - | - | Dual Regulator |
| 4 | 1 | 1 | $<\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ | Active | Active | $\begin{aligned} & \hline<29 \% \text { of } \\ & \mathrm{V}_{\mathrm{CC}}(\mathrm{I}) \end{aligned}$ | Active | - | $-60^{\circ}$ | - | - | DDR Mode |
| 5A | 1 | 1 | $\mathrm{V}_{\mathrm{Cc}}$ | GND | - | $60^{\circ}$ | VMON1 <br> or <br> Divider | - | $180^{\circ}$ | - | - | 2-Phase |
| 5B | 1 | 1 | $\mathrm{V}_{\mathrm{Cc}}$ | GND | - | $60^{\circ}$ | Divider | Divider | $180^{\circ}$ | 5B | 5B | 6-Phase |
| 5C | 1 | 1 | $\mathrm{V}_{\mathrm{CC}}$ | GND | - | $60^{\circ}$ | VMON1 or Divider | Active | $180^{\circ}$ | 5C | 5 C | 3 Outputs |
| 6 | 1 | 1 | $\mathrm{V}_{\mathrm{Cc}}$ | $\mathrm{V}_{\mathrm{Cc}}$ | GND | $120^{\circ}$ | $\begin{gathered} 953 \Omega \\ / / 22 n F \end{gathered}$ | Active | $240^{\circ}$ | 2B | - | 3-Phase |
| 7A | 1 | 1 | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{Cc}}$ | $90^{\circ}$ | $\begin{gathered} 953 \Omega \\ / / 22 \mathrm{nF} \end{gathered}$ | Divider | $180^{\circ}$ | 7A | - | 4-Phase |
| 7B | 1 | 1 | $\mathrm{V}_{\mathrm{Cc}}$ | $\mathrm{V}_{\mathrm{Cc}}$ | $\mathrm{V}_{\mathrm{Cc}}$ | $90^{\circ}$ | $\begin{gathered} 953 \Omega \\ / / 22 n F \end{gathered}$ | Active | $180^{\circ}$ | 7B | - | 2 Outputs (1st module in Mode 7A) |
| 7 C | 1 | 1 | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{Cc}}$ | $90^{\circ}$ | $\begin{gathered} 953 \Omega \\ / / 22 n F \end{gathered}$ | Active | $180^{\circ}$ | 3, 4 | - | 3 Outputs (1st module in Mode 7A) |
| 8 | Cascaded Module Operation MODEs 5B+5B+7A +5B+5B+5B/7A, No External Clock Required |  |  |  |  |  |  |  |  |  |  | 12-Phase |
| 9 | External Clock or External Logic Circuits Required for Equal Phase Interval |  |  |  |  |  |  |  |  |  |  | $\begin{gathered} 5,7,8,9,9 \\ 10,11, \text { or } \\ \text { (PHASE } \\ >12 \text { ) } \end{gathered}$ |

## Notes:

1. "2nd CHANNEL WRT 1ST" means "second channel with respect to first;" in other words, Channel 2 lags Channel 1 by the degrees specified in this column. For example, $90^{\circ}$ means Channel 2 lags Channel 1 by $90^{\circ}$; $-60^{\circ}$ means Channel 2 leads Channel 1 by $60^{\circ}$.
2. "VMON1" means that the pin is tied to the VMON1 pin of the same module.
3. "Divider" means that there is a resistor divider from VOUT to SGND; see the "Six-Phase 90A 1.2V Output Circuit" figure in the ISL8225M datasheet.
4. " $953 \Omega / / 22 n \mathrm{~F}$ " means that there is a $953 \Omega$ resistor and a 22 nF capacitor connecting the pin to SGND; see the " 4 -Phase Paralleled at $1.5 \mathrm{~V} / 60 \mathrm{~A}$ with $90^{\circ}$ Interleaving" figure in the ISL8225M datasheet.

## 2．2 ISL8225MEVAL4Z Schematic



Figure 2．ISL8225MEVAL4Z Board Schematic


Figure 3. Top Silk Screen


Figure 5. Layer 2


Figure 4. Top Layer


Figure 6.



Figure 7．Bottom Layer Solder Side
Figure 8．Botto

### 2.4 Bill of Materials

| Part Number | Reference Designation | Qty | Value | Tol. | Voltage | Power | Package Type | Jedec Type |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 10TPB330M | C04, C08 | 2 | $330 \mu \mathrm{~F}$ | 20\% | 10 V |  | SMD | CAP_7343_149 |
| 131-4353-00 | J1, J4 | 2 |  |  |  |  | CONN | TEK131-4353-00 |
| 2N7002-7-F | Q1 | 1 |  |  |  |  | SOT23 | SOT23 |
| 31-5329-52RFX | J2, J5 | 2 |  |  |  |  | CONN | CON_BNC_31_5329_52RFX |
| 5002 | P1-P8 | 8 |  |  |  |  | THOLE | MTP500X |
| 575-4 | BA1-BA8 | 8 |  |  |  |  | CONN | CON_BAN_575 |
| EEVHA1E331UP | CIN1, CIN4 | 2 | $330 \mu \mathrm{~F}$ | 20\% | 25 V |  | SMD | CAPAE_315X402 |
| GRM21BR71C475KA73L | C1 | 1 | $4.7 \mu \mathrm{~F}$ | 10\% | 16 V |  | 805 | CAP_0805 |
| GRM32ER71A476KE15L | C01, C03, C05, C07 | 4 | $47 \mu \mathrm{~F}$ | 10\% | 10 V |  | 1210 | CAP_1210 |
| H1045-OPEN | C2, C3, C6, C7 | 4 | OPEN | 5\% | OPEN |  | 603 | CAP_0603 |
| H1045-00102-16V10 | C15, C16 | 2 | 1000pF | 10\% | 16 V |  | 603 | CAP_0603 |
| H1045-00102-50V10 | C4, C5, C8, C9 | 4 | 1000pF | 10\% | 50 V |  | 603 | CAP_0603 |
| H1045-OPEN | C10, C11, C12, C14 | 6 | OPEN | 5\% | OPEN |  | 603 | CAP_0603 |
| H1082-OPEN | C02, C06, C09, C010 | 4 | OPEN | 10\% | OPEN |  | 1210 | CAP_1210 |
| H2505-DNP-DNP-1 | R14-R16, R21, RFSET | 5 | DNP | 1\% |  | DNP | 603 | RES_0603 |
| H2511-00R00-1/16W1 | R9, R10, R13, R17, R20 | 5 | $0 \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2511-01001-1/16W1 | R1, R2, R3, R6, R8 | 4 | $1 \mathrm{k} \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2511-03321-1/16W1 | R11, R12 | 2 | $3.32 \mathrm{k} \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2511-16501-1/16W1 | R5, R7 | 2 | $16.5 \mathrm{k} \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2511-04121-1/16W1 | R6, R8 | 2 | $4.12 \mathrm{k} \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2511-06650-1/16W1 | R4 | 1 | $665 \Omega$ | 1\% |  | 1/16W | 603 | RES_0603 |
| H2512-OPEN | R18, R19 | 2 | OPEN | 0\% |  | 1/10W | 805 | RES_0805 |
| ISL8225MIRZ | U1 | 1 |  |  |  |  | QFN | QFN26_670X670_ISL8225M |
| JUMPER2_100 | JP1-JP7 | 7 |  |  |  |  | THOLE | JUMPER-1 |
| SSL-LXA3025IGC | LED1 | 1 |  |  |  |  | SMD | LED_3X2_5MM |
| TMK325B7226MM-TR | CIN2, CIN3, CIN5, CIN6 | 4 | $22 \mu \mathrm{~F}$ | 20\% | 25V |  | 1210 | CAP_1210 |

3. ISL8225MEVAL4Z Efficiency Curves


Figure 9. Efficiency vs Load Current ( $5 \mathrm{~V}_{\mathrm{IN}}$ at 500 kHz )


Figure 10. Efficiency vs Load Current (12V $\mathrm{IN}_{\mathrm{IN}}$ )

## 4. Revision History

| Rev. | Date | Description |
| :--- | :---: | :--- |
| 4.00 | Jun.25.19 | Applied new formatting throughout document. <br> Replaced QR code with link to video on page 1. <br> Updated Schematics with Orchad version. <br> Added Revision History section. |

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