

ISL8272M

50A Digital DC/DC PMBus Power Module

FN8670  
Rev.5.00  
Nov 8, 2017

The [ISL8272M](#) is a 50A step-down PMBus compliant digital power module. Integrated in the module is a high performance digital PWM controller, dual-phase power MOSFETs, inductors, and the passives. This high efficiency power module is capable of delivering 50A without the need for airflow and heatsinks. The ISL8272M can be placed in a current sharing configuration with up to four modules in parallel to deliver 200A continuous current.

The ISL8272M operates with the ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. The ISL8272M comes with operating in a pin strap mode; output voltage, switching frequency device, SMBus address, input UVLO, soft-start/stop, and current sharing can be programmed through external resistors. More configuration such as fault limits, fault response, margining, and sequencing can be easily programmed using the PMBus interface. PMBus can be used to monitor voltages, currents, temperatures, and fault status. The ISL8272M is supported by the PowerNavigator™ software, a graphical user interface (GUI) that can be used to configure modules to a desired solution.

The ISL8272M is built in a compact (18mmx23mmx7.5mm) and low profile overmolded HDA package, suitable for automated assembly by standard surface mount equipment.

Features

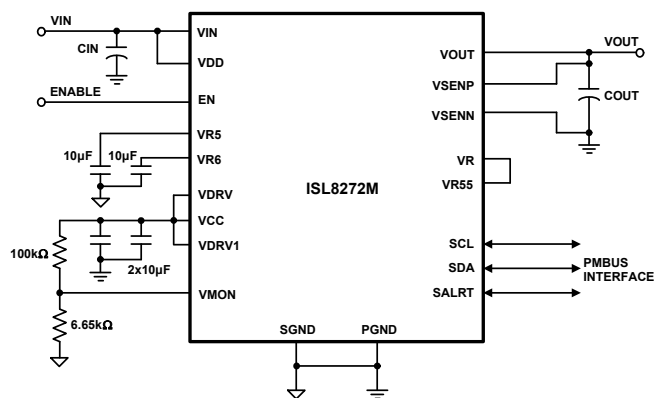
- Complete digital switch mode power supply
- Wide input voltage range: 4.5V to 14V
- Programmable output voltage range: 0.6V to 5V
- PMBus compliant communication interface
- Programmable V<sub>OUT</sub>, margining, UV/OV, UC/OC, UT/OT, soft-start/stop, sequencing and external synchronization
- Monitor of V<sub>IN</sub>, V<sub>OUT</sub>, I<sub>OUT</sub>, temperature, duty cycle, switching frequency, power-good, and faults
- Fast response ChargeMode control architecture
- Multiphase current sharing with up to four modules
- ±1.0% V<sub>OUT</sub> accuracy over line, load, and temperature
- Internal nonvolatile memory and fault logging
- Thermally enhanced HDA package

Applications

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Related Literature

- For a full list of related documents, visit our website - [ISL8272M](#) product page



NOTE:  
1. Figure 1 represents a typical implementation of the ISL8272M. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

FIGURE 1. 50A APPLICATION CIRCUIT

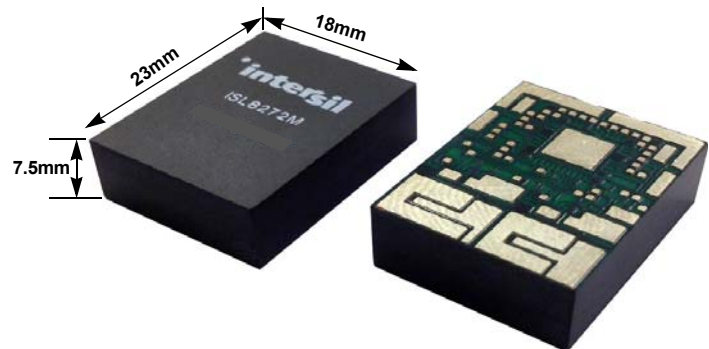


FIGURE 2. A SMALL PACKAGE FOR HIGH POWER DENSITY

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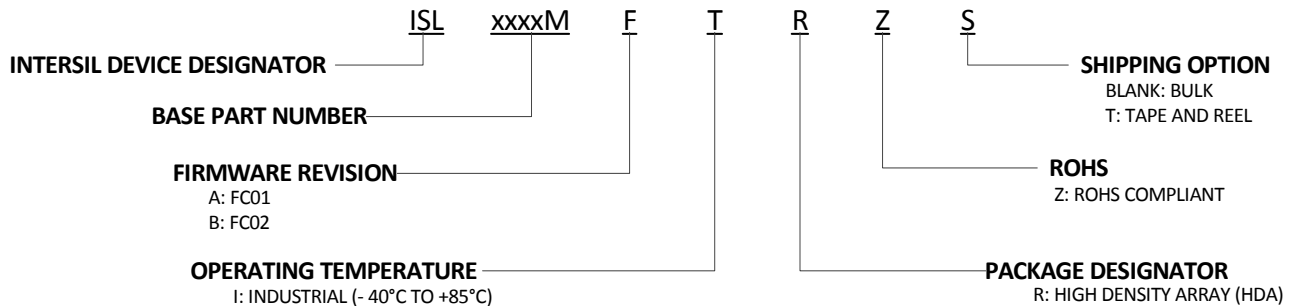
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## Ordering Information

| PART NUMBER<br>(Notes 2, 3, 4) | PART MARKING                                                                                                             | TEMP RANGE<br>(°C) | PACKAGE<br>(RoHS Compliant) | PKG.<br>DWG. # |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------|----------------|
| ISL8272MAIRZ                   | ISL8272M                                                                                                                 | -40 to +85         | 58 LD 18x23 HDA             | Y58.18x23      |
| ISL8272MBIRZ                   | ISL8272MB                                                                                                                | -40 to +85         | 58 LD 18x23 HDA             | Y58.18x23      |
| ISL8272MEVAL1Z                 | Single-Module Evaluation Board (see <a href="#">UG003</a> , "ISL8272MEVAL1Z Evaluation Board User Guide")                |                    |                             |                |
| ISL8272MEVAL2Z                 | Three-Module Current Sharing Evaluation Board (see <a href="#">UG004</a> , "ISL8272MEVAL2Z Evaluation Board User Guide") |                    |                             |                |

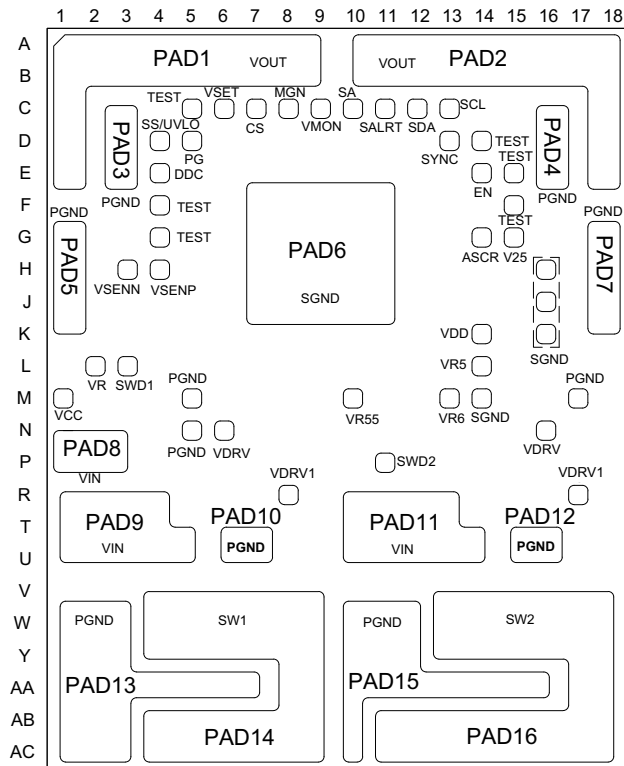
### NOTES:

- Add "-T" suffix for 100 unit tape and reel option. Refer to [TB347](#) for details on reel specifications.
- These Intersil Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), refer to the [ISL8272M](#) product information page. For more information about MSL, refer to [TB363](#).



## Pin Configuration

ISL8272M  
(58 LD HDA)  
TOP VIEW



## Pin Descriptions

| PIN                           | LABEL    | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                    |
|-------------------------------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PAD1, 2                       | VOUT     | PWR  | Power supply output voltage. Output voltage from 0.6V to 5V. Tie these two pins together to achieve a single output. For higher output voltage, refer to the derating curves starting on <a href="#">page 15</a> to set the maximum output current from these pads.                                                                            |
| PAD3, 4, 5, 7, 10, 12, 13, 15 | PGND     | PWR  | Power ground. Refer to " <a href="#">Layout Guide</a> " on <a href="#">page 23</a> for the PGND pad connections and I/O capacitor placement.                                                                                                                                                                                                   |
| PAD6                          | SGND     | PWR  | Signal ground. Refer to " <a href="#">Layout Guide</a> " on <a href="#">page 23</a> for the SGND pad connections.                                                                                                                                                                                                                              |
| PAD8, 9, 11                   | VIN      | PWR  | Input power supply voltage to power the module. Input voltage range from 4.5V to 14V.                                                                                                                                                                                                                                                          |
| PAD14, 16                     | SW1, SW2 | PWR  | Switching node pads. The SW pads dissipate the heat and provide good thermal performance. Refer to " <a href="#">Layout Guide</a> " on <a href="#">page 23</a> for the SW pad connections.                                                                                                                                                     |
| C6                            | VSET     | I    | Output voltage selection pin. Used to set $V_{OUT}$ set point and $V_{OUT}$ max.                                                                                                                                                                                                                                                               |
| C7                            | CS       | I    | Current sharing configuration pin. Used to program current sharing configurations such as SYNC selection, phase spreading, and $V_{OUT}$ droop.                                                                                                                                                                                                |
| C8                            | MGN      | I    | External $V_{OUT}$ margin control pin. Active high (>2V) sets $V_{OUT}$ margin high; active low (<0.8V) sets $V_{OUT}$ margin low; high impedance (floating) sets $V_{OUT}$ to normal voltage. Factory default range for margining is nominal $V_{OUT} \pm 5\%$ . When using PMBus to control margin command, leave this pin as no connection. |
| C9                            | VMON     | I    | Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider.                                                                                                                                                                                                                                             |
| C10                           | SA       | I    | Serial address selection pin. Used to assign unique address for each individual device or to enable certain management features.                                                                                                                                                                                                               |
| C11                           | SALRT    | O    | Serial alert. Connect to external host if desired. SALRT is asserted low upon a warning or a fault event and deasserted when warning or fault is cleared. A pull-up resistor is required.                                                                                                                                                      |

## Pin Descriptions (Continued)

| PIN                          | LABEL         | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                        |
|------------------------------|---------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C12                          | SDA           | I/O  | Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required.                                                                                                                                                                                                                         |
| C13                          | SCL           | I/O  | Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required.                                                                                                                                                                                                                         |
| D4                           | SS/<br>UVLO   | I    | Soft-start/stop and undervoltage lockout selection pin. Used to set turn on/off delay and ramp time as well as input UVLO threshold levels.                                                                                                                                                                                        |
| D5                           | PG            | O    | Power-good output. Power-good output can be an open drain that requires a pull-up resistor or push-pull output that can drive a logic input.                                                                                                                                                                                       |
| D13                          | SYNC          | I/O  | Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock.                                                                                                                                                                                     |
| E14                          | EN            | I    | Enable pin. Logic high to enable the module output.                                                                                                                                                                                                                                                                                |
| E4                           | DDC           | I/O  | A Digital-DC bus. This dedicated bus provides the communication between devices for features such as sequencing, fault spreading and current sharing. The DDC pin on all Digital-DC devices should be connected together. A pull-up resistor is required.                                                                          |
| C5, D14, E15,<br>F4, F15, G4 | TEST          | -    | Test pins. Do not connect these pins.                                                                                                                                                                                                                                                                                              |
| G14                          | ASCR          | I    | ChargeMode™ control ASCR parameters selection pin. Used to set ASCR gain and residual values.                                                                                                                                                                                                                                      |
| G15                          | V25           | PWR  | Internal 2.5V reference used to power internal circuitry. No external capacitor required for this pin.                                                                                                                                                                                                                             |
| H3                           | VSENN         | I    | Differential output voltage sense feedback. Connect to negative output regulation point.                                                                                                                                                                                                                                           |
| H4                           | VSENP         | I    | Differential output voltage sense feedback. Connect to positive output regulation point.                                                                                                                                                                                                                                           |
| H16, J16, K16,<br>M14        | SGND          | PWR  | Signal grounds. Using multiple vias to connect the SGND pins to the internal SGND layer.                                                                                                                                                                                                                                           |
| K14                          | VDD           | PWR  | Input supply voltage for controller. Connect VDD pad to $V_{IN}$ supply.                                                                                                                                                                                                                                                           |
| L2                           | VR            | PWR  | Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace.                                                                                                                                                                                                                                                            |
| L3, P11                      | SWD1,<br>SWD2 | PWR  | Switching node driving pins. Directly connect to the SW1 and SW2 pads with short loop wires.                                                                                                                                                                                                                                       |
| L14                          | VR5           | PWR  | Internal 5V reference used to power internal circuitry. Place a 10 $\mu$ F decoupling capacitor for this pin.                                                                                                                                                                                                                      |
| M1                           | VCC           | PWR  | Internal LDO output. Connect VCC to VDRV for internal LDO driving.                                                                                                                                                                                                                                                                 |
| M5, M17, N5                  | PGND          | PWR  | Power grounds. Using multiple vias to connect the PGND pins to the internal PGND layer.                                                                                                                                                                                                                                            |
| M10                          | VR55          | PWR  | Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to VR pin.                                                                                                                                                                                                                                             |
| M13                          | VR6           | PWR  | Internal 6V reference used to power internal circuitry. Place a 10 $\mu$ F decoupling capacitor for this pin.                                                                                                                                                                                                                      |
| N6, N16                      | VDRV          | PWR  | Power supply for internal FET drivers. Connect 10 $\mu$ F bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input application, use external supply or connect this pin to VIN. |
| R8, R17                      | VDRV1         | I    | Bias pin of the internal FET drivers. Always tie to VDRV.                                                                                                                                                                                                                                                                          |

# ISL8272M Internal Block Diagram

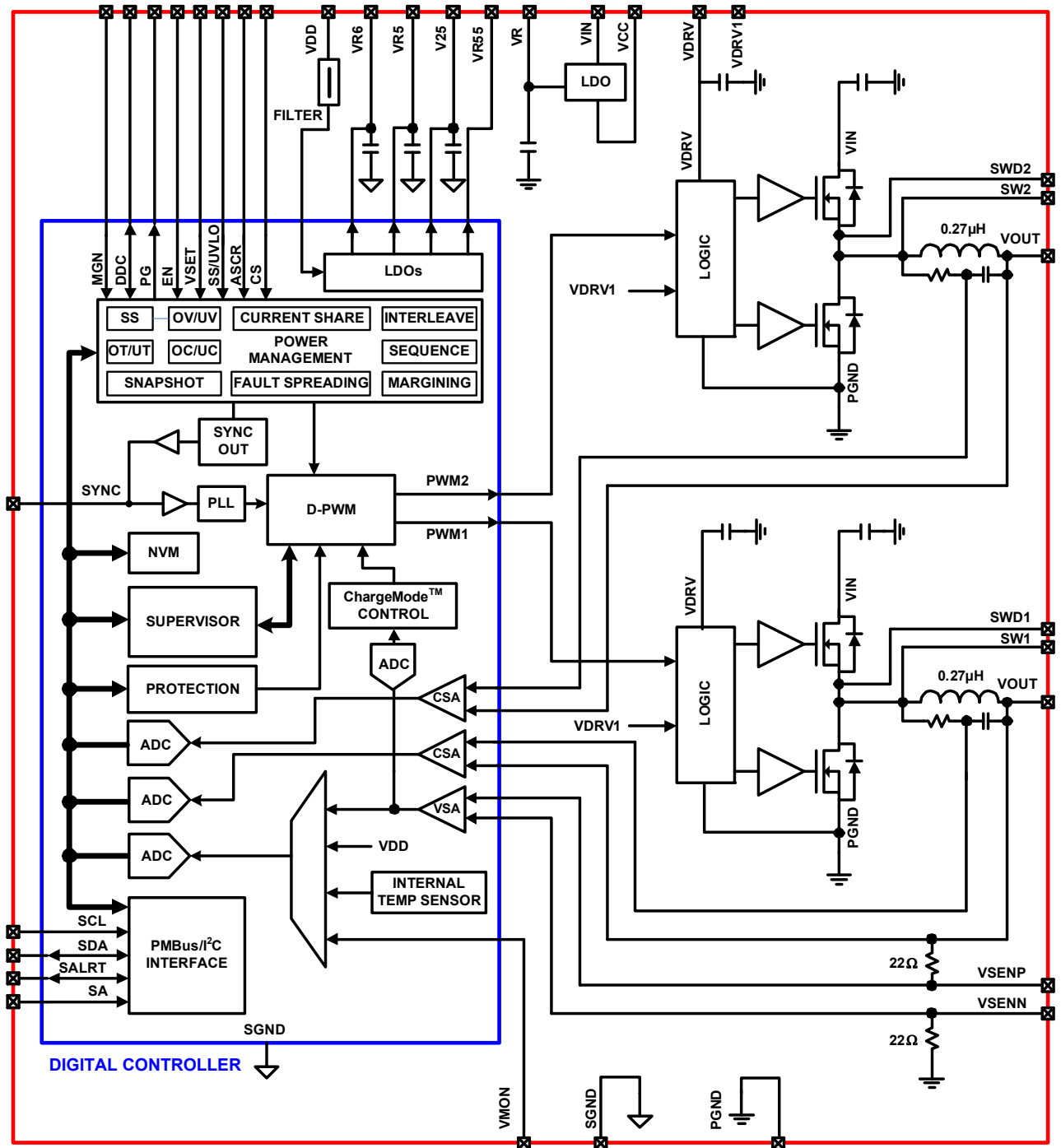
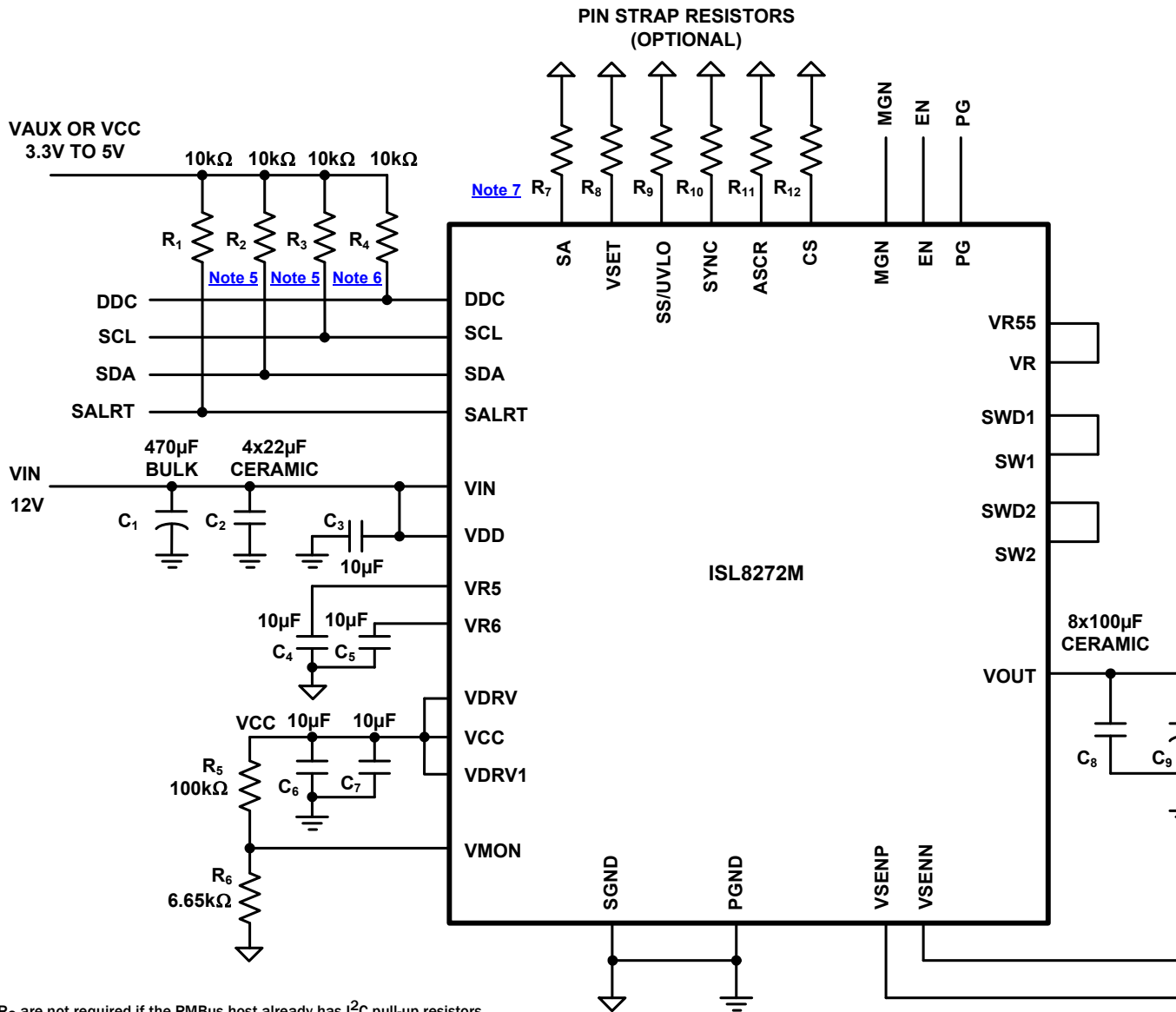


FIGURE 3. INTERNAL BLOCK DIAGRAM

## Typical Application Circuit - Single Module



NOTES:

5. R<sub>2</sub> and R<sub>3</sub> are not required if the PMBus host already has I<sup>2</sup>C pull-up resistors.
6. Only one R<sub>4</sub> per DDC bus is required when multiple modules share the same DDC bus.
7. R<sub>7</sub> through R<sub>12</sub> can be selected according to the tables for the pin-strap resistor setting in this document. If the PMBus configuration is chosen to overwrite the pin-strap configuration, R<sub>8</sub> through R<sub>12</sub> can be non-populated.
8. V<sub>25</sub>, VR and VR55 do not need external capacitors. V<sub>25</sub> can be no connection.

FIGURE 4. TYPICAL APPLICATION CIRCUIT - SINGLE MODULE

# Typical Application Circuit - Three Module Current Sharing

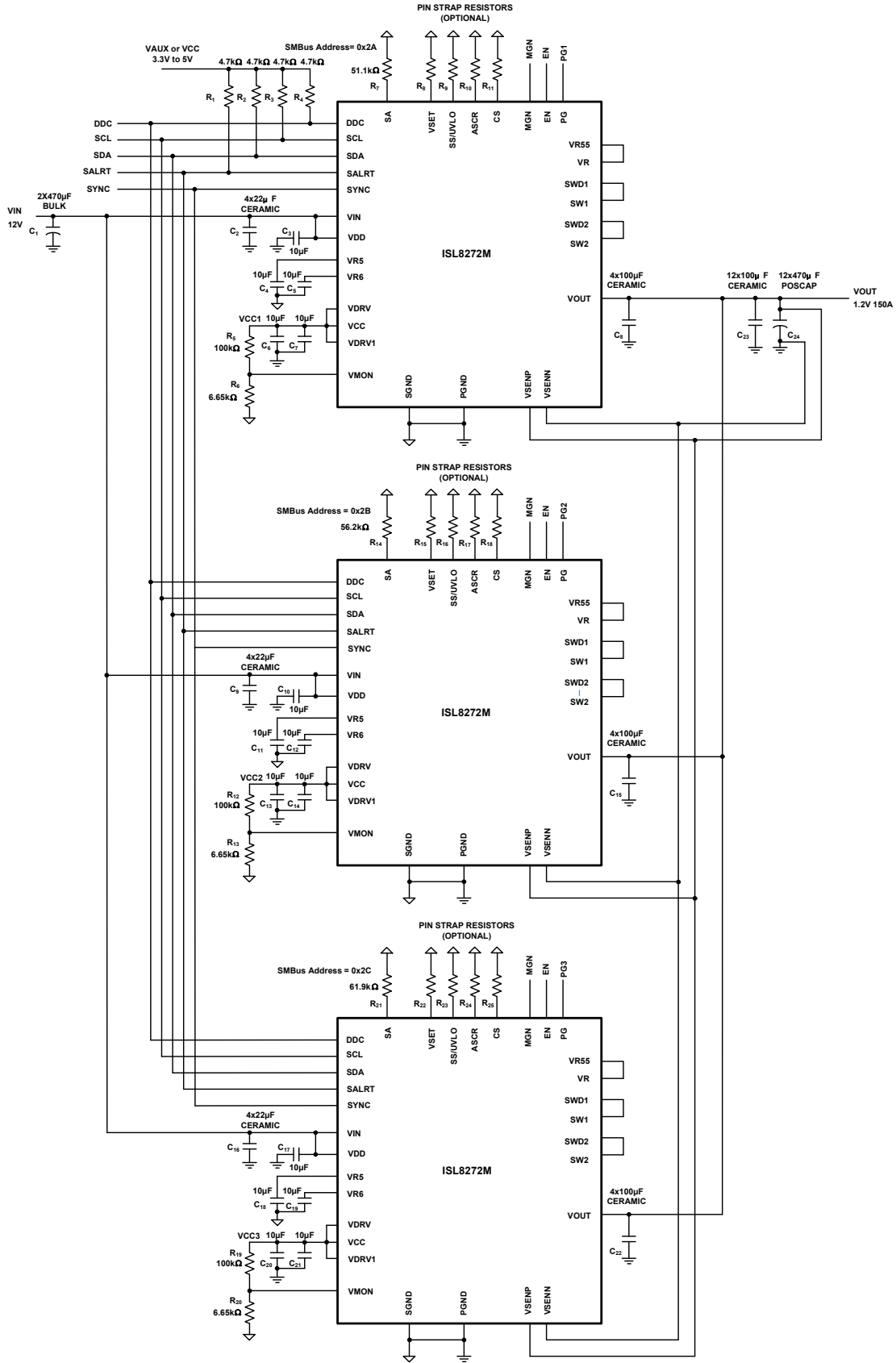


FIGURE 5. TYPICAL APPLICATION CIRCUIT - THREE MODULE CURRENT SHARING



TABLE 1. ISL8272M DESIGN GUIDE MATRIX AND OUTPUT VOLTAGE RESPONSE

| V <sub>IN</sub><br>(V) | V <sub>OUT</sub><br>(V) | C <sub>IN</sub> (BULK)<br>(Note 9)<br>( $\mu$ F) | C <sub>IN</sub> (CERAMIC)<br>( $\mu$ F) | C <sub>OUT</sub> (BULK)<br>( $\mu$ F) | C <sub>OUT</sub> (CERAMIC)<br>( $\mu$ F) | ASCR GAIN<br>(Note 10) | ASCR RESIDUAL<br>(Note 10) | P-P DEVIATION<br>(mV) | RECOVERY TIME<br>( $\mu$ s) | LOAD STEP (A)<br>(Note 11) | FREQ.<br>(kHz) |
|------------------------|-------------------------|--------------------------------------------------|-----------------------------------------|---------------------------------------|------------------------------------------|------------------------|----------------------------|-----------------------|-----------------------------|----------------------------|----------------|
| 5                      | 1                       | 1x470                                            | 6x47                                    | 4x470                                 | 12x100                                   | 220                    | 90                         | 50                    | 20                          | 0/25                       | 300            |
| 5                      | 1                       | 1x470                                            | 4x47                                    | 4x470                                 | 8x100                                    | 550                    | 100                        | 45                    | 15                          | 0/25                       | 533            |
| 12                     | 1                       | 1x470                                            | 6x22                                    | 4x470                                 | 12x100                                   | 220                    | 90                         | 55                    | 22                          | 0/25                       | 300            |
| 12                     | 1                       | 1x470                                            | 4x22                                    | 4x470                                 | 8x100                                    | 550                    | 100                        | 50                    | 15                          | 0/25                       | 533            |
| 5                      | 1.8                     | 1x470                                            | 6x47                                    | 4x470                                 | 8x100                                    | 200                    | 90                         | 60                    | 25                          | 0/25                       | 300            |
| 5                      | 1.8                     | 1x470                                            | 4x47                                    | 2x470                                 | 6x100                                    | 250                    | 90                         | 70                    | 20                          | 0/25                       | 533            |
| 12                     | 1.8                     | 1x470                                            | 6x22                                    | 4x470                                 | 8x100                                    | 220                    | 90                         | 70                    | 20                          | 0/25                       | 300            |
| 12                     | 1.8                     | 1x470                                            | 4x22                                    | 2x470                                 | 6x100                                    | 280                    | 100                        | 70                    | 20                          | 0/25                       | 533            |
| 5                      | 2.5                     | 1x470                                            | 6x47                                    | 2x470                                 | 6x100                                    | 120                    | 90                         | 100                   | 30                          | 0/25                       | 300            |
| 5                      | 2.5                     | 1x470                                            | 4x47                                    | 2x470                                 | 4x100                                    | 250                    | 90                         | 80                    | 20                          | 0/25                       | 533            |
| 12                     | 2.5                     | 1x470                                            | 6x22                                    | 2x470                                 | 6x100                                    | 110                    | 90                         | 100                   | 20                          | 0/25                       | 300            |
| 12                     | 2.5                     | 1x470                                            | 4x22                                    | 2x470                                 | 4x100                                    | 220                    | 90                         | 100                   | 15                          | 0/25                       | 533            |
| 5                      | 3.3                     | 1x470                                            | 6x47                                    | 2x470                                 | 4x100                                    | 100                    | 90                         | 120                   | 50                          | 0/25                       | 300            |
| 5                      | 3.3                     | 1x470                                            | 4x47                                    | 2x470                                 | 4x100                                    | 220                    | 90                         | 100                   | 30                          | 0/25                       | 533            |
| 12                     | 3.3                     | 1x470                                            | 4x22                                    | 2x470                                 | 4x100                                    | 220                    | 90                         | 100                   | 10                          | 0/25                       | 533            |
| 12                     | 5                       | 1x470                                            | 6x22                                    | 2x470                                 | 4x100                                    | 230                    | 90                         | 120                   | 10                          | 0/25                       | 533            |

## NOTES:

9. C<sub>IN</sub> bulk capacitor is optional only for energy buffer from the long input power supply cable.
10. ASCR gain and residual are selected to ensure phase margin higher than 60° and gain margin higher than 6dB at room temperature and full load (50A).
11. Output voltage response is tested with load step slew rate higher than 100A/ $\mu$ s.

TABLE 2. RECOMMENDED INPUT/OUTPUT CAPACITOR

| VENDORS                    | VALUE                   | PART NUMBER        |
|----------------------------|-------------------------|--------------------|
| MURATA, Input Ceramic      | 47 $\mu$ F, 16V, 1210   | GRM32ER61C476ME15L |
| MURATA, Input Ceramic      | 22 $\mu$ F, 16V, 1210   | GRM32ER61E226KE15L |
| TAIYO YUDEN, Input Ceramic | 47 $\mu$ F, 16V, 1210   | EMK325BJ476MM-T    |
| TAIYO YUDEN, Input Ceramic | 22 $\mu$ F, 25V, 1210   | TMK325BJ226MM-T    |
| MURATA, Output Ceramic     | 100 $\mu$ F, 6.3V, 1210 | GRM32ER60J107M     |
| TDK, Output Ceramic        | 100 $\mu$ F, 6.3V, 1210 | C3225X5R0J107M     |
| AVX, Output Ceramic        | 100 $\mu$ F, 6.3V, 1210 | 12106D107MAT2A     |
| SANYO POSCAP, Output Bulk  | 470 $\mu$ F, 4V         | 4TPE470MCL         |
| SANYO POSCAP, Output Bulk  | 470 $\mu$ F, 6.3V       | 6TPF470MAH         |

**Absolute Maximum Ratings**

|                                                      |               |
|------------------------------------------------------|---------------|
| Input Supply Voltage, VIN Pin                        | -0.3V to 17V  |
| Input Supply Voltage for Controller, VDD Pin         | -0.3V to 17V  |
| MOSFET Switch Node Voltage, SW1/2, SWD1/2            | -0.3V to 17V  |
| MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin        | -0.3V to 6.0V |
| Output Voltage, VOUT pin                             | -0.3V to 6.0V |
| Internal Reference Supply Voltage, VR6 Pin           | -0.3V to 6.6V |
| Internal Reference Supply Voltage, VR, VR5, VR55 Pin | -0.3V to 6.5V |
| Internal Reference Supply Voltage, V25 Pin           | -0.3V to 3V   |
| Logic I/O Voltage for DDC, EN, MGN, PG, ASCR, CS     |               |
| SA, SCL, SDA, SALRT, SYNC, SS/UVLO, VMON, VSET       | -0.3V to 6.0V |
| Analog Input Voltages for                            |               |
| VSENP                                                | -0.3V to 6.0V |
| VSENN                                                | -0.3V to 0.3V |
| ESD Rating                                           |               |
| Human Body Model (Tested per JESD22-A114F)           | 2000V         |
| Machine Model (Tested per JESD22-A115C)              | 200V          |
| Charged Device Model (Tested per JESD22-C110D)       | 750V          |
| Latch-Up (Tested per JESD78C; Class 2, Level A)      | 100mA         |

**Thermal Information**

|                                                |                      |                      |
|------------------------------------------------|----------------------|----------------------|
| Thermal Resistance (Typical)                   | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
| 58 LD HDA Package (Notes 12, 13)               | 6.55                 | 1.6                  |
| Maximum Junction Temperature (Plastic Package) | +125°C               |                      |
| Storage Temperature Range                      | -55°C to +150°C      |                      |
| Pb-Free Reflow Profile                         | Refer to Figure 30   |                      |

**Recommended Operating Conditions**

|                                                |                 |
|------------------------------------------------|-----------------|
| Input Supply Voltage Range, VIN                | 4.5V to 14V     |
| Input Supply Voltage Range for Controller, VDD | 4.5V to 14V     |
| Output Voltage Range, VOUT                     | 0.6V to 5V      |
| Output Current Range, IOUT(DC) (Note 16)       | 0A to 50A       |
| Operating Junction Temperature Range, TJ       | -40°C to +125°C |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- $\theta_{JA}$  is measured in free air with the module mounted on an 6-layer evaluation board 4.7x4.8inch in size with 2oz surface and 2oz buried planes and multiple via interconnects as specified in the ISL8272MEVAL1Z Evaluation Board User Guide.
- For  $\theta_{JC}$ , the “case temp” location is the center of the package underside.

**Electrical Specifications**

$V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .**

| SYMBOL                                  | PARAMETER                                                           | TEST CONDITIONS                                                                 | MIN<br>(Note 14) | TYP         | MAX<br>(Note 14) | UNITS |
|-----------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------------------------|------------------|-------------|------------------|-------|
| <b>INPUT AND SUPPLY CHARACTERISTICS</b> |                                                                     |                                                                                 |                  |             |                  |       |
| $I_{DD}$                                | Input Supply Current for Controller                                 | $V_{IN} = V_{DD} = 12V$ , $V_{OUT} = 0V$ , module not enabled                   |                  | 40          | <b>50</b>        | mA    |
| $V_{R6}$                                | 6V Internal Reference Supply Voltage                                |                                                                                 | <b>5.5</b>       | 6.1         | <b>6.6</b>       | V     |
| $V_{R5}$                                | 5V Internal Reference Supply                                        | $I_{VR5} < 5mA$                                                                 | <b>4.5</b>       | 5.2         | <b>5.5</b>       | V     |
| $V_{25}$                                | 2.5V Internal Reference Supply                                      |                                                                                 | <b>2.25</b>      | 2.5         | <b>2.75</b>      | V     |
| $V_{CC}$                                | Internal LDO Output Voltage                                         |                                                                                 |                  | 5.3         |                  | V     |
| $I_{VCC}$                               | Internal LDO Output Current                                         | $V_{IN} = V_{DD} = 12V$ , $V_{CC}$ connected to VDRV, module enabled            | <b>50</b>        |             |                  | mA    |
| $V_{DD\_READ\_RES}$                     | Input Supply Voltage for Controller Read Back Resolution            |                                                                                 |                  | 10          |                  | Bits  |
| $V_{DD\_READ\_ERR}$                     | Input Supply Voltage for Controller Read Back Total Error (Note 17) | PMBus Read                                                                      |                  | $\pm 2$     |                  | %FS   |
| <b>OUTPUT CHARACTERISTICS</b>           |                                                                     |                                                                                 |                  |             |                  |       |
| $V_{OUT\_RANGE}$                        | Output Voltage Adjustment Range                                     | $V_{IN} > V_{OUT} + 1.8V$                                                       | <b>0.54</b>      |             | <b>5.5</b>       | V     |
| $V_{OUT\_RES}$                          | Output Voltage Set-Point Range                                      | Configured using PMBus                                                          |                  | $\pm 0.025$ |                  | %     |
| $V_{OUT\_ACCY}$                         | Output Voltage Set-Point Accuracy (Notes 15, 17)                    | Includes line, load and temperature ( $-20^\circ C \leq T_A \leq +85^\circ C$ ) | <b>-1</b>        |             | <b>+1</b>        | %VOUT |
| $V_{OUT\_READ\_RES}$                    | Output Voltage Read Back Resolution                                 |                                                                                 |                  | 10          |                  | Bits  |
| $V_{OUT\_READ\_ERR}$                    | Output Voltage Read Back Total Error (Note 17)                      | PMBus read                                                                      | <b>-2</b>        |             | <b>+2</b>        | %VOUT |
| $I_{OUT\_READ\_RES}$                    | Output Current Read Back Resolution                                 |                                                                                 |                  | 10          |                  | Bits  |

**Electrical Specifications**  $V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

| SYMBOL                           | PARAMETER                                                               | TEST CONDITIONS                                  | MIN<br>(Note 14)           | TYP                  | MAX<br>(Note 14)           | UNITS           |
|----------------------------------|-------------------------------------------------------------------------|--------------------------------------------------|----------------------------|----------------------|----------------------------|-----------------|
| I <sub>OUT_RANGE</sub>           | Output Current Range (Note 16)                                          |                                                  |                            |                      | <b>50</b>                  | A               |
| I <sub>OUT_READ_ERR</sub>        | Output Current Read back Total Error                                    | PMBus read at max load. V <sub>OUT</sub> = 1V    |                            | ±3                   |                            | A               |
| <b>SOFT-START AND SEQUENCING</b> |                                                                         |                                                  |                            |                      |                            |                 |
| t <sub>ON_DELAY</sub>            | Delay Time From Enable to V <sub>OUT</sub> Rise                         | Configured using PMBus                           | <b>2</b>                   |                      | <b>5000</b>                | ms              |
| t <sub>ON_DELAY_ACCY</sub>       | t <sub>ON_DELAY</sub> Accuracy                                          |                                                  |                            | ±2                   |                            | ms              |
| t <sub>ON_RISE</sub>             | Output Voltage Ramp-Up Time                                             | Configured using PMBus. Single module standalone | <b>0.5</b>                 |                      | <b>100</b>                 | ms              |
| t <sub>ON_RISE_ACCY</sub>        | Output Voltage Ramp-Up Time Accuracy                                    | Single module standalone                         |                            | ±250                 |                            | µs              |
| t <sub>OFF_DELAY</sub>           | Delay Time From disable to V <sub>OUT</sub> Fall                        | Configured using PMBus                           | <b>2</b>                   |                      | <b>5000</b>                | ms              |
| t <sub>OFF_DELAY_ACCY</sub>      | t <sub>OFF_DELAY</sub> Accuracy                                         |                                                  |                            | ±2                   |                            | ms              |
| t <sub>OFF_FALL</sub>            | Output Voltage Fall Time                                                | Configured using PMBus. Single module standalone | <b>0.5</b>                 |                      | <b>100</b>                 | ms              |
| t <sub>ON_FALL_ACCY</sub>        | Output Voltage Fall Time Accuracy                                       | Single module standalone                         |                            | ±250                 |                            | µs              |
| <b>POWER-GOOD</b>                |                                                                         |                                                  |                            |                      |                            |                 |
| V <sub>PG_DELAY</sub>            | Power-Good Delay                                                        | Configured using PMBus                           | <b>0</b>                   |                      | <b>5000</b>                | ms              |
| <b>TEMPERATURE SENSE</b>         |                                                                         |                                                  |                            |                      |                            |                 |
| T <sub>SENSE_RANGE</sub>         | Temperature Sense Range                                                 | Configurable using PMBus                         | <b>-50</b>                 |                      | <b>150</b>                 | °C              |
| INT_TEMP <sub>ACCY</sub>         | Internal Temperature Sensor Accuracy                                    | Tested at +100°C                                 | -5                         |                      | +5                         | °C              |
| <b>FAULT PROTECTION</b>          |                                                                         |                                                  |                            |                      |                            |                 |
| V <sub>DD_UVLO_RANGE</sub>       | V <sub>DD</sub> Undervoltage Threshold Range                            | Measured internally                              | <b>4.18</b>                |                      | <b>16</b>                  | V               |
| V <sub>DD_UVLO_ACCY</sub>        | V <sub>DD</sub> Undervoltage Threshold Accuracy (Note 17)               |                                                  |                            | ±2                   |                            | %FS             |
| V <sub>DD_UVLO_DELAY</sub>       | V <sub>DD</sub> Undervoltage Response Time                              |                                                  |                            | 10                   |                            | µs              |
| V <sub>OUT_OV_RANGE</sub>        | V <sub>OUT</sub> Overvoltage Threshold Range                            | Factory default                                  |                            | 1.15V <sub>OUT</sub> |                            | V               |
|                                  |                                                                         | Configured using PMBus                           | <b>1.05V<sub>OUT</sub></b> |                      | <b>V<sub>OUT_MAX</sub></b> | V               |
| V <sub>OUT_UV_RANGE</sub>        | V <sub>OUT</sub> Undervoltage Threshold Range                           | Factory default                                  |                            | 0.85V <sub>OUT</sub> |                            | V               |
|                                  |                                                                         | Configured using PMBus                           | <b>0</b>                   |                      | <b>0.95V<sub>OUT</sub></b> | V               |
| V <sub>OUT_OV/UV_ACCY</sub>      | V <sub>OUT</sub> OV/UV Threshold Accuracy (Note 15)                     |                                                  | <b>-2</b>                  |                      | <b>+2</b>                  | %               |
| V <sub>OUT_OV/UV_DELAY</sub>     | V <sub>OUT</sub> OV/UV Response Time                                    |                                                  |                            | 10                   |                            | µs              |
| I <sub>LIMIT_ACCY</sub>          | Output Current Limit Set-Point Accuracy (Note 17)                       | Tested at I <sub>OUT_OC_FAULT_LIMIT</sub> = 50A  |                            | ±10                  |                            | % FS            |
| I <sub>LIMIT_DELAY</sub>         | Output Current Fault Response Time (Note 18)                            | Factory default                                  |                            | 3                    |                            | t <sub>sw</sub> |
| T <sub>JUNCTION</sub>            | Over-temperature Protection Threshold (Controller Junction Temperature) | Factory default                                  |                            | 125                  |                            | °C              |
|                                  |                                                                         | Configured using PMBus                           | <b>-40</b>                 |                      | <b>125</b>                 | °C              |
| T <sub>JUNCTION_HYS</sub>        | Thermal Protection Hysteresis                                           |                                                  |                            | 15                   |                            | °C              |

**Electrical Specifications**  $V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

| SYMBOL                                          | PARAMETER                                             | TEST CONDITIONS                                                          | MIN<br>(Note 14) | TYP | MAX<br>(Note 14) | UNITS |
|-------------------------------------------------|-------------------------------------------------------|--------------------------------------------------------------------------|------------------|-----|------------------|-------|
| <b>OSCILLATOR AND SWITCHING CHARACTERISTICS</b> |                                                       |                                                                          |                  |     |                  |       |
| $f_{SW\_RANGE}$                                 | Switching Frequency Range                             |                                                                          | <b>296</b>       |     | <b>1067</b>      | kHz   |
| $f_{SW\_ACCY}$                                  | Switching Frequency Set-Point Accuracy                |                                                                          | <b>-5</b>        |     | <b>+5</b>        | %     |
| EXT_SYNC <sub>PW</sub>                          | Minimum Pulse Width Required from External SYNC Clock | Measured at 50% amplitude                                                | <b>150</b>       |     |                  | ns    |
| EXT_SYNC <sub>DRIFT</sub>                       | Drift Tolerance for External SYNC Clock               | External SYNC Clock equal to 500kHz is not supported                     | <b>-10</b>       |     | <b>+10</b>       | %     |
| <b>LOGIC INPUT/OUTPUT CHARACTERISTICS</b>       |                                                       |                                                                          |                  |     |                  |       |
| $I_{LOGIC\_BIAS}$                               | Bias Current at the Logic Input Pins                  | DDC, EN, MGN, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, $V_{MON}$ , $V_{SET}$ | <b>-100</b>      |     | <b>+100</b>      | nA    |
| $V_{LOGIC\_IN\_LOW}$                            | Logic Input Low Threshold Voltage                     |                                                                          |                  |     | <b>0.8</b>       | V     |
| $V_{LOGIC\_IN\_HIGH}$                           | Logic Input High Threshold Voltage                    |                                                                          | <b>2.0</b>       |     |                  | V     |
| $V_{LOGIC\_OUT\_LOW}$                           | Logic Output Low Threshold Voltage                    | 2mA sinking                                                              |                  |     | <b>0.5</b>       | V     |
| $V_{LOGIC\_OUT\_HIGH}$                          | Logic Output High Threshold Voltage                   | 2mA sourcing                                                             | <b>2.25</b>      |     |                  | V     |
| <b>PMBus INTERFACE TIMING CHARACTERISTIC</b>    |                                                       |                                                                          |                  |     |                  |       |
| $f_{SMB}$                                       | PMBus Operating Frequency                             |                                                                          | <b>100</b>       |     | <b>400</b>       | kHz   |

## NOTES:

14. Compliance to datasheet limits is assured by one or more methods: Production test, characterization and/or design. Controller is independently tested before module assembly.
15.  $V_{OUT}$  measured at the termination of the VSENP and VSENN sense points.
16. The MAX load current is determined by the thermal "[Derating Curves](#)" on page 15 provided with this document.
17. "FS" stands for full scale of recommended maximum operation range.
18. " $t_{SW}$ " stands for time period of operation switching frequency.

# Typical Performance Curves

**Efficiency Performance** Operating condition:  $T_A = +25^\circ\text{C}$ , no air flow.  $C_{OUT} = 1340\mu\text{F}$ . Typical values are used unless otherwise noted.

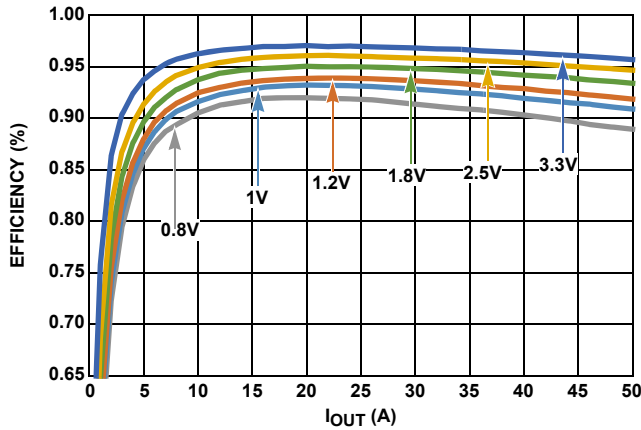


FIGURE 6. EFFICIENCY vs OUTPUT CURRENT AT  $V_{IN} = 5\text{V}$ ,  $f_{SW} = 300\text{kHz}$  FOR VARIOUS OUTPUT VOLTAGES

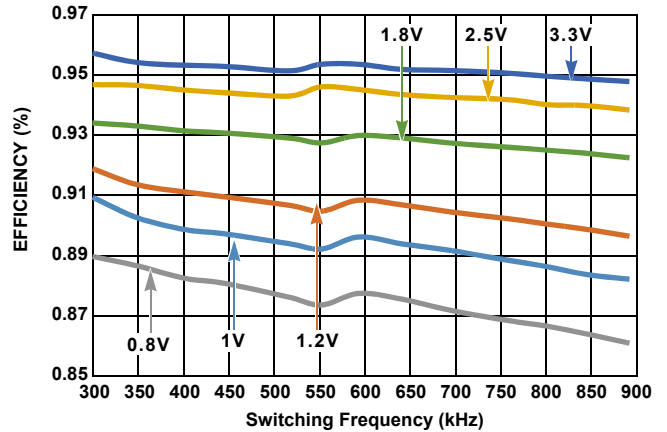


FIGURE 7. EFFICIENCY vs SWITCHING FREQUENCY AT  $V_{IN} = 5\text{V}$ ,  $I_{OUT} = 50\text{A}$  FOR VARIOUS OUTPUT VOLTAGES

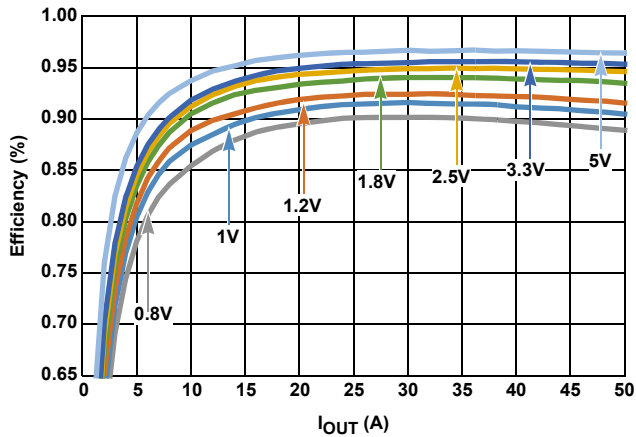


FIGURE 8. EFFICIENCY vs OUTPUT CURRENT AT  $V_{IN} = 9\text{V}$ ,  $f_{SW} = 300\text{kHz}$  FOR VARIOUS OUTPUT VOLTAGES

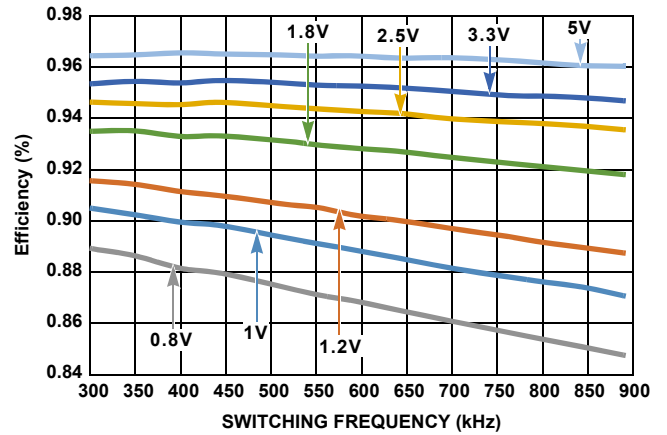


FIGURE 9. EFFICIENCY vs SWITCHING FREQUENCY AT  $V_{IN} = 9\text{V}$ ,  $I_{OUT} = 50\text{A}$  FOR VARIOUS OUTPUT VOLTAGES

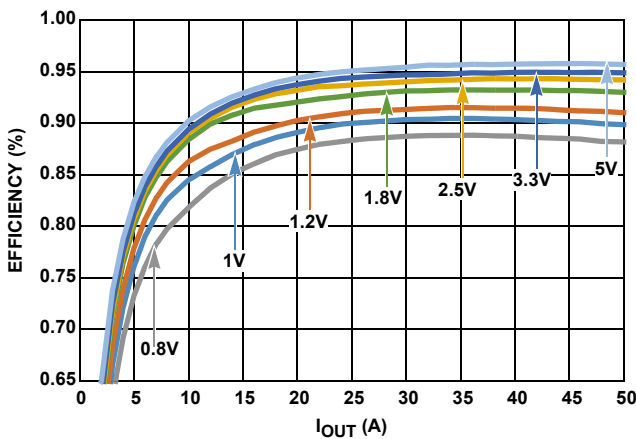


FIGURE 10. EFFICIENCY vs OUTPUT CURRENT AT  $V_{IN} = 12\text{V}$ ,  $f_{SW} = 300\text{kHz}$  FOR VARIOUS OUTPUT VOLTAGES

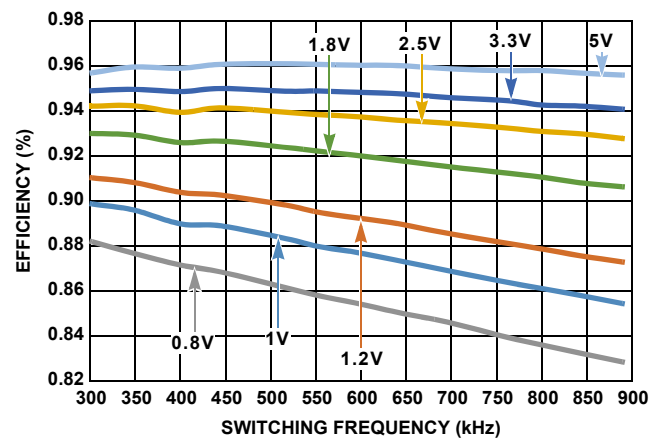


FIGURE 11. EFFICIENCY vs SWITCHING FREQUENCY AT  $V_{IN} = 12\text{V}$ ,  $I_{OUT} = 50\text{A}$  FOR VARIOUS OUTPUT VOLTAGES

## Typical Performance Curves (Continued)

**Transient Response Performance** Operating condition:  $V_{IN} = 12V$ ,  $f_{SW} = 533kHz$ ,  $I_{OUT} = 0A/25A$ ,  $I_{OUT}$  slew rate  $> 100A/\mu s$ ,  $T_A = +25^\circ C$ , no air flow. Typical values are used unless otherwise noted.

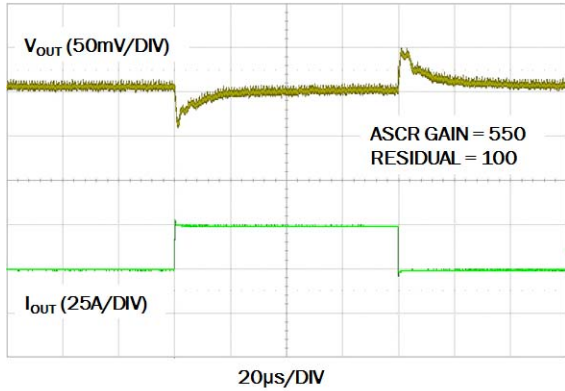


FIGURE 12. 1V TRANSIENT RESPONSE.  $C_{OUT} = 8 \times 100\mu F$  CERAMIC +  $4 \times 470\mu F$  POSCAP

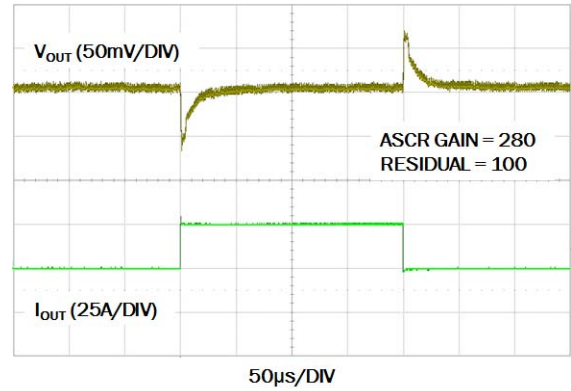


FIGURE 13. 1.8V TRANSIENT RESPONSE.  $C_{OUT} = 6 \times 100\mu F$  CERAMIC +  $2 \times 470\mu F$  POSCAP

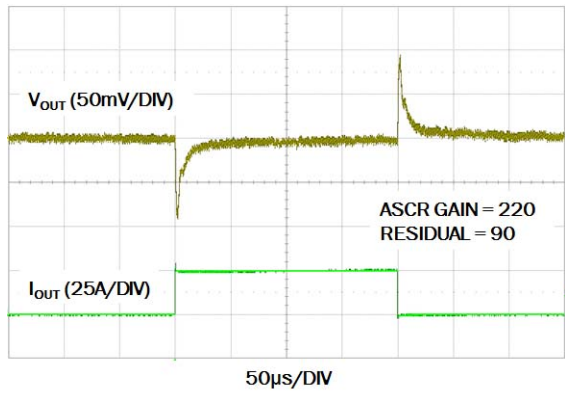


FIGURE 14. 2.5V TRANSIENT RESPONSE.  $C_{OUT} = 4 \times 100\mu F$  CERAMIC +  $2 \times 470\mu F$  POSCAP

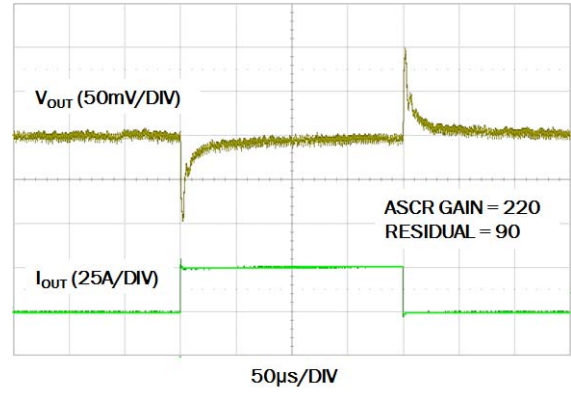


FIGURE 15. 3.3V TRANSIENT RESPONSE.  $C_{OUT} = 4 \times 100\mu F$  CERAMIC +  $2 \times 470\mu F$  POSCAP

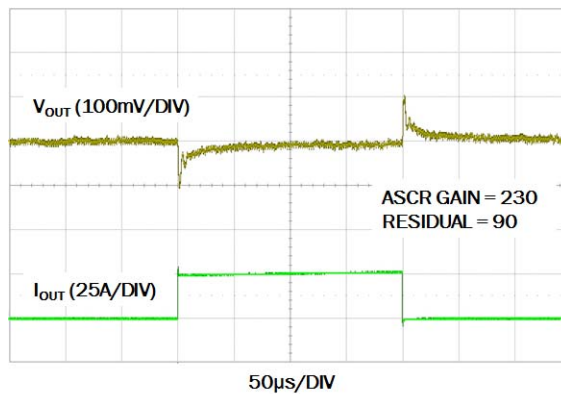


FIGURE 16. 5V TRANSIENT RESPONSE.  $C_{OUT} = 4 \times 100\mu F$  CERAMIC +  $2 \times 470\mu F$  POSCAP

## Typical Performance Curves (Continued)

**Derating Curves** All of the following curves were plotted at  $T_J = +115^\circ\text{C}$ .

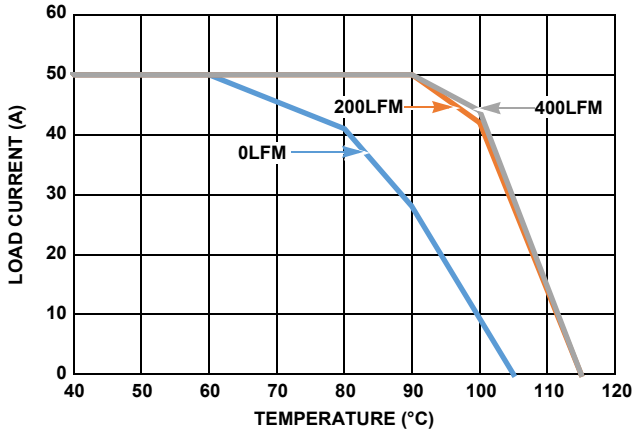


FIGURE 17.  $5V_{IN}$  TO  $1V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

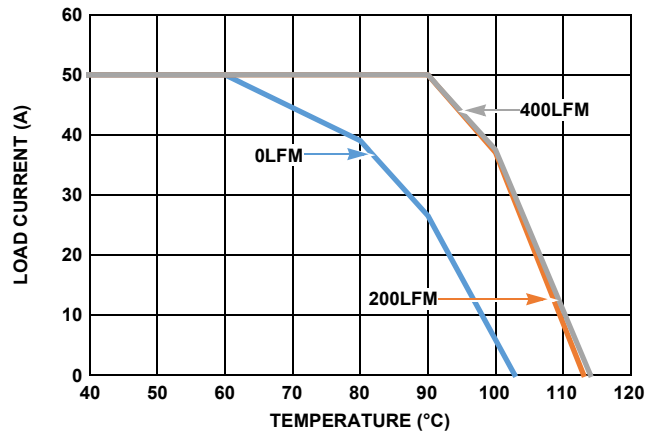


FIGURE 18.  $12V_{IN}$  TO  $1V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

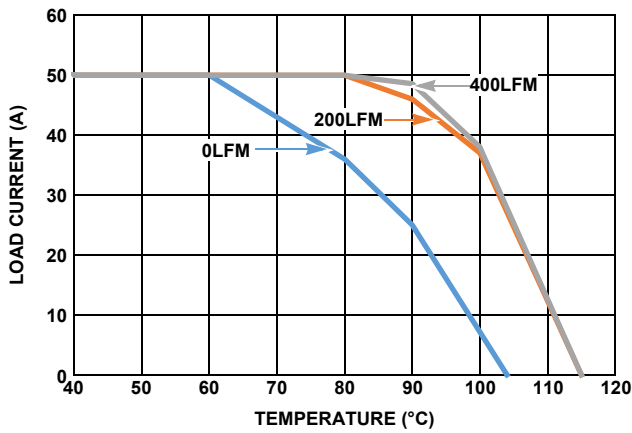


FIGURE 19.  $5V_{IN}$  TO  $1.8V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

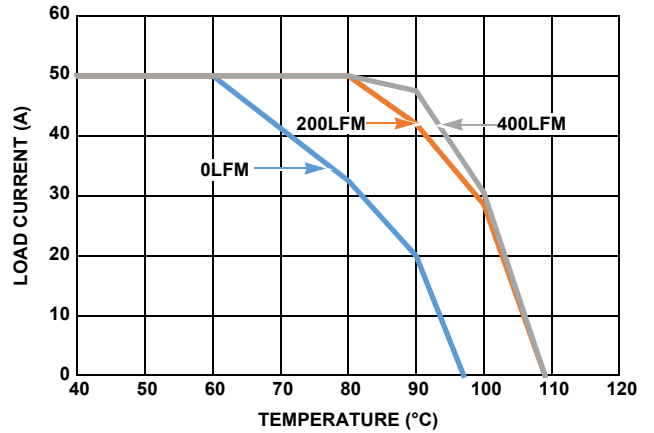


FIGURE 20.  $12V_{IN}$  TO  $1.8V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

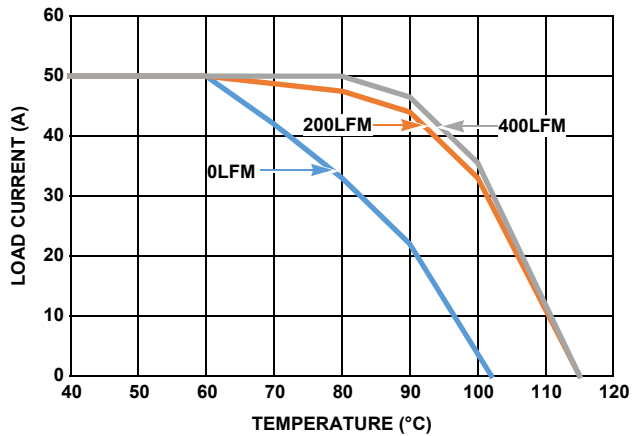


FIGURE 21.  $5V_{IN}$  TO  $2.5V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

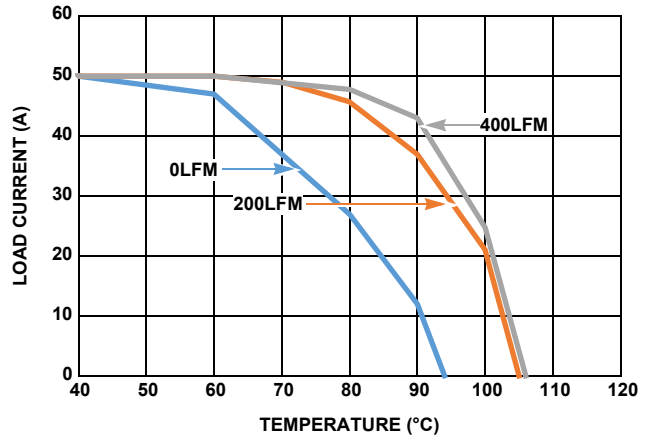


FIGURE 22.  $12V_{IN}$  TO  $2.5V_{OUT}$ ,  $f_{SW} = 300\text{kHz}$

## Typical Performance Curves (Continued)

### Derating Curves

All of the following curves were plotted at  $T_J = +115^\circ\text{C}$ .

The READ\_INTERNAL\_TEMP command value in the PowerNavigator™ software is the temperature reading value of the internal controller.

The junction temperature of the power stage in the module may be higher than the READ\_INTERNAL\_TEMP command value. The temperature difference depends on the operating conditions; in some extreme cases, the junction temperature of the power stage can be 30 °C higher than the READ\_INTERNAL\_TEMP command value.

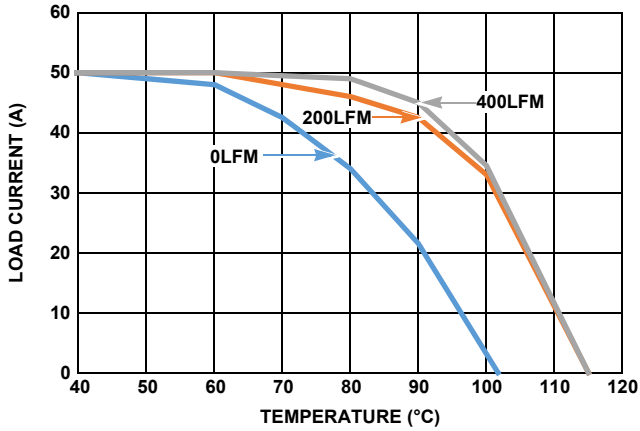


FIGURE 23. 5V<sub>IN</sub> TO 3.3V<sub>OUT</sub>, f<sub>SW</sub> = 300kHz

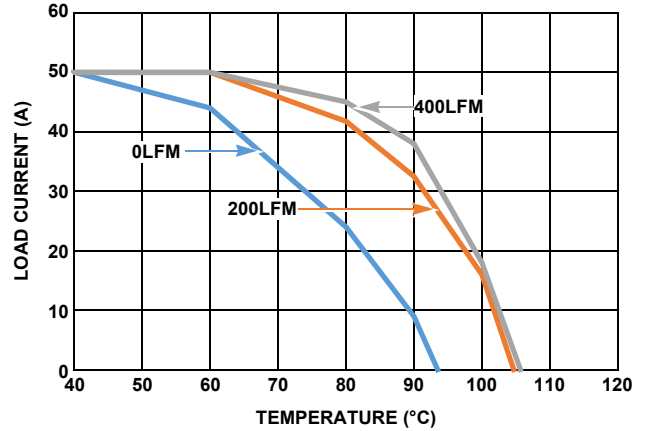


FIGURE 24. 12V<sub>IN</sub> TO 3.3V<sub>OUT</sub>, f<sub>SW</sub> = 533kHz

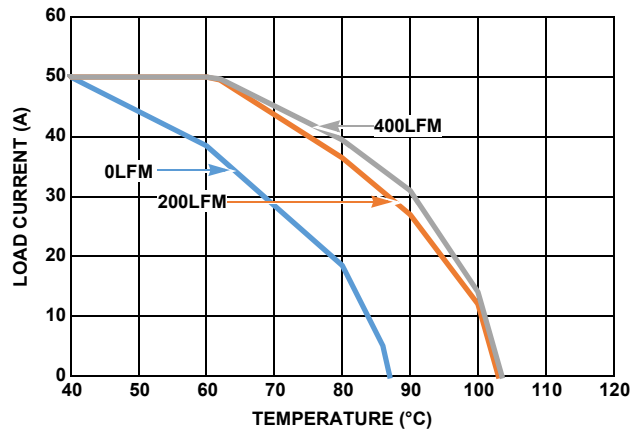


FIGURE 25. 12V<sub>IN</sub> TO 5V<sub>OUT</sub>, f<sub>SW</sub> = 533kHz



## Functional Description

### SMBus Communications

The ISL8272M provides a PMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ISL8272M can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The ISL8272M accepts most standard PMBus commands. When configuring the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

The SMBus device address is the only parameter that must be set by external pins. All other device parameters can be set with PMBus commands.

The ISL8272M can operate without the PMBus in pin-strap mode with configurations programmed by pin-strap resistors, such as output voltage, switching frequency, device SMBus address, input UVLO, soft-start/stop, and current sharing. Note: pin-strap resistors with 1% tolerance or better should be used for all the pin-strap settings.

### Output Voltage Selection

The output voltage may be set to a voltage between 0.6V and 5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET pin is used to set the output voltage to levels as shown in [Table 3](#). The R<sub>SET</sub> resistor is placed between the VSET pin and SGND. A standard 1% resistor is required.

TABLE 3. OUTPUT VOLTAGE RESISTOR SETTINGS

| V <sub>OUT</sub> (V) | R <sub>SET</sub> (kΩ)    |
|----------------------|--------------------------|
| 0.60                 | 10                       |
| 0.65                 | 11                       |
| 0.70                 | 12.1                     |
| 0.75                 | 13.3                     |
| 0.80                 | 14.7                     |
| 0.85                 | 16.2                     |
| 0.90                 | 17.8                     |
| 0.95                 | 19.6                     |
| 1.00                 | 21.5, or connect to SGND |
| 1.05                 | 23.7                     |
| 1.10                 | 26.1                     |
| 1.15                 | 28.7                     |
| 1.20                 | 31.6, or OPEN            |
| 1.25                 | 34.8                     |
| 1.30                 | 38.3                     |
| 1.40                 | 42.2                     |
| 1.50                 | 46.4                     |
| 1.60                 | 51.1                     |

TABLE 3. OUTPUT VOLTAGE RESISTOR SETTINGS (Continued)

| V <sub>OUT</sub> (V) | R <sub>SET</sub> (kΩ)  |
|----------------------|------------------------|
| 1.70                 | 56.2                   |
| 1.80                 | 61.9                   |
| 1.90                 | 68.1                   |
| 2.00                 | 75                     |
| 2.10                 | 82.5                   |
| 2.20                 | 90.9                   |
| 2.30                 | 100                    |
| 2.50                 | 110, or connect to V25 |
| 2.80                 | 121                    |
| 3.00                 | 133                    |
| 3.30                 | 147                    |
| 4.00                 | 162                    |
| 5.00                 | 178                    |

The output voltage may also be set to any value between 0.6V and 5V using the PMBus command VOUT\_COMMAND. This device supports dynamic voltage scaling by allowing change to the output voltage set point during regulation. The voltage transition rate is specified with the PMBus command VOUT\_TRANSITION\_RATE.

By default, V<sub>OUT\_MAX</sub> is set 110% higher than V<sub>OUT</sub> set by the pin strap resistor, which can be changed to any value up to 5.5V with the PMBus command VOUT\_MAX.

### Soft-Start/Stop Delay and Ramp Times

The ISL8272M follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. Once this process is completed, the device is ready to accept commands from the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V<sub>OUT</sub> to ramp to its target value after the delay period has expired. These features may be used as part of an overall in-rush current management strategy or to precisely control how fast a load IC is turned on. The ISL8272M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp up time can be programmed to custom values with the PMBus commands TON\_DELAY and TON\_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally

recommended to set the soft-start ramp to a value greater than 1ms to prevent inadvertent fault conditions due to excessive in-rush current.

Similar to the soft-start delay and ramp up time, the delay and ramp down time for soft-stop/off can be programmed with the PMBus commands TOFF\_DELAY and TOFF\_FALL. In addition, the module can be configured as “immediate off” with the command ON\_OFF\_CONFIG, such that the FETs are turned off immediately after the delay time expires.

In Current Sharing mode where multiple ISL8272M modules are connected in parallel, ASCR must be disabled for the ramp up with the USER\_CONFIG command. Therefore, the soft-start rise time is not equal to TON\_RISE. It can be calculated approximately by [Equation 1](#).

$$(EQ. 1) \quad \text{Rise Time (ms)} \approx \frac{\text{TON\_RISE}}{V_{\text{IN}} \times f_{\text{SW}}} \times 330\text{kHz} \times 12\text{V}$$

In Current Sharing mode, ASCR will be enabled automatically upon power good assertion after the ramp completes. To avoid premature ASCR turn on, it is recommended to increase POWER\_GOOD\_DELAY if the rise time exceeds 10ms. In addition, only “immediate off” is supported for current sharing.

The SS/UVLO pin can be used to program the soft start/stop delay time and ramp time to some typical values as shown in [Table 4](#). A standard 1% resistor is required.

**TABLE 4. SOFT START/STOP RESISTOR SETTINGS**

| DELAY TIME (ms) | RAMP TIME (ms) | R <sub>SET</sub> (kΩ)    |
|-----------------|----------------|--------------------------|
| 5               | 2              | 19.6, or connect to SGND |
| 10              | 2              | 21.5                     |
| 5               | 5              | 23.7, or OPEN            |
| 10              | 5              | 26.1                     |
| 20              | 5              | 28.7                     |
| 5               | 10             | 31.6                     |
| 10              | 10             | 34.8, or connect to V25  |
| 20              | 10             | 38.3                     |
| 5               | 2              | 42.2                     |
| 10              | 2              | 46.4                     |
| 5               | 5              | 51.1                     |
| 10              | 5              | 56.2                     |
| 20              | 5              | 61.9                     |
| 5               | 10             | 68.1                     |
| 10              | 10             | 75                       |
| 20              | 10             | 82.5                     |

## Power-Good

The ISL8272M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit may be changed using the PMBus command POWER\_GOOD\_ON.

A PG delay period is defined as the time from when all conditions within the ISL8272M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A PG delay can be programmed with the PMBus command POWER\_GOOD\_DELAY.

## Switching Frequency and PLL

The device's switching frequency is set from 296kHz to 1067kHz using the pin strap method (for standalone non-current sharing module only) as shown in [Table 5](#), or by using the PMBus command FREQUENCY\_SWITCH. The ISL8272M incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. The incoming clock signal must be in the range of 300kHz to 1.33MHz and must be stable when the enable pin is asserted. When using an external clock, the frequencies are not limited to discrete values as when using the internal clock. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. It is recommended that when using an external clock, the same frequency should be set in the FREQUENCY\_SWITCH command. In case the external clock is lost, the module will automatically switch to the internal clock. When using the internal oscillator, the SYNC pin can be configured as a clock source as an external sync to other modules. Refer to the SYNC\_CONFIG command on [page 48](#) for more information. Note: if the pin-strap method is used, a standard 1% resistor is required.

**TABLE 5. SWITCHING FREQUENCY RESISTOR SETTINGS**

| f <sub>SW</sub> (kHz) | R <sub>SET</sub> (kΩ)    |
|-----------------------|--------------------------|
| 296                   | 14.7, or connect to SGND |
| 320                   | 16.2                     |
| 364                   | 17.8                     |
| 400                   | 19.6                     |
| 421                   | 21.5, or OPEN            |
| 471                   | 23.7                     |
| 533                   | 26.1                     |
| 571                   | 28.7                     |
| 615                   | 31.6, or connect to V25  |
| 727                   | 34.8                     |
| 800                   | 38.3                     |
| 842                   | 42.2                     |
| 889                   | 46.4                     |
| 1067                  | 51.1                     |

## Loop Compensation

The module loop response is programmable using the PMBus command ASCR\_CONFIG or by using the pin-strap method (ASCR pin) according to [Table 6](#). A standard 1% resistor is required. The ISL8272M uses the ChargeMode™ control algorithm that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

TABLE 6. ASCR RESISTOR SETTINGS

| ASCR GAIN | ASCR RESIDUAL | R <sub>SET</sub> (kΩ)  |
|-----------|---------------|------------------------|
| 80        | 90            | 10                     |
| 120       | 90            | 11, or connect to SGND |
| 160       | 90            | 12.1                   |
| 200       | 90            | 13.3, or OPEN          |
| 240       | 90            | 14.7                   |
| 280       | 90            | 16.2                   |
| 320       | 90            | 17.8                   |
| 360       | 90            | 19.6                   |
| 400       | 90            | 21.5                   |
| 450       | 90            | 23.7                   |
| 500       | 90            | 26.1                   |
| 550       | 90            | 28.7                   |
| 600       | 90            | 31.6                   |
| 700       | 90            | 34.8                   |
| 800       | 90            | 38.3                   |
| 80        | 100           | 42.2                   |
| 120       | 100           | 46.4                   |
| 160       | 100           | 51.1                   |
| 200       | 100           | 56.2                   |
| 240       | 100           | 61.9                   |
| 280       | 100           | 68.1                   |
| 320       | 100           | 75                     |
| 360       | 100           | 82.5                   |
| 400       | 100           | 90.9                   |
| 450       | 100           | 100                    |
| 500       | 100           | 110, or connect to V25 |
| 550       | 100           | 121                    |
| 600       | 100           | 133                    |
| 700       | 100           | 147                    |
| 800       | 100           | 162                    |

## Input Undervoltage Lockout (UVLO)

The input undervoltage lockout (UVLO) prevents the ISL8272M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V<sub>UVLO</sub>) can be set between 4.18V and 16V by using a PMBus command VIN\_UV\_FAULT\_LIMIT. Using the pin strap method (SS/UVLO pin) as shown in [Table 7](#), allows to set the V<sub>UVLO</sub> to two typical values. A standard 1% resistor is required.

Fault response to an input undervoltage fault can be programmed with PMBus command VIN\_UV\_FAULT\_RESPONSE. If the input undervoltage fault retry is enabled, the module will shut down immediately once the input voltage falls below V<sub>UVLO</sub> and then check the input voltage every 70ms. If the input voltage rises above the input undervoltage warning level, the module will restart. The input undervoltage warning is 1.05\*V<sub>UVLO</sub> by default and can be programmed with the PMBus command VIN\_UV\_WARN\_LIMIT. Note that fault retry is not supported in the current sharing configuration.

TABLE 7. UVLO RESISTOR SETTINGS

| UVLO (V) | R <sub>SET</sub> (kΩ)                          |
|----------|------------------------------------------------|
| 4.5      | OPEN                                           |
| 4.5      | Connect to V25                                 |
| 4.5      | Connect to SGND                                |
| 4.5      | 19.6, 21.5, 23.7, 26.1, 28.7, 31.6, 34.8, 38.3 |
| 10.8     | 42.2, 46.4, 51.1, 56.2, 61.9, 68.1, 75, 82.5,  |

## SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. [Table 8](#) lists the available module addresses. A standard 1% resistor is required.

TABLE 8. SMBus ADDRESS RESISTOR SELECTION

| R <sub>SA</sub> (kΩ)     | SMBus ADDRESS |
|--------------------------|---------------|
| 10                       | 19h           |
| 11                       | 1Ah           |
| 12.1                     | 1Bh           |
| 13.3                     | 1Ch           |
| 14.7                     | 1Dh           |
| 16.2                     | 1Eh           |
| 17.8                     | 1Fh           |
| 19.6                     | 20h           |
| 21.5                     | 21h           |
| 23.7                     | 22h           |
| 26.1                     | 23h           |
| 28.7                     | 24h           |
| 31.6                     | 25h           |
| 34.8, or connect to SGND | 26h           |
| 38.3                     | 27h           |
| 42.2, or Open            | 28h           |
| 46.4                     | 29h           |
| 51.1                     | 2Ah           |
| 56.2                     | 2Bh           |
| 61.9                     | 2Ch           |
| 68.1                     | 2Dh           |
| 75                       | 2Eh           |

TABLE 8. SMBus ADDRESS RESISTOR SELECTION (Continued)

| $R_{SA}$ (k $\Omega$ ) | SMBus ADDRESS |
|------------------------|---------------|
| 82.5                   | 2Fh           |
| 90.9                   | 30h           |
| 100                    | 31h           |
| 110                    | 32h           |
| 121                    | 33h           |
| 133                    | 34h           |
| 147                    | 35h           |
| 162                    | 36h           |
| 178                    | 37h           |

## Output Overvoltage Protection

The ISL8272M offers an internal output overvoltage protection circuit that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator compares the actual output voltage (seen at the VSENp and VSENN pins) to a threshold set to 15% higher than the target output voltage (the default setting). The fault threshold can be programmed to a desired level with the PMBus command VOUT\_OV\_FAULT\_LIMIT. If the VSENp voltage exceeds this threshold, the module will initiate an immediate shutdown without retry. A 70ms continuous retry can be enabled with the PMBus command VOUT\_OV\_FAULT\_RESPONSE. Note that fault retry is not supported in the current sharing configuration.

Internal to the module, two 22 $\Omega$  resistors are populated from V<sub>OUT</sub> to VSENp and SGND to VSENN to protect from overvoltage conditions in case of open at voltage sensing pins and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V<sub>OUT</sub> regulation accuracy is not sacrificed.

## Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ISL8272M provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the pre-configured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage; however, the total time elapsed from when the delay period expires to when the output reaches its target value will match the pre-configured ramp time (see [Figure 26](#)).

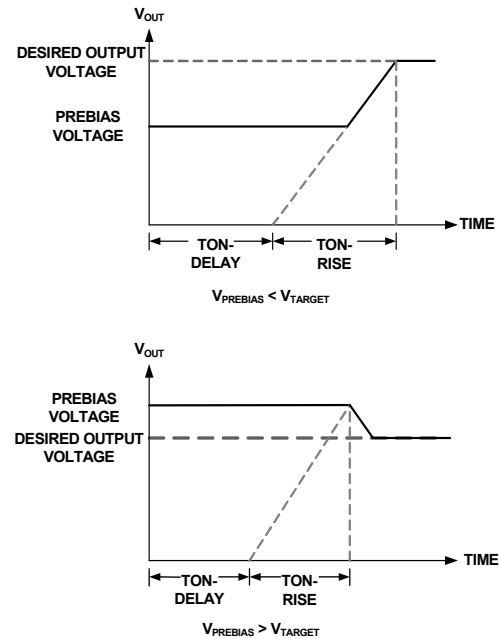


FIGURE 26. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage is higher than the target voltage after the pre-configured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

Once the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the pre-configured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition. The device then responds based on the output overvoltage fault response setting programmed with the PMBus command VOUT\_OV\_FAULT\_RESPONSE.

## Output Overcurrent Protection

The ISL8272M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Average output overcurrent fault threshold can be programmed with the PMBus command IOUT\_OC\_FAULT\_LIMIT. The module automatically programs the peak inductor current fault threshold by calculating the inductor ripple current from the input voltage, switching frequency, and the VOUT\_COMMAND. When the peak inductor current crosses the peak inductor current fault threshold for three successive switching cycles it will initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown without retry. A 70ms continuous retry can be enabled with the PMBus command MFR\_IOUT\_OC\_FAULT\_RESPONSE. It is required to enable the output undervoltage fault retry with the PMBus command VOUT\_UV\_FAULT\_RESPONSE command simultaneously if the overcurrent fault retry is enabled. Note that fault retry is not supported in the current sharing configuration.

### Thermal Overload Protection

The ISL8272M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but can be changed with PMBus command OT\_FAULT\_LIMIT.

The default response from an over-temperature fault is an immediate shutdown without retry. Retry settings can be programmed with the PMBus command OT\_FAULT\_RESPONSE. Hysteresis is implemented with the over-temperature fault retry. If retry is enabled, the module will shut down immediately upon an over-temperature fault event and then check the temperature every 70ms. If the temperature falls below the over-temperature warning level, the module will restart. The over-temperature warning is +105° by default and programmable with the PMBus command OT\_WARN\_LIMIT. Note that fault retry is not supported in the current sharing configuration.

### Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil digital power modules and digital controllers. This dedicated bus provides the communication channel between devices for features such as current sharing, sequencing, and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as shown in Equation 2:

$$(EQ. 2) \quad \text{Rise Time} = R_{PU} * C_{LOAD} < 1 \mu s$$

where  $R_{PU}$  is the DDC bus pull-up resistance and  $C_{LOAD}$  is the bus loading. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. In principle, each device connected to the DDC bus presents approximately 10pF of capacitive loading and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance.

### Active Current Sharing

Paralleling multiple ISL8272M modules can increase the output current capability of a single power rail. By connecting the DDC and SYNC pins of each module together and configuring the modules as a current sharing rail, the units will share the current equally within a few percent.

Figure 27 illustrates a typical connection for two modules.

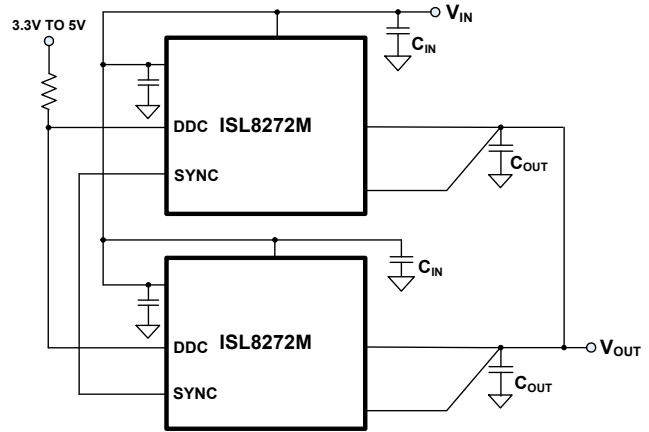


FIGURE 27. CURRENT SHARING GROUP

The ISL8272M uses a DDC bus based digital current sharing technique to balance the steady state module output current by aligning the load lines of member modules to a reference module.

When multiple ISL8272M modules are connected for current sharing, a non-zero active droop resistance must be set to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout. The active droop resistance can be programmed with the PMBus command VOUT\_DROOP based on Equation 3. Typically, higher droop value offers a more accurate dynamic current sharing at the sacrifice of output load regulation. 1% droop at full load will be a good trade-off between output load regulation and dynamic current sharing.

$$(EQ. 3) \quad \frac{V_{OUT}}{I_{LOAD(MAX)}} \times 0.005 \leq \text{Droop} \leq \frac{V_{OUT}}{I_{LOAD(MAX)}} \times 0.015$$

Upon system start-up, the module with the lowest device position as selected in DDC\_CONFIG is defined as the reference module. The remaining modules are members. The reference module broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages ( $V_{MEMBER}$ ) to balance the current loading of each module in the system.

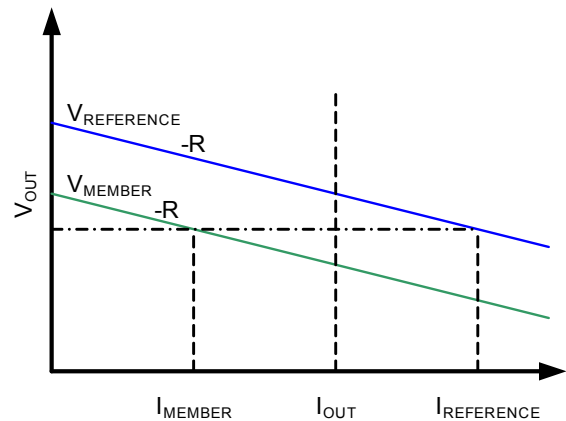


FIGURE 28. ACTIVE CURRENT SHARING



Figure 28 on page 21 shows that, for load lines with identical slopes, the member voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by Equation 4:

$$(EQ. 4) \quad V_{MEMBER} = V_{OUT} + R \times (I_{REFERENCE} - I_{MEMBER})$$

where  $R$  is the value of the droop resistance.

The DDC\_CONFIG command configures the module for active current sharing. The default setting is a standalone non current sharing module.

For fault configuration, it is required to enable the fault spreading mode in the current sharing rail with the PMBus command DDC\_GROUP. Broadcast operation must be enabled with the DDC\_GROUP command to allow start up/shut down and margining operations. It is optional to enable  $V_{OUT}$  broadcast in the DDC\_GROUP command to allow  $V_{OUT}$  set point change dynamically during operation.

In the multiple-module current sharing configuration, it is required to synchronize all modules to the same switching clock by tying the SYNC pins together. The clock source can be selected either from one module or from an external clock with the SYNC\_CONFIG command. The phase offset of current sharing modules is automatically set according to the device positions and number of devices specified in the DDC\_CONFIG command.

The pin strap method is offered for the current sharing configuration with the CS pin. Table 9 lists the current sharing pin strap settings. A standard 1% resistor is required. Note that fault retry is not supported in the current sharing configuration.

TABLE 9. CURRENT SHARING RESISTOR SETTINGS

| CLOCK CONFIGURATION | DEVICE POSITION - NUMBER OF DEVICES | DROOP (mV/A) | R <sub>SET</sub> (kΩ) |
|---------------------|-------------------------------------|--------------|-----------------------|
| Output internal     | 1-2                                 | 0.1          | 10                    |
| External            | 2-2                                 | 0.1          | 11                    |
| Output internal     | 1-2                                 | 0.15         | 12.1                  |
| External            | 2-2                                 | 0.15         | 13.3                  |
| Output internal     | 1-2                                 | 0.2          | 14.7                  |
| External            | 2-2                                 | 0.2          | 16.2                  |
| Output internal     | 1-2                                 | 0.25         | 17.8                  |
| External            | 2-2                                 | 0.25         | 19.6                  |
| Output internal     | 1-2                                 | 0.3          | 21.5                  |
| External            | 2-2                                 | 0.3          | 23.7                  |
| Output internal     | 1-3                                 | 0.07         | 26.1                  |
| External            | 2-3                                 | 0.07         | 28.7                  |
| External            | 3-3                                 | 0.07         | 31.6                  |
| Output internal     | 1-3                                 | 0.1          | 34.8                  |
| External            | 2-3                                 | 0.1          | 38.3                  |
| External            | 3-3                                 | 0.1          | 42.2                  |

TABLE 9. CURRENT SHARING RESISTOR SETTINGS (Continued)

| CLOCK CONFIGURATION | DEVICE POSITION - NUMBER OF DEVICES | DROOP (mV/A) | R <sub>SET</sub> (kΩ)                   |
|---------------------|-------------------------------------|--------------|-----------------------------------------|
| Output internal     | 1-3                                 | 0.13         | 46.4                                    |
| External            | 2-3                                 | 0.13         | 51.1                                    |
| External            | 3-3                                 | 0.13         | 56.2                                    |
| Output internal     | 1-3                                 | 0.16         | 61.9                                    |
| External            | 2-3                                 | 0.16         | 68.1                                    |
| External            | 3-3                                 | 0.16         | 75                                      |
| Output internal     | 1-3                                 | 0.2          | 82.5                                    |
| External            | 2-3                                 | 0.2          | 90.9                                    |
| External            | 3-3                                 | 0.2          | 100                                     |
| Output internal     | 1-4                                 | 0.14         | 110 (available with FC02 firmware only) |
| External            | 2-4                                 | 0.14         | 121 (available with FC02 firmware only) |
| External            | 3-4                                 | 0.14         | 133 (available with FC02 firmware only) |
| External            | 4-4                                 | 0.14         | 147 (available with FC02 firmware only) |
| Internal only       | 1-1                                 | 0            | Connect to SGND (for immediate off)     |
| Internal only       | 1-1                                 | 0            | OPEN (for soft off)                     |

## Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the  $I_{RMS}^2$  are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments with the PMBus command INTERLEAVE. The internal two phases of the module always maintain a phase difference of 180°.

## Fault Spreading

Digital-DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group with the PMBus command DDC\_GROUP. When a nondestructive fault occurs, the device shuts down and broadcasts the fault

event over the DDC bus. The other devices on the DDC bus shut down simultaneously if configured to do so, and attempt to restart.

Note that fault retry is not supported in multiple modules with fault spreading enabled, such as the current sharing configuration.

## Output Sequencing

A group of Digital-DC modules or devices may be configured to power-up in a predetermined sequence. This feature is especially useful when powering advanced processors (FPGAs and ASICs) that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up. Multi-device sequencing can be achieved by configuring each device with the PMBus command SEQUENCE. Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows in the sequencing.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group. It is recommended to enable fault spreading with the PMBus command DDC\_GROUP within a sequencing group.

## Monitoring with SMBus

A system controller can monitor a wide variety of different ISL8272M system parameters with PMBus commands:

- READ\_VIN
- READ\_VOUT
- READ\_IOUT
- READ\_INTERNAL\_TEMP
- READ\_DUTY\_CYCLE
- READ\_FREQUENCY
- READ\_VMON

## Snapshot Parameter Capture

The ISL8272M offers a special feature to capture parametric data and some fault status following a fault. A detailed description is provided in [“PMBus Commands Description” on page 29](#) under the PMBus commands SNAPSHOT and SNAPSHOT\_CONTROL.

## Nonvolatile Memory

The ISL8272M has internal nonvolatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them. During the initialization process, the ISL8272M checks for stored values contained in its internal nonvolatile memory.

Modules are shipped with a factory default configuration and most settings can be overwritten with PMBus commands and can be stored in nonvolatile memory with the PMBus command STORE\_USER\_ALL.

## Layout Guide

To achieve stable operation, low losses, and good thermal performance, proper layout ([Figure 29](#)) is important.

- Establish separate SGND plane and PGND planes, then connect SGND to the PGND plane on the middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5, and M17..., use multiple vias for each pin to connect to the inner SGND or PGND layer.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND and bypass capacitors between VDD, VDRV and the ground plane, as close to the module as possible to minimize high frequency noise. It is critical to place the output ceramic capacitors as close to the center of the two VOUT pads as possible, to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. It is recommended to enlarge PAD11 and PAD15 and to put more vias on these pads. The ceramic caps CIN can be put on the bottom layer under these two pads.
- Connect remote sensed traces to the regulation points to achieve a tight output voltage regulation and keep them in parallel. Route a trace from VSENN and VSENP to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing point near the SW pins.
- The SW1 and SW2 pads are noisy pads, but they are beneficial for thermal dissipations. If the noise issue is critical for the applications, it is recommended to use top layer only for SW pads. For better thermal performance, use multiple vias on these pads to connect into SW inner and bottom layer. However, be very careful when placing limited SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop wires. The wire width should be greater than 20 mils.

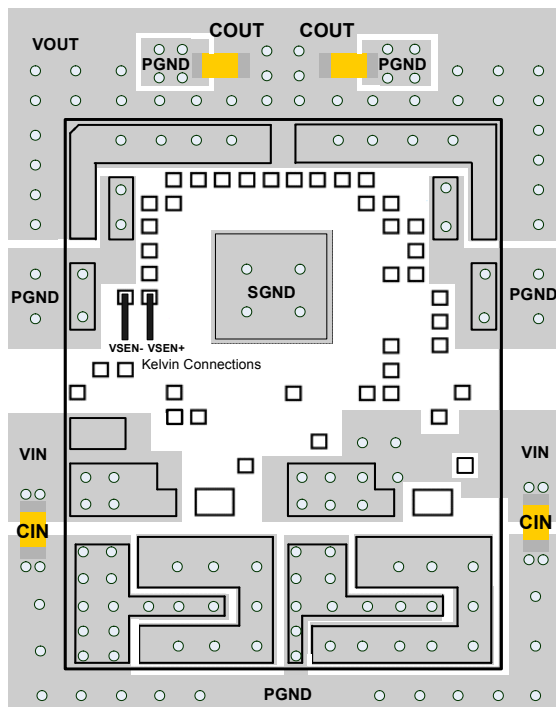


FIGURE 29. RECOMMENDED LAYOUT

## Thermal Considerations

Experimental power loss curves along with  $\theta_{JA}$  from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual applications, other heat sources and design margins should be considered.

## Package Description

The structure of the ISL8272M belongs to the High Density Array No-lead package (HDA). This package offers good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8272M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8272M is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the [“Package Outline Drawing”](#) starting on [page 53](#). The module has a small size of 18mmx23mmx7.5mm.

## PCB Layout Pattern Design

The bottom of the ISL8272M is a lead-frame footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on [pages 57 to 59](#). The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout

also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

## Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

## Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the [“Package Outline Drawing”](#) starting on [page 55](#). The gap width between pad to pad is 0.6mm. Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls, resulting in reduced surface friction and better paste release which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

## Reflow Parameters

Due to the HDA's low mount height, “No Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile in [Figure 30](#) is a guideline to be customized for varying manufacturing practices and applications.

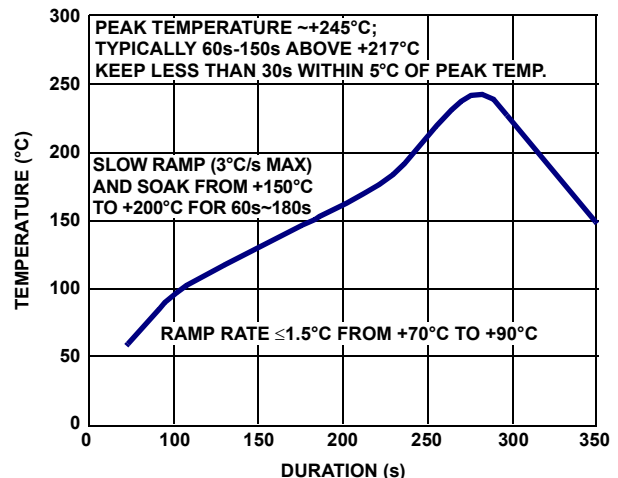


FIGURE 30. TYPICAL REFLOW PROFILE



## PMBus Command Summary

| COMMAND CODE | COMMAND NAME           | DESCRIPTION                                                                  | TYPE      | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING             | PAGE               |
|--------------|------------------------|------------------------------------------------------------------------------|-----------|-------------|---------------|-----------------------------|--------------------|
| 01h          | OPERATION              | Sets Enable, Disable and $V_{OUT}$ Margin modes.                             | R/W BYTE  | BIT         |               |                             | <a href="#">29</a> |
| 02h          | ON_OFF_CONFIG          | Configures the EN pin and PMBus commands to turn the unit ON/OFF             | R/W BYTE  | BIT         | 16h           | Hardware Enable, Soft Off   | <a href="#">29</a> |
| 03h          | CLEAR_FAULTS           | Clears fault indications.                                                    | SEND BYTE |             |               |                             | <a href="#">30</a> |
| 15h          | STORE_USER_ALL         | Stores all PMBus values written since last restore at user level.            | SEND BYTE |             |               |                             | <a href="#">30</a> |
| 16h          | RESTORE_USER_ALL       | Restores PMBus settings that were stored using STORE_USER_ALL.               | SEND BYTE |             |               |                             | <a href="#">30</a> |
| 20h          | VOUT_MODE              | Preset to defined data format of $V_{OUT}$ commands.                         | READ BYTE | BIT         | 13h           | Linear Mode, Exponent = -13 | <a href="#">30</a> |
| 21h          | VOUT_COMMAND           | Sets the nominal value of the output voltage.                                | R/W WORD  | L16u        |               | Pin Strap                   | <a href="#">30</a> |
| 23h          | VOUT_CAL_OFFSET        | Applies a fixed offset voltage to the VOUT_COMMAND.                          | R/W WORD  | L16s        | 0000h         | 0V                          | <a href="#">31</a> |
| 24h          | VOUT_MAX               | Sets the maximum possible value of $V_{OUT}$ . 110% of pin strap $V_{OUT}$ . | R/W WORD  | L16u        |               | $1.1 * V_{OUT}$ Pin Strap   | <a href="#">31</a> |
| 25h          | VOUT_MARGIN_HIGH       | Sets the value of the $V_{OUT}$ during a margin high.                        | R/W WORD  | L16u        |               | $1.05 * V_{OUT}$ Pin Strap  | <a href="#">31</a> |
| 26h          | VOUT_MARGIN_LOW        | Sets the value of the $V_{OUT}$ during a margin low.                         | R/W WORD  | L16u        |               | $0.95 * V_{OUT}$ Pin Strap  | <a href="#">31</a> |
| 27h          | VOUT_TRANSITION_RATE   | Sets the transition rate during margin or other change of $V_{OUT}$ .        | R/W WORD  | L11         | BA00h         | 1V/ms                       | <a href="#">31</a> |
| 28h          | VOUT_DROOP             | Sets the loadline (V/I Slope) resistance for the rail.                       | R/W WORD  | L11         |               | Pin Strap                   | <a href="#">32</a> |
| 33h          | FREQUENCY_SWITCH       | Sets the switching frequency.                                                | R/W WORD  | L11         |               | Pin Strap                   | <a href="#">32</a> |
| 37h          | INTERLEAVE             | Configures a phase offset between devices sharing a SYNC clock.              | R/W WORD  | BIT         | 0000h         |                             | <a href="#">32</a> |
| 38h          | IOUT_CAL_GAIN          | Sense resistance for inductor DCR current sensing.                           | R/W WORD  | L11         | B370h         | 0.86m $\Omega$              | <a href="#">32</a> |
| 39h          | IOUT_CAL_OFFSET        | Sets the current-sense offset.                                               | R/W WORD  | L11         | 0000h         | 0A                          | <a href="#">32</a> |
| 40h          | VOUT_OV_FAULT_LIMIT    | Sets the $V_{OUT}$ overvoltage fault threshold.                              | R/W WORD  | L16u        |               | $1.15 * V_{OUT}$ Pin Strap  | <a href="#">33</a> |
| 41h          | VOUT_OV_FAULT_RESPONSE | Configures the $V_{OUT}$ overvoltage fault response.                         | R/W BYTE  | BIT         | 80h           | Disable and No Retry        | <a href="#">33</a> |
| 42h          | VOUT_OV_WARN_LIMIT     | Sets the $V_{OUT}$ overvoltage warn threshold.                               | R/W WORD  | L16u        |               | $1.10 * V_{OUT}$ Pin Strap  | <a href="#">33</a> |
| 43h          | VOUT_UV_WARN_LIMIT     | Sets the $V_{OUT}$ undervoltage warn threshold.                              | R/W WORD  | L16u        |               | $0.9 * V_{OUT}$ Pin Strap   | <a href="#">33</a> |
| 44h          | VOUT_UV_FAULT_LIMIT    | Sets the $V_{OUT}$ undervoltage fault threshold.                             | R/W WORD  | L16u        |               | $0.85 * V_{OUT}$ Pin Strap  | <a href="#">33</a> |
| 45h          | VOUT_UV_FAULT_RESPONSE | Configures the $V_{OUT}$ undervoltage fault response.                        | R/W BYTE  | BIT         | 80h           | Disable and No Retry        | <a href="#">34</a> |
| 46h          | IOUT_OC_FAULT_LIMIT    | Sets the $I_{OUT}$ average overcurrent fault threshold.                      | R/W WORD  | L11         | E3C0h         | 60A                         | <a href="#">34</a> |
| 4Bh          | IOUT_UC_FAULT_LIMIT    | Sets the $I_{OUT}$ average undercurrent fault threshold.                     | R/W WORD  | L11         | E440h         | -60A                        | <a href="#">34</a> |
| 4Fh          | OT_FAULT_LIMIT         | Sets the over-temperature fault threshold.                                   | R/W WORD  | L11         | EBE8h         | +125 °C                     | <a href="#">34</a> |
| 50h          | OT_FAULT_RESPONSE      | Configures the over-temperature fault response.                              | R/W BYTE  | BIT         | 80h           | Disable and No Retry        | <a href="#">35</a> |

## PMBus Command Summary (Continued)

| COMMAND CODE | COMMAND NAME          | DESCRIPTION                                                        | TYPE      | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING                       | PAGE               |
|--------------|-----------------------|--------------------------------------------------------------------|-----------|-------------|---------------|---------------------------------------|--------------------|
| 51h          | OT_WARN_LIMIT         | Sets the over-temperature warning limit.                           | R/W WORD  | L11         | EB48h         | +105 °C                               | <a href="#">35</a> |
| 52h          | UT_WARN_LIMIT         | Sets the under-temperature warning limit.                          | R/W WORD  | L11         | DC40h         | -30 °C                                | <a href="#">35</a> |
| 53h          | UT_FAULT_LIMIT        | Sets the under-temperature fault threshold.                        | R/W WORD  | L11         | E580h         | -40 °C                                | <a href="#">35</a> |
| 54h          | UT_FAULT_RESPONSE     | Configures the under-temperature fault response.                   | R/W BYTE  | BIT         | 80h           | Disable and No Retry                  | <a href="#">36</a> |
| 55h          | VIN_OV_FAULT_LIMIT    | Sets the $V_{IN}$ overvoltage fault threshold.                     | R/W WORD  | L11         | D380h         | 14V                                   | <a href="#">36</a> |
| 56h          | VIN_OV_FAULT_RESPONSE | Configures the $V_{IN}$ overvoltage fault response.                | R/W BYTE  | BIT         | 80h           | Disable and No Retry                  | <a href="#">36</a> |
| 57h          | VIN_OV_WARN_LIMIT     | Sets the input overvoltage warning limit.                          | R/W WORD  | L11         | D353h         | 13.3V                                 | <a href="#">36</a> |
| 58h          | VIN_UV_WARN_LIMIT     | Sets the input undervoltage warning limit.                         | R/W WORD  | L11         |               | $1.05 \cdot V_{IN}$<br>UV Fault Limit | <a href="#">37</a> |
| 59h          | VIN_UV_FAULT_LIMIT    | Sets the $V_{IN}$ undervoltage fault threshold.                    | R/W WORD  | L11         |               | Pin Strap                             | <a href="#">37</a> |
| 5Ah          | VIN_UV_FAULT_RESPONSE | Configures the $V_{IN}$ undervoltage fault response.               | R/W BYTE  | BIT         | 80h           | Disable and No Retry                  | <a href="#">37</a> |
| 5Eh          | POWER_GOOD_ON         | Sets the voltage threshold for Power-Good indication.              | R/W WORD  | L16u        |               | $0.9 \cdot V_{OUT}$<br>Pin Strap      | <a href="#">37</a> |
| 60h          | TON_DELAY             | Sets the delay time from ENABLE to start of $V_{OUT}$ rise.        | R/W WORD  | L11         |               | Pin Strap                             | <a href="#">37</a> |
| 61h          | TON_RISE              | Sets the rise time of $V_{OUT}$ after ENABLE and TON_DELAY.        | R/W WORD  | L11         |               | Pin Strap                             | <a href="#">38</a> |
| 64h          | TOFF_DELAY            | Sets the delay time from DISABLE to start of $V_{OUT}$ fall.       | R/W WORD  | L11         |               | Pin Strap                             | <a href="#">38</a> |
| 65h          | TOFF_FALL             | Sets the fall time for $V_{OUT}$ after DISABLE and TOFF_DELAY.     | R/W WORD  | L11         |               | Pin Strap                             | <a href="#">38</a> |
| 78h          | STATUS_BYTE           | Returns an abbreviated status for fast reads.                      | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">38</a> |
| 79h          | STATUS_WORD           | Returns information with a summary of the units's fault condition. | READ WORD | BIT         | 0000h         | No Faults                             | <a href="#">39</a> |
| 7Ah          | STATUS_VOUT           | Returns the $V_{OUT}$ specific status.                             | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">39</a> |
| 7Bh          | STATUS_IOUT           | Returns the $I_{OUT}$ specific status.                             | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">40</a> |
| 7Ch          | STATUS_INPUT          | Returns specific status specific to the input.                     | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">40</a> |
| 7Dh          | STATUS_TEMPERATURE    | Returns the temperature specific status.                           | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">40</a> |
| 7Eh          | STATUS_CML            | Returns the Communication, Logic and Memory specific status.       | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">41</a> |
| 80h          | STATUS_MFR_SPECIFIC   | Returns the VMON and External Sync clock specific status.          | READ BYTE | BIT         | 00h           | No Faults                             | <a href="#">41</a> |
| 88h          | READ_VIN              | Returns the input voltage reading.                                 | READ WORD | L11         |               |                                       | <a href="#">41</a> |
| 8Bh          | READ_VOUT             | Returns the output voltage reading.                                | READ WORD | L16u        |               |                                       | <a href="#">41</a> |
| 8Ch          | READ_IOUT             | Returns the output current reading.                                | READ WORD | L11         |               |                                       | <a href="#">42</a> |
| 8Dh          | READ_INTERNAL_TEMP    | Returns the temperature reading internal to the device.            | READ WORD | L11         |               |                                       | <a href="#">42</a> |

## PMBus Command Summary (Continued)

| COMMAND CODE | COMMAND NAME               | DESCRIPTION                                                               | TYPE       | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING                               | PAGE               |
|--------------|----------------------------|---------------------------------------------------------------------------|------------|-------------|---------------|-----------------------------------------------|--------------------|
| 94h          | READ_DUTY_CYCLE            | Returns the duty cycle reading during the ENABLE state.                   | READ WORD  | L11         |               |                                               | <a href="#">42</a> |
| 95h          | READ_FREQUENCY             | Returns the measured operating switch frequency.                          | READ WORD  | L11         |               |                                               | <a href="#">42</a> |
| 96h          | READ_IOUT_0                | Returns phase 1 current reading.                                          | READ WORD  | L11         |               |                                               | <a href="#">42</a> |
| 97h          | READ_IOUT_1                | Returns phase 2 current reading.                                          | READ WORD  | L11         |               |                                               | <a href="#">42</a> |
| 99h          | MFR_ID                     | Sets a user defined identification.                                       | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">43</a> |
| 9Ah          | MFR_MODEL                  | Sets a user defined model.                                                | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">43</a> |
| 9Bh          | MFR_REVISION               | Sets a user defined revision.                                             | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">43</a> |
| 9Ch          | MFR_LOCATION               | Sets a user defined location identifier.                                  | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">43</a> |
| 9Dh          | MFR_DATE                   | Sets a user defined date.                                                 | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">43</a> |
| 9Eh          | MFR_SERIAL                 | Sets a user defined serialized identifier.                                | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">44</a> |
| A8H          | LEGACY_FAULT_GROUP         | Sets rail IDs of legacy devices for fault spreading                       | R/W BLOCK  | BIT         | 00000000h     | No rail ID specified                          | <a href="#">44</a> |
| B0h          | USER_DATA_00               | Sets a user defined data.                                                 | R/W BLOCK  | ASC         |               | Null                                          | <a href="#">44</a> |
| D0h          | ISENSE_CONFIG              | Configures ISENSE related features.                                       | R/W BYTE   | BIT         | 05h           | 256ns Blanking Time, Mid Range                | <a href="#">44</a> |
| D1h          | USER_CONFIG                | Configures several user-level features.                                   | R/W BYTE   | BIT         |               | Pin Strap (ASCR on/off for start up)          | <a href="#">45</a> |
| D3h          | DDC_CONFIG                 | Configures the DDC bus.                                                   | R/W WORD   | BIT         |               | Pin Strap (set based on PMBus address and CS) | <a href="#">45</a> |
| D4h          | POWER_GOOD_DELAY           | Sets the delay between $V_{OUT} > PG$ threshold and asserting the PG pin. | R/W WORD   | L11         | C300h         | 3ms                                           | <a href="#">46</a> |
| DFh          | ASCR_CONFIG                | Configures ASCR control loop.                                             | R/W BLOCK  | CUS         |               | Pin Strap                                     | <a href="#">46</a> |
| E0h          | SEQUENCE                   | Identifies the Rail DDC ID to perform multi-rail sequencing.              | R/W WORD   | BIT         | 0000h         | Prequel and Sequel Disabled                   | <a href="#">46</a> |
| E2h          | DDC_GROUP                  | Sets rail DDC IDs to obey faults and margining spreading information.     | R/W BLOCK  | BIT         |               | Pin Strap (set based on CS)                   | <a href="#">47</a> |
| E4h          | DEVICE_ID                  | Returns the 16-byte (character) device identifier string.                 | READ BLOCK | ASC         |               | Reads Device Version                          | <a href="#">47</a> |
| E5h          | MFR_IOUT_OC_FAULT_RESPONSE | Configures the $I_{OUT}$ overcurrent fault response.                      | R/W BYTE   | BIT         | 80h           | Disable and No Retry                          | <a href="#">47</a> |
| E6h          | MFR_IOUT_UC_FAULT_RESPONSE | Configures the $I_{OUT}$ undercurrent fault response.                     | R/W BYTE   | BIT         | 80h           | Disable and No Retry                          | <a href="#">48</a> |
| E9h          | SYNC_CONFIG                | Configures the Sync pin.                                                  | R/W BYTE   | BIT         |               | Pin Strap (set based on CS)                   | <a href="#">48</a> |
| EAh          | SNAPSHOT                   | Returns 32-byte read-back of parametric and status values.                | READ BLOCK | BIT         |               |                                               | <a href="#">49</a> |
| EBh          | BLANK_PARAMS               | Returns recently changed parameter values.                                | READ BLOCK | BIT         | FF...FFh      |                                               | <a href="#">49</a> |
| F3h          | SNAPSHOT_CONTROL           | Snapshot feature control command.                                         | R/W BYTE   | BIT         |               |                                               | <a href="#">49</a> |
| F4h          | RESTORE_FACTORY            | Restores device to the factory default values.                            | SEND BYTE  |             |               |                                               | <a href="#">50</a> |
| F5h          | MFR_VMON_OV_FAULT_LIMIT    | Returns the VMON overvoltage threshold.                                   | READ WORD  | L11         | CB00h         | 6V                                            | <a href="#">50</a> |

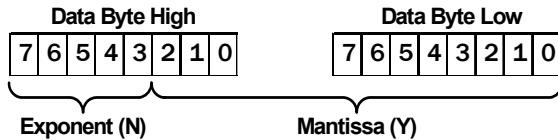
## PMBus Command Summary (Continued)

| COMMAND CODE | COMMAND NAME            | DESCRIPTION                              | TYPE      | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING      | PAGE               |
|--------------|-------------------------|------------------------------------------|-----------|-------------|---------------|----------------------|--------------------|
| F6h          | MFR_VMON_UV_FAULT_LIMIT | Returns the VMON undervoltage threshold. | READ WORD | L11         | CA00h         | 4V                   | <a href="#">50</a> |
| F7h          | MFR_READ_VMON           | Returns the VMON voltage reading.        | READ WORD | L11         |               |                      | <a href="#">50</a> |
| F8h          | VMON_OV_FAULT_RESPONSE  | Returns the VMON overvoltage response.   | READ BYTE | BIT         | 80h           | Disable and No Retry | <a href="#">50</a> |
| F9h          | VMON_UV_FAULT_RESPONSE  | Returns the VMON undervoltage response.  | READ BYTE | BIT         | 80h           | Disable and No Retry | <a href="#">50</a> |

## PMBus Data Formats

### Linear-11 (L11)

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X).



The relation between real world decimal value (X), N and Y is:  $X = Y \cdot 2^N$

### Linear-16 Unsigned (L16u)

L16u data format uses a fixed exponent (hard-coded to  $N = -13h$ ) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is:  $X = Y \cdot 2^{-13}$

### Linear-16 Signed (L16s)

The L16s data format uses a fixed exponent (hard-coded to  $N = -13h$ ) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X).

Relation between real world decimal value (X), N and Y is:  $X = Y \cdot 2^{-13}$

### Bit Field (BIT)

An explanation of Bit Field is provided in [“PMBus Commands Description” on page 29](#).

### Custom (CUS)

An explanation of Custom data format is provided in [“PMBus Commands Description” on page 29](#). A combination of Bit Field and integer are common type of Custom data format.

### ASCII (ASC)

A variable length string of text characters that uses the ASCII data format.

## PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON\_OFF\_CONFIG, CLEAR\_FAULTS, VOUT\_COMMAND, VOUT\_MARGIN\_HIGH, VOUT\_MARGIN\_LOW, and ASCCR\_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE\_DEFAULT\_ALL, STORE\_USER\_ALL, RESTORE\_DEFAULT\_ALL, and RESTORE\_USER\_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device. Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands may result in unexpected operation.

### Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT\_MARGIN\_HIGH.

To be sure a change to a device setting has taken effect, write the STORE\_USER\_ALL command, then cycle input power and re-enable.

## PMBus Commands Description

### OPERATION (01h)

**Definition:** Sets Enable, Disable, and  $V_{OUT}$  Margin settings. OPERATION data values that force the margin high or low only take effect when the MGN pin is left open (in the NOMINAL margin state).

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:**

**Units:** N/A

| SETTINGS | ACTIONS                       |
|----------|-------------------------------|
| 04h      | Immediate off (no sequencing) |
| 44h      | Soft off (with sequencing)    |
| 84h      | On - Nominal                  |
| 94h      | On - Margin low               |
| A4h      | On - Margin high              |

### ON\_OFF\_CONFIG (02h)

**Definition:** Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 16h (Device starts from ENABLE pin with soft off)

**Units:** N/A

| SETTINGS | ACTIONS                                                  |
|----------|----------------------------------------------------------|
| 16h      | Device starts from ENABLE pin with soft off.             |
| 17h      | Device starts from ENABLE pin with immediate off.        |
| 1Ah      | Device starts from OPERATION command with soft off.      |
| 1Bh      | Device starts from OPERATION command with immediate off. |

---

### **CLEAR\_FAULTS (03h)**

**Definition:** Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

**Data Length in Bytes:** 0 Byte

**Data Format:** N/A

**Type:** Write only

**Default Value:** N/A

**Units:** N/A

**Reference:** N/A

### **STORE\_USER\_ALL (15h)**

**Definition:** Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE\_FACTORY then STORE\_USER\_ALL. To add to the USER store, perform a RESTORE\_USER\_ALL, write commands to be added, then STORE\_USER\_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

**Data Length in Bytes:** 0

**Data Format:** N/A

**Type:** Write only

**Default Value:** N/A

**Units:** N/A

### **RESTORE\_USER\_ALL (16h)**

**Definition:** Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

**Data Length in Bytes:** 0

**Data Format:** N/A

**Type:** Write only

**Default Value:** N/A

**Units:** N/A

### **VOUT\_MODE (20h)**

**Definition:** Reports the  $V_{OUT}$  mode and provides the exponent used in calculating several  $V_{OUT}$  settings. Fixed with linear mode with default exponent (N) = -13

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 13h (Linear Mode, N = -13)

**Units:** N/A

### **VOUT\_COMMAND (21h)**

**Definition:** Sets or reports the target output voltage. This command cannot set a value higher than either  $V_{OUT\_MAX}$  or 110% of the pin strap  $V_{OUT}$  setting.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** Volts

**Range:** 0V to  $V_{OUT\_MAX}$

### **VOUT\_CAL\_OFFSET (23h)**

**Definition:** Applies a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit.

**Data Length in Bytes:** 2

**Data Format:** L16s

**Type:** R/W

**Default Value:** 0000h

**Units:** Volts

### **VOUT\_MAX (24h)**

**Definition:** Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. The default value can be changed using PMBus.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 1.10xVOUT\_COMMAND pin strap setting

**Units:** Volts

**Range:** 0V to 5.5V

### **VOUT\_MARGIN\_HIGH (25h)**

**Definition:** Sets the value of the  $V_{OUT}$  during a margin high. The VOUT\_MARGIN\_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command or MGN pin is set to "Margin High".

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default value:** 1.05 x VOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

### **VOUT\_MARGIN\_LOW (26h)**

**Definition:** Sets the value of the  $V_{OUT}$  during a margin low. The VOUT\_MARGIN\_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command or MGN pin is set to "Margin Low".

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default value:** 0.95 x VOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

### **VOUT\_TRANSITION\_RATE (27h)**

**Definition:** Sets the rate at which the output should change voltage when the device receives the VOUT\_COMMAND or an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default value:** BA00h (1.0 V/ms)

**Units:** V/ms

**Range:** 0.1 to 4V/ms

**VOUT\_DROOP (28h)**

**Definition:** Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning schemes or multi-module current sharing. In the current sharing configuration, VOUT\_DROOP set in each module stands for the droop seen by the load.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default value:** Pin strap setting

**Units:** mV/A

**Range:** 0 to 40mV/A

**FREQUENCY\_SWITCH (33h)**

**Definition:** Sets the switching frequency of the device. The initial default value is defined by a pin strap and this value can be overridden by writing this command using PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** kHz

**Range:** 300kHz to 1066kHz

**INTERLEAVE (37h)**

**Definition:** Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments. The internal two phases of the module always maintain a phase difference of 180°.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** R/W

**Default Value:** 0000h

**Units:** N/A

| BITS | PURPOSE           | VALUE   | DESCRIPTION                                          |
|------|-------------------|---------|------------------------------------------------------|
| 15:4 | Reserved          | 0       | Reserved                                             |
| 3:0  | Position in Group | 0 to 15 | Sets position of the device's rail within the group. |

**IOUT\_CAL\_GAIN (38h)**

**Definition:** Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** B370h (0.86mΩ)

**Units:** mΩ

**IOUT\_CAL\_OFFSET (39h)**

**Definition:** Used to null out any offsets in the output current sensing circuit and to compensate for delayed measurements of current ramp due to Isense blanking time.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** 0000h (0A)

**Units:** A



**VOUT\_OV\_FAULT\_LIMIT (40h)**

**Definition:** Sets the  $V_{OUT}$  overvoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 1.15xVOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

**VOUT\_OV\_FAULT\_RESPONSE (41h)**

**Definition:** Configures the  $V_{OUT}$  overvoltage fault response. Note that the device cannot be set to ignore this fault mode.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**VOUT\_OV\_WARN\_LIMIT (42h)**

**Definition:** Sets the  $V_{OUT}$  overvoltage warning threshold. The power-good signal is pulled low when output voltage goes higher than this threshold.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 1.10xVOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

**VOUT\_UV\_WARN\_LIMIT (43h)**

**Definition:** Sets the  $V_{OUT}$  undervoltage warning threshold. The power-good signal is pulled low when output voltage goes lower than this threshold.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 0.90xVOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

**VOUT\_UV\_FAULT\_LIMIT (44h)**

**Definition:** Sets the  $V_{OUT}$  undervoltage fault threshold. This fault is masked during ramp or when disabled.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 0.85xVOUT\_COMMAND pin strap setting

**Units:** V

**Range:** 0V to VOUT\_MAX

**VOUT\_UV\_FAULT\_RESPONSE (45h)**

**Definition:** Configures the  $V_{OUT}$  undervoltage fault response.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable, no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**IOUT\_OC\_FAULT\_LIMIT (46h)**

**Definition:** Sets the  $I_{OUT}$  average overcurrent fault threshold. The device will automatically calculate the peak inductor overcurrent fault limit for each phase based on the equation:  $I_{OUT}(PEAK\ OC\ LIMIT) = (0.5 * I_{OUT\_OC\_FAULT\_LIMIT} + 0.5 * I_{RIPPLE(P-P)}) * 120\%$ . A hard bound of 42A is applied to the peak overcurrent fault limit per phase.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** E3C0h (60A)

**Units:** A

**Range:** -100 to 100A

**IOUT\_UC\_FAULT\_LIMIT (4Bh)**

**Definition:** Sets the  $I_{OUT}$  average undercurrent fault threshold. The device will automatically calculate the valley inductor undercurrent fault limit for each phase based on the equation:  $I_{OUT}(VALLEY\ UC\ LIMIT) = (0.5 * I_{OUT\_UC\_FAULT\_LIMIT} - 0.5 * I_{RIPPLE(P-P)}) * 120\%$ . A hard bound of -42A is applied to the valley undercurrent fault limit per phase.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** -1xIOUT\_OC\_FAULT\_LIMIT

**Units:** A

**Range:** -100 to 100A

**OT\_FAULT\_LIMIT (4Fh)**

**Definition:** Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT\_WARN\_LIMIT to clear this fault.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** EBE8h (+125°C)

**Units:** Celsius

**Range:** 0°C to +175°C

**OT\_FAULT\_RESPONSE (50h)**

**Definition:** Instructs the device on what action to take in response to an over-temperature fault.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Fault Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**OT\_WARN\_LIMIT (51h)**

**Definition:** Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT\_WARN\_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS\_WORD, sets the OT\_WARNING bit in STATUS\_TEMPERATURE, and notifies the host.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** EB48h (+105 °C)

**Units:** Celsius

**Range:** 0 °C to +175 °C

**UT\_WARN\_LIMIT (52h)**

**Definition:** Sets the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT\_WARN\_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS\_WORD, sets the UT\_WARNING bit in STATUS\_TEMPERATURE, and notifies the host.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** DC40h (-30 °C)

**Units:** Celsius

**Range:** -55 °C to +25 °C

**UT\_FAULT\_LIMIT (53h)**

**Definition:** Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above UT\_WARN\_LIMIT to clear this fault.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** E580h (-40 °C)

**Units:** Celsius

**Range:** -55 °C to +25 °C

**UT\_FAULT\_RESPONSE (54h)**

**Definition:** Configures the under-temperature fault response as defined by the following table. The delay time is the time between restart attempts.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable, no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**VIN\_OV\_FAULT\_LIMIT (55h)**

**Definition:** Sets the  $V_{IN}$  overvoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** D380h (14V)

**Units:** V

**Range:** 0V to 16V

**VIN\_OV\_FAULT\_RESPONSE (56h)**

**Definition:** Configures the  $V_{IN}$  overvoltage fault response as defined by the following table. The delay time is the time between restart attempts.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**VIN\_OV\_WARN\_LIMIT (57h)**

**Definition:** Sets the  $V_{IN}$  overvoltage warning threshold. In response to the OV\_WARN\_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS\_WORD, sets the VIN\_OV\_WARNING bit in STATUS\_INPUT, and notifies the host.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Protectable:** Yes

**Default Value:** D353h (13.3V)

**Units:** V

**Range:** 0V to 16V

**VIN\_UV\_WARN\_LIMIT (58h)**

**Definition:** Sets the  $V_{IN}$  undervoltage warning threshold. If a VIN\_UV\_FAULT occurs, the input voltage must rise above VIN\_UV\_WARN\_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV\_WARN\_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS\_WORD, sets the VIN\_UV\_WARNING bit in STATUS\_INPUT, and notifies the host.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** 1.05 x VIN\_UV\_FAULT\_LIMIT pin strap setting

**Units:** V

**Range:** 0V to 12V

**VIN\_UV\_FAULT\_LIMIT (59h)**

**Definition:** Sets the  $V_{IN}$  undervoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** V

**Range:** 0V to 12V

**VIN\_UV\_FAULT\_RESPONSE (5Ah)**

**Definition:** Configures the  $V_{IN}$  undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                      |
|----------|----------------------------------------------|
| 80h      | Disable with no retry                        |
| BFh      | Disable and continuous retry with 70ms delay |

**POWER\_GOOD\_ON (5Eh)**

**Definition:** Sets the voltage threshold for Power-good indication. Power-good asserts with a delay specified in POWER\_GOOD\_DELAY after the output voltage exceeds POWER\_GOOD\_ON and deasserts when the output voltage is less than VOUT\_UV\_WARN\_LIMIT.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 0.9xVOUT\_COMMAND pin strap setting

**Units:** V

**TON\_DELAY (60h)**

**Definition:** Sets the delay time from when the device is enabled to the start of  $V_{OUT}$  rise.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** ms

**Range:** 0 to 500ms

**TON\_RISE (61h)**

**Definition:** Sets the rise time of  $V_{OUT}$  after ENABLE and TON\_DELAY. In multi-module current sharing configuration where ASCR is disabled for start up, the rise time of  $V_{OUT}$  can be approximately calculated by [Equation 1](#).

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** ms

**Range:** 0 to 200ms

**TOFF\_DELAY (64h)**

**Definition:** Sets the delay time from DISABLE to the start of  $V_{OUT}$  fall.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** ms

**Range:** 0 to 500ms

**TOFF\_FALL (65h)**

**Definition:** Sets the soft-off fall time for  $V_{OUT}$  after DISABLE and TOFF\_DELAY.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** ms

**Range:** 0 to 200ms

**STATUS\_BYTE (78h)**

**Definition:** Returns one byte of information with a summary of the most critical faults.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME   | MEANING                                                                                                                              |
|------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7          | BUSY              | A fault was declared because the device was busy and unable to respond.                                                              |
| 6          | OFF               | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5          | VOUT_OV_FAULT     | An output overvoltage fault has occurred.                                                                                            |
| 4          | IOUT_OC_FAULT     | An output overcurrent fault has occurred.                                                                                            |
| 3          | VIN_UV_FAULT      | An input undervoltage fault has occurred.                                                                                            |
| 2          | TEMPERATURE       | A temperature fault or warning has occurred.                                                                                         |
| 1          | CML               | A communications, memory or logic fault has occurred.                                                                                |
| 0          | NONE OF THE ABOVE | A fault or warning not listed in Bits 7:1 has occurred.                                                                              |

**STATUS\_WORD (79h)**

**Definition:** Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS\_WORD is the same register as the STATUS\_BYTE (78h) command.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 0000h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME   | MEANING                                                                                                                              |
|------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 15         | VOUT              | An output voltage fault or warning has occurred.                                                                                     |
| 14         | IOUT/POUT         | An output current or output power fault or warning has occurred.                                                                     |
| 13         | INPUT             | An input voltage, input current, or input power fault or warning has occurred.                                                       |
| 12         | MFG_SPECIFIC      | A manufacturer specific fault or warning has occurred.                                                                               |
| 11         | POWER_GOOD#       | The POWER_GOOD signal, if present, is negated.                                                                                       |
| 10         | FANS              | A fan or airflow fault or warning has occurred.                                                                                      |
| 9          | OTHER             | A bit in STATUS_OTHER is set.                                                                                                        |
| 8          | UNKNOWN           | A fault type not given in bits 15:1 of the STATUS_WORD has been detected.                                                            |
| 7          | BUSY              | A fault was declared because the device was busy and unable to respond.                                                              |
| 6          | OFF               | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5          | VOUT_OV_FAULT     | An output overvoltage fault has occurred.                                                                                            |
| 4          | IOUT_OC_FAULT     | An output overcurrent fault has occurred.                                                                                            |
| 3          | VIN_UV_FAULT      | An input undervoltage fault has occurred.                                                                                            |
| 2          | TEMPERATURE       | A temperature fault or warning has occurred.                                                                                         |
| 1          | CML               | A communications, memory or logic fault has occurred.                                                                                |
| 0          | NONE OF THE ABOVE | A fault or warning not listed in Bits 7:1 has occurred.                                                                              |

**STATUS\_VOUT (7Ah)**

**Definition:** Returns one data byte with the status of the output voltage.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME | MEANING                                   |
|------------|-----------------|-------------------------------------------|
| 7          | VOUT_OV_FAULT   | Indicates an output overvoltage fault.    |
| 6          | VOUT_OV_WARNING | Indicates an output overvoltage warning.  |
| 5          | VOUT_UV_WARNING | Indicates an output undervoltage warning. |
| 4          | VOUT_UV_FAULT   | Indicates an output undervoltage fault.   |
| 3:0        | N/A             | These bits are not used.                  |

**STATUS\_IOUT (7Bh)**

**Definition:** Returns one data byte with the status of the output current.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME  | MEANING                                                   |
|------------|------------------|-----------------------------------------------------------|
| 7          | IOUT_OC_FAULT    | An output overcurrent fault has occurred.                 |
| 6          | IOUT_OC_LV_FAULT | An output overcurrent and low voltage fault has occurred. |
| 5          | IOUT_OC_WARNING  | An output overcurrent warning has occurred.               |
| 4          | IOUT_UC_FAULT    | An output undercurrent fault has occurred.                |
| 3:0        | N/A              | These bits are not used.                                  |

**STATUS\_INPUT (7Ch)**

**Definition:** Returns input voltage and input current status information.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME | MEANING                                     |
|------------|-----------------|---------------------------------------------|
| 7          | VIN_OV_FAULT    | An input overvoltage fault has occurred.    |
| 6          | VIN_OV_WARNING  | An input overvoltage warning has occurred.  |
| 5          | VIN_UV_WARNING  | An input undervoltage warning has occurred. |
| 4          | VIN_UV_FAULT    | An input undervoltage fault has occurred.   |
| 3:0        | N/A             | These bits are not used.                    |

**STATUS\_TEMP (7Dh)**

**Definition:** Returns one byte of information with a summary of any temperature related faults or warnings.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME | MEANING                                    |
|------------|-----------------|--------------------------------------------|
| 7          | OT_FAULT        | An over-temperature fault has occurred.    |
| 6          | OT_WARNING      | An over-temperature warning has occurred.  |
| 5          | UT_WARNING      | An under-temperature warning has occurred. |
| 4          | UT_FAULT        | An under-temperature fault has occurred.   |
| 3:0        | N/A             | These bits are not used.                   |



**STATUS\_CML (7Eh)**

**Definition:** Returns one byte of information with a summary of any communications, logic, and/or memory errors.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read-only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | MEANING                                                                                                                                             |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7          | Invalid or unsupported PMBus command was received.                                                                                                  |
| 6          | The PMBus command was sent with invalid or unsupported data.                                                                                        |
| 5          | packet error was detected in the PMBus command.                                                                                                     |
| 4:2        | Not Used                                                                                                                                            |
| 1          | A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred. |
| 0          | Not Used                                                                                                                                            |

**STATUS\_MFR\_SPECIFIC (80h)**

**Definition:** Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default value:** 00h

**Units:** N/A

| BIT NUMBER | FIELD NAME                      | MEANING                                                                             |
|------------|---------------------------------|-------------------------------------------------------------------------------------|
| 7:6        | Reserved                        | Reserved.                                                                           |
| 5          | VMON UV Warning                 | The voltage on the VMON pin has dropped below 4V.                                   |
| 4          | VMON OV Warning                 | The voltage on the VMON pin has risen above 5.9V.                                   |
| 3          | External Switching Period Fault | Loss of external clock synchronization has occurred.                                |
| 2          | Reserved                        | Reserved.                                                                           |
| 1          | VMON UV Fault                   | The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT_LIMIT. |
| 0          | VMON OV Fault                   | The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT_LIMIT.   |

**READ\_VIN (88h)**

**Definition:** Returns the input voltage reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read-only

**Units:** V

**READ\_VOUT (8Bh)**

**Definition:** Returns the output voltage reading.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** Read-only

**Units:** V

**READ\_IOUT (8Ch)**

**Definition:** Returns the output current reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read-only

**Default Value:** N/A

**Units:** A

**READ\_INTERNAL\_TEMP (8Dh)**

**Definition:** Returns the controller junction temperature reading from internal temperature sensor.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read-only

**Units:** °C

**READ\_DUTY\_CYCLE (94h)**

**Definition:** Reports the actual duty cycle of the converter during the enable state.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** %

**READ\_FREQUENCY (95h)**

**Definition:** Reports the actual switching frequency of the converter during the enable state.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** kHz

**READ\_IOUT\_0 (96h)**

**Definition:** Returns the Phase 1 current reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read-only

**Default Value:** N/A

**Units:** A

**READ\_IOUT\_1 (97h)**

**Definition:** Returns the Phase 2 current reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read-only

**Default Value:** N/A

**Units:** A

**MFR\_ID (99h)**

**Definition:** Sets user defined identification. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** user defined

**Data Format:** ASCII

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**MFR\_MODEL (9Ah)**

**Definition:** Sets a user defined model. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL, and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** user defined

**Data Format:** ASC

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**MFR\_REVISION (9Bh)**

**Definition:** Sets a user defined revision. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL, and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** user defined

**Data Format:** ASC

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**MFR\_LOCATION (9Ch)**

**Definition:** Sets a user defined location identifier. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** User defined

**Data Format:** ASC

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**MFR\_DATE (9Dh)**

**Definition:** Sets a user defined date. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** User defined

**Data Format:** ASC

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**Reference:** N/A

**MFR\_SERIAL (9Eh)**

**Definition:** Sets a user defined serialized identifier. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL, and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** User defined

**Data Format:** ASC

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**LEGACY\_FAULT\_GROUP (A8h)**

**Definition:** Specifies which rail DDC IDs should be listened to for fault spreading with legacy devices. The data sent is a 4-byte, 32-bit, bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

**Data Length in Bytes:** 4

**Data Format:** BIT

**Type:** R/W

**Default Value:** 00000000h

**USER\_DATA\_00 (B0h)**

**Definition:** Sets user defined data. The sum total of characters in MFR\_ID, MFR\_MODEL, MFR\_REVISION, MFR\_LOCATION, MFR\_DATE, MFR\_SERIAL, and USER\_DATA\_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

**Data Length in Bytes:** User defined

**Data Format:** ASCII

**Type:** Block R/W

**Default Value:** null

**Units:** N/A

**ISENSE\_CONFIG (D0h)**

**Definition:** Configures current sense circuitry.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 05h

**Units:** N/A

| BIT | FIELD NAME                  | VALUE | SETTING    | DESCRIPTION                                         |
|-----|-----------------------------|-------|------------|-----------------------------------------------------|
| 7:4 | Reserved                    | 000   |            |                                                     |
| 3:2 | Current Sense Blanking Time | 00    | 192ns      | Sets the blanking time current sense blanking time. |
|     |                             | 01    | 256ns      |                                                     |
|     |                             | 10    | 412ns      |                                                     |
|     |                             | 11    | 640ns      |                                                     |
| 1:0 | Current Sense Range         | 00    | Low Range  | ±25mV                                               |
|     |                             | 01    | Mid Range  | ±35mV                                               |
|     |                             | 10    | High Range | ±50mV                                               |
|     |                             | 11    | Not Used   |                                                     |

**USER\_CONFIG (D1h)**

**Definition:** Configures several user-level features. This command overrides the CONFIG pin settings.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** N/A

| BIT | FIELD NAME                               | VALUE | SETTING    | DESCRIPTION                                                       |
|-----|------------------------------------------|-------|------------|-------------------------------------------------------------------|
| 7   | ASCR on for Start up                     | 0     | Disabled   | ASCR is disabled for start up. Use this for current sharing mode. |
|     |                                          | 1     | Enabled    | ASCR is enabled for start up. Use this for stand alone mode.      |
| 6:5 | Reserved                                 | 0     |            | Reserved                                                          |
| 4:3 | Ramp-Up and Ramp-Down Minimum Duty Cycle | 00    | 0.39%      | Sets the minimum duty-cycle during start-up and shutdown ramp.    |
|     |                                          | 01    | 0.78%      |                                                                   |
|     |                                          | 10    | 1.17%      |                                                                   |
|     |                                          | 11    | 1.56%      |                                                                   |
| 2   | Minimum Duty Cycle Control               | 0     | Disable    | Control for minimum duty cycle.                                   |
|     |                                          | 1     | Enable     |                                                                   |
| 1   | Power-Good Pin Configuration             | 0     | Open Drain | 0 = PG is open drain output.                                      |
|     |                                          | 1     | Push-Pull  | 1 = PG is push-pull output.                                       |
| 0   | Reserved                                 | 0     |            |                                                                   |

**DDC\_CONFIG (D3h)**

**Definition:** Configures DDC addressing and current sharing. With pin strap for stand alone configuration, the DDC rail ID is set according to the SMBus address. With pin strap for multi-module current sharing, the DDC rail ID is set according to the number of devices. Device position and number of devices in the rail can be programmed as needed.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** R/W

**Default Value:** Pin strap setting

**Units:** N/A

| BIT   | FIELD NAME                       | VALUE               | SETTING  | DESCRIPTION                                                                                                                       |
|-------|----------------------------------|---------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | Device Position                  | 0, 1, 2, 3          |          | Sets the device position in a current sharing rail.<br>0-Position 1<br>1-Position 2<br>2-Position 3<br>3-Position 4               |
| 12:8  | Rail ID                          | 0 to 31 (00 to 1Fh) |          | Configures the DDC rail ID.                                                                                                       |
| 7:4   | Reserved                         | 0                   | Reserved | Reserved                                                                                                                          |
| 3     | Device Internal Phase Difference | 0, 1                |          | Sets the internal phase difference of the phase. The 0-phase difference is 180°. The 1-phase difference is 0°.                    |
| 2:0   | Number of Devices in Rail        | 1, 3, 5, 7          |          | Identifies the number of devices in a current sharing rail.<br>1-standalone<br>3-two devices<br>5-three devices<br>7-four devices |

## POWER\_GOOD\_DELAY (D4h)

**Definition:** Sets the delay applied between the output exceeding the PG threshold (POWER\_GOOD\_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper de-bounce to this signal.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** 3ms

**Units:** ms

**Range:** 0 to 5s

## ASCR\_CONFIG (DFh)

**Definition:** Allows user configuration of ASCR settings. ASCR Gain is analogous to bandwidth and ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR Gain settings range from 50 to 1000 and ASCR Residual settings range from 10 to 100.

**Data Length in Bytes:** 4

**Data Format:** CUS

**Type:** R/W

**Default Value:** Pin strap setting

| BIT   | PURPOSE               | DATA Format | VALUE    | DESCRIPTION   |
|-------|-----------------------|-------------|----------|---------------|
| 31:25 | Unused                |             | 0000000h | Unused        |
| 24    | ASCR Enable           | BIT         | 1        | Enable        |
|       |                       |             | 0        | Disable       |
| 23:16 | ASCR Residual Setting | Integer     |          | ASCR residual |
| 15:0  | ASCR Gain Setting     | Integer     |          | ASCR gain     |

## SEQUENCE (E0h)

**Definition:** Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device will enable its output when its EN or OPERATION enable states, as defined by ON\_OFF\_CONFIG, are set and the prequel device has issued a Power-Good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a Power-Down event on the DDC bus.

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** R/W

**Default Value:** 0000h (Prequel and Sequel disabled)

| BIT   | FIELD NAME          | VALUE | SETTING  | DESCRIPTION                                           |
|-------|---------------------|-------|----------|-------------------------------------------------------|
| 15    | Prequel Enable      | 0     | Disable  | Disable, no prequel preceding this rail.              |
|       |                     | 1     | Enable   | Enable, prequel to this rail is defined by bits 12:8. |
| 14:13 | Reserved            | 0     | Reserved | Reserved                                              |
| 12:8  | Prequel Rail DDC ID | 0-31  | DDC ID   | Set to the DDC ID of the prequel rail.                |
| 7     | Sequel Enable       | 0     | Disable  | Disable, no sequel following this rail.               |
|       |                     | 1     | Enable   | Enable, sequel to this rail is defined by bits 4:0.   |
| 6:5   | Reserved            | 0     | Reserved | Reserved                                              |
| 4:0   | Sequel Rail DDC ID  | 0-31  | DDC ID   | Set to the DDC ID of the sequel rail.                 |

**DDC\_GROUP (E2h)**

**Definition:** Configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT\_COMMAND group ID and enable.

**Data Length in Bytes:** 3

**Data Format:** BIT

**Type:** R/W

**Default Value:** Pin strap setting (ignore BROADCAST VOUT\_COMMAND, OPERATIONn and fault for stand alone operation. Enable BROADCAST VOUT\_COMMAND, OPERATION, and fault for current sharing).

| BITS  | PURPOSE                         | VALUE | DESCRIPTION                                                                    |
|-------|---------------------------------|-------|--------------------------------------------------------------------------------|
| 23:22 | Reserved                        | 0     | Reserved                                                                       |
| 21    | BROADCAST_VOUT_COMMAND Response | 1     | Responds to BROADCAST_VOUT_COMMAND with same Group ID.                         |
|       |                                 | 0     | Ignores BROADCAST_VOUT_COMMAND.                                                |
| 20:16 | BROADCAST_VOUT_COMMAND Group ID | 0-31d | Group ID sent as data for broadcast BROADCAST_VOUT_COMMAND events.             |
| 15:14 | Reserved                        | 0     | Reserved                                                                       |
| 13    | BROADCAST_OPERATION Response    | 1     | Responds to BROADCAST_OPERATION with same Group ID.                            |
|       |                                 | 0     | Ignores BROADCAST_OPERATION.                                                   |
| 12:8  | BROADCAST_OPERATION Group ID    | 0-31d | Group ID sent as data for broadcast BROADCAST_OPERATION events.                |
| 7:6   | Reserved                        | 0     | Reserved                                                                       |
| 5     | POWER_FAIL Response             | 1     | Responds to POWER_FAIL events with same Group ID by shutting down immediately. |
|       |                                 | 0     | Responds to POWER_FAIL events with same Group ID with sequenced shutdown.      |
| 4:0   | POWER_FAIL group ID             | 0-31d | Group ID sent as data for broadcast POWER_FAIL events.                         |

**DEVICE\_ID (E4h)**

**Definition:** Returns the 16-byte (character) device identifier string.

**Data Length in Bytes:** 16

**Data Format:** ASCII

**Type:** Block Read

**Default Value:** Part number/Die revision/Firmware revision

**MFR\_IOUT\_OC\_FAULT\_RESPONSE (E5h)**

**Definition:** Configures the I<sub>OUT</sub> overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS\_IOUT.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**MFR\_IOUT\_UC\_FAULT\_RESPONSE (E6h)**

**Definition:** Configures the I<sub>OUT</sub> undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS\_IOUT.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 80h (Disable and no retry)

**Units:** N/A

| SETTINGS | ACTIONS                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| BFh      | Disable and continuous retry with 70ms delay. |

**SYNC\_CONFIG (E9h)**

**Definition:** Sets options for SYNC output configurations.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** Pin strap setting

| SETTINGS | ACTIONS                                                                   |
|----------|---------------------------------------------------------------------------|
| 00h      | Use Internal clock. Clock frequency is set by pin strap or PMBus command. |
| 02h      | Use internal clock and output internal clock.                             |
| 04h      | Use external clock.                                                       |



## SNAPSHOT (EAh)

**Definition:** A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, the last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set stored, device will no longer automatically capture parametric and status values following fault until stored data are erased. Use the SNAPSHOT\_CONTROL command to erase store data and clear the status bit before next ramp up. Data erased is not allowed when the module is enabled.

**Data Length in Bytes:** 32

**Data Format:** Bit field

**Type:** Block Read

| BYTE NUMBER | VALUE                                                      | PMBUS COMMAND             | FORMAT |
|-------------|------------------------------------------------------------|---------------------------|--------|
| 31:23       | Reserved                                                   | Reserved                  | 00h    |
| 22          | Flash Memory Status Byte<br>FF - Not Stored<br>00 - Stored | N/A                       | BIT    |
| 21          | Manufacturer Specific Status Byte                          | STATUS_MFR_SPECIFIC (80h) | Byte   |
| 20          | CML Status Byte                                            | STATUS_CML (7Eh)          | Byte   |
| 19          | Temperature Status Byte                                    | STATUS_TEMPERATURE (7Dh)  | Byte   |
| 18          | Input Status Byte                                          | STATUS_INPUT (7Ch)        | Byte   |
| 17          | I <sub>OUT</sub> Status Byte                               | STATUS_IOUT (7Bh)         | Byte   |
| 16          | V <sub>OUT</sub> Status Byte                               | STATUS_VOUT (7Ah)         | Byte   |
| 15:14       | Switching Frequency                                        | READ_FREQUENCY (95h)      | L11    |
| 13:12       | Reserved                                                   | Reserved                  | 00h    |
| 11:10       | Internal Temperature                                       | READ_INTERNAL_TEMP (8Dh)  | L11    |
| 9:8         | Duty Cycle                                                 | READ_DUTY_CYCLE (94h)     | L11    |
| 7:6         | Highest Measured Output Current                            | N/A                       | L11    |
| 5:4         | Output Current                                             | READ_IOUT (8Ch)           | L11    |
| 3:2         | Output Voltage                                             | READ_VOUT (8Bh)           | L16u   |
| 1:0         | Input Voltage                                              | READ_VIN (88h)            | L11    |

## BLANK\_PARAMS (EBh)

**Definition:** Returns a 16-byte string indicating which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK\_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

**Data Length in Bytes:** 16

**Data Format:** BIT

**Type:** Block Read

**Default Value:** FF...FFh

## SNAPSHOT\_CONTROL (F3h)

**Definition:** Writing a 01h will cause the device to copy the current SNAPSHOT values from NVRAM to the 32-byte SNAPSHOT command parameter. Writing a 02h will cause the device to write the current SNAPSHOT values to NVRAM, and writing a 03h will erase all SNAPSHOT values from NVRAM. Write (02h) and Erase (03h) may only be used when the device is disabled. All other values are ignored.

**Data Length in Bytes:** 1

**Data Format:** Bit field

**Type:** R/W byte

| VALUE | DESCRIPTION                             |
|-------|-----------------------------------------|
| 01h   | Read SNAPSHOT values from NV RAM        |
| 02h   | Write SNAPSHOT values to NV RAM         |
| 03h   | Erase SNAPSHOT values stored in NV RAM. |

---

## RESTORE\_FACTORY (F4h)

**Definition:** Restores the device to the hard-coded Factory default values and pin strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

**Data Length in Bytes:** 0

**Data Format:** N/A

**Type:** Write only

**Default Value:** N/A

**Units:** N/A

## MFR\_VMON\_OV\_FAULT\_LIMIT (F5h)

**Definition:** Reads the VMON OV fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** CB00h (6V)

**Units:** V

**Range:** 4V to 6V

## MFR\_VMON\_UV\_FAULT\_LIMIT (F6h)

**Definition:** Reads the VMON UV fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** CA00h (4V)

**Units:** V

**Range:** 4V to 6V

## MFR\_READ\_VMON (F7h)

**Definition:** Reads the VMON voltage.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** N/A

**Units:** V

**Range:** 4V to 6V

## VMON\_OV\_FAULT\_RESPONSE (F8h)

**Definition:** Reads the VMON OV fault response.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 80h (Disable and no retry)

**Units:**

## VMON\_UV\_FAULT\_RESPONSE (F9h)

**Definition:** Reads the VMON UV fault response, which follows VIN\_UV\_FAULT\_RESPONSE.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 80h (Disable and no retry)

**Units:** V

## Firmware Revision History

TABLE 10. ISL8272M NOMENCLATURE GUIDE

| FIRMWARE REVISION CODE | CHANGE DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | NOTE                            |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|
| ISL8272-000-FC02       | <ul style="list-style-type: none"> <li>- Enhanced fault management during start-up</li> <li>- Enhanced IOOUT UC fault management during start-up</li> <li>- Enhanced PMBus immunity to noise and lockup</li> <li>- Added paged ISENGain and ISENOffset factors which are storable in default memory</li> <li>- Added temperature compensation for the paged ISENGain and ISENOffset factors and reduced temperature drift</li> <li>- Improved intra-device current balance within the two internal phases</li> <li>- Fixed the synchronization issue during VOUT_COMMAND change on-the-fly current sharing conditions</li> <li>- Added more pin-strap resistor settings for the CS pin for four-module current sharing conditions</li> <li>- Added the capability to change the device internal phase difference from 180° to 0° in DDC_CONFIG and optimized module-to-module phase shift in Current Sharing mode</li> <li>- VMON UV/OV warning value changed</li> </ul> | Recommended for new designs     |
| ISL8272-000-FC01       | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Not recommended for new designs |

**Revision History** The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE         | REVISION | CHANGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Nov 8, 2017  | FN8670.5 | <p>Added clock configurations to Table 9, Current Sharing Resistor Settings on page 22.</p> <p>STATUS_MFR_SPECIFIC (80h) PMBus command on page 41 - updated command definition and the meanings of Bits 4 and 5.</p> <p>DDC_CONFIG (D3h) PMBus command on page 45 - updated bit descriptions.</p> <p>Added Firmware Revision B (FC02) to Firmware Revision History on page 51 and firmware graphic on page 3.</p> <p>Renumbered figures to fix issue in which Figure 4 was listed twice.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Mar 31, 2017 | FN8670.4 | <p>Related Literature on page 1 updated.</p> <p>Ordering Information, page 3: Updated Note 2 - added Tape and Reel option and Note 3 - added exemptions 7C-I and 7A.</p> <p>Added the notation "A standard 1% resistor is required" to the following sections:</p> <ul style="list-style-type: none"> <li>-Soft-Start/Stop Delay and Ramp Times, Switching Frequency and PLL, Loop Compensation, Input Undervoltage Lockout (UVLO), SMBus Module Address Selection, Active Current Sharing</li> </ul> <p>Added "Note that fault retry is not supported in the current sharing configuration." to the following sections:</p> <ul style="list-style-type: none"> <li>Input Undervoltage Lockout (UVLO), Output Overvoltage Protection, Output Overcurrent Protection, Thermal Overload Protection, Active Current Sharing,</li> <li>Fault Spreading ("Note that fault retry is not supported in multiple modules with fault spreading enabled, such as the current sharing configuration.").</li> </ul> <p>SMBus Communications section on page 17, paragraph added (3rd paragraph)</p> <p>Soft-Start/Stop Delay and Ramp Times section page 17 - a paragraph was added (1st paragraph)</p> <p>PMBus Use Guidelines - added "Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands may result in unexpected operation."</p> <p>POD Y58.18x23 revised from rev 1 to rev 3. Changes since rev 1:</p> <ol style="list-style-type: none"> <li>1) Pages 1 and 2 of POD Y58.18x23 remain unchanged for this update.</li> <li>2) Deleted remaining pages 3-5 of existing POD and replaced with: New drawings - 2 drawings per page</li> </ol> <p>On page 2, in the "Size Details for the 16 Exposed Pads" (Bottom View) changed dimension 8.40 (2X) to 8.30 (2x) and 8.00 (2x) to 1.00 (2X).</p> |
| Mar 16, 2016 | FN8670.3 | <p>Added "PMBus Use Guidelines" on page 29.</p> <p>Updated POD Y58.18x23 to the latest revision changes are as follows:</p> <ul style="list-style-type: none"> <li>-Detail A on page 1: Added Reference Radius for rounded corners on small I/O pads.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Jan 14, 2015 | FN8670.2 | <p>"Electrical Specifications" on page 10 under VOUT_ACCY and VOUT_READ_ERR: Updated unit value from "% FS" to "%VOUT".</p> <p>Updated "Switching Frequency and PLL" on page 18.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Sep 17, 2014 | FN8670.1 | <p>Removed the words "in forced CCM Mode" from 2nd paragraph on page 1, which read "The ISL8272M operated in forced CCM Mode with the ChargeMode™ control architecture,..."</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Sep 12, 2014 | FN8670.0 | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

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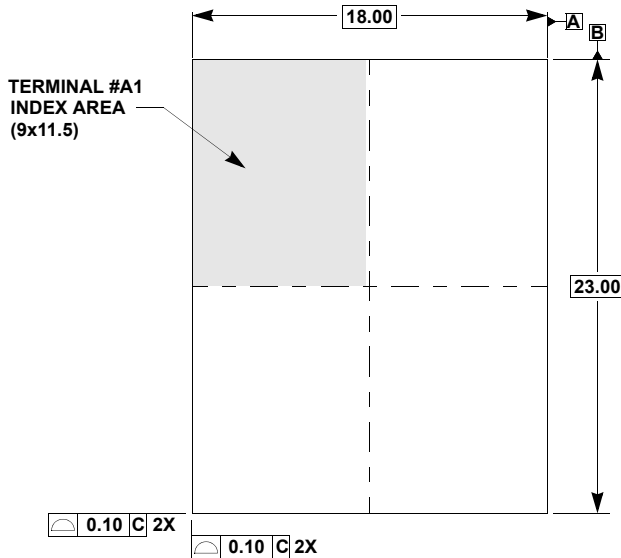
# Package Outline Drawing

## Y58.18x23

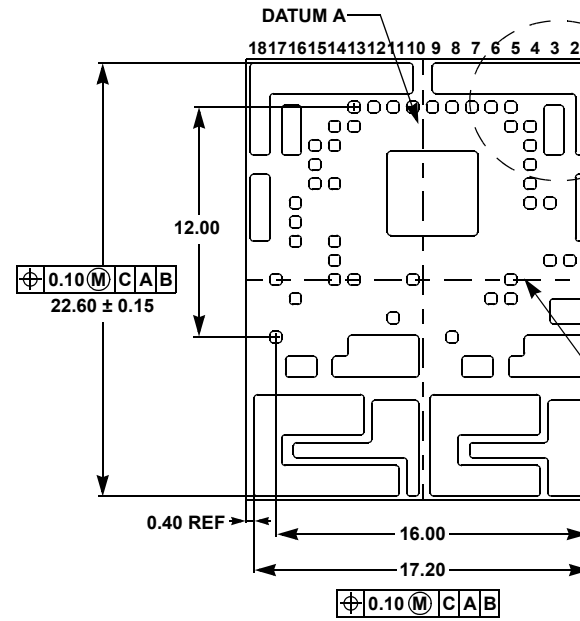
58 I/O 18mmx23mmx7.5mm CUSTOM HDA MODULE

Rev 3, 12/16

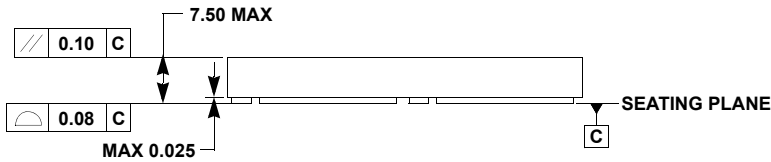
For the most recent package



TOP VIEW



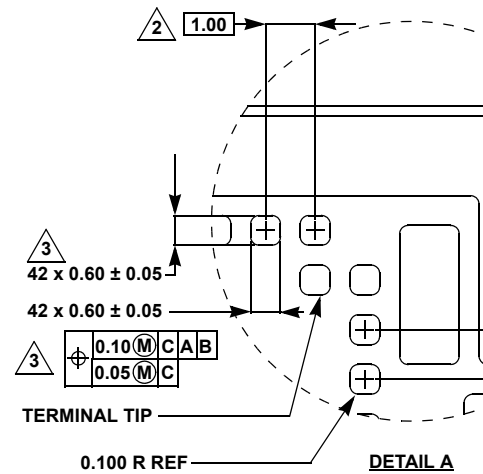
BOTTOM VIEW



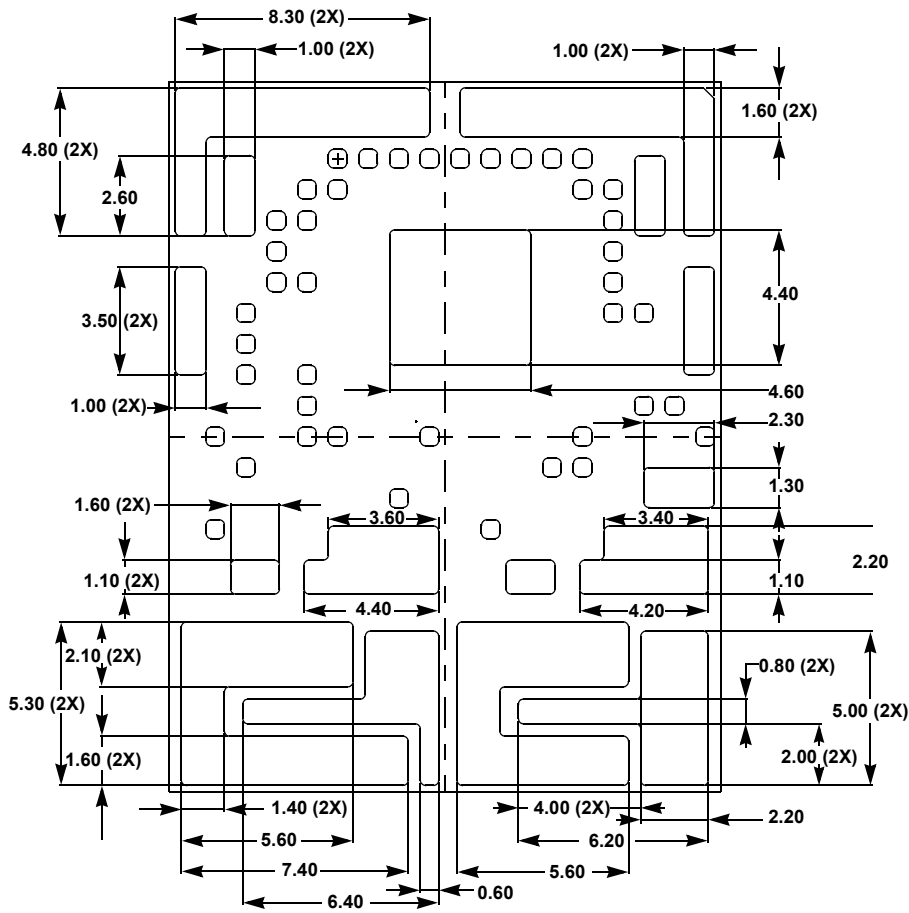
SIDE VIEW

NOTES:

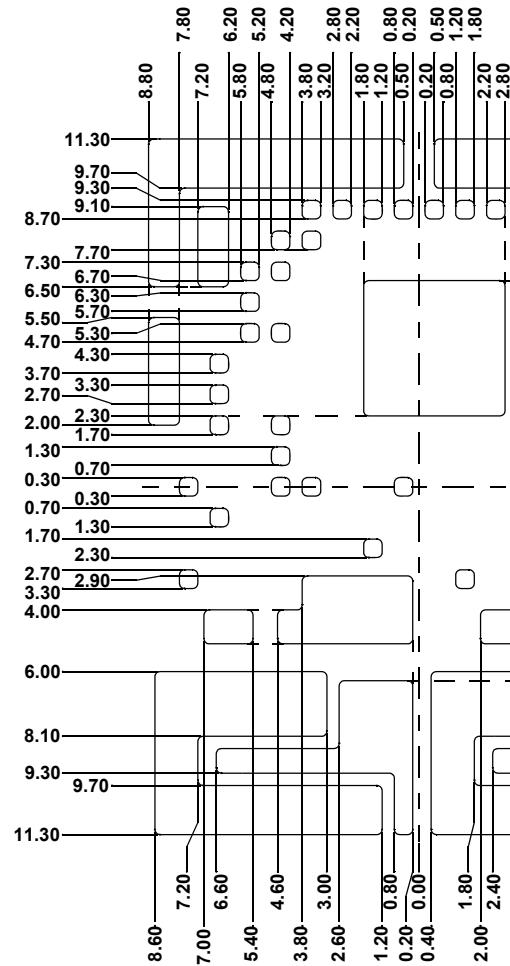
1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.



DETAIL A

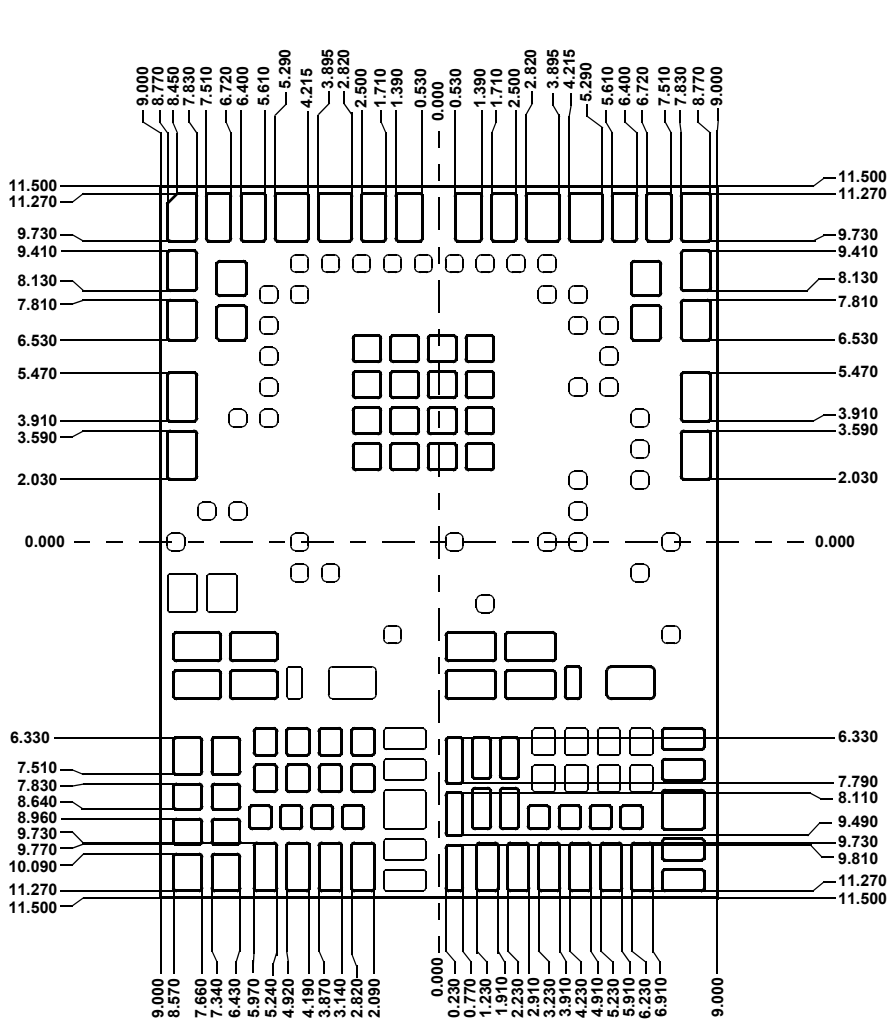


SIZE DETAILS FOR THE 16 EXPOSED PADS

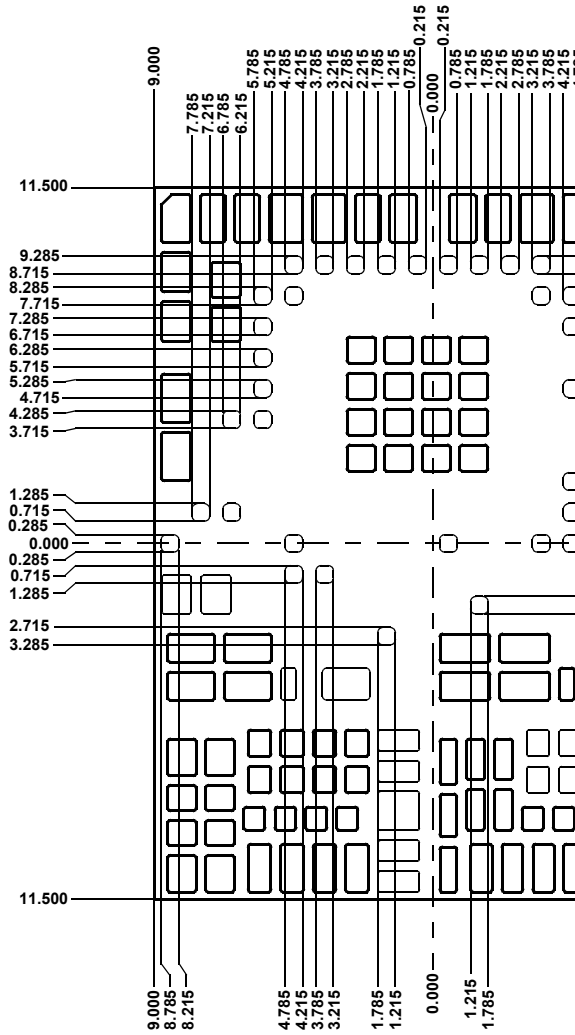


TERMINAL AND PAD EDGE DIMENSIONS

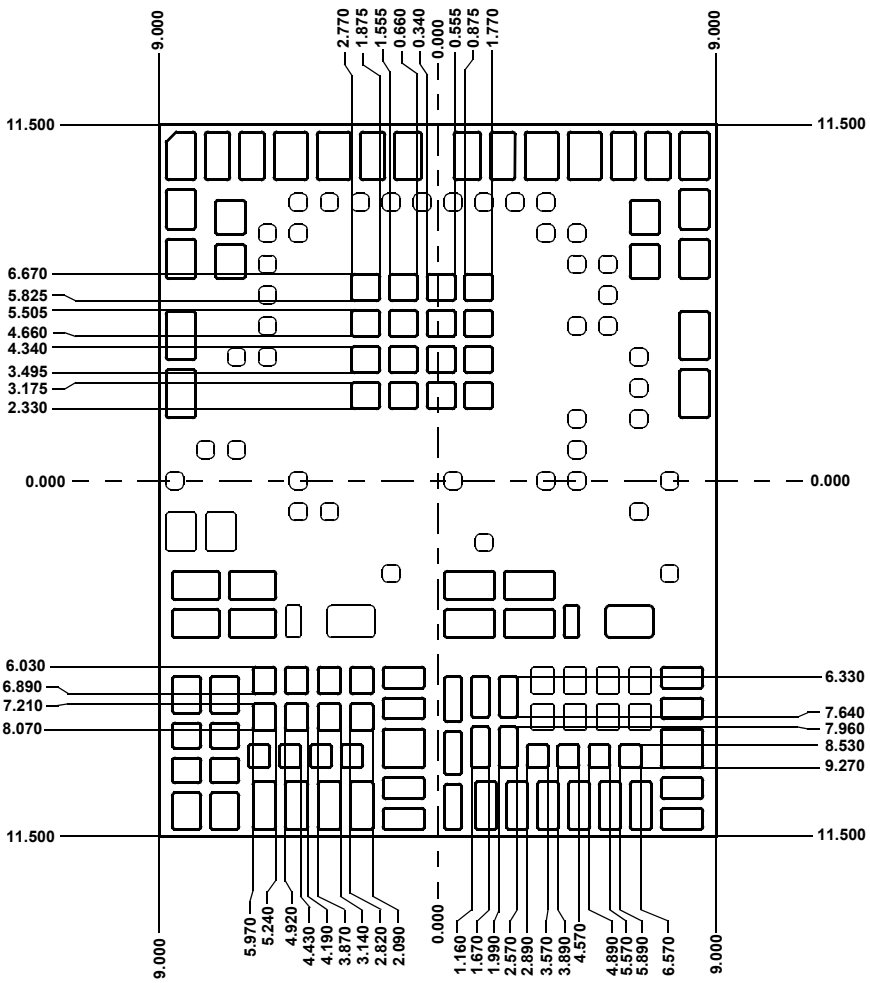
BOTTOM VIEW



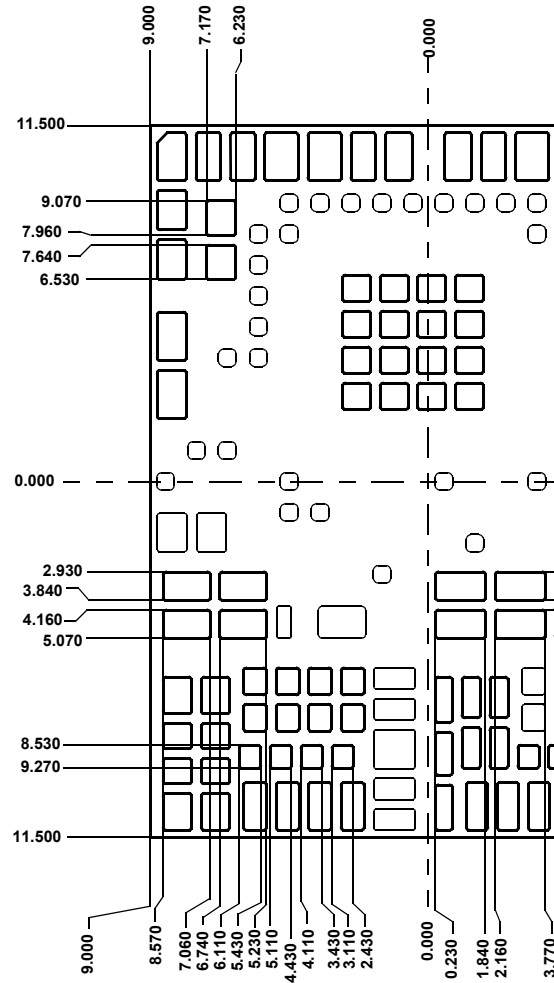
STENCIL OPENING EDGE POSITION - 1



STENCIL OPENING EDGE POSITION



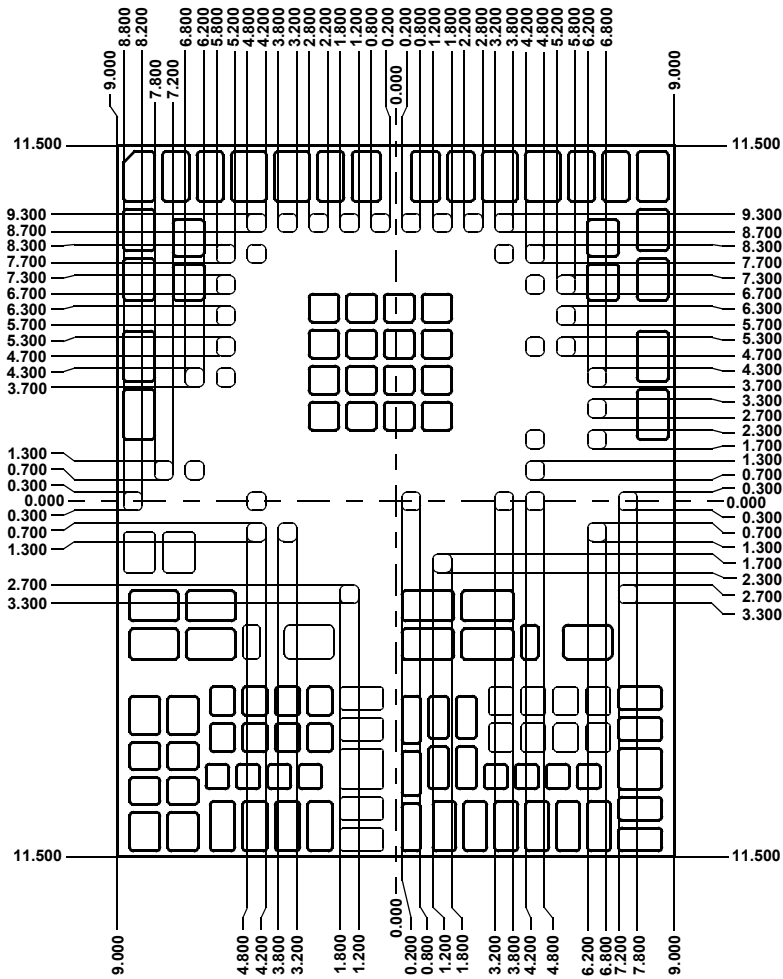
STENCIL OPENING EDGE POSITION - 3



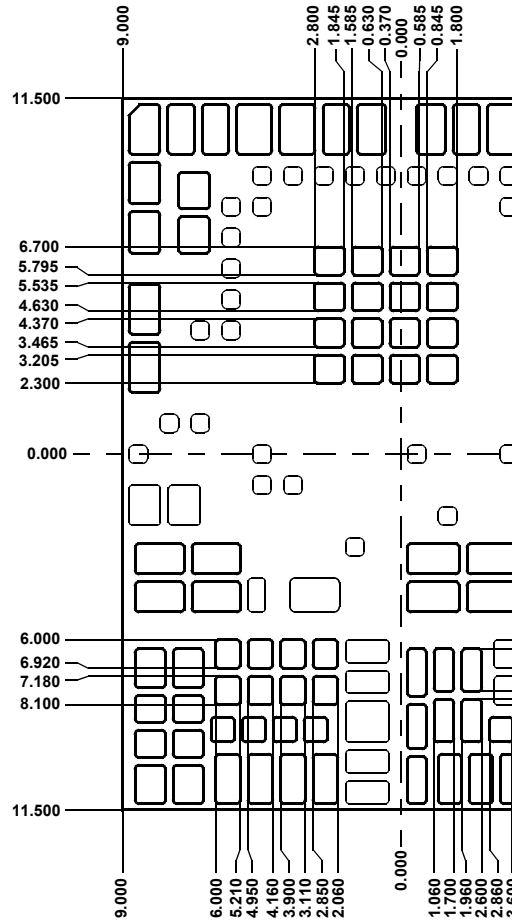
STENCIL OPENING EDGE POSITION - 4



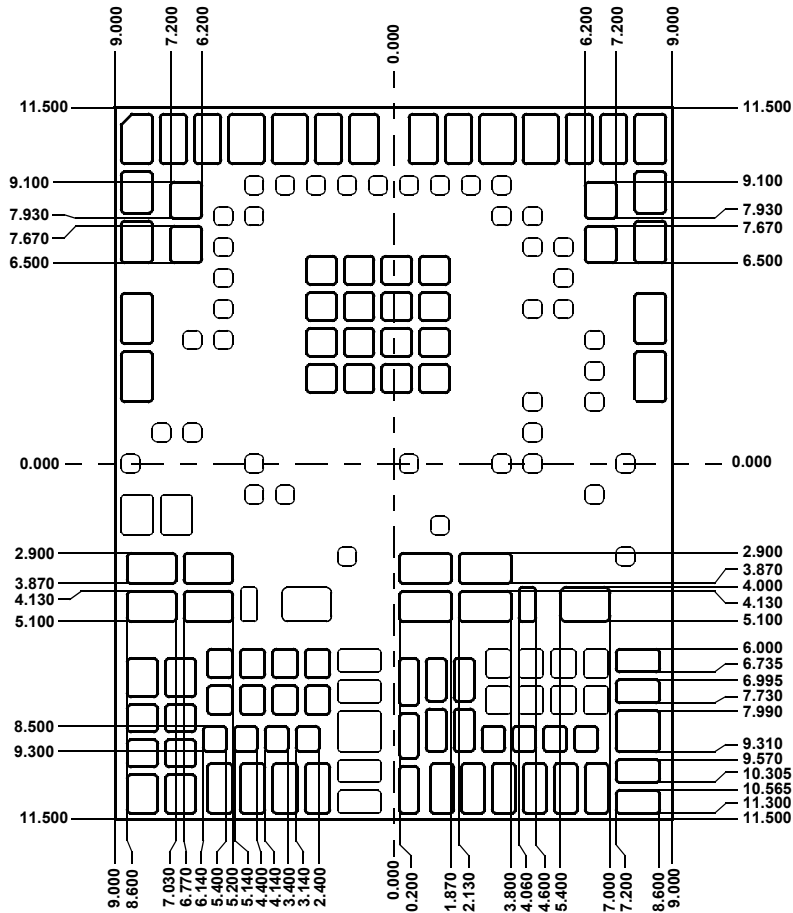




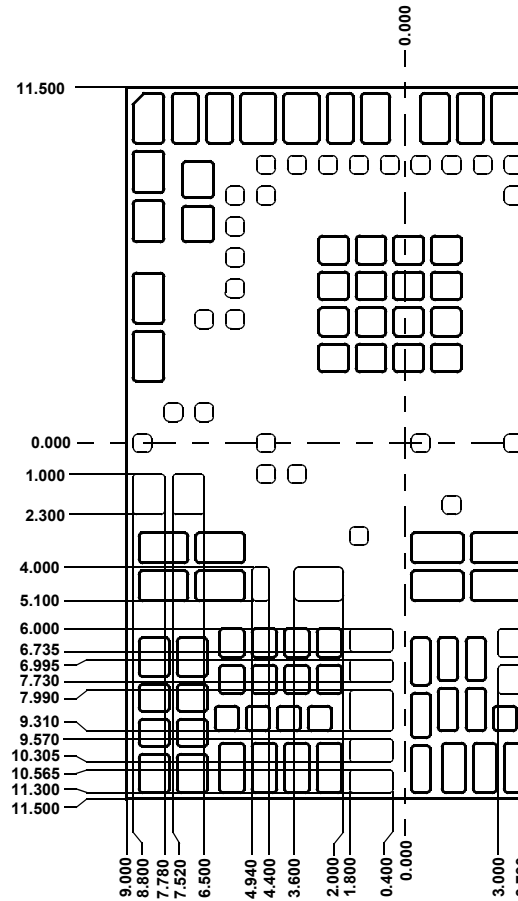
PCB LAND PATTERN - 2 (FOR REFERENCE)



PCB LAND PATTERN - 3 (FOR REFERENCE)



**PCB LAND PATTERN - 4 (FOR REFERENCE)**



**PCB LAND PATTERN - 5 (FOR REFERENCE)**

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