

## ISL84581

Low-Voltage, Single and Dual Supply, 8-to-1 Multiplexer

FN6416  
Rev 3.00  
April 13, 2009

The Intersil ISL84581 device contains precision, bidirectional, analog switches configured as an 8-to-1 multiplexer/demultiplexer. It was designed to operate from a single +2V to +12V single supply or from dual  $\pm 2V$  to  $\pm 6V$  supplies. The device has an inhibit pin to simultaneously open all signal paths.

The ISL84581 has an ON-resistance of  $39\Omega$  with a dual  $\pm 5V$  supply and  $125\Omega$  with a single +3.3V supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 0.02nA at +25°C or 0.2nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single 3.3V or +5V supply or dual  $\pm 5V$  supplies.

The ISL84581 is a single 8-to-1 multiplexer device. Table 1 summarizes the performance of the part.

**TABLE 1. FEATURES AT A GLANCE**

| CONFIGURATION             | SINGLE 8:1 MUX          |
|---------------------------|-------------------------|
| $\pm 5V$ $r_{ON}$         | 39 $\Omega$             |
| $\pm 5V$ $t_{ON}/t_{OFF}$ | 32ns/18ns               |
| 12V $r_{ON}$              | 32 $\Omega$             |
| 12V $t_{ON}/t_{OFF}$      | 23ns/15ns               |
| 5V $r_{ON}$               | 65 $\Omega$             |
| 5V $t_{ON}/t_{OFF}$       | 38ns/19ns               |
| 3.3V $r_{ON}$             | 125 $\Omega$            |
| 3.3V $t_{ON}/t_{OFF}$     | 70ns/32ns               |
| Package                   | 16 Ld TSSOP, 16 Ld QSOP |

### Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”
- Application Note AN520 “CMOS Analog Multiplexers and Switches; Specifications and Application Considerations.”
- Application Note AN1034 “Analog Switch and Multiplexer Applications”

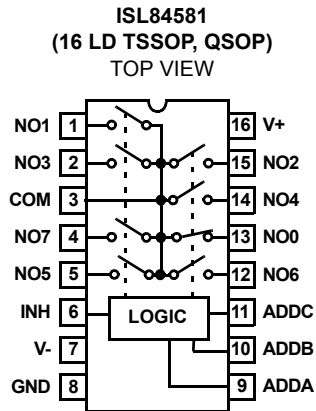
### Features

- Fully Specified at 3.3V, 5V,  $\pm 5V$ , and 12V Supplies for 10% Tolerances
- ON-Resistance ( $r_{ON}$ ) Max,  $V_S = \pm 4.5V$  . . . . . 50 $\Omega$
- ON-Resistance ( $r_{ON}$ ) Max,  $V_S = +3V$ . . . . . 155 $\Omega$
- $r_{ON}$  Matching Between Channels,  $V_S = \pm 5V$  . . . . . <2 $\Omega$
- Low Charge Injection,  $V_S = \pm 5V$  . . . . . 1pC (Max)
- Single Supply Operation. . . . . +2V to +12V
- Dual Supply Operation . . . . .  $\pm 2V$  to  $\pm 6V$
- Fast Switching Action ( $V_S = +5V$ )
  - $t_{ON}$  . . . . . 38ns
  - $t_{OFF}$  . . . . . 19ns
- Guaranteed Max Off-leakage . . . . . 2.5nA
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible
- Pb-free (RoHS Compliant)

### Applications

- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

## Pinout



NOTE: Switches Shown for Logic "0" Inputs.

## Truth Tables

| ISL84581 |      |      |      |           |
|----------|------|------|------|-----------|
| INH      | ADDC | ADDB | ADDA | SWITCH ON |
| 0        | 0    | 0    | 0    | NO0       |
| 0        | 0    | 0    | 1    | NO1       |
| 0        | 0    | 1    | 0    | NO2       |
| 0        | 0    | 1    | 1    | NO3       |
| 0        | 1    | 0    | 0    | NO4       |
| 0        | 1    | 0    | 1    | NO5       |
| 0        | 1    | 1    | 0    | NO6       |
| 0        | 1    | 1    | 1    | NO7       |
| 1        | X    | X    | X    | NONE      |

NOTE: Logic "0"  $\leq 0.8V$ . Logic "1"  $\geq 2.4V$ , with V+ between 2.7V and 10V. X = Don't Care.

## Pin Descriptions

| PIN  | FUNCTION  |
|------|---|
| V+   | Positive Power Supply Input   |
| V-   | Negative Power Supply Input. Connect to GND for Single Supply Configurations.                       |
| GND  | Ground Connection   |
| INH  | Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off. |
| ADDx | Address Input Pin   |
| COM  | Analog Switch Common Pin  |
| NOx  | Analog Switch Normally Open Pin   |

## Ordering Information

| PART NUMBER<br>(Note) | PART<br>MARKING | TEMP RANGE<br>(°C) | PACKAGE<br>(Pb-free)              | PKG.<br>DWG. # |
|-----------------------|-----------------|--------------------|-----------------------------------|----------------|
| ISL84581IVZ           | 84581 IVZ       | -40 to +85         | 16 Ld TSSOP (4.4mm)               | M16.173        |
| ISL84581IVZ-T*        | 84581 IVZ       | -40 to +85         | 16 Ld TSSOP (4.4mm) Tape and Reel | M16.173        |
| ISL84581IAZ           | 84581 IAZ       | -40 to +85         | 16 Ld QSOP (4.4mm)                | M16.15A        |
| ISL84581IAZ-T*        | 84581 IAZ       | -40 to +85         | 16 Ld QSOP (4.4mm) Tape and Reel  | M16.15A        |

\* Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Absolute Maximum Ratings**

|   |                       |
|---|-----------------------|
| V+ to V-  | -0.3V to 15V          |
| V+ to GND   | -0.3V to 15V          |
| V- to GND   | -15V to 0.3V          |
| Input Voltages                                    |                       |
| INH, NOx, ADDx (Note 1)                           | -0.3 to ((V+) + 0.3V) |
| Output Voltages                                   |                       |
| COM (Note 1)                                      | -0.3 to ((V+) + 0.3V) |
| Continuous Current (Any Terminal)                 | ±30mA                 |
| Peak Current NOx, COM                             |                       |
| (Pulsed 1ms, 10% Duty Cycle, Max)                 | ±100mA                |
| ESD Rating  |                       |
| Human Body Model (Per Mil-STD-883, Method 3015.7) | >2.5kV                |

**Thermal Information**

|  |   |
|--|---|
| Thermal Resistance (Typical, Note 2)           | $\theta_{JA}$ (°C/W)  |
| 16 Ld TSSOP Package                            | 110   |
| 16 Ld QSOP Package                             | 160   |
| Maximum Junction Temperature (Plastic Package) | +150°C  |
| Maximum Storage Temperature Range              | -65°C to +150°C   |
| Pb-free Reflow Profile                         | see link below  |
|  | <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |

**Operating Conditions**

|                   |                |
|-------------------|----------------|
| Temperature Range | -40°C to +85°C |
|-------------------|----------------|

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

1. Signals on NOx, COM, ADDx, INH exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
2.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications ±5V Supply**

Test Conditions:  $V_{SUPPLY} = \pm 4.5V$  to  $\pm 5.5V$ , GND = 0V,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified.

| PARAMETER  | TEST CONDITIONS   | TEMP (°C) | MIN (Notes 4, 8) | TYP  | MAX (Notes 4, 8) | UNITS    |
|--|---|-----------|------------------|------|------------------|----------|
| <b>ANALOG SWITCH CHARACTERISTICS</b>                           |   |           |                  |      |                  |          |
| Analog Signal Range, $V_{ANALOG}$                              | (Note 10)   | Full      | V-               | -    | V+               | V        |
| ON-Resistance, $r_{ON}$  | $V_S = \pm 4.5V$ , $I_{COM} = 2mA$ , $V_{NO} = 3V$<br>(See Figure 5)  | 25        | -                | 44   | 60               | $\Omega$ |
|  |   | Full      | -                | -    | 80               | $\Omega$ |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$            | $V_S = \pm 4.5V$ , $I_{COM} = 2mA$ , $V_{NO} = 3V$ (Note 5)   | 25        | -                | 1.3  | 4                | $\Omega$ |
|  |   | Full      | -                | -    | 6                | $\Omega$ |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$                              | $V_S = \pm 4.5V$ , $I_{COM} = 2mA$ , $V_{NO} = \pm 3V$ , 0.1V<br>(Note 6)   | 25        | -                | 7.5  | 9                | $\Omega$ |
|  |   | Full      | -                | -    | 12               | $\Omega$ |
| NO OFF Leakage Current, $I_{NO(OFF)}$                          | $V_S = \pm 5.5V$ , $V_{COM} = \pm 4.5V$ , $V_{NO} = \mp 4.5V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM OFF Leakage Current, $I_{COM(OFF)}$                        | $V_S = \pm 5.5V$ , $V_{COM} = \pm 4.5V$ , $V_{NO} = \mp 4.5V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM ON Leakage Current, $I_{COM(ON)}$                          | $V_S = \pm 5.5V$ , $V_{COM} = V_{NO} = \pm 4.5V$ (Note 7)   | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                           |   |           |                  |      |                  |          |
| Input Voltage High, $V_{INH}$ , $V_{ADDH}$                     |   | Full      | 2.4              | -    | -                | V        |
| Input Voltage Low, $V_{INL}$ , $V_{ADDL}$                      |   | Full      | -                | -    | 0.8              | V        |
| Input Current, $I_{ADDH}$ , $I_{ADDL}$ , $I_{INH}$ , $I_{INL}$ | $V_S = \pm 5.5V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V+$ , (Note 9)  | Full      | -0.5             | -    | 0.5              | $\mu A$  |
| <b>DYNAMIC CHARACTERISTICS</b>                                 |   |           |                  |      |                  |          |
| INHIBIT Turn-ON Time, $t_{ON}$                                 | $V_S = \pm 4.5V$ , $V_{NO} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to 3 (See Figure 1, Note 9) | 25        | -                | 35   | 50               | ns       |
|  |   | Full      | -                | -    | 60               | ns       |
| INHIBIT Turn-OFF Time, $t_{OFF}$                               | $V_S = \pm 4.5V$ , $V_{NO} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to 3 (See Figure 1, Note 9) | 25        | -                | 22   | 35               | ns       |
|  |   | Full      | -                | -    | 40               | ns       |
| Address Transition Time, $t_{TRANS}$                           | $V_S = \pm 4.5V$ , $V_{NO} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to 3 (See Figure 1, Note 9) | 25        | -                | 43   | 60               | ns       |
|  |   | Full      | -                | -    | 70               | ns       |

**Electrical Specifications ±5V Supply**

Test Conditions:  $V_{SUPPLY} = \pm 4.5V$  to  $\pm 5.5V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified. (Continued)

| PARAMETER                           | TEST CONDITIONS   | TEMP (°C) | MIN (Notes 4, 8) | TYP | MAX (Notes 4, 8) | UNITS   |
|-------------------------------------|---|-----------|------------------|-----|------------------|---------|
| Break-Before-Make Time, $t_{BBM}$   | $V_S = \pm 5.5V$ , $V_{NO} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3V$ (See Figure 3, Note 9) | Full      | 2                | 7   | -                | ns      |
| Charge Injection, $Q$               | $C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (See Figure 2, Note 9)   | 25        | -                | 0.3 | 1                | pC      |
| NO OFF Capacitance, $C_{OFF}$       | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)   | 25        | -                | 3   | -                | pF      |
| COM OFF Capacitance, $C_{OFF}$      | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)   | 25        | -                | 21  | -                | pF      |
| COM ON Capacitance, $C_{COM(ON)}$   | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)   | 25        | -                | 26  | -                | pF      |
| OFF-Isolation                       | $R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NOx} = 1V_{RMS}$ (See Figures 4 and 18)                      | 25        | -                | 92  | -                | dB      |
| <b>POWER SUPPLY CHARACTERISTICS</b> |   |           |                  |     |                  |         |
| Power Supply Range                  | (Note 10)   | Full      | $\pm 2$          | -   | $\pm 6$          | V       |
| Positive Supply Current, $I_+$      | $V_S = \pm 5.5V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$ , Switch On or Off, (Note 9)                               | Full      | -7               | -   | 7                | $\mu A$ |
| Negative Supply Current, $I_-$      |   | Full      | -1               | -   | 1                | $\mu A$ |

**Electrical Specifications +12V Supply**

Test Conditions:  $V_+ = +10.8V$  to  $+13.2V$ ,  $GND = 0V$ ,  $V_{INH} = 4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified.

| PARAMETER  | TEST CONDITIONS  | TEMP (°C) | MIN (Notes 4, 8) | TYP  | MAX (Notes 4, 8) | UNITS    |
|--|--|-----------|------------------|------|------------------|----------|
| <b>ANALOG SWITCH CHARACTERISTICS</b>                             |  |           |                  |      |                  |          |
| Analog Signal Range, $V_{ANALOG}$                                | (Note 10)  | Full      | 0                | -    | $V_+$            | V        |
| ON-Resistance, $r_{ON}$  | $V_+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 9V$ (See Figure 5)   | 25        | -                | 37   | 45               | $\Omega$ |
|  |  | Full      | -                | -    | 55               | $\Omega$ |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$              | $V_+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 9V$ (Note 5)   | 25        | -                | 1.2  | 2                | $\Omega$ |
|  |  | Full      | -                | -    | 2                | $\Omega$ |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$                                | $V_+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 3V, 6V, 9V$ (Note 6)   | Full      | -                | 5    | -                | $\Omega$ |
| NO OFF Leakage Current, $I_{NO(OFF)}$                            | $V_+ = 13.2V$ , $V_{COM} = 1V, 12V$ , $V_{NO} = 12V, 1V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |  | Full      | -                | 0.2  | -                | nA       |
| COM OFF Leakage Current, $I_{COM(OFF)}$                          | $V_+ = 13.2V$ , $V_{COM} = 12V, 1V$ , $V_{NO} = 1V, 12V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |  | Full      | -                | 0.2  | -                | nA       |
| COM ON Leakage Current, $I_{COM(ON)}$                            | $V_+ = 13.2V$ , $V_{COM} = 1V, 12V$ , $V_{NO} = 1V, 12V$ , or floating (Note 7)                                | 25        | -                | 0.02 | -                | nA       |
|  |  | Full      | -                | 0.2  | -                | nA       |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                             |  |           |                  |      |                  |          |
| Input Voltage High, $V_{INHh}$ , $V_{ADDH}$                      |  | Full      | 3.7              | 3.3  | -                | V        |
| Input Voltage Low, $V_{INHL}$ , $V_{ADDL}$                       |  | Full      | -                | 2.7  | 0.8              | V        |
| Input Current, $I_{ADDH}$ , $I_{ADDL}$ , $I_{INHh}$ , $I_{INHL}$ | $V_+ = 13.2V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$  | Full      | -0.5             | -    | 0.5              | $\mu A$  |
| <b>DYNAMIC CHARACTERISTICS</b>                                   |  |           |                  |      |                  |          |
| INHIBIT Turn-ON Time, $t_{ON}$                                   | $V_+ = 10.8V$ , $V_{NO} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $4$ (See Figure 1, Note 9) | 25        | -                | 24   | 40               | ns       |
|  |  | Full      | -                | -    | 45               | ns       |
| INHIBIT Turn-OFF Time, $t_{OFF}$                                 | $V_+ = 10.8V$ , $V_{NO} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $4$ (See Figure 1, Note 9) | 25        | -                | 15   | 30               | ns       |
|  |  | Full      | -                | -    | 35               | ns       |

**Electrical Specifications +12V Supply**

Test Conditions:  $V_+ = +10.8V$  to  $+13.2V$ ,  $GND = 0V$ ,  $V_{INH} = 4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified. (Continued)

| PARAMETER                            | TEST CONDITIONS  | TEMP (°C) | MIN (Notes 4, 8) | TYP | MAX (Notes 4, 8) | UNITS   |
|--------------------------------------|--|-----------|------------------|-----|------------------|---------|
| Address Transition Time, $t_{TRANS}$ | $V_+ = 10.8V$ , $V_{NO} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to 4 (See Figure 1, Note 9) | 25        | -                | 27  | 50               | ns      |
|                                      |  | Full      | -                | -   | 55               | ns      |
| Break-Before-Make Time Delay, $t_D$  | $V_+ = 13.2V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{NO} = 10V$ , $V_{IN} = 0$ to 4 (See Figure 3, Note 9) | Full      | 2                | 5   | -                | ns      |
| Charge Injection, Q                  | $C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (See Figure 2, Note 9)  | 25        | -                | 2.7 | 5                | pC      |
| OFF-Isolation                        | $R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ (See Figures 4 and 18)  | 25        | -                | 92  | -                | dB      |
| NO OFF Capacitance, $C_{OFF}$        | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)  | 25        | -                | 3   | -                | pF      |
| COM OFF Capacitance, $C_{COM(OFF)}$  | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)  | 25        | -                | 21  | -                | pF      |
| COM ON Capacitance, $C_{COM(ON)}$    | $f = 1MHz$ , $V_{NO} = V_{COM} = 0V$ (See Figure 6)  | 25        | -                | 26  | -                | pF      |
| <b>POWER SUPPLY CHARACTERISTICS</b>  |  |           |                  |     |                  |         |
| Power Supply Range                   | (Note 10)  | Full      | 2                | -   | 12               | V       |
| Positive Supply Current, $I_+$       | $V_+ = 13.2V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$ , all channels on or off                                 | Full      | -7               | -   | 7                | $\mu A$ |

**Electrical Specifications 5V Supply**

Test Conditions:  $V_+ = +4.5V$  to  $+5.5V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified.

| PARAMETER  | TEST CONDITIONS   | TEMP (°C) | MIN (Notes 4, 8) | TYP  | MAX (Notes 4, 8) | UNITS    |
|--|---|-----------|------------------|------|------------------|----------|
| <b>ANALOG SWITCH CHARACTERISTICS</b>                           |   |           |                  |      |                  |          |
| Analog Signal Range, $V_{ANALOG}$                              | (Note 10)   | Full      | 0                | -    | $V_+$            | V        |
| ON-Resistance, $r_{ON}$  | $V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 3.5V$ (See Figure 5)   | 25        | -                | 81   | 100              | $\Omega$ |
|  |   | Full      | -                | -    | 120              | $\Omega$ |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$            | $V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 3V$ (Note 5)   | 25        | -                | 2.2  | 4                | $\Omega$ |
|  |   | Full      | -                | -    | 6                | $\Omega$ |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$                              | $V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 1V, 2V, 3V$ (Note 6)   | Full      | -                | 11.5 | -                | $\Omega$ |
| NO OFF Leakage Current, $I_{NO(OFF)}$                          | $V_+ = 5.5V$ , $V_{COM} = 1V, 4.5V$ , $V_{NO} = 4.5V, 1V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM OFF Leakage Current, $I_{COM(OFF)}$                        | $V_+ = 5.5V$ , $V_{COM} = 1V, 4.5V$ , $V_{NO} = 4.5V, 1V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM ON Leakage Current, $I_{COM(ON)}$                          | $V_+ = 5.5V$ , $V_{COM} = V_{NO} = 4.5V$ (Note 7)   | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                           |   |           |                  |      |                  |          |
| Input Voltage High, $V_{INH}$ , $V_{ADDH}$                     |   | Full      | 2.4              | -    | -                | V        |
| Input Voltage Low, $V_{INL}$ , $V_{ADDL}$                      |   | Full      | -                | -    | 0.8              | V        |
| Input Current, $I_{ADDH}$ , $I_{ADDL}$ , $I_{INH}$ , $I_{INL}$ | $V_+ = 5.5V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$ , (Note 9)   | Full      | -0.5             | -    | 0.5              | $\mu A$  |
| <b>DYNAMIC CHARACTERISTICS</b>                                 |   |           |                  |      |                  |          |
| INHIBIT Turn-ON Time, $t_{ON}$                                 | $V_+ = 4.5V$ , $V_{NO} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to 3V (see Figure 1, Note 9) | 25        | -                | 43   | 60               | ns       |
|  |   | Full      | -                | -    | 70               | ns       |

**Electrical Specifications 5V Supply**

Test Conditions:  $V_+ = +4.5V$  to  $+5.5V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3),  
Unless Otherwise Specified. (Continued)

| PARAMETER                            | TEST CONDITIONS  | TEMP (°C) | MIN (Notes 4, 8) | TYP | MAX (Notes 4, 8) | UNITS   |
|--------------------------------------|--|-----------|------------------|-----|------------------|---------|
| INHIBIT Turn-OFF Time, $t_{OFF}$     | $V_+ = 4.5V$ , $V_{NO} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to $3V$ (see Figure 1, Note 9) | 25        | -                | 20  | 35               | ns      |
|                                      |  | Full      | -                | -   | 40               | ns      |
| Address Transition Time, $t_{TRANS}$ | $V_+ = 4.5V$ , $V_{NO} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to $3V$ (see Figure 1, Note 9) | 25        | -                | 51  | 70               | ns      |
|                                      |  | Full      | -                | -   | 85               | ns      |
| Break-Before-Make Time, $t_{BBM}$    | $V_+ = 5.5V$ , $V_{NO} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0$ to $3V$ (see Figure 3, Note 9) | Full      | 2                | 9   | -                | ns      |
| Charge Injection, Q                  | $C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (see Figure 2, Note 9)  | 25        | -                | 0.6 | 1.5              | pC      |
| OFF-Isolation                        | $R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NOx} = 1V_{RMS}$<br>(see Figures 4 and 18)                  | 25        | -                | 92  | -                | dB      |
| <b>POWER SUPPLY CHARACTERISTICS</b>  |  |           |                  |     |                  |         |
| Power Supply Range                   | (Note 10)  | Full      | 2                | -   | 12               | V       |
| Positive Supply Current, $I_+$       | $V_+ = 5.5V$ , $V_- = 0V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$ ,<br>Switch On or Off, (Note 9)                  | Full      | -7               | -   | 7                | $\mu A$ |
| Positive Supply Current, $I_-$       |  | Full      | -1               | -   | 1                | $\mu A$ |

**Electrical Specifications 3.3V Supply**

Test Conditions:  $V_+ = +3.0V$  to  $+3.6V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3),  
Unless Otherwise Specified

| PARAMETER  | TEST CONDITIONS   | TEMP (°C) | MIN (Notes 4, 8) | TYP  | MAX (Notes 4, 8) | UNITS    |
|--|---|-----------|------------------|------|------------------|----------|
| <b>ANALOG SWITCH CHARACTERISTICS</b>                             |   |           |                  |      |                  |          |
| Analog Signal Range, $V_{ANALOG}$                                |   | Full      | 0                | -    | $V_+$            | V        |
| ON-Resistance, $r_{ON}$  | $V_+ = 3.0V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 1.5V$ (see Figure 5)   | 25        | -                | 135  | 180              | $\Omega$ |
|  |   | Full      | -                | -    | 200              | $\Omega$ |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$              | $V_+ = 3.0V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 1.5V$ (Note 5)   | 25        | -                | 3.4  | 8                | $\Omega$ |
|  |   | Full      | -                | -    | 10               | $\Omega$ |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$                                | $V_+ = 3.0V$ , $I_{COM} = 1.0mA$ , $V_{NO} = 0.5V, 1V, 2V$<br>(Note 6)  | Full      | -                | 34   | -                | $\Omega$ |
| NO OFF Leakage Current, $I_{NO(OFF)}$                            | $V_+ = 3.6V$ , $V_{COM} = 0V, 4.5V$ , $V_{NO} = 3V, 1V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM OFF Leakage Current, $I_{COM(OFF)}$                          | $V_+ = 3.6V$ , $V_{COM} = 0V, 4.5V$ , $V_{NO} = 3V, 1V$ (Note 7)  | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| COM ON Leakage Current, $I_{COM(ON)}$                            | $V_+ = 3.6V$ , $V_{COM} = V_{NO} = 3V$ (Note 7)   | 25        | -                | 0.02 | -                | nA       |
|  |   | Full      | -                | 0.2  | -                | nA       |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                             |   |           |                  |      |                  |          |
| Input Voltage High, $V_{INHh}$ , $V_{ADDh}$                      |   | Full      | 2.4              | -    | -                | V        |
| Input Voltage Low, $V_{INLh}$ , $V_{ADDl}$                       |   | Full      | -                | -    | 0.8              | V        |
| Input Current, $I_{ADDh}$ , $I_{ADDl}$ , $I_{INHh}$ , $I_{INLh}$ | $V_+ = 3.6V$ , $V_{INH}$ , $V_{ADD} = 0V$ or $V_+$ , (Note 9)   | Full      | -0.5             | -    | 0.5              | $\mu A$  |
| <b>DYNAMIC CHARACTERISTICS</b>                                   |   |           |                  |      |                  |          |
| INHIBIT Turn-ON Time, $t_{ON}$                                   | $V_+ = 3.0V$ , $V_{NO} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ ,<br>$V_{IN} = 0V$ to $3V$ (see Figure 1, Note 9) | 25        | -                | 82   | 100              | ns       |
|  |   | Full      | -                | -    | 120              | ns       |

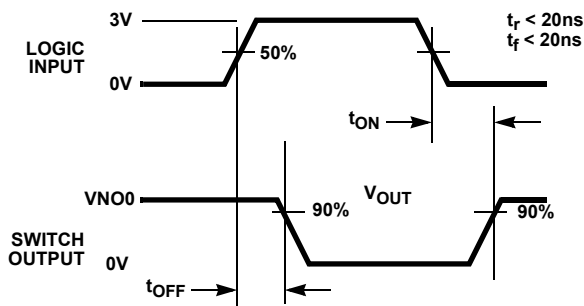
**Electrical Specifications 3.3V Supply** Test Conditions:  $V_+ = +3.0V$  to  $+3.6V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 3), Unless Otherwise Specified **(Continued)**

| PARAMETER                            | TEST CONDITIONS  | TEMP (°C) | MIN (Notes 4, 8) | TYP | MAX (Notes 4, 8) | UNITS |
|--------------------------------------|--|-----------|------------------|-----|------------------|-------|
| INHIBIT Turn-OFF Time, $t_{OFF}$     | $V_+ = 3.0V$ , $V_{NO} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $3V$ (see Figure 1, Note 9) | 25        | -                | 37  | 50               | ns    |
|                                      |  | Full      | -                | -   | 60               | ns    |
| Address Transition Time, $t_{TRANS}$ | $V_+ = 3.0V$ , $V_{NO} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $3V$ (see Figure 1, Note 9) | 25        | -                | 96  | 120              | ns    |
|                                      |  | Full      | -                | -   | 145              | ns    |
| Break-Before-Make Time, $t_{BBM}$    | $V_+ = 3.6V$ , $V_{NO} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $3V$ (see Figure 3, Note 9) | Full      | 3                | 13  | -                | ns    |
| Charge Injection, Q                  | $C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (see Figure 2, Note 9)  | 25        | -                | 0.3 | 1                | pC    |
| OFF-Isolation                        | $R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NO} = 1V_{RMS}$ (see Figures 4 and 18)                      | 25        | -                | 92  | -                | dB    |
| <b>POWER SUPPLY CHARACTERISTICS</b>  |  |           |                  |     |                  |       |
| Power Supply Range                   | (Note 10)  | Full      | 2                | -   | 12               | V     |

NOTES:

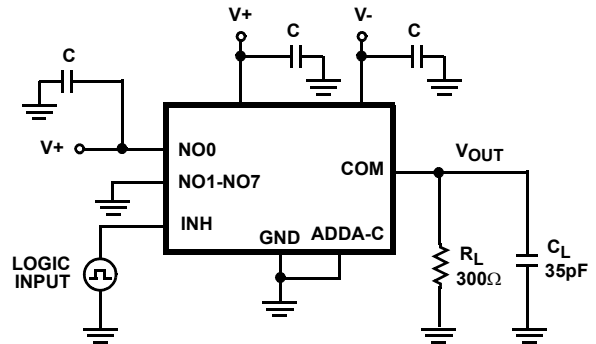
- $V_{IN}$  = Input logic voltage to configure the device in a given state.
- The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- $\Delta r_{ON} = r_{ON} (MAX) - r_{ON} (MIN)$ .
- Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
- Leakage parameter is 100% tested at high temp, and guaranteed by correlation at  $+25^\circ C$ .
- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Limits established by characterization and are not production tested.
- Limits should be considered typical and are not production tested.

**Test Circuits and Waveforms**



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. INHIBIT  $t_{ON}/t_{OFF}$  MEASUREMENT POINTS

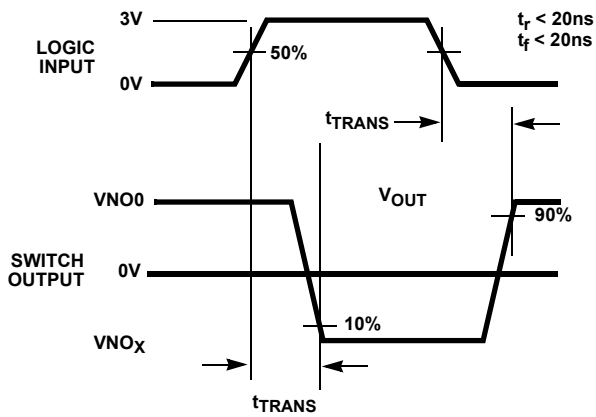


Repeat test for other switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{ON}}$$

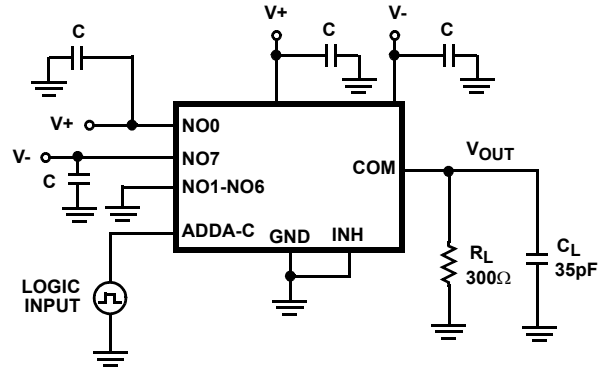
FIGURE 1B. INHIBIT  $t_{ON}/t_{OFF}$  TEST CIRCUIT

**Test Circuits and Waveforms** (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS  $t_{TRANS}$  MEASUREMENT POINTS



Repeat test for other switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1D. ADDRESS  $t_{TRANS}$  TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

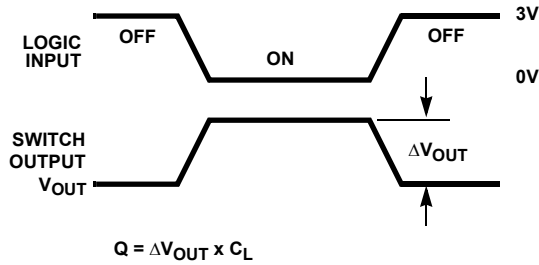
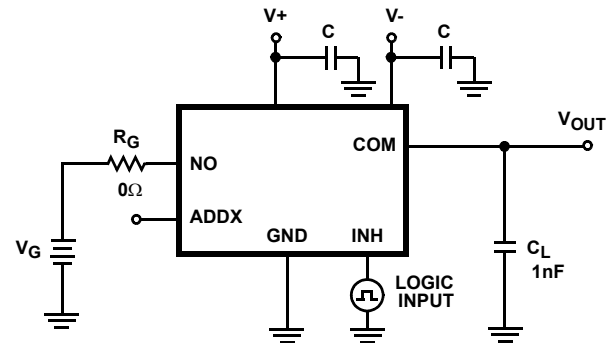


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

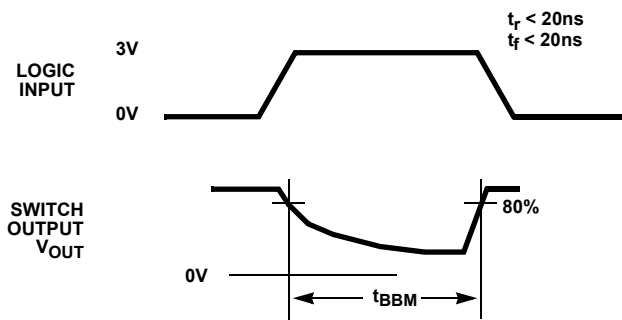
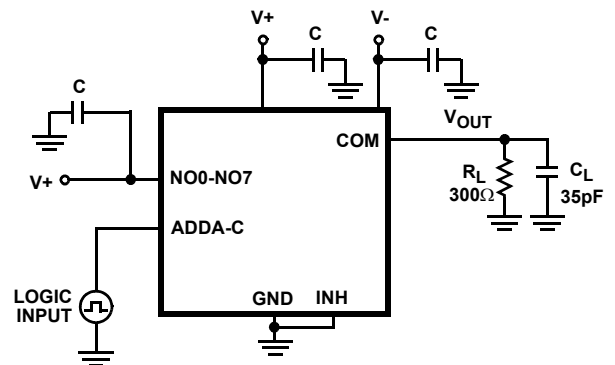


FIGURE 3A.  $t_{BBM}$  MEASUREMENT POINTS



Repeat test for other switches.  $C_L$  includes fixture and stray capacitance.

FIGURE 3B.  $t_{BBM}$  TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



**Test Circuits and Waveforms** (Continued)

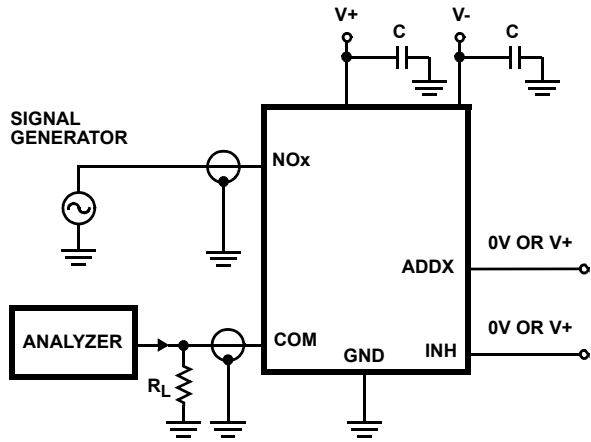


FIGURE 4. OFF-ISOLATION TEST CIRCUIT

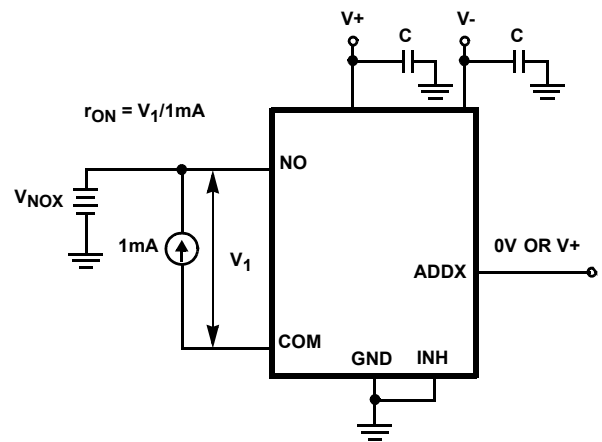


FIGURE 5.  $r_{ON}$  TEST CIRCUIT

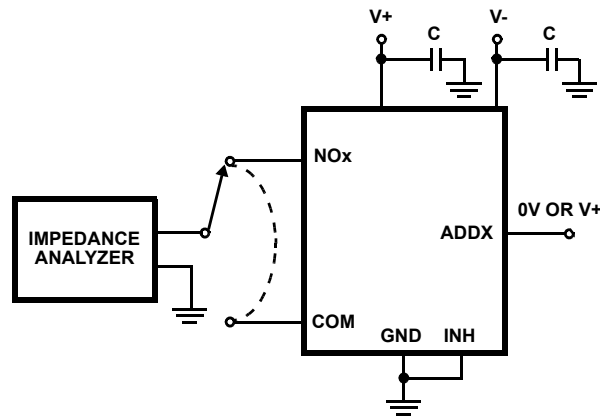


FIGURE 6. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL84581 multiplexer offers precise switching capability from bipolar  $\pm 2V$  to  $\pm 6V$  supplies or a single 2V to 12V supply. When powered with dual  $\pm 5V$  supplies the part has low ON-resistance ( $39\Omega$ ) and high speed operation ( $t_{ON} = 38ns$ ,  $t_{OFF} = 19ns$ ).

It has an inhibit pin to simultaneously open all signal paths.

The device is especially well suited for applications using  $\pm 5V$  supplies. With  $\pm 5V$  supplies the performance ( $r_{ON}$ , Leakage, Charge Injection, etc.) is best in class.

High frequency applications also benefit from the wide bandwidth and high off-isolation.

### Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 7). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a  $1k\Omega$  resistor in series with the input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low  $r_{ON}$  switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 7). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

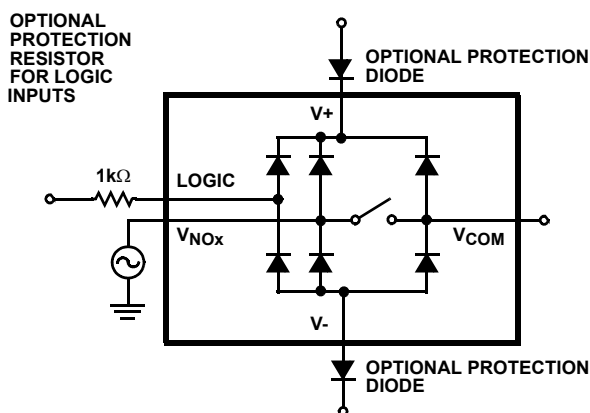


FIGURE 7. INPUT OVERVOLTAGE PROTECTION

## Power-Supply Considerations

The ISL84581 construction is typical of most CMOS analog switches, in that it has three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL84581 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies ( $\pm 6V$  or 12V single supply), as well as room for overshoot and noise spikes.

The part performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V single supply or  $\pm 2V$  dual supply. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the "Electrical Specification" tables on page 4 and "Typical Performance Curves" on page 11 for details.

V+ and GND power the internal logic setting the digital switching point of the level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

### Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no effect on logic thresholds. This ISL84581 is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the  $V_{IH}$  level is about 3.3V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a  $V_{OH}$  greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

### High-Frequency Performance

In  $50\Omega$  systems, signal response is reasonably flat even past 100MHz (see Figures 16 and 17). Figures 16 and 17 also illustrate that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off-isolation is the resistance to this feed through. Figure 18 details the high off isolation of the ISL84581. At 10MHz, off-isolation is about 55dB in  $50\Omega$  systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off-isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

**Leakage Considerations**

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either

V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified

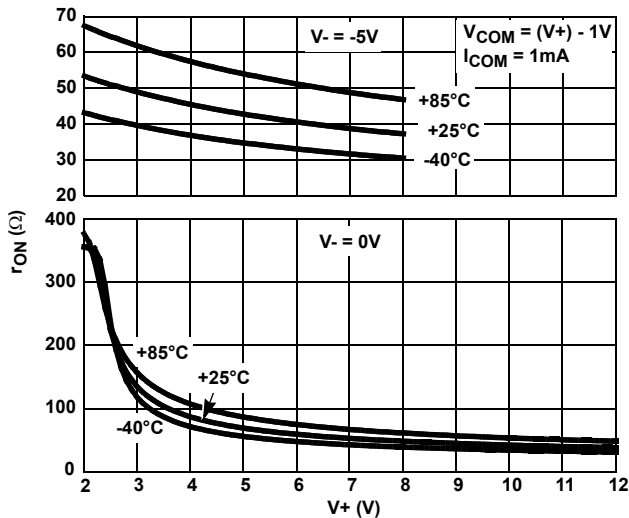


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE

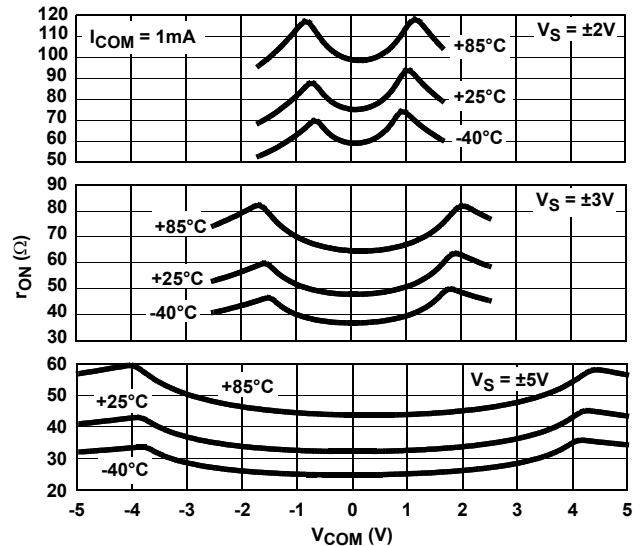


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

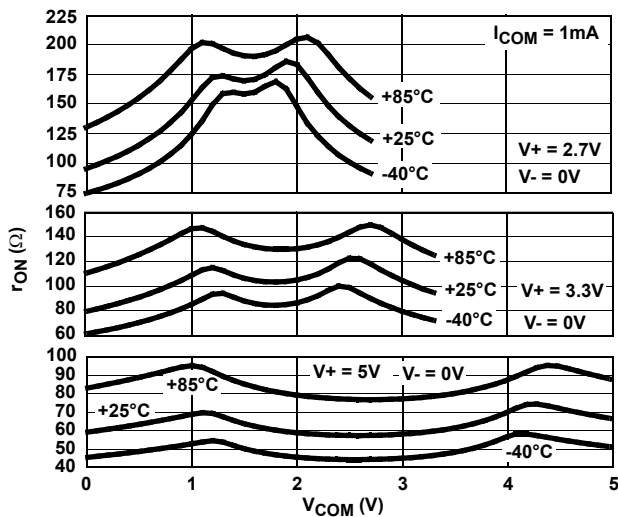


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

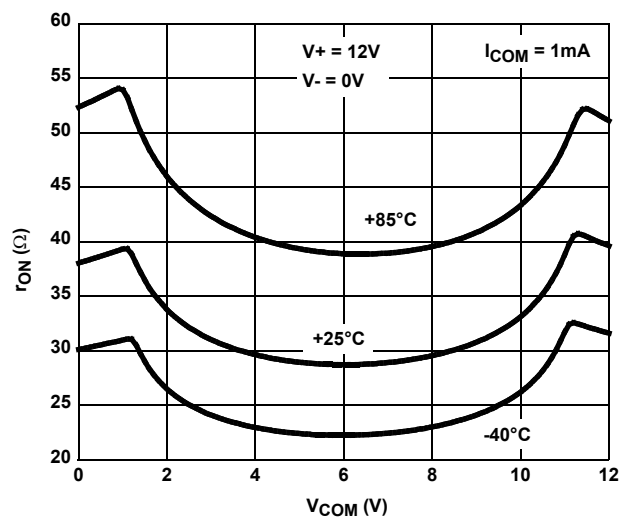


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

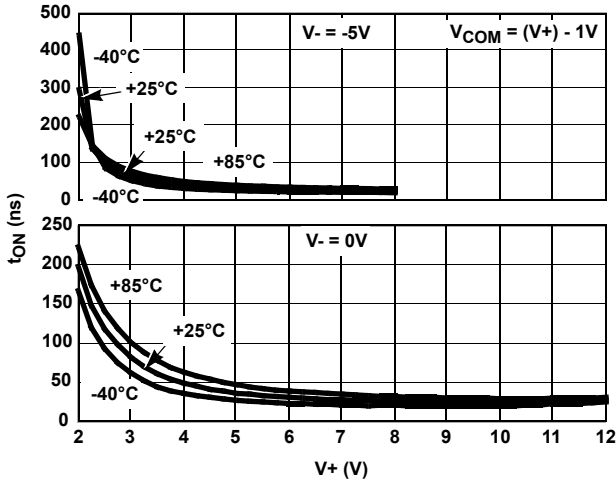


FIGURE 12. INHIBIT TURN-ON TIME vs SUPPLY VOLTAGE

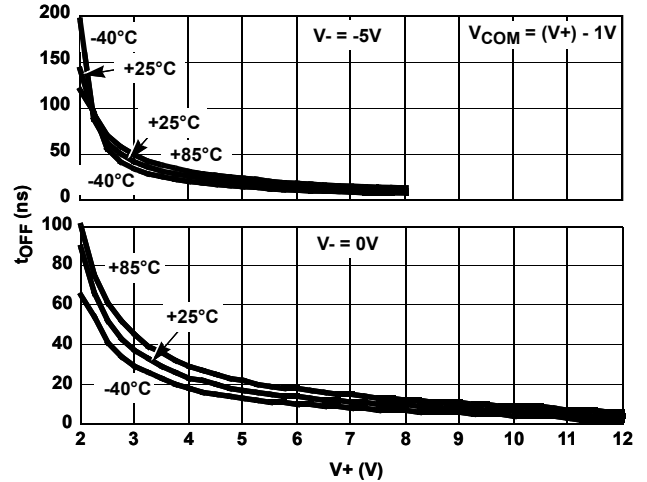


FIGURE 13. INHIBIT TURN-OFF TIME vs SUPPLY VOLTAGE

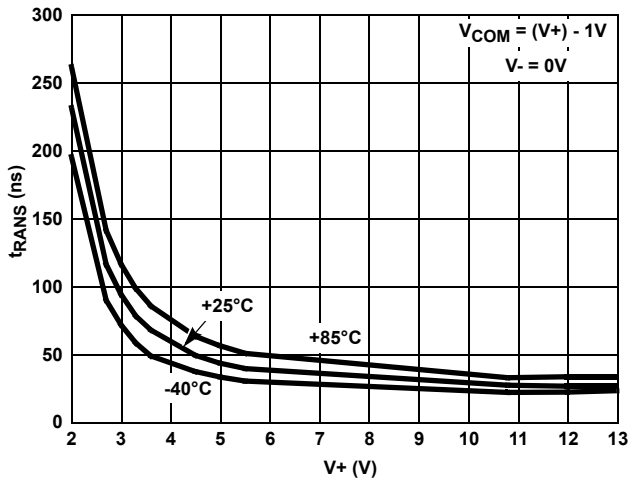


FIGURE 14. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

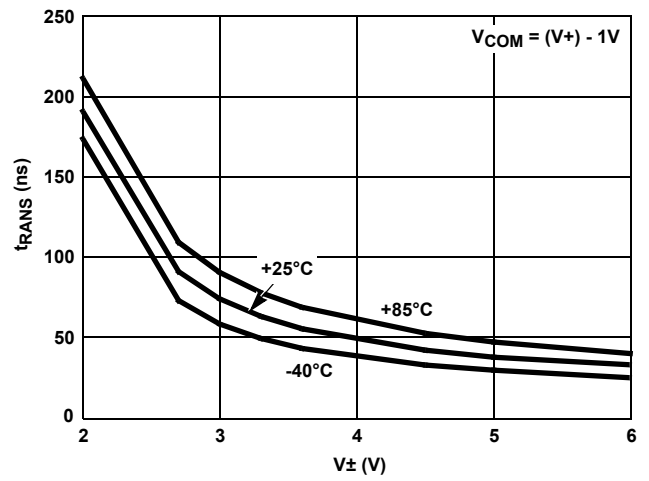


FIGURE 15. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

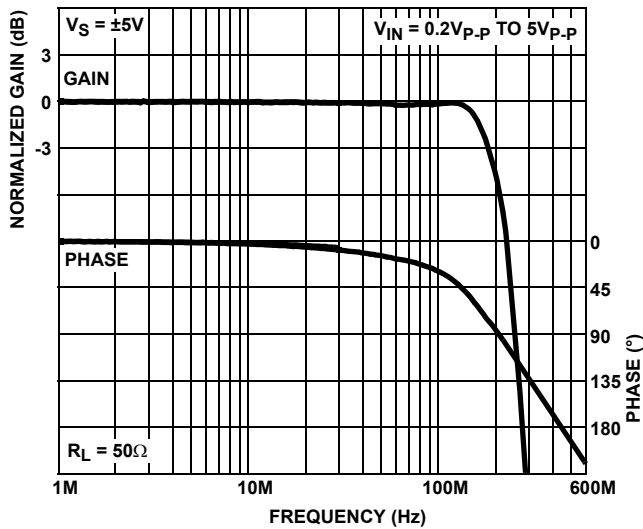


FIGURE 16. FREQUENCY RESPONSE

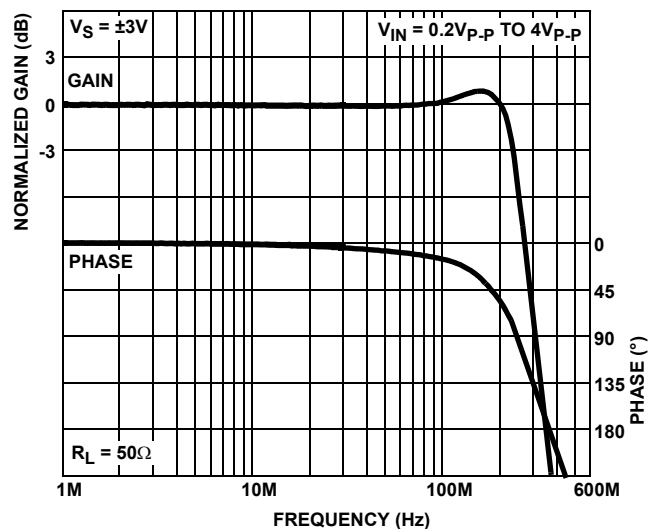


FIGURE 17. FREQUENCY RESPONSE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

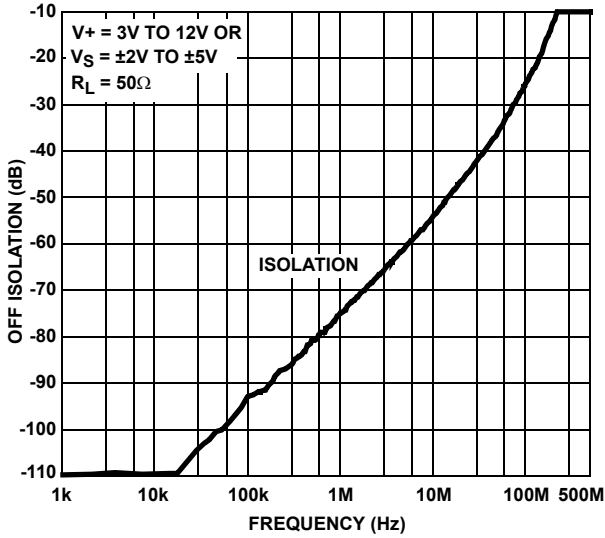


FIGURE 18. OFF ISOLATION

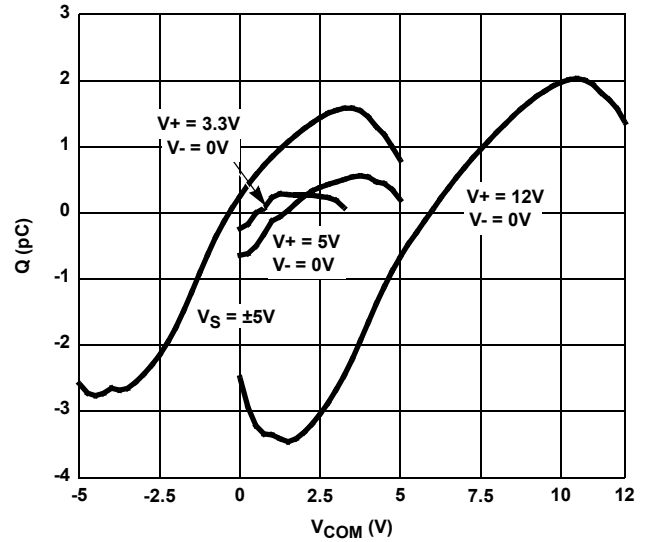


FIGURE 19. CHARGE INJECTION vs SWITCH VOLTAGE

**Die Characteristics**

**SUBSTRATE POTENTIAL (POWERED UP):**

$V_-$

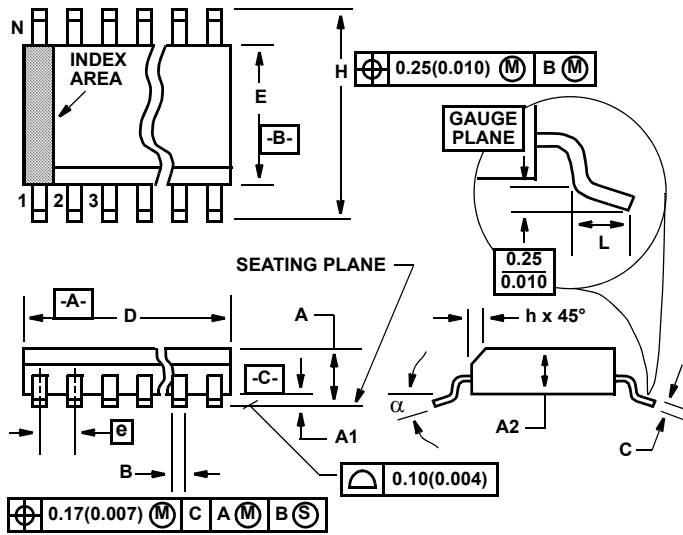
**TRANSISTOR COUNT:**

193

**PROCESS:**

Si Gate CMOS

**Shrink Small Outline Plastic Packages (SSOP)  
Quarter Size Outline Plastic Packages (QSOP)**



**M16.15A**  
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE  
(0.150" WIDE BODY)

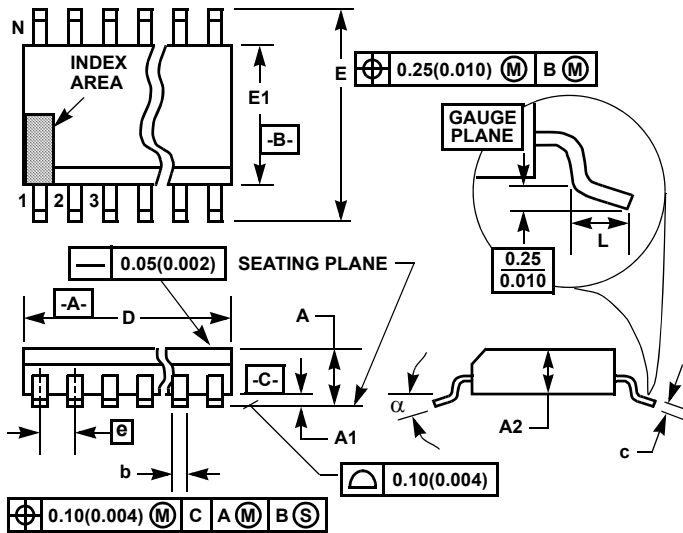
| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN       | MAX    | MIN         | MAX   |       |
| A      | 0.061     | 0.068  | 1.55        | 1.73  | -     |
| A1     | 0.004     | 0.0098 | 0.102       | 0.249 | -     |
| A2     | 0.055     | 0.061  | 1.40        | 1.55  | -     |
| B      | 0.008     | 0.012  | 0.20        | 0.31  | 9     |
| C      | 0.0075    | 0.0098 | 0.191       | 0.249 | -     |
| D      | 0.189     | 0.196  | 4.80        | 4.98  | 3     |
| E      | 0.150     | 0.157  | 3.81        | 3.99  | 4     |
| e      | 0.025 BSC |        | 0.635 BSC   |       | -     |
| H      | 0.230     | 0.244  | 5.84        | 6.20  | -     |
| h      | 0.010     | 0.016  | 0.25        | 0.41  | 5     |
| L      | 0.016     | 0.035  | 0.41        | 0.89  | 6     |
| N      | 16        |        | 16          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    | -     |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Rev. 2 6/04

**Thin Shrink Small Outline Plastic Packages (TSSOP)**



**M16.173**  
**16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | -         | 0.043 | -           | 1.10 | -     |
| A1     | 0.002     | 0.006 | 0.05        | 0.15 | -     |
| A2     | 0.033     | 0.037 | 0.85        | 0.95 | -     |
| b      | 0.0075    | 0.012 | 0.19        | 0.30 | 9     |
| c      | 0.0035    | 0.008 | 0.09        | 0.20 | -     |
| D      | 0.193     | 0.201 | 4.90        | 5.10 | 3     |
| E1     | 0.169     | 0.177 | 4.30        | 4.50 | 4     |
| e      | 0.026 BSC |       | 0.65 BSC    |      | -     |
| E      | 0.246     | 0.256 | 6.25        | 6.50 | -     |
| L      | 0.020     | 0.028 | 0.50        | 0.70 | 6     |
| N      | 16        |       | 16          |      | 7     |
| alpha  | 0°        | 8°    | 0°          | 8°   | -     |

Rev. 1 2/02

**NOTES:**

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

© Copyright Intersil Americas LLC 2007-2009. All Rights Reserved.  
 All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Multiplexer Switch ICs](#) category:*

*Click to view products by [Renesas](#) manufacturer:*

Other Similar products are found below :

[NLV74HC4066ADR2G](#) [HEF4051BP](#) [MC74HC4067ADTG](#) [DG508AAK/883B](#) [NLV14051BDG](#) [016400E](#) [PI3V512QE](#) [7705201EC](#)  
[PI2SSD3212NCE](#) [NLAS3257CMX2TCG](#) [PI3DBS12412AZLEX](#) [PI3V512QEX](#) [PI3DBS16213ZLEX](#) [PI3DBS16415ZHEX](#)  
[MUX36S16IRSNR](#) [TC7W53FK,LF](#) [CD4053BM96](#) [MC74HC4053ADWR2G](#) [SN74LV4051APWR](#) [HEF4053BT.653](#) [PI3L720ZHEX](#)  
[ADG5408BRUZ-REEL7](#) [ADG1404YRUZ-REEL7](#) [ADG1208YRZ-REEL7](#) [MAX4704EUB+T](#) [ADG1406BRUZ-REEL7](#)  
[LTC4305IDHD#PBF](#) [CD4053BPWRG4](#) [74HC4053D.653](#) [74HCT4052PW.118](#) [74LVC2G53DP.125](#) [74HC4052DB.112](#) [74HC4052PW.112](#)  
[74HC4053DB.112](#) [74HC4067DB.112](#) [74HC4351DB.112](#) [74HCT4052D.112](#) [74HCT4052DB.112](#) [74HCT4053DB.112](#) [74HCT4067D.112](#)  
[74HCT4351D.112](#) [74LV4051PW.112](#) [FSA1256L8X\\_F113](#) [PI5V330QE](#) [PI5V331QE](#) [5962-8771601EA](#) [5962-87716022A](#) [ADG5249FBRUZ](#)  
[ADG1438BRUZ](#) [AD7506JNZ](#)