ISL85403

2.5A Regulator with Integrated High-side MOSFET for Synchronous Buck or Boost Buck Converter

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The ISL85403 is a 40V, 2.5A synchronous buck or boost buck controller with an integrated high-side MOSFET and low-side driver. In Buck mode, the ISL85403 supports a wide input range of 3V to 40V. In Boost-Buck mode, the input range can be extended down to 2.5V and output regulation can be maintained when V_{IN} drops below V_{OUT}, enabling sensitive electronics to remain on in low input voltage conditions.

The ISL85403 has a flexible selection of Forced PWM mode and PFM mode. In PFM mode, the quiescent input current is as low as 180µA (AUXVCC connected to V_{OUT}). The load boundary between PFM and PWM can be programmed to cover wide applications.

The low-side driver can either be used to drive an external low-side MOSFET for a synchronous buck or left unused for a standard non-synchronous buck. The low-side driver can also be used to drive a boost converter as a preregulator followed by a buck controlled by the same IC, which greatly expands the operating input voltage range down to 2.5V or lower (See Figure 5).

ISL85403 offers robust current protection. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback under current limit condition; also, the hiccup overcurrent mode ensures reliable operations under harsh short conditions.

The ISL85403 has comprehensive protections against various faults including overvoltage and over-temperature protections.

Related Literature

For a full list of related documents, visit our website:

- ISL85403 device page

Features

- Buck mode: input voltage range 3V to 40V (See "Input Voltage" for more details)
- Boost mode expands operating input voltage lower than 2.5V (See "Input Voltage" for more details)
- Selectable Forced PWM mode or PFM mode
- 300µA IC quiescent current (PFM, no load); 180µA input quiescent current (PFM, no load, V_{OUT} tied to AUXVCC)
- Less than 5µA (MAX) shutdown input current (IC disabled)
- Operational topologies
  - Synchronous buck
  - Non-synchronous buck
  - Two-stage boost buck
  - Non-inverting single inductor buck boost
- Programmable frequency from 200kHz to 2.2MHz and frequency synchronization capability
- ±1% tight voltage regulation accuracy
- Reliable overcurrent protection
  - Temperature compensated current sense
  - Cycle-by-cycle current limiting with frequency foldback
  - Hiccup mode for worst case short condition
- 20 Ld 4x4 QFN package
- Pb-free (RoHS compliant)

Applications

- General purpose
- 24V bus power
- Battery power
- Point-of-load
- Embedded processor and I/O supplies

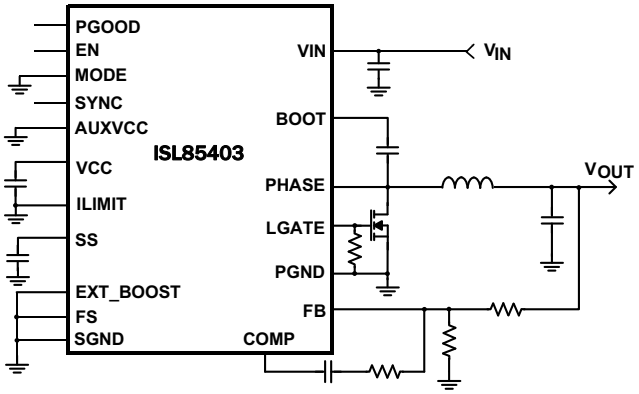

FIGURE 1. TYPICAL APPLICATION

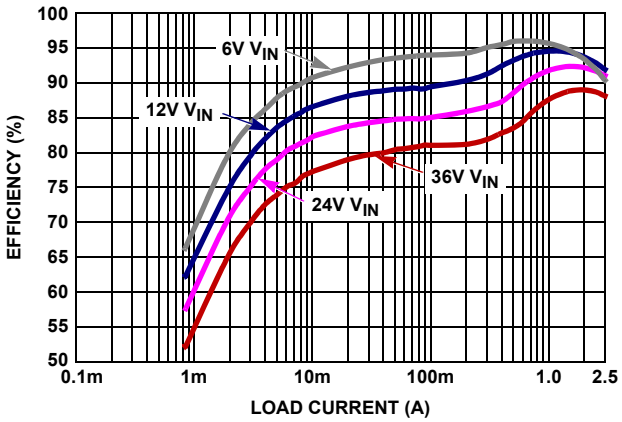

FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 5V, T_A = +25°C

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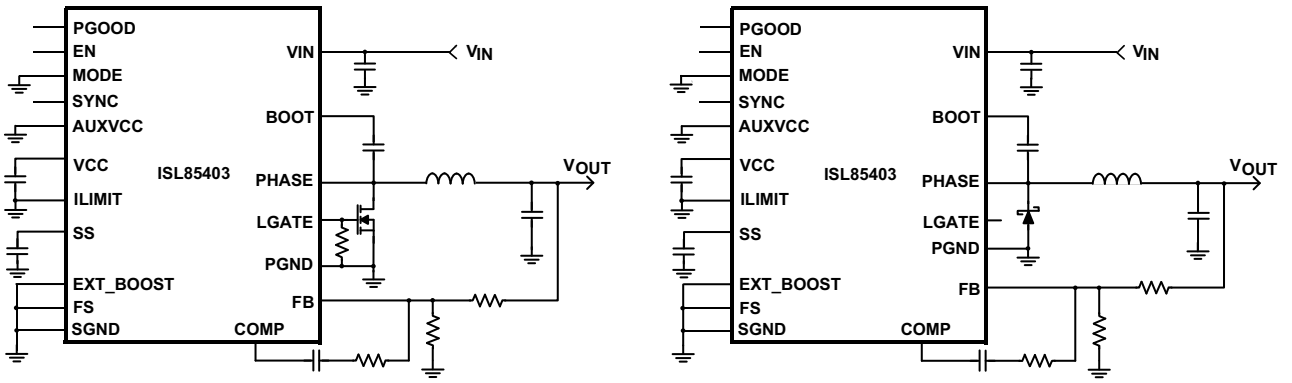
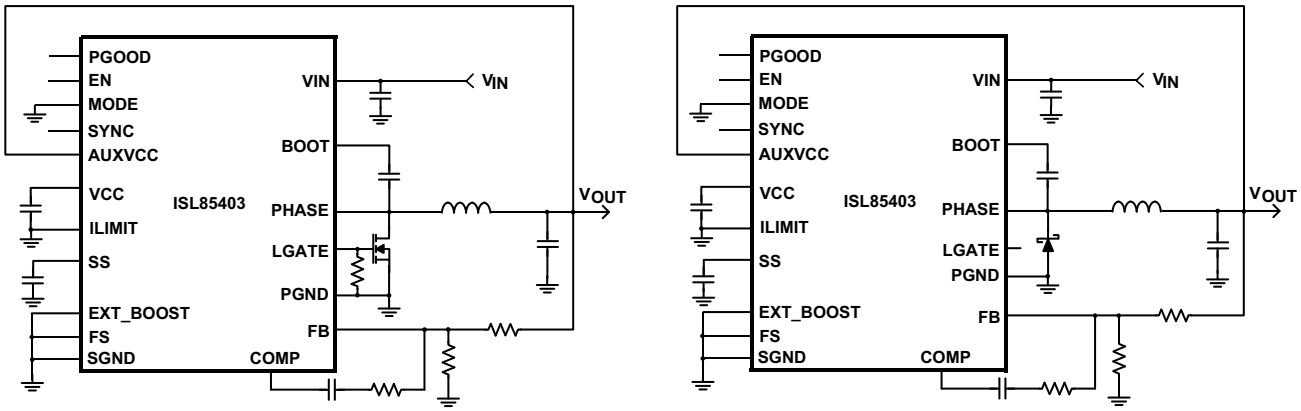
Typical Application Schematics



(a) SYNCHRONOUS BUCK

(b) NON-SYNCHRONOUS BUCK

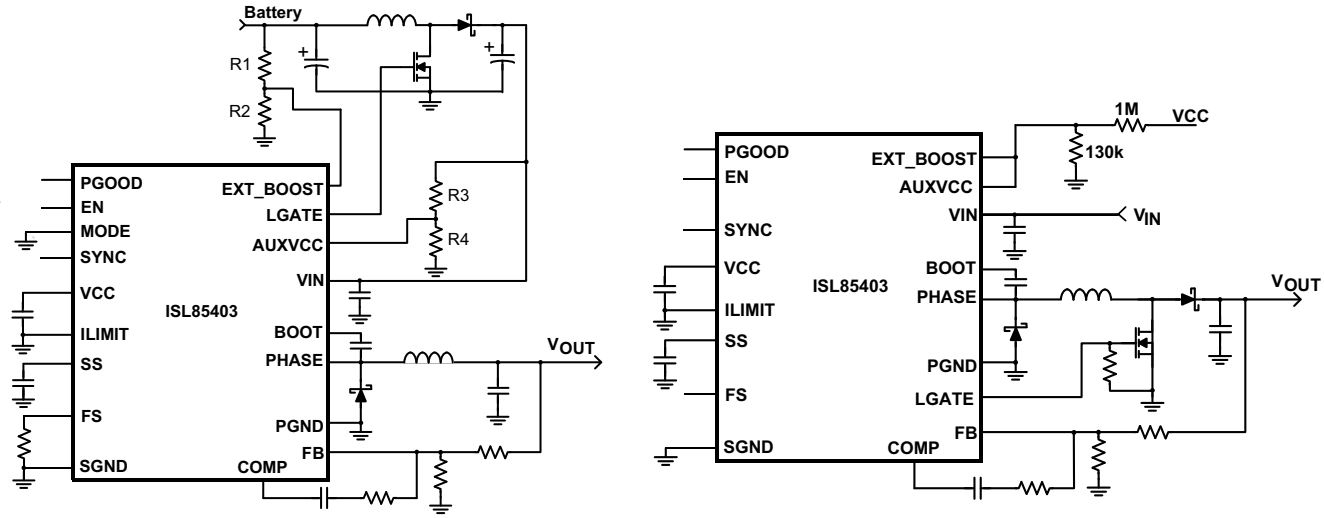
FIGURE 3. TYPICAL APPLICATION SCHEMATIC I



(a) SYNCHRONOUS BUCK

(b) NON-SYNCHRONOUS BUCK

FIGURE 4. TYPICAL APPLICATION SCHEMATIC II - VCC SWITCHOVER TO V_{OUT}



(a) 2-STAGE BOOST BUCK

(b) NON-INVERTING SINGLE INDUCTOR BUCK BOOST

FIGURE 5. TYPICAL APPLICATION SCHEMATIC III - BOOST BUCK CONVERTER

Block Diagram

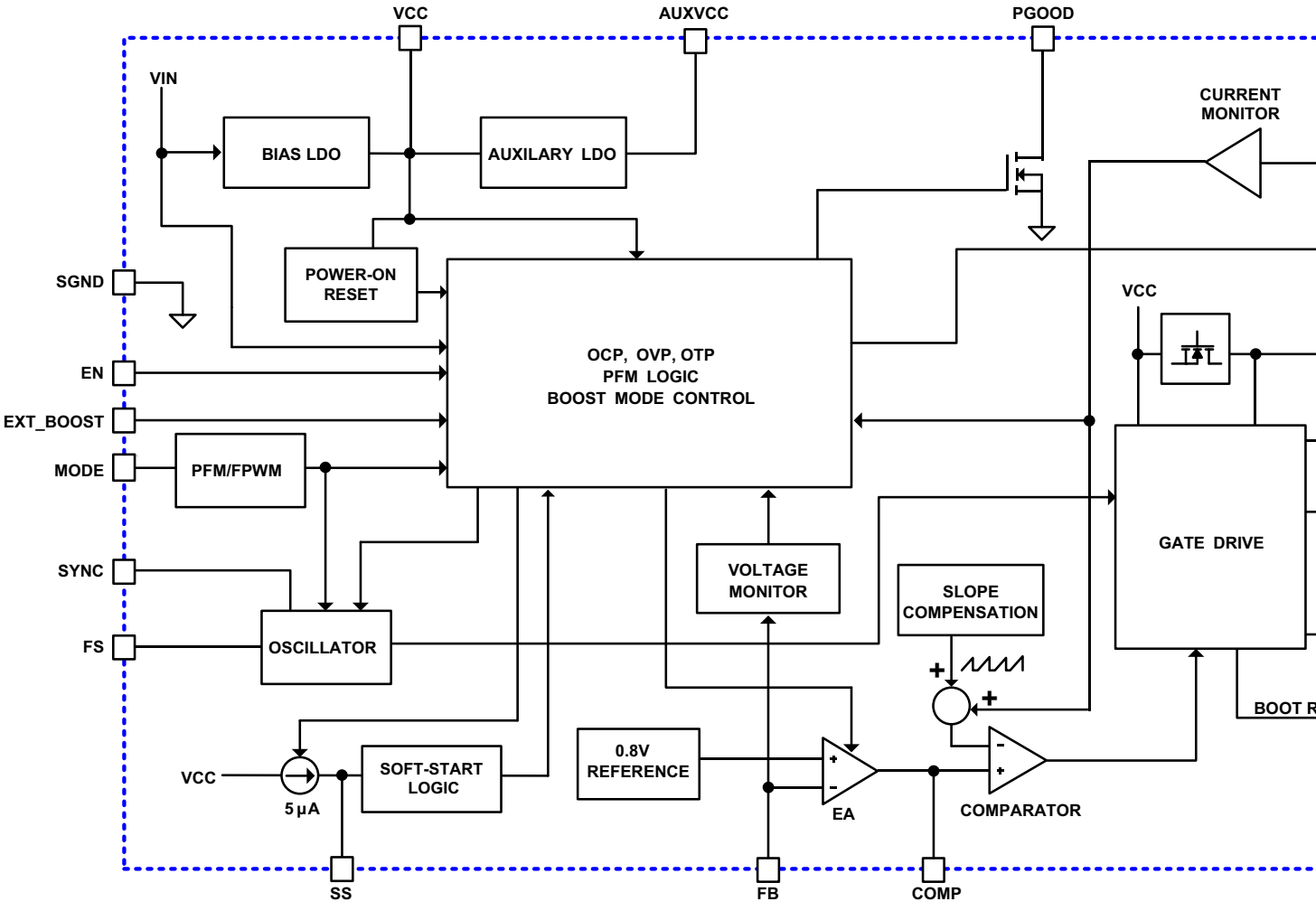


FIGURE 6. BLOCK DIAGRAM

Ordering Information

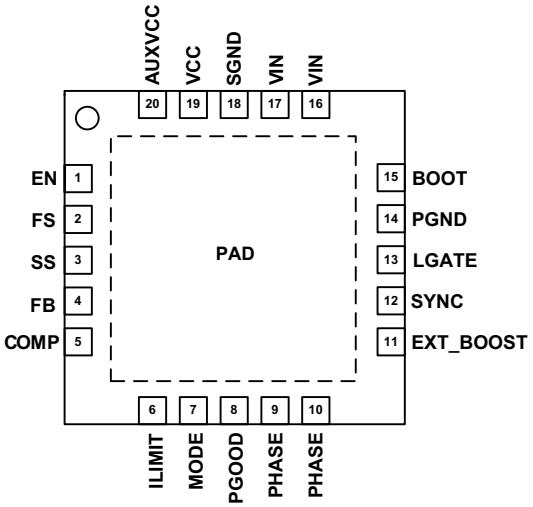
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	Tape and Reel (Units) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL85403FRZ	85 403FRZ	-40 to +105	-	20 Ld 4x4 QFN	L20.4x4C
ISL85403FRZ-T	85 403FRZ	-40 to +105	6k	20 Ld 4x4 QFN	L20.4x4C
ISL85403FRZ-T7A	85 403FRZ	-40 to +105	250	20 Ld 4x4 QFN	L20.4x4C
ISL85403FRZ-TK	85 403FRZ	-40 to +105	1k	20 Ld 4x4 QFN	L20.4x4C
ISL85403DEMO1Z	Compact size demo board for SYNC buck				
ISL85403EVAL1Z	Evaluation Board				
ISL85403EVAL2Z	Evaluation Board for non-inverting buck-boost configuration				

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL85403 device page. For more information about MSL see TB363.

Pin Configuration

20 LD QFN
TOP VIEW



Functional Pin Descriptions

PIN NAME	PIN #	DESCRIPTION
EN	1	Enable the IC by leaving the EN pin floating or pulling it HIGH. Disable the IC by pulling this pin LOW. Range: 0V to 5.5V.
FS	2	Force the IC to have a 500kHz switching frequency by connecting the FS pin to VCC or GND, or by leaving the FS pin open. Program the oscillator switching frequency by adjusting the resistor from this pin to GND.
SS	3	Connect a capacitor from this pin to ground. The capacitor, along with an internal 5µA current source, sets the converter's soft-start interval. Also, this pin can be used to track a ramp on this pin.
FB	4	The inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from V_{OUT} to FB, the output voltage can be set to any voltage between the power rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Connect an R-C network across COMP and FB for loop compensation. The FB pin is also monitored for overvoltage events.
COMP	5	Output of the voltage feedback error amplifier.

Functional Pin Descriptions (Continued)

PIN NAME	PIN #	DESCRIPTION
ILIMIT	6	Programmable current limit pin. With this pin connected to the VCC pin, or to GND, or left open, the current limiting threshold is set to default of 3.6A; the current limiting threshold can be programmed with a resistor from this pin to GND.
MODE	7	Mode selection pin. Pull this pin to GND for Forced PWM mode; leave it floating or connected to VCC to enable PFM mode when the peak inductor current is below the default threshold of 700mA. The current boundary threshold between PFM and PWM can also be programmed with a resistor at this pin to ground. See "PFM Mode Operation" for more details.
PGOOD	8	An open-drain output and pull-up pin with a resistor to VCC for proper function. PGOOD is pulled low when the output is out of regulation (OV or UV) or the EN pin is pulled low. PGOOD rising has a fixed 128 cycle delay.
PHASE	9, 10	The PHASE pins are the PHASE nodes that should be connected to the output inductor. These pins are connected to the source of the high-side N-channel MOSFET.
EXT_BOOST	11	Set Boost mode and monitors the battery voltage that is the input of the boost converter. After VCC POR, the controller detects the voltage on this pin; if the voltage on this pin is below 200mV, the controller is set in synchronous/non-synchronous Buck mode and latches in this state unless VCC is below POR falling threshold; if the voltage on this pin after VCC POR is above 200mV, the controller is set in Boost mode and latches in this state. In Boost mode, the low-side driver outputs PWM with the same duty cycle as the upper-side driver to drive the boost switch. In Boost mode, this pin is used to monitor input voltage through a resistor divider. By setting the resistor divider, the high threshold and hysteresis can be programmed. When voltage on this pin is above 0.8V, the PWM output (LGATE) for the boost converter is disabled. When voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled. In Boost mode operation, PFM is disabled when boost PWM is enabled. Check the "2-Stage Boost Buck Converter Operation" for more details.
SYNC	12	This pin can be used to synchronize two or more ISL85403 controllers. Multiple ISL85403s can be synchronized with their SYNC pins connected together. 180° phase shift is automatically generated between the master and slave ICs. The internal oscillator can also lock to an external frequency source applied on this pin with a square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). Range: 0V to 5.5V. Leave this pin floating if not used.
LGATE	13	In synchronous Buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. Add a 5.1k or smaller value resistor to connect LGATE to ground to avoid falsely turning on LGATE caused by coupling noise. When a diode is used as the bottom side power device in non-synchronous Buck mode, connect this pin to VCC through a resistor (less than 5k) before IC start-up to disable the low-side driver (LGATE). In Boost mode, this pin can drive the boost power MOSFET. The boost control PWM is the same with the buck control PWM.
PGND	14	The ground connection of the power flow, including the driver. Connect this pin to a large ground plane.
BOOT	15	Provides bias voltage to the high-side MOSFET driver. A bootstrap circuit creates a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside of the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended between BOOT and PHASE pin.
VIN	16, 17	Connected to the drain of the integrated high-side MOSFET as well as the source for the internal linear regulator that provides the bias of the IC. Connect the input rail to these VIN pins. Range: 3V to 40V. With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding the "Absolute Maximum Ratings".
SGND	18	Provides the return path for the control and monitor portions of the IC. Connect it to a quiet ground plane.
VCC	19	Output of the internal linear regulator that supplies the bias for the IC including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between VCC to ground.
AUXVCC	20	Input of the auxiliary internal linear regulator, which can be supplied by the regulator output after power-up. With such configuration, the power dissipation inside of the IC is reduced. The input range for this LDO is 4.5V to 20V. In Boost mode operation, this pin works as a boost output overvoltage detection pin. It detects the boost output through a resistor divider. When voltage on this pin is above 0.8V, the boost PWM is disabled; when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled. Range: 0V to 20V.
PAD	-	Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout it must be connected to a PCB ground copper plane with an area as large as possible to effectively reduce the thermal impedance.

Absolute Maximum Ratings

VIN, PHASE . . . . . GND - 0.3V to +44V
VCC . . . . . GND - 0.3V to +6.0V
AUXVCC . . . . . GND - 0.3V to +22V
Absolute Boot Voltage, V_{BOOT} . . . . . +50.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +6.0V
All Other Pins . . . . . GND - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2.5kV
Machine Model (Tested per JESD22-A115C) 250V
Charged Device Model (Tested per JESD22-C101E) 1kV
Latch-Up Rating (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN 4x4 Package (Notes 4, 5)	40	3.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free reflow profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage on V_{IN} . . . . . 3V to 40V
AUXVCC, Buck Mode . . . . . 4.5V to +20V
AUXVCC, Boost-Buck Mode . . . . . 0V to +20V
Ambient Temperature Range . . . . . -40°C to +105°C
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

See Figure 6 and the "Typical Application Schematics" on page 3. Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V ±10%, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
VIN PIN SUPPLY						
VIN Pin Voltage Range		VIN pin	**3.05**		**40**	V
		VIN pin connected to VCC	**3.05**		**5.5**	V
Operating Supply Current	I_Q	MODE = VCC/FLOATING (PFM), no load at the output		300		µA
		MODE = GND (forced PWM), V_{IN} = 12V, IC operating, not including driving current		1.3		mA
Shutdown Supply Current	I_{IN_SD}	EN connected to GND, V_{IN} = 12V		2.8	**4.5**	µA
INTERNAL MAIN LINEAR REGULATOR						
MAIN LDO V_{CC} Voltage	V_{CC}	V_{IN} > 5V	**4.2**	4.5	**4.8**	V
MAIN LDO Dropout Voltage	$V_{DROPOUT\_MAIN}$	V_{IN} = 4.2V, I_{VCC} = 35mA		0.3	**0.52**	V
		V_{IN} = 3V, I_{VCC} = 25mA		0.25	**0.42**	V
V_{CC} Current Limit of MAIN LDO				60		mA
INTERNAL AUXILIARY LINEAR REGULATOR						
AUXVCC Input Voltage Range	V_{AUXVCC}		**4.5**		**20**	V
AUX LDO V_{CC} Voltage	V_{CC}	V_{AUXVCC} > 5V	**4.2**	4.5	**4.8**	V
LDO Dropout Voltage	$V_{DROPOUT\_AUX}$	V_{AUXVCC} = 4.2V, I_{VCC} = 35mA		0.3	**0.52**	V
		V_{AUXVCC} = 3V, I_{VCC} = 25mA		0.25	**0.42**	V
Current Limit of AUX LDO				60		mA
AUX LDO Switchover Rising Threshold	V_{AUXVCC_RISE}	AUXVCC voltage rise; switch to auxiliary LDO	**2.97**	3.1	**3.2**	V
AUX LDO Switchover Falling Threshold Voltage	V_{AUXVCC_FALL}	AUXVCC voltage fall; switch back to main BIAS LDO	**2.73**	2.87	**2.97**	V
AUX LDO Switchover Hysteresis	V_{AUXVCC_HYS}	AUXVCC switchover hysteresis		0.2		V

Electrical Specifications See Figure 6 and the "Typical Application Schematics" on page 3. Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V ±10%, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
POWER-ON RESET						
Rising V_{CC} POR Threshold	V_{PORH_RISE}		**2.82**	2.9	**3.05**	V
Falling V_{CC} POR Threshold	V_{PORL_FALL}			2.6	**2.8**	V
V_{CC} POR Hysteresis	V_{PORL_HYS}			0.3		V
ENABLE						
Enable On Voltage	V_{ENH}		**1.7**			V
Enable Off voltage	V_{ENL}				**1**	V
EN Pull-Up Current	I_{EN_PULLUP}	V_{EN} = 1.2V, V_{IN} = 24V		1.5		µA
		V_{EN} = 1.2V, V_{IN} = 12V		1.2		µA
		V_{EN} = 1.2V, V_{IN} = 5V		0.9		µA
OSCILLATOR						
PWM Frequency	F_{OSC}	R_T = 665kΩ	**160**	200	**240**	kHz
		R_T = 51.1kΩ	**1870**	2200	**2530**	kHz
		FS pin connected to VCC or floating or GND	**450**	500	**550**	kHz
MIN ON-Time	t_{MIN_ON}			130	**225**	ns
MIN OFF-Time	t_{MIN_OFF}			210	**330**	ns
SYNCHRONIZATION						
Input High Threshold	VIH			2		V
Input Low Threshold	VIL			0.5		V
Input Minimum Pulse Width				25		ns
Input Impedance				100		kΩ
Input Minimum Frequency Divided by Free Running Frequency				1.1		
Input Maximum Frequency Divided by Free Running Frequency				1.6		
Output Pulse Width		C_{SYNC} = 100pF		100		ns
Output Pulse High	VOH	R_{LOAD} = 1kΩ		VCC-0.25		V
Output Pulse Low	VOL			GND		V
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.8		V
System Accuracy			**-1.0**		**+1.0**	%
FB Pin Source Current				5		nA
Soft-Start						
Soft-Start Current	I_{SS}		**3**	5	**7**	µA
ERROR AMPLIFIER						
Unity Gain-Bandwidth		C_{LOAD} = 50pF		10		MHz
DC Gain		C_{LOAD} = 50pF		88		dB
Maximum Output Voltage				3.6		V
Minimum Output Voltage				0.5		V
Slew Rate	SR	C_{LOAD} = 50pF		5		V/µs

Electrical Specifications

See Figure 6 and the "Typical Application Schematics" on page 3. Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{CC} = 4.5V ±10%, T_A = -40°C to +105°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PFM MODE CONTROL						
Default PFM Current Threshold		MODE = VCC or floating		700		mA
INTERNAL HIGH-SIDE MOSFET						
Upper MOSFET $r_{DS(ON)}$	$r_{DS(ON)\_UP}$	Limits apply for +25°C only		127	140	mΩ
LOW-SIDE MOSFET GATE DRIVER						
LGate Source Resistance		100mA source current		3.5		Ω
LGATE Sink Resistance		100mA sink current		2.8		Ω
BOOST CONVERTER CONTROL						
EXT_BOOST Boost_Off Threshold Voltage			**0.74**	0.8	**0.86**	V
EXT_BOOST Hysteresis Sink Current	$I_{EXT\_BOOST\_HYS}$		**2.1**	3.2	**4.2**	µA
AUXVCC Boost Turn-Off Threshold Voltage			**0.74**	0.8	**0.86**	V
AUXVCC Hysteresis Sink Current	I_{AUXVCC_HYS}		**2.1**	3.2	**4.2**	µA
POWER-GOOD MONITOR						
Overvoltage Rising Trip Point	V_{FB}/V_{REF}	Percentage of reference point	**104**	110	**116**	%
Overvoltage Rising Hysteresis	V_{FB}/V_{OVTRIP}	Percentage below OV trip point		3		%
Undervoltage Falling Trip Point	V_{FB}/V_{REF}	Percentage of reference point	**84**	90	**96**	%
Undervoltage Falling Hysteresis	V_{FB}/V_{UVTRIP}	Percentage above UV trip point		3		%
PGOOD Rising Delay	$t_{PGOOD\_R\_DELAY}$			128		cycles
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 4.5V		10		nA
PGOOD Low Voltage	V_{PGOOD}	PGOOD LOW, IPGOOD = 0.2mA		0.10		V
OVERCURRENT PROTECTION						
Default Cycle-by-Cycle Current Limit Threshold	I_{OC_1}	I_{LIMIT} = GND or VCC or floating	**3**	3.6	**4.2**	A
Hiccup Current Limit Threshold	I_{OC_2}	Hiccup, I_{OC_2}/I_{OC_1}		115		%
OVERVOLTAGE PROTECTION						
OV 120% Trip Point		Active in and after soft-start. Percentage of reference point LG = UG = LOW		120		%
OV 120% Release Point		Active in and after soft-start. Percentage of reference point		102.5		%
OV 110% Trip Point		Active after soft-start done. Percentage of reference point LG = UG = LOW		110		%
OV 110% Release Point		Active after soft-start done. Percentage of reference point		102.5		%
OVER-TEMPERATURE PROTECTION						
Over-Temperature Trip Point				160		°C
Over-Temperature Recovery Threshold				140		°C

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

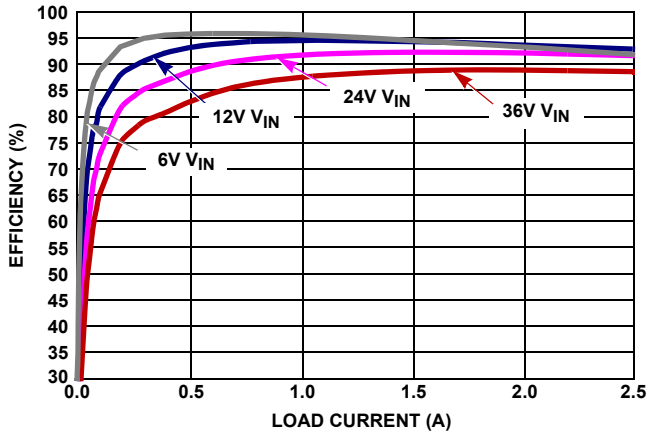


FIGURE 7. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, V_{OUT} 5V, T_A = +25°C

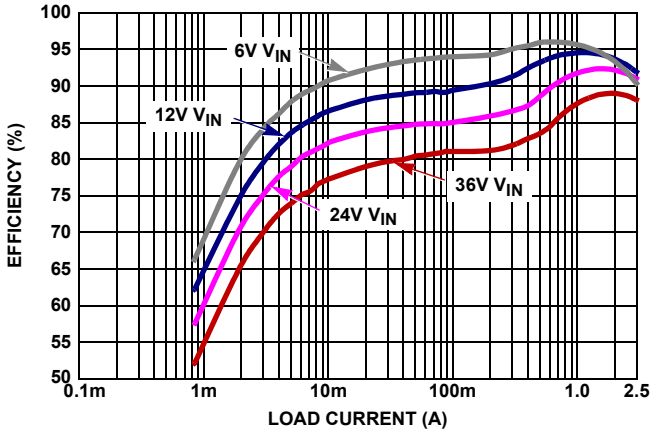


FIGURE 8. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 5V, T_A = +25°C

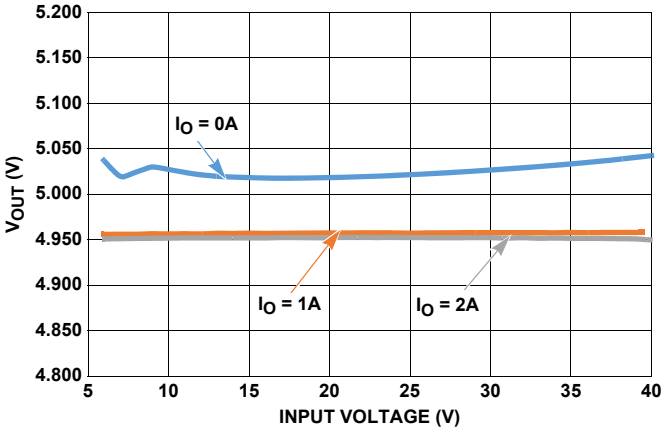


FIGURE 9. LINE REGULATION, V_{OUT} 5V, T_A = +25°C

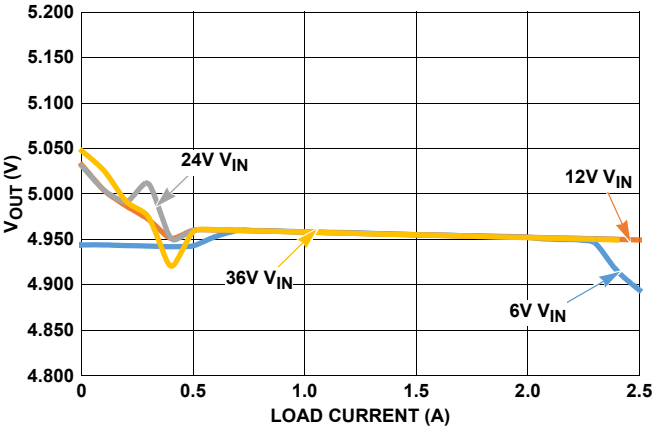


FIGURE 10. LOAD REGULATION, V_{OUT} 5V, T_A = +25°C

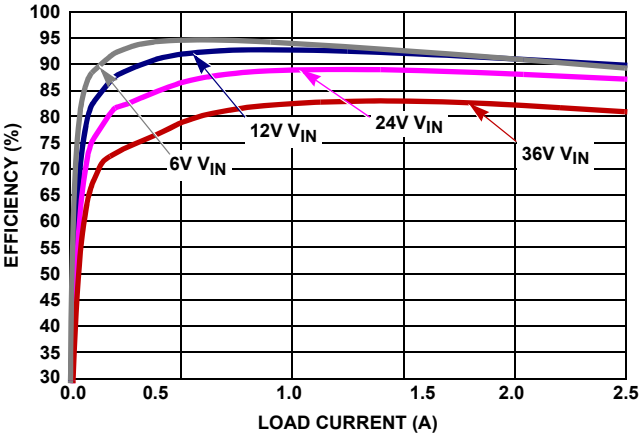


FIGURE 11. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, V_{OUT} 3.3V, T_A = +25°C

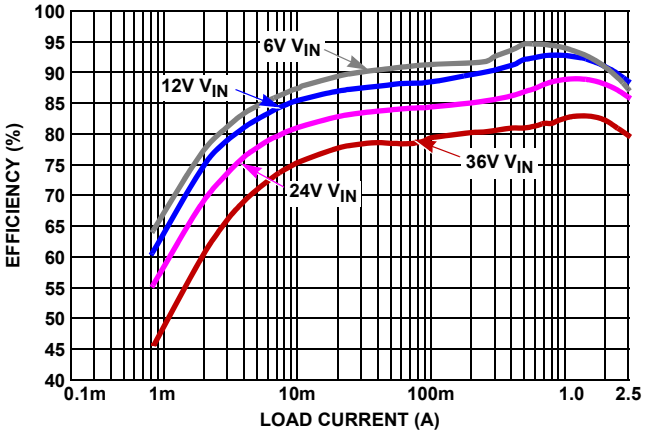


FIGURE 12. EFFICIENCY, SYNCHRONOUS BUCK, PFM MODE, V_{OUT} 3.3V, T_A = +25°C

Typical Performance Curves (Continued)

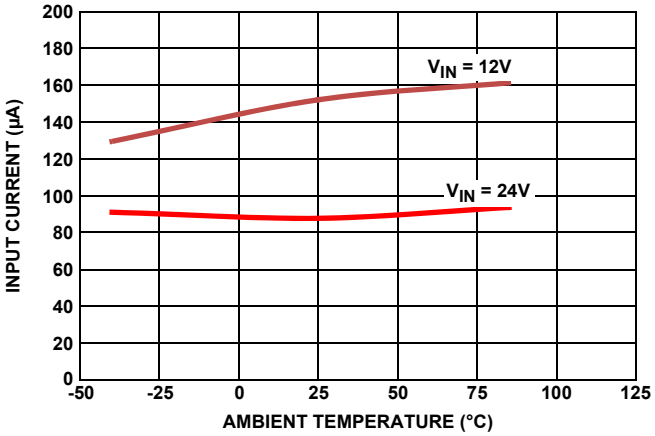


FIGURE 13. INPUT QUIESCENT CURRENT UNDER NO LOAD, PFM MODE, V_{OUT} = 5V

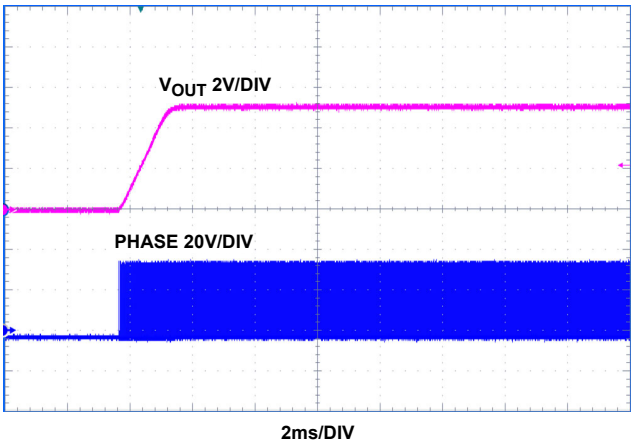


FIGURE 14. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE ON

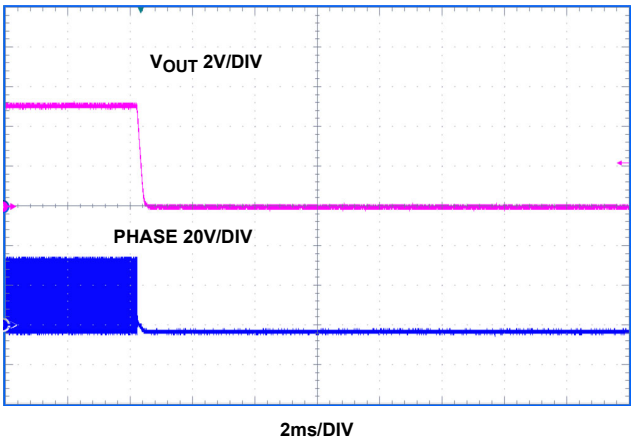


FIGURE 15. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE OFF

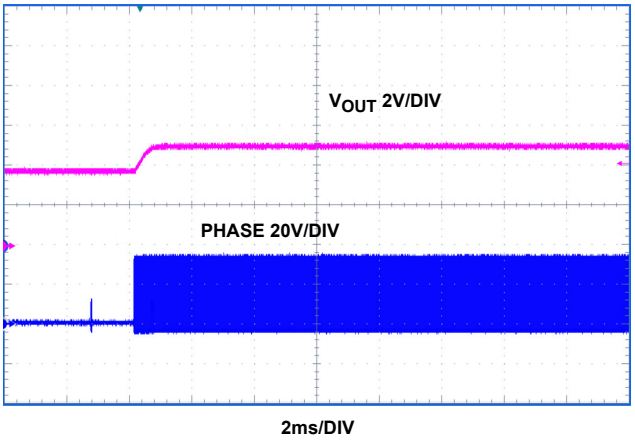


FIGURE 16. V_{IN} 36V, PREBIASED START-UP

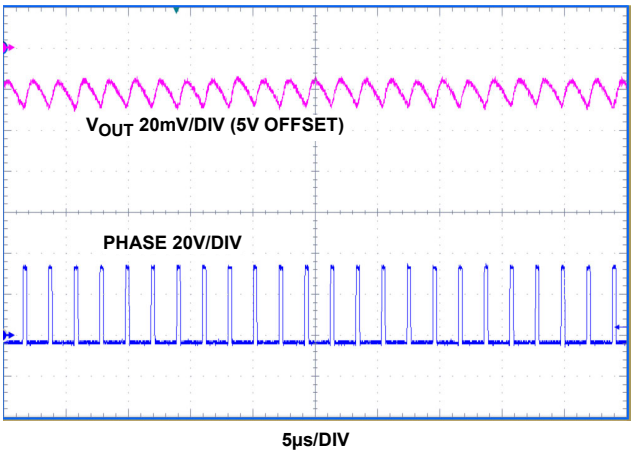


FIGURE 17. SYNCHRONOUS BUCK WITH FORCE PWM MODE, V_{IN} 36V, I_O 2A

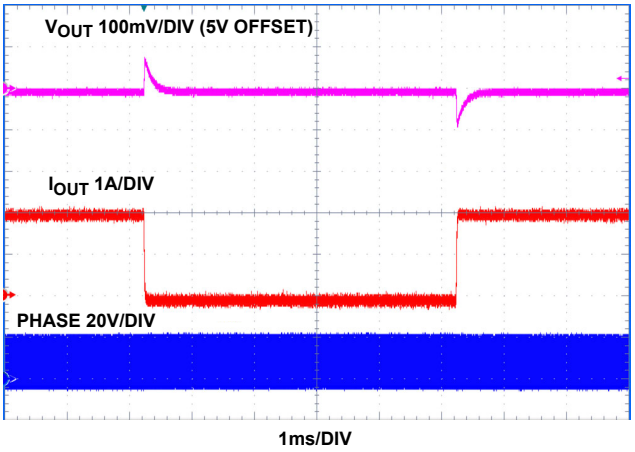


FIGURE 18. V_{IN} 24V, 0 TO 2A STEP LOAD, FORCE PWM MODE

Typical Performance Curves (Continued)

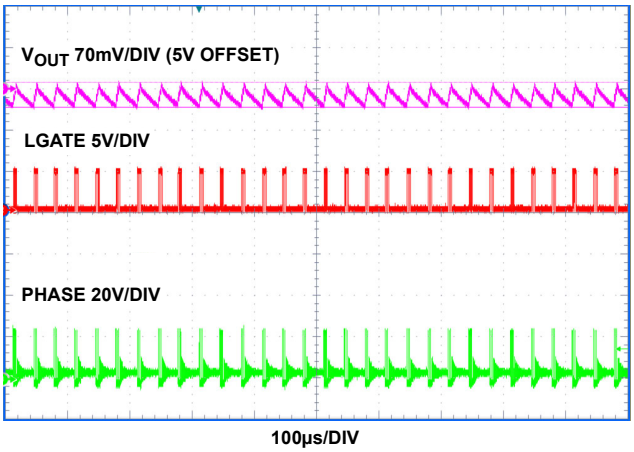


FIGURE 19. V_{IN} 24V, 80mA LOAD, PFM MODE

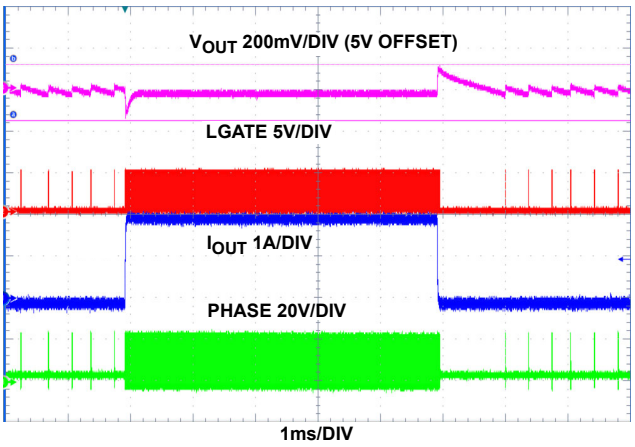


FIGURE 20. V_{IN} 24V, 0 TO 2A STEP LOAD, PFM MODE

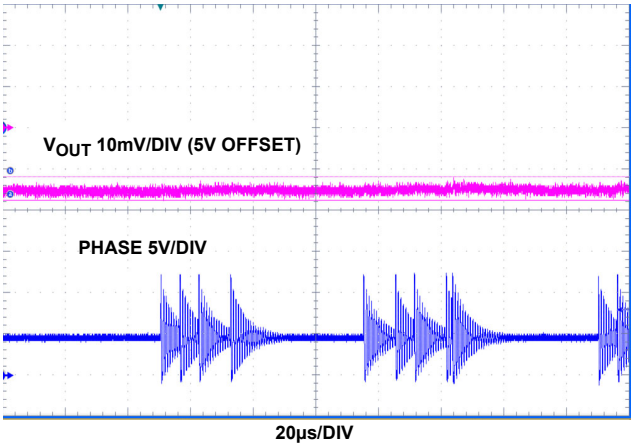


FIGURE 21. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, NO LOAD

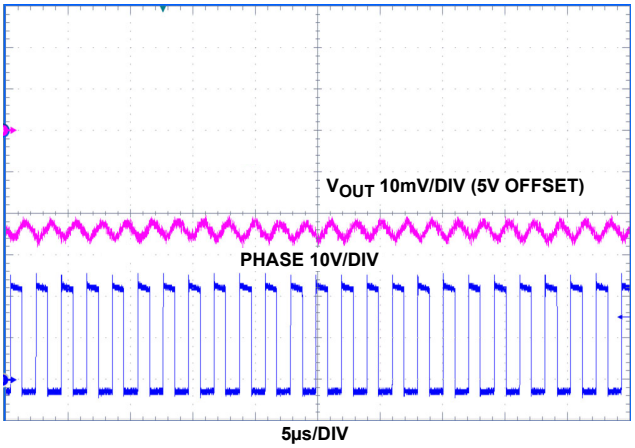


FIGURE 22. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, 2A

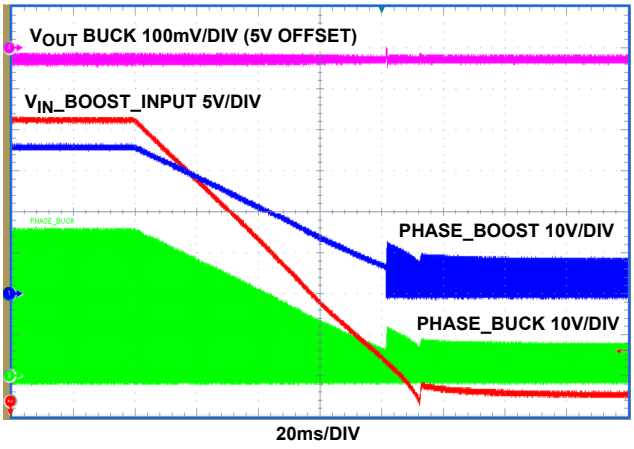


FIGURE 23. BOOST BUCK MODE, BOOST INPUT STEP FROM 36V TO 3V, V_{OUT} BUCK = 5V, I_{OUT_BUCK} = 1A

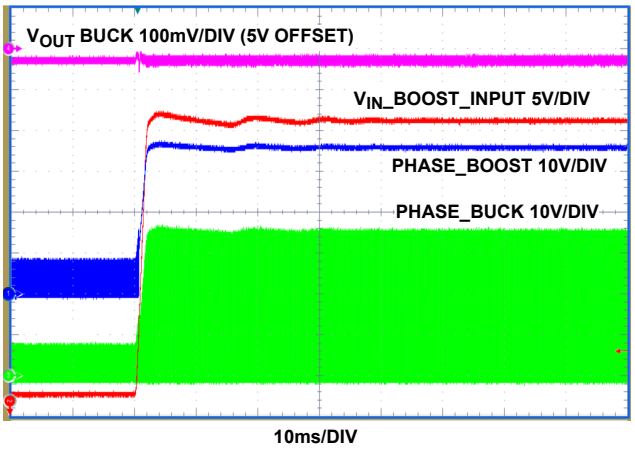


FIGURE 24. BOOST BUCK MODE, BOOST INPUT STEP FROM 3V TO 36V, V_{OUT} BUCK = 5V, I_{OUT_BUCK} = 1A

Typical Performance Curves (Continued)

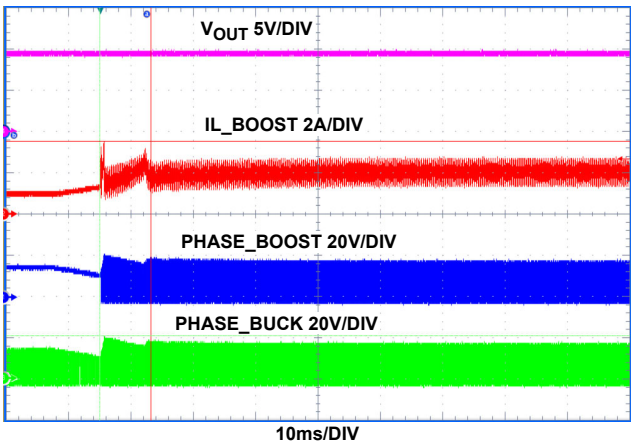


FIGURE 25. BOOST BUCK MODE, V_O = 9V, I_O = 1.8A, BOOST INPUT DROPS FROM 16V TO 9V DC

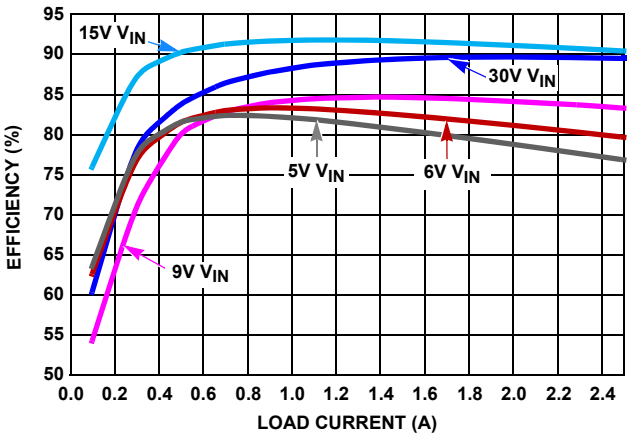


FIGURE 26. EFFICIENCY, BOOST BUCK, 500kHz, V_{OUT} 12V, T_A = +25°C

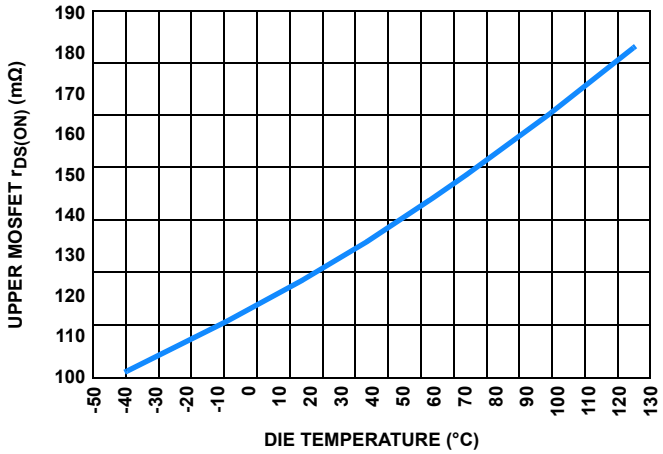


FIGURE 27. UPPER MOSFET $r_{DS(ON)}$ (mΩ) OVER-TEMPERATURE

Functional Description

Initialization

Initially the ISL85403 continually monitors the voltage at the EN pin. When the voltage on the EN pin exceeds its rising ON threshold, the internal LDO starts up to build up VCC. Soft-starts initiates after Power-on Reset (POR) circuits detect that VCC voltage has exceeded the POR threshold.

Soft-Start

The soft-start (SS) ramp is built up in the external capacitor on the SS pin, which is charged by an internal 5µA current source.

The SS ramp starts from 0V to a voltage above 0.8V. When SS reaches 0.8V, the bandgap reference takes over and the IC begins steady state operation. The soft-start time refers to the duration that the SS pin ramps from 0V to 0.8V while the output voltage ramps up with the same rate from 0V to the target regulated voltage. The required capacitance at the SS pin can be calculated from Equation 1.

$$C_{SS}[\mu F] = 6.5 \times t_{SS}[S] \quad \text{(EQ. 1)}$$

The SS plays a vital role in Hiccup mode. The IC applies cycle-by-cycle peak current limiting at over load conditions. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. During the dummy SS cycle, the current to charge soft-start capacitor is reduced to 1/5 of its normal value. Thus, a dummy SS cycle takes five times as long as the regular SS cycle. During the dummy SS period, the control loop is disabled and there is no PWM output. At the end of this cycle, it starts the normal SS. Hiccup mode persists until the second overcurrent threshold is no longer reached.

The ISL85403 is capable of starting up with prebiased output.

PWM Control

Pull the MODE pin to GND directly or with a resistor no greater than 10kΩ to set the IC in Forced PWM mode. The ISL85403 employs the Peak Current mode PWM control for fast transient response and cycle-by-cycle current limiting. See Figure 6 on page 4.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is triggered to shut down the PWM logic to turn off the high-side MOSFET. The high-side MOSFET stays off until the next clock signal comes for the next cycle.

The output voltage is sensed by a resistor divider from V_{OUT} to the FB pin. The difference between the FB voltage and the 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shut down the PWM.

PFM Mode Operation

Pull the MODE pin HIGH (>2.5V) or leave the MODE pin floating to set the IC to have PFM (Pulse Frequency Modulation) operation in light load. In PFM mode, the switching frequency is dramatically reduced to minimize the switching loss. The ISL85403 enters PFM mode when the MOSFET peak current is lower than the PWM/PFM boundary current threshold. The default threshold is 700mA when there is no programming resistor at the MODE pin.

The current threshold for the PWM/PFM boundary can be programmed by connecting a resistor between the MODE pin and ground. The MODE pin resistor value can be calculated using Equation 2.

$$R_{MODE} = \frac{118500}{I_{PFM} + 0.2} \quad \text{(EQ. 2)}$$

where I_{PFM} is the required PWM/PFM boundary current threshold and R_{MODE} is the programming resistor. The usable resistor value range to program the PFM current threshold is 150kΩ to 200kΩ. Do not use R_{MODE} values outside this range.

For applications with output voltages higher than 5V and rated load currents below 1A, Renesas recommends non-synchronous operation by using a diode for the low-side device instead of a MOSFET. If the rated load current is higher than 1A, synchronous operation with a low-side MOSFET can be used but Forced PWM mode must be enabled by connecting the MODE pin to GND.

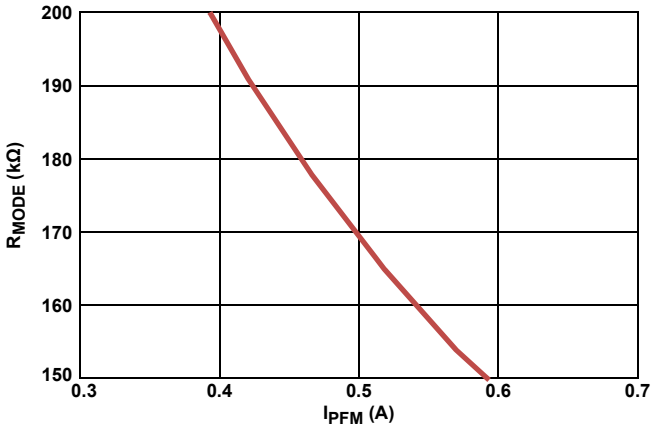


FIGURE 28. R_{MODE} vs I_{PFM}

Synchronous and Non-Synchronous Buck

The ISL85403 supports both Synchronous and Non-Synchronous buck operations.

In Synchronous buck configuration, add a 5.1k or smaller value resistor from the LGATE to ground to avoid false turn-on of the LGATE caused by coupling noise.

For a non-synchronous buck operation when a power diode is used as the low-side power device, the LGATE driver can be disabled with the LGATE connected to VCC (before IC start-up). For non-synchronous buck operation, the phase node shows oscillations after the high-side device turns off (as shown in Figure 21 on page 12 - blue trace). This is normal due to the oscillations among the parasitic capacitors at phase node and output inductor. An RC snubber (200Ω and 2.2nF as typical) at the phase node can reduce ringing.

AUXVCC Switchover

The ISL85403 has an auxiliary LDO integrated as shown in the Figure 6. It is used to replace the internal MAIN LDO function after the IC start-up. Figure 4 shows its basic application setup with output voltage connected to AUXVCC. After IC soft-start is done and the output voltage is built up to steady state, and when the AUXVCC pin voltage is over the AUX LDO Switchover Rising Threshold, the MAIN LDO is shut off and the AUXILIARY LDO is activated to bias VCC. Because the AUXVCC pin voltage is lower than the input voltage V_{IN}, the internal LDO dropout voltage and the consequent power loss are reduced. This feature brings substantial efficiency improvements in light load range, especially at high input voltage applications. Because both Vin LDO and AUX LDO are regulated at 4.5V, it is better to use the AUX LDO with input voltage at AUXVCC pin in the range between 4.5V to 20V.

When the voltage at AUXVCC falls below the AUX LDO Switchover Falling Threshold, the AUXILIARY LDO is shut off and the MAIN LDO is reactivated to bias VCC. At the OV/UV fault events, the IC also switches back over from AUXILIARY LDO to MAIN LDO.

The AUXVCC switchover function is offered in buck configuration. It is not offered in boost configuration when the AUXVCC pin is used to monitor the boost output voltage for OVP.

Input Voltage

With the part switching, the operating ISL85403 input voltage must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to the part switching while not exceeding the 44V, as stated in the "Absolute Maximum Ratings" on page 7.

The lowest IC operating input voltage (VIN pin) depends on the VCC voltage and the Rising and Falling V_{CC} POR Threshold in Electrical Specifications table on page 8. At IC start-up when VCC is just over the rising POR threshold, there is no switching before soft-start. Therefore, the IC minimum start-up voltage on the VIN pin is 3.05V (MAX of Rising V_{CC} POR). When the soft-start is initiated, the regulator is switching and the dropout voltage across the internal LDO increases due to driving current. Thus, the IC VIN pin shutdown voltage is related to driving current and VCC POR falling threshold. The internal upper side MOSFET has a typical 10nC gate drive. For a typical example of synchronous buck with 4nC lower MOSFET gate drive and 500kHz switching frequency, the driving current is 7mA total, causing a 70mV drop across internal LDO under 3V V_{IN}. Then the IC shutdown voltage on the VIN pin is 2.87V (2.8V + 0.07V). In practical design, extra room should be taken into account with concern to voltage spikes at VIN.

In boost buck configuration, the input voltage range can be expanded further down to 2.5V or lower depending on the boost stage voltage drop upon maximum duty cycle. Because the boost output voltage is connected to the VIN pin as the buck inputs, after the IC starts up, the IC keeps operating and switching as long as the boost output voltage can keep the VCC voltage higher than the falling threshold. See "2-Stage Boost Buck Converter Operation" on page 16 for more details.

Output Voltage

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB. For a buck converter, the maximum achievable voltage is (V_{IN}*D_{MAX} - V_{DROP}), where V_{DROP} is the voltage drop in the power path including mainly the MOSFET $r_{DS(ON)}$ and inductor DCR. The maximum duty cycle D_{MAX} is ($1 - f_{SW} * t_{MIN(OFF)}$).

For applications with output voltages higher than 5V and rated load currents below 1A, Renesas recommends use non-synchronous operation by using a diode for the low-side device instead of a MOSFET. If the rated load current is higher than 1A, synchronous operation with a low-side MOSFET can be used but Forced PWM mode must be enabled by connecting the MODE pin to GND.

Output Current

With the high-side MOSFET integrated, the maximum output current the ISL85403 can support is decided by the package and many operating conditions including input voltage, output voltage, duty cycle, switching frequency and temperature the die temperature should not exceed +125°C with the power loss dissipated inside of the IC.

Note that more temperature rise is expected at higher ambient temperature due to more conduction loss caused by $r_{DS(ON)}$ increase.

The die temperature is equal to the sum of the ambient temperature and the temperature rise resulting from the power dissipated by the IC package with a certain junction to ambient thermal impedance θ_{JA}. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss, and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency, and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and θ_{JA} is greatly reduced. The θ_{JA} is highly related to layout and air flow conditions. In layout, multiple vias (≥9) are strongly recommended in the IC bottom pad. The bottom pad with its vias should be placed in the ground copper plane with an area as large as possible across multiple layers. The θ_{JA} can be reduced further with air flow. See Figures 12 and 13 for the thermal performance with 100 CFM air flow.

For applications with high output current and bad operating conditions (such as compact board size or high ambient temperature), synchronous buck is highly recommended because the external low-side MOSFET generates less heat than the external low-side power diode. This helps to reduce PCB temperature rise around the ISL85403 and reduce junction temperature rise.

2-Stage Boost Buck Converter Operation

The Figure 5 on page 3, shows the boost function circuits. Schematic (a) shows a boost working as a pre-stage to provide input to the following Buck stage. This is for applications when the input voltage could drop to a very low voltage in some constants (for example, in some battery powered systems), causing the output voltage to drop out of regulation. The boost converter can be enabled to boost the input voltage up to keep the output voltage in regulation. When system input voltage recovers back to normal, the boost stage is disabled while only the buck stage is switching.

The EXT_BOOST pin is used to set Boost mode and monitor the boost input voltage. At IC start-up before soft-start, the controller is latched in Boost mode when the voltage is at or above 200mV; it latches in synchronous Buck mode if the voltage on the EXT_BOOST pin is below 200mV. In Boost mode, the low-side driver output PWM has the same PWM signal as the buck regulator.

In Boost mode, the EXT_BOOST pin is used to monitor boost input voltage to turn on and turn off the boost PWM. The AUXVCC pin is used to monitor the boost output voltage to turn on and turn off the boost PWM.

Referring to Figure 29, a resistor divider from the boost input voltage to the EXT_BOOST pin is used to detect the boost input voltage. When the voltage on the EXT_BOOST pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start and the boost duty cycle increases linearly from $t_{MIN(ON)}$*Fs to ~50%. A 3µA sinking current is enabled at the EXT_BOOST pin for hysteresis purposes. When the voltage on the EXT_BOOST pin recovers to be above 0.8V, boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_{UP} (R_1 in Figure 29) for a required hysteresis V_{HYS} at the boost input voltage.

$$R_{UP}[M\Omega] = \frac{V_{HYS}}{3[\mu A]} \quad \text{(EQ. 3)}$$

Use Equation 4 to calculate the lower resistor R_{LOW} (R_2 in Figure 29) according to a required boost enable threshold.

$$R_{LOW} = \frac{R_{UP} \times 0.8}{VFTH - 0.8} \quad \text{(EQ. 4)}$$

where VFTH is the required falling threshold on boost input voltage to turn on the boost, 3µA is the hysteresis current, and 0.8V is the reference voltage to be compared with.

Note that the boost start-up threshold has to be selected in a way that the buck is operating correctly and kept in close loop regulation before boost start-up. Otherwise, a large inrush current at boost start-up can occur at boost input due to the buck open loop saturation. Set the boost start-up input voltage threshold high enough to cover the boost inductor and diode DC voltage drop, and the buck's maximum duty cycle and voltage conduction drop. This ensures the buck does not reach maximum duty cycle before boost start-up.

Similarly, a resistor divider from the boost output voltage to the AUXVCC pin is used to detect the boost output voltage. When the voltage on the AUXVCC pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start and a 3µA sinking current is enabled at AUXVCC pin for hysteresis purposes. When the voltage on the AUXVCC pin recovers to be above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor R_{UP} (R_3 in Figure 29) according to a required hysteresis V_{HY} at boost output voltage. Use Equation 4 to calculate the lower resistor R_{LOW} (R_4 in Figure 29) according to a required boost enable threshold at boost output.

Assuming V_{BAT} is the boost input voltage, V_{OUT_BST} is the boost output voltage and V_{OUT} is the buck output voltage, the steady state DC transfer function are:

$$V_{OUTBST} = \frac{1}{1-D} \times V_{BAT} \quad \text{(EQ. 5)}$$

$$V_{OUT} = D \cdot V_{OUTBST} = \frac{D}{1-D} \times V_{BAT} \quad \text{(EQ. 6)}$$

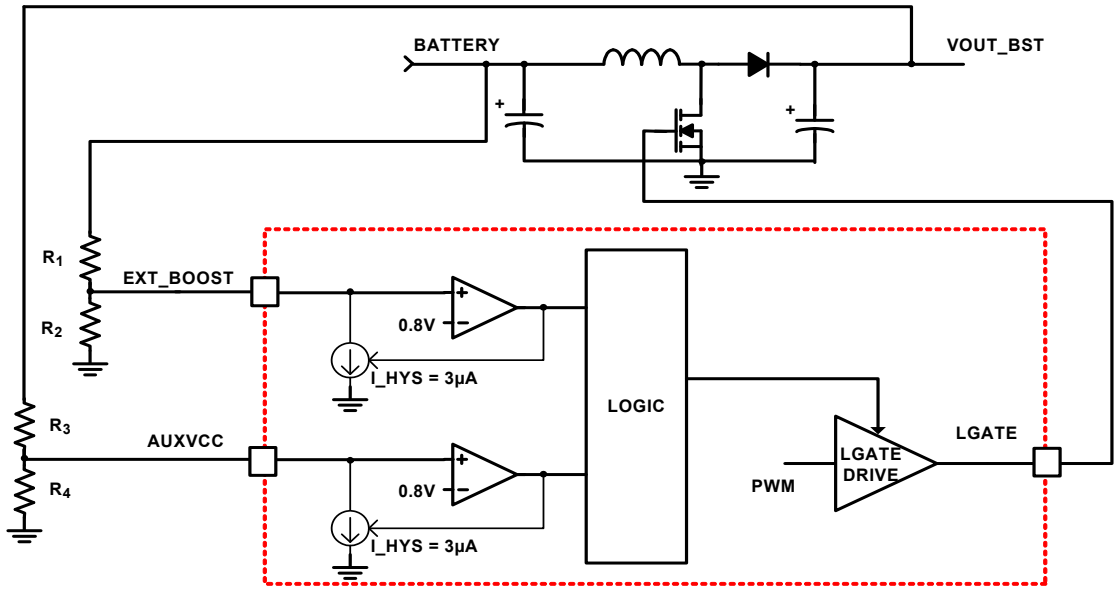


FIGURE 29. BOOST CONVERTER CONTROL

From Equations 5 and 6, Equation 7 can be derived to estimate the steady state boost output voltage asa function of V_{BAT} and V_{OUT}:

$$V_{OUTBST} = V_{BAT} + V_{OUT} \quad \text{(EQ. 7)}$$

After the IC starts up, the boost buck converters can keep working when the battery voltage drops extremely low because the IC's bias (VCC) LDO is powered by the boost output. For example, if a 3.3V output application battery drops to 2V and the VIN pin voltage is powered by the 5.2V boost output voltage (Equation 7), the VIN pin (buck input) still sees 5.2V to keep the IC working.

Note that in the previously mentioned case, the boost input current could be high because the input voltage is very low ($V_{IN}*I_{IN} = V_{OUT}*I_{OUT}$/Efficiency). For the design to achieve the low input operation with full load, the inductor and MOSFET have to be selected with enough current ratings to handle the high current appearing at boost input. The boost inductor current is the same with the boost input current, which can be estimated as Equation 8, where P_{OUT} is the output power, V_{BAT} is the boost input voltage, and EFF is the estimated efficiency of the whole boost and buck stages.

$$IL_{IN} = \frac{P_{OUT}}{V_{BAT} \times EFF} \quad \text{(EQ. 8)}$$

Based on the same concerns of boost input current, the start-up sequence must follow the rule that the IC is enabled after the boost input voltage rise above a certain level. The shutdown sequence must follow the rule that the IC is disabled first before the boost input power source is turned off. In Boost mode applications where there is no external control signal to enable/disable the IC, an external input UVLO circuit must be implemented for the start-up and shutdown sequence.

Non-Inverting Single Inductor Buck Boost Converter Operation

In Figure 5 on page 3, schematic (b) shows a non-inverting single inductor buck boost configuration. The recommended setting is to use 1MΩ and 130kΩ resistor dividers (as shown in TYP Schematic III b) connecting from VCC to both the EXT_BOOST and AUXVCC pins (the EXT_BOOST and AUXVCC pins are directly connected). In this way, the EXT_BOOST pin voltage is a fixed voltage of 0.52V that is higher than the Boost mode detection threshold of 0.2V to set the IC in Boost mode and lower than the boost switching threshold of 800mV to have boost being constantly switching (during and after soft-start).

Similar to 2-stage boost Buck mode, LGATE switches ON the same phase that the upper FETs switch ON, meaning both upper and lower side FETs are ON and OFF at the same time with the same duty cycle. When both FETs are ON, input voltage charges the inductor current ramping up for duration of DT; when both FETs are OFF, the inductor current is free wheeling through the two power diodes to output and output voltage discharge the inductor current ramping down for (1-D)T (in CCM mode). The steady state DC transfer function is:

$$V_{OUT} = \frac{D}{1-D} \times V_{IN} \quad \text{(EQ. 9)}$$

where V_{IN} is the input voltage, V_{OUT} is the buck boost output voltage, and D is duty cycle.

Use Equation 10 to calculate the inductor DC current as below:

$$IL_{DC} = \frac{1}{1-D} \times I_{OUT} \quad \text{(EQ. 10)}$$

where IL_{DC} is the inductor DC current and I_{OUT} is the output DC current.

Equation 10 shows the inductor current is charging output only during (1-D)T, which means inductor current has larger DC current than output load current. Thus, for this IC with high-side FET integrated, the non-inverting buck boost configuration has less load current capability compared with buck and 2-stage boost buck configurations. Its load current capability depends mainly on the duty cycle and inductor current.

Inductor ripple current can be calculated using Equation 11:

$$IL_{RIPPLE} = \frac{V_{OUT}(1-D)T}{L} \quad \text{(EQ. 11)}$$

The inductor peak current is:

$$IL_{PEAK} = IL_{DC} + \frac{1}{2} \times IL_{RIPPLE} \quad \text{(EQ. 12)}$$

In power stage DC calculations, use Equation 9 to calculate D, then use Equation 10 to calculate IL_{DC}. D and IL_{DC} are useful for estimating the high-side FET's power losses and checking if the part can meet the load current requirements.

Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the FS pin connected to VCC or ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from the FS pin to GND.

$$R_{FS}[k\Omega] = \frac{145000 - 16 \times f_{SW}[kHz]}{f_{SW}[kHz]} \quad \text{(EQ. 13)}$$

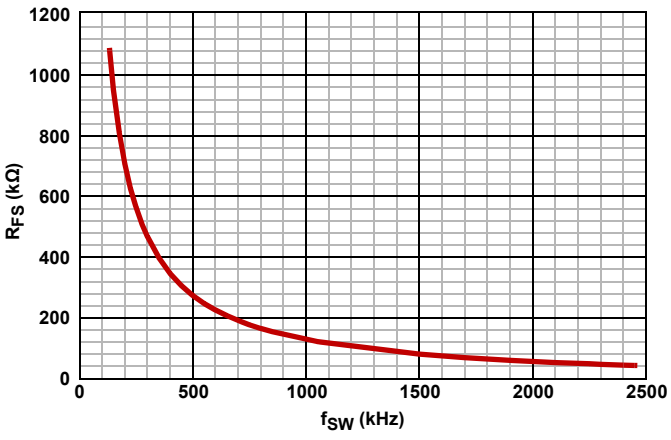


FIGURE 30. R_{FS} vs FREQUENCY

The SYNC pin is bidirectional and it outputs the IC's default or programmed local clock signal when it is free running. The IC locks to an external clock injected to the SYNC pin (external clock frequency is recommended to be 10% higher than the free running frequency). The delay from the rising edge of the external clock signal to the PHASE rising edge is half of the free running switching period pulse 220ns, ($0.5t_{SW}$+220ns). The maximum

external clock frequency is recommended to be 1.6 times of the free running frequency.

When the part enters PFM pulse skipping mode, the synchronization function is shut off and no clock signal is output in SYNC pin.

With the SYNC pins connected together, multiple ISL85403s can be synchronized. The slave ICs automatically have 180° phase shift with respect to the master IC.

PGOOD

The PGOOD pin is the output of an open-drain transistor (See Figure 6 on page 4). An external resistor is required to be pulled up to VCC for proper PGOOD function. At start-up, PGOOD is turned HIGH (internal PGOOD open-drain transistor is turned off) with 128 cycles delay after soft-start is finished (soft-start ramp reaches 1.02V) and the FB voltage is within the OV/UV window (90%REF < FB < 110%REF).

At normal operation, PGOOD is pulled low with one cycle (minimum) and six cycles (maximum) delay if any of the OV (110%) or UV (90%) comparators are tripped. PGOOD is released HIGH with 128 cycles delay after FB recovers to be within the OV/UV window (90%REF < FB < 110%REF). When EN is pulled low or VCC is below POR, PGOOD is pulled low with no delay.

If the PGOOD pin is pulled up by the external bias supply instead of VCC by itself, when the part is disabled, the internal PGOOD open-drain transistor is off, the external bias supply can charge PGOOD pin HIGH. This is known as false PGOOD reporting. At start-up when VCC rises from 0V, PGOOD is pulled low when VCC reaches 1V. After EN is pulled low and VCC is falling, the PGOOD internal open-drain transistor opens with high impedance when VCC falls below 1V. The time between when EN is pulled low and PGOOD OPEN depends on the VCC falling time to 1V.

Fault Protection

Overcurrent Protection

The overcurrent function protects against any overload condition and output short at worst case by monitoring the current flowing through the upper MOSFET.

There are two current limiting thresholds: I_{OC1} and I_{OC2}. I_{OC1} limits the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set at 3.6A (default) with the ILIMIT pin connected to GND or VCC, or left open. The current limit threshold can also be programmed by a resistor, R_{LIM}, at the ILIMIT pin to ground. Use Equation 14 to calculate the resistor.

$$R_{LIM} = \frac{300000}{I_{OC}[A] + 0.018} \quad \text{(EQ. 14)}$$

Note that I_{OC1} is higher with lower R_{LIM}. The resistor value range to program the OC1 peak current threshold is 40kΩ to 330kΩ. R_{LIM} values out of this range are not recommended.

The second current protection threshold, I_{OC2}, is 15% higher than I_{OC1}. Instantly after the high-side MOSFET current reaches I_{OC2}, the PWM is shut off after a two-cycle delay and the IC enters Hiccup mode. In Hiccup mode, the PWM is disabled for a dummy soft-start cycle that is equal to five regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The I_{OC2} offers a robust and reliable protection against the worst case conditions.

The frequency foldback is implemented on the ISL85403. When overcurrent limiting, the switching frequency is reduced to be proportional to the output voltage to keep the inductor current under the limit threshold during an overload condition. The low frequency limit under frequency foldback operation is 40kHz.

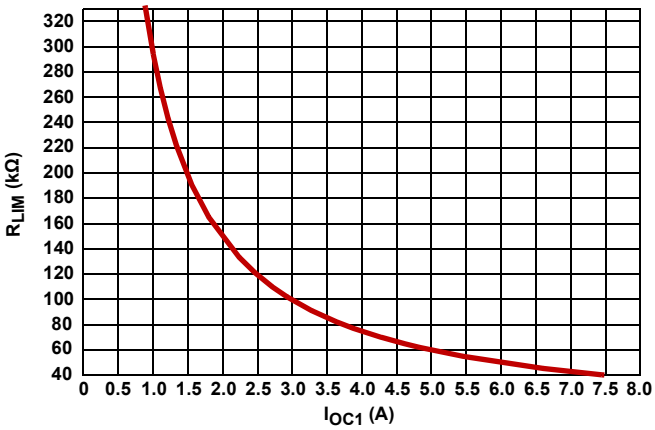


FIGURE 31. R_{LIM} vs I_{OC1}

Overvoltage Protection

If the voltage detected on the FB pin is over 110% or 120% of reference, the high-side and low-side drivers shut down immediately and stay off until the FB voltage drops to 0.8V. When the FB voltage drops to 0.8V, the drivers are released ON. 110% OVP is off during soft-start and active after soft-start is complete. 120% OVP is active during and after soft-start.

Thermal Protection

The ISL85403 PWM is disabled if the junction temperature reaches +160°C. There is +20°C hysteresis for OTP. The part restarts after the junction temperature drops below +140°C.

Component Selections

The ISL85403 iSim model can be used to simulate for both the time domain behaviors and small signal loop stability analysis.

Output Capacitors - Buck

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors can also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings with no DC bias. In DC/DC converter applications, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer's datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias

so this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction generally suffices. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

In buck topology, the following equations allow calculation of the required capacitance to meet a required ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 \times f_{SW} \times C_{OUT}} \quad \text{(EQ. 15)}$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency, and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 16)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. Equation 17 determines the required output capacitor value to achieve a wanted overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times (V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 17)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load.

Input Capacitors - Buck

Depending on the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage. Thus, restrict the switching frequency pulse current in a small area over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at the VIN pin of the IC and multiple capacitors including 1µF and 0.1µF are recommended. Place these capacitors as close as possible to the IC.

Output Inductor - Buck

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% to 40% of total load current. The inductor value is calculated using Equation 18:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 18)}$$

Increasing the value of inductance reduces the ripple current and therefore the ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient.

The inductor current rating should not saturate in overcurrent conditions.

Low-Side Power MOSFET

In a synchronous buck application, a power N MOSFET is needed as the synchronous low-side MOSFET and a good one should have low Qgd, low $r_{DS(ON)}$, and small Rg (Rg_typ < 1.5Ω recommended). The Vgth_min is recommended to be 1.2V or higher. A good example is SQS462EN.

Add a 5.1k or smaller value resistor to connect LGATE to ground to avoid false turn-on of the LGATE caused by coupling noise.

Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB according to Equation 19.

$$V_{OUT} = 0.8 \bullet \left(1 + \frac{R_{UP}}{R_{LOW}}\right) \quad \text{(EQ. 19)}$$

In an application requiring low input quiescent current, use large resistors for the divider. Generally, a resistor value of 10k to 300k can be used for the upper resistor.

Boost Inductor (2-Stage Boost Buck)

Besides the need to sustain the current ripple to be within a certain range (30% to 50%), the boost inductor current at its soft-start is a more important perspective to be considered in selection of the boost inductor. Each time the boost starts up, there is a fixed 500µs soft-start time when the duty cycle increases linearly from $t_{MIN(ON)} * f_{SW}$ to ~50%. Before and after boost start-up, the boost output voltage jumps from V_{IN_BOOST} to voltage (V_{IN_BOOST} + V_{OUT_BUCK}). The design target in boost soft-start is to ensure the boost input current is sustained to a minimum but is able to charge the boost output voltage to have a voltage step equaling to V_{OUT_BUCK}. A large inductor prevents the inductor current from increasing and is not high enough to be able to charge the output capacitor to the final steady state value (V_{IN_BOOST} + V_{OUT_BUCK}) within 500µs. A 6.8µH inductor is a good starting point for its selection in design. Check the boost inductor current at start-up with an oscilloscope to ensure it is under an acceptable range. It is suggested to run the iSim model (use the ISL85403 iSim model) to assist in the proper inductor value.

Boost Output Capacitor (2-Stage Boost Buck)

Based on the same theory in boost start-up, a large capacitor at boost output causes high inrush current at boost PWM start-up. 22µF is a good choice for applications with a buck output voltage less than 10V. Also some minimum amount of capacitance has to be used in boost output to keep the system stable. Renesas recommends running the iSim model to assist in designing the proper capacitor value.

Loop Compensation Design - Buck

The ISL85403 uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered a state variable because its peak current is constant and the system becomes a single order system. It is much easier to design the compensator to stabilize the loop compared with voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 32 shows the small signal model of a buck regulator.

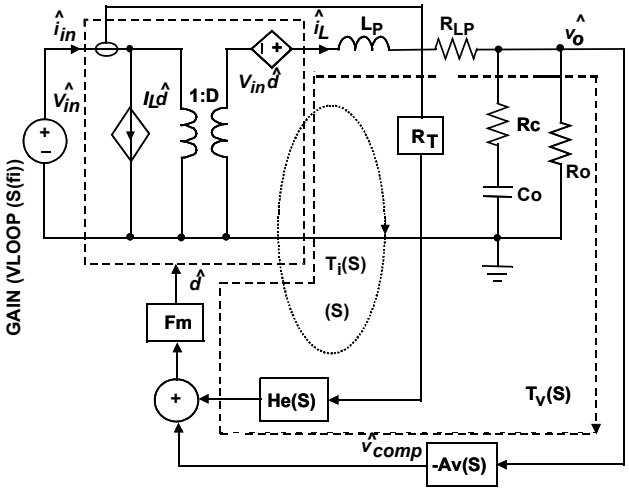


FIGURE 32. SMALL SIGNAL MODEL OF BUCK REGULATOR

PWM Comparator Gain F_m

The PWM comparator gain, F_m, for peak current mode control is given by Equation 20:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \quad \text{(EQ. 20)}$$

where S_e is the slew rate of the slope compensation and S_n is given by Equation 21:

$$S_n = R_t\frac{V_{in} - V_o}{L_P} \quad \text{(EQ. 21)}$$

where R_t is the gain of the current amplifier.

Current Sampling Transfer Function $H_e(S)$

In a current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 22:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \quad \text{(EQ. 22)}$$

where Q_n and ω_n are given by $Q_n = \frac{2}{\pi}, \omega_n = \pi f_{SW}$

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 23)}$$

where:,

$$\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L_P}}, \omega_o = \frac{1}{\sqrt{L_P C_o}}$$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 24:

$$F_2(S) = \frac{\hat{I}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_{LP}}\frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 24)}$$

where $\omega_z = \frac{1}{R_o C_o}$.

Current loop gain $T_i(S)$ is expressed as Equation 25:

$$T_i(S) = R_t F_m F_2(S) H_e(S) \quad \text{(EQ. 25)}$$

The voltage loop gain with open current loop is expressed in Equation 26:

$$T_v(S) = KF_m F_1(S) A_v(S) \quad \text{(EQ. 26)}$$

The Voltage loop gain with current loop closed is given by Equation 27:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \quad \text{(EQ. 27)}$$

If $T_i(S)>>1$, then Equation 27 can be simplified as Equation 28:

$$L_v(S) = \frac{R_o + R_{LP}}{R_t}\frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}}\frac{A_v(S)}{H_e(S)}, \omega_p \approx \frac{1}{R_o C_o} \quad \text{(EQ. 28)}$$

Equation 28 shows that the system is a single order system. Therefore, a simple type II compensator can be easily used to stabilize the system. A type III compensator is needed to expand the bandwidth for current mode control in some cases.

A compensator with two zeros and one pole is recommended for this part, as shown in Figure 33.

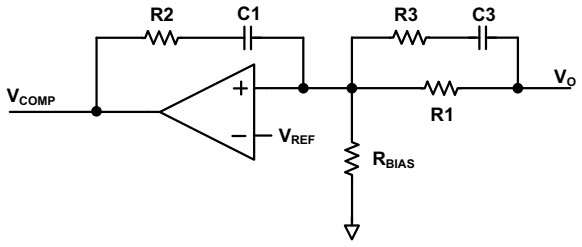


FIGURE 33. TYPE III COMPENSATOR

Its transfer function is expressed as Equation 29:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_O} = \frac{1}{SR_1C_1} \frac{\left(1+\frac{S}{\omega_{cz1}}\right)\left(1+\frac{S}{\omega_{cz2}}\right)}{\left(1+\frac{S}{\omega_{cp}}\right)} \quad \text{(EQ. 29)}$$

where:

$$\omega_{cz1} = \frac{1}{R_2C_1},\ \omega_{cz2} = \frac{1}{(R_1+R_3)C_3},\ \omega_{cp} = \frac{1}{R_3C_3}$$

Compensator design goal:

Loop bandwidth f_c: $\left(\frac{1}{4}\text{to}\frac{1}{10}\right)f_{SW}$

Gain margin: >10dB

Phase margin: 45°

The compensator design procedure is as follows:

1. Position ω_{CZ2} and ω_{CP} to derive R_3 and C_3.

   Put the compensator zero ω_{CZ2} at (1 to 3)/(R_oC_o)

   $$\omega_{cz2} = \frac{3}{R_oC_o} \quad \text{(EQ. 30)}$$

   Put the compensator pole ω_{CP} at ESR zero or 0.35 to 0.5 times of switching frequency, whichever is lower. In an all-ceramic-cap design, the ESR zero is normally higher than half of the switching frequency. R_3 and C_3 can be derived as follows:

   Case A: ESR zero $\frac{1}{2\pi R_cC_o}$ less than (0.35 to 0.5)f_{SW}

   $$C_3 = \frac{R_oC_o - 3R_cC_o}{3R_1} \quad \text{(EQ. 31)}$$

   $$R_3 = \frac{3R_cR_1}{R_o - 3R_c} \quad \text{(EQ. 32)}$$

   Case B: ESR zero $\frac{1}{2\pi R_cC_o}$ larger than (0.35 to 0.5)f_{SW}

   $$C_3 = \frac{0.33R_oC_of_{SW} - 0.46}{f_{SW}R_1} \quad \text{(EQ. 33)}$$

   $$R_3 = \frac{R_1}{0.73R_oC_of_s - 1} \quad \text{(EQ. 34)}$$

2. Derive R_2 and C_1.

   The loop gain $L_V(S)$ at crossover frequency of f_c has unity gain. Therefore, C_1 is determined by Equation 35.

   $$C_1 = \frac{(R_1+R_3)C_3}{2\pi f_cR_tR_1C_o} \quad \text{(EQ. 35)}$$

   The compensator zero ω_{CZ1} can boost the phase margin and bandwidth. To put ω_{CZ1} at two times of crossover frequency f_c is a good starting point. It can be adjusted according to the specific design. R_1 can be derived from Equation 36.

   $$R_2 = \frac{1}{4\pi f_cC_1} \quad \text{(EQ. 36)}$$

   Example: V_{IN} = 12V, V_o = 5V, I_o = 2A, f_{SW} = 500kHz, C_o = 60µF/3mΩ, L = 10µH, R_t = 0.20V/A, f_c = 50kHz, R_1 = 105k, R_{BIAS} = 20kΩ.

   Select the crossover frequency to be 35kHz. Because the output capacitors are all ceramic, use Equations 33 and 34 to derive R_3 to be 20k and C_3 to be 470pF.

   Then use Equations 35 and 36 to calculate C_1 to be 180pF and R_2 to be 12.7k. Select 150pF for C_1 and 15k for R_2.

There is approximately 30pF parasitic capacitance between COMP to FB pins that contributes to a high frequency pole. Any extra external capacitor is not recommended between COMP and FB.

Figure 34 shows the simulated Bode plot of the loop. It has 26kHz loop bandwidth with 70° phase margin and -28 dB gain margin.

Note in applications where the PFM mode is required especially when type III compensation network is used, the value of the capacitor between the COMP pin and the FB pin (not the capacitor in series with the resistor between COMP and FB) should be minimal to reduce the noise coupling for proper PFM operation. No external capacitor between COMP and FB is recommended for PFM applications.

In PFM mode operations, an RC filter from FB to ground (R in series with C, connecting from FB to ground) can help reduce the noise effects injected to FB pin. The recommended values for the filter are 499Ω to 1k for the R and 470pF for the C.

Loop Compensation Design for 2-Stage Boost Buck and Single-Stage Buck Boost

For 2-stage boost buck and single-stage non-inverting buck boost configurations, it is highly recommended to use the iSim model to evaluate the loop bandwidth and phase margin.

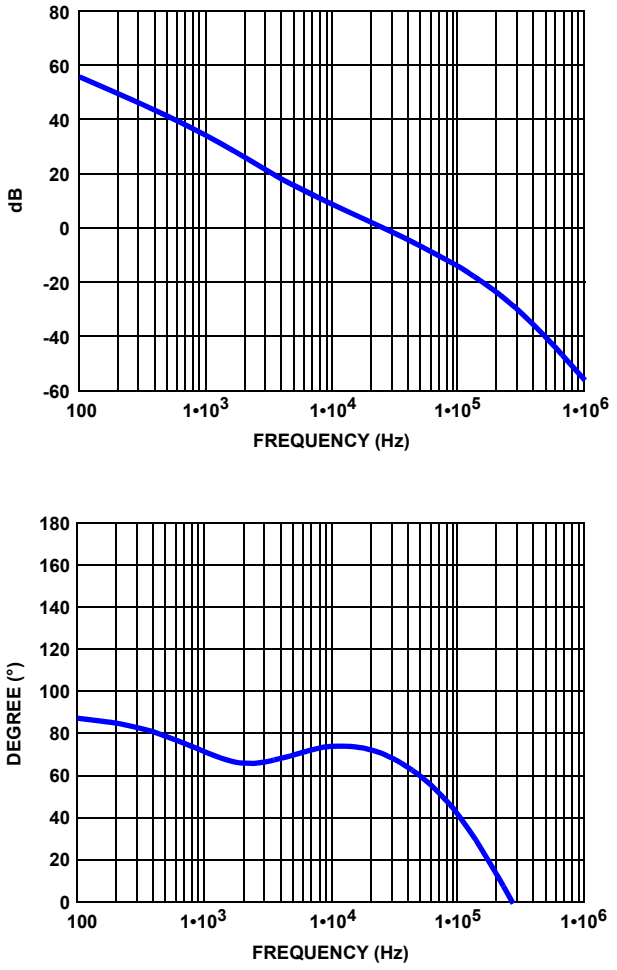


FIGURE 34. SIMULATED LOOP BODE PLOT

Layout Suggestions

1. Place the input ceramic capacitors as close as possible to the IC VIN pin and power ground connecting to the power MOSFET or diode. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET/diode) as small as possible to achieve the fewest voltage spikes induced by the trace parasitic inductance.
2. Place the input aluminum capacitors as close as possible to the IC VIN pin.
3. Keep the phase node copper area small but large enough to handle the load current.
4. Place the output ceramic and aluminum capacitors close to the power stage components as well.
5. Place vias (≥9) in the bottom pad of the IC. Place the bottom pad in the ground copper plane with an area as large as possible in multiple layers to effectively reduce the thermal impedance.
6. Place the 4.7µF ceramic decoupling capacitor at the VCC pin (the closest place to the IC). Put multiple vias (≥3) close to the ground pad of this capacitor.
7. Keep the bootstrap capacitor close to the IC.
8. Keep the LGATE drive trace as short as possible and try to avoid using vias in the LGATE drive path to achieve the lowest impedance.
9. Place the positive voltage sense trace close to the place that is strictly regulated.
10. Place all the peripheral control components close to the IC.

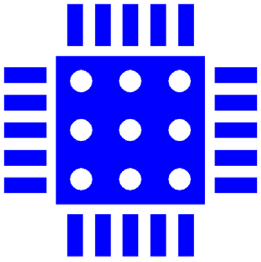


FIGURE 35. PCB VIA PATTERN

Revision History

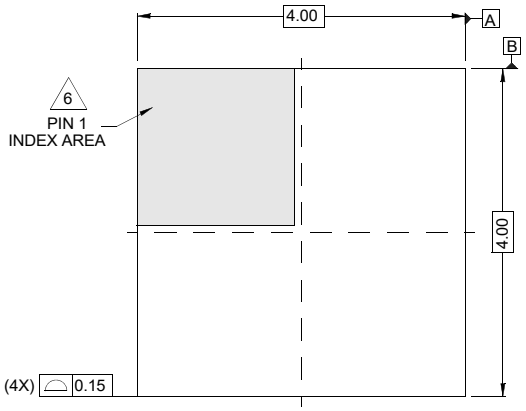
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 28, 2020	4.00	Updated the AUXVCC pin description by changing 3V to 4.5V. Updated the AUXVCC Input Voltage Range minimum specification from 3V to 4.5V. Updated Recommended Operating Condition for AUXVCC. Updated AUXVCC Switchover section.
Aug 8, 2019	3.00	Updated first sentence in PWM Control section on page 14. Updated second paragraph in PFM Mode Operation section on page 14.
Mar 11, 2019	2.00	Updated Releated literature section. Updated order of datasheet. Updated ordering information table by updating Note 1, adding tape and reel versions and column. Updated PFM Mode Operation section by adding last paragraph. Updated Output Voltage section by adding last paragraph. Removed About Intersil section. Updated Disclaimer.
March 13, 2015	1.00	Changed the max input Voltage (Vin) from 36V to 40V on the following pages: On page 1: In the description and features sections On page 6: V_{IN} pin description On page 7: Recommended operating conditions for V_{IN} On page 15: Application description for the “Input Voltage” section On page 1, added “Related Literature” section. On page 5, added ISL85403EVAL2Z to the Ordering Information table. Replaced Figures 9 and 10. Removed Figures 10 and 11 and the references on page 15.
March 12, 2014	0.00	Initial Release

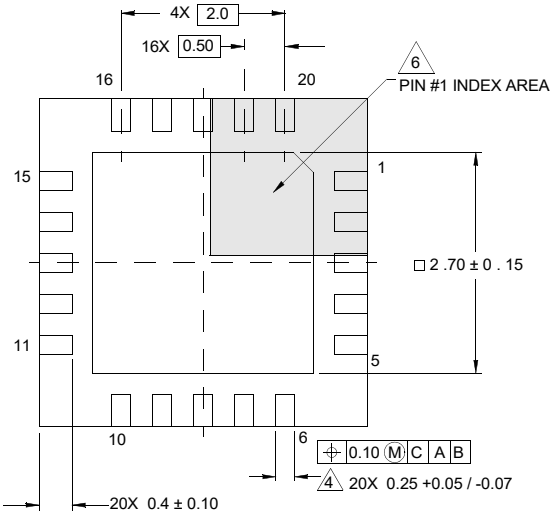
Package Outline Drawing

For the most recent package outline drawing, see L20.4x4C.

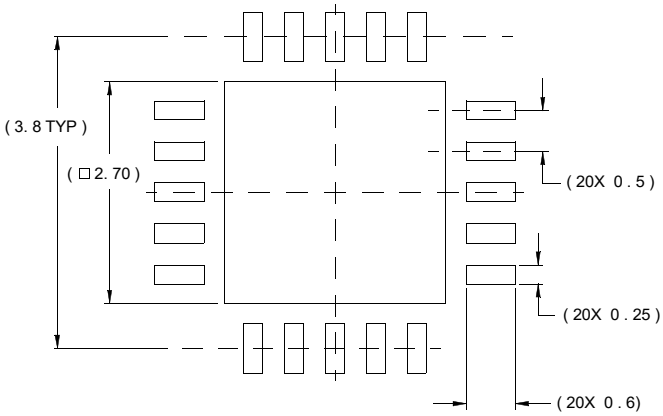
L20.4x4C
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06



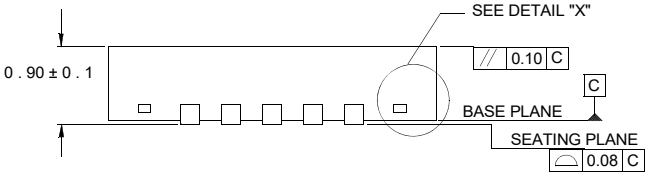
TOP VIEW



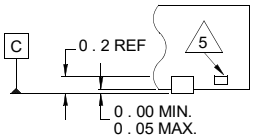
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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(Rev.1.0 Mar 2020)

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