# ISL88550A

Synchronous Step-Down Controller with Sourcing and Sinking LDO Regulator

FN6168
Rev 3.00
April 23, 2008

ISL88550A integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT, and a 10mA reference output buffer to generate VTTR. The buck controller drives two external N-Channel MOSFETs to generate output voltages down to 0.7V from a 2V to 25V input with output currents up to 15A. The LDO can source up to 2.5A and sink up to -2.0A continuously. Both the LDO output and the 10mA reference buffer output can be made to track the REFIN voltage via a built-in resistive divider. These features make the ISL88550A ideally suited for DDR memory applications in desktops, notebooks and graphics cards.

The PWM controller in the ISL88550A uses constant-on-time PWM architecture with a programmable switching frequency of up to 600kHz. This control scheme handles wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining high efficiency and a relatively constant switching frequency. The ISL88550A offers full programmable UVP/OVP and skip mode options ideal in portable applications. Skip mode allows for improved efficiency at lighter loads.

The VTT and VTTR outputs track to VREFIN/2. The high bandwidth of this LDO regulator allows excellent transient response without the need for bulk capacitors, thus reducing the cost and size.

The buck controller and LDO regulators are provided with independent current limits. Adjustable loss-less fold-back current limit for the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low side synchronous MOSFET. Once overcurrent is removed, the regulator is allowed to enter soft-start again. This helps minimize power dissipation during short-circuit condition. Additionally, overvoltage and undervoltage protection mechanisms are built in. The ISL88550A allow flexible sequencing and standby power management using SHDNA#, and STBY# inputs.

## Features

- Pb-Free (RoHS Compliant)

### Buck Controller

- Constant-On PWM with 100ns Load-Step Response
- Start-up with Pre-biased Output Voltage
- Up to 95% Efficiency
- 2V to 25V Input Voltage Range
- 2.5V Fixed or 0.7V to 3.5V Adjustable Output
- 200kHz/300kHz/450kHz/600kHz Switching Frequencies
- Programmable Current Limit with Foldback Capability
- 1.7ms Digital Soft-Start and Independent Shutdown
- Overvoltage/Undervoltage Protection Option
- Power-Good Window Comparator

### LDO Section

- Fully Integrated VTT and VTTR Capability
- VTT has +2.5A/-2.0A Sourcing/Sinking Capability
- Start-Up with Pre-Biased Output Voltage
- VTT and VTTR Outputs Track VREFIN/2
- VTT and VTTR 1% of VREFIN/2
- Low All-Ceramic Output Capacitor Designs
- 1.0V to 2.8V Input REFIN Range
- Analog Soft-Start Option and Independent Shutdown
- Power-Good Window Comparator

## Applications

- DDR, DDR II and DDR III Memory Power Supplies
- Desktop Computers
- Notebooks and Desknotes
- Graphics Cards
- Game Consoles
- Networking and RAID

## Ordering Information

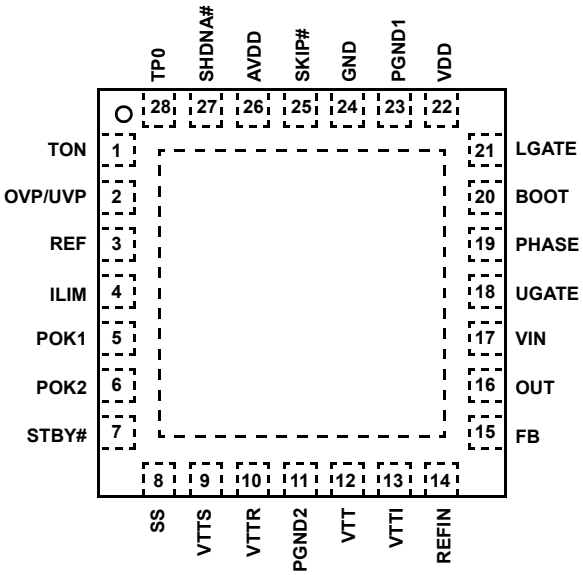
| PART NUMBER (Note) | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL88550AIRZ | ISL88 550AIRZ | -40 to +85 | 28 Ld 5×5 TQFN | L28.5x5B |
| ISL88550AIRZ-T* | ISL88 550AIRZ | -40 to +85 | 28 Ld 5×5 TQFN Tape and Reel | L28.5x5B |

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## *Pinout*

**ISL88550A**
**(28 LD TQFN)**
TOP VIEW



## Absolute Maximum Ratings

VIN to GND . . . . . -0.3V to +25V
VDD, AVDD, VTTI to GND . . . . . -0.3V to 6V
SHDNA#, REFIN to GND . . . . . -0.3V to 6V
SS, POK1, POK2, SKIP#, ILIM, FB to GND . . . . . -0.3V to 6V
STBY#, TON, REF, UVP/OVP to GND . . . . . -0.3V to $AV_{DD}$ + 0.3V
OUT, VTTR to GND . . . . . -0.3V to $AV_{DD}$ + 0.3V
LGATE to PGND1 . . . . . -0.3V to $V_{DD}$ + 0.3V
UGATE to PHASE . . . . . -0.3V to VBOOT + 0.3V
BOOT to PHASE . . . . . -0.3V to 6V
BOOT to GND . . . . . -0.3V to +33V
VTT to GND. . . . . -0.3V to VTTI + 0.3V
VTTS to GND. . . . . -0.3V to $AV_{DD}$ + 0.3V
PGND1, PGND2 to GND . . . . . -0.3V to +0.3V
REF Short Circuit to GND. . . . . Continuous

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 28 Ld TQFN Package (Notes 1, 2). . . . | 32 | 2.5 |

## Operating Conditions

Junction Temperature Range. . . . . -55°C to +150°C
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C + 150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

1. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
3. Following are target specifications. Final limits may change as a result of characterization.

## Electrical Specifications

$V_{IN}$ = +15V, $V_{DD}$ = $AV_{DD}$ = SHDNA# = STBY# = BOOT = ILIM = 5V, OUT = REFIN = VTTI = 2.5V, FB = SKIP# = OVP/UVP = GND. PGND1 = PGND2 = PHASE = GND, VTTS = VTT, $t_{ON}$ = OPEN, $T_A$ = -40°C to +85°C, Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. (Note 4).

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MAIN PWM CONTROLLER** | | | | | | |
| $V_{IN}$ Input Voltage Range | | | 2 | | 25 | V |
| $V_{DD}$, $AV_{DD}$ Input Voltage Range | | | 4.5 | | 5.5 | V |
| Output Adjust Range | | | 0.7 | | 3.5 | V |
| Output Voltage Accuracy (Note 5) | FB = OUT | | 0.693 | 0.7 | 0.707 | V |
| | FB = GND | | 2.470 | 2.5 | 2.53 | V |
| Soft-Start Ramp Time | Rising edge of SHDNA# to full current limit | | | 1.7 | | ms |
| ON-Time | $V_{IN}$ = 15V, $V_{OUT}$ = 1.5V (Note 6) | $t_{ON}$ = GND (600kHz) | 170 | 194 | 219 | ns |
| | | $t_{ON}$ = REF (450kHz) | 213 | 243 | 273 | ns |
| | | $t_{ON}$ = OPEN (300kHz) | 316 | 352 | 389 | ns |
| | | $t_{ON}$ = $AV_{DD}$ (200kHz) | 461 | 516 | 571 | ns |
| Minimum, OFF-Time | (Note 6) | | 200 | 300 | 450 | ns |
| $V_{IN}$ Quiescent Supply Current | | | | 25 | 40 | µA |
| $V_{IN}$ Shutdown Supply Current | SHDNA# = STBY# = GND | | | 1 | 5 | µA |
| Combined $AV_{DD}$ and $V_{DD}$ Quiescent Supply Current | All on (PWM, VTT, and VTTR on), $V_{FB}$ = 0.75V | | | 2.5 | 5 | mA |
| | STBY# = GND (only VTTR and PWM on), $V_{FB}$ = 0.75V | | | 1 | 2 | mA |
| Combined $AV_{DD}$ and $V_{DD}$ Shutdown Supply Current | SHDNA# = STBY# = GND | | | 2 | 10 | µA |
| $AV_{DD}$ Undervoltage Lockout Threshold | Rising edge of $AV_{DD}$ | | 4.1 | 4.25 | 4.4 | V |
| | Hysteresis | | | 50 | | mV |
| **REFERENCE** | | | | | | |
| Reference Voltage | $AV_{DD}$ = 4.5V to 5.5V; $I_{REF}$ = 0µA to 130µA | | 1.98 | 2 | 2.02 | V |
| Reference Load Regulation | $I_{REF}$ = 0µA to 50µA | | | | 0.01 | V |

**Electrical Specifications** $V_{IN}$ = +15V, $V_{DD}$ = $AV_{DD}$ = SHDNA# = STBY# = BOOT = ILIM = 5V, OUT = REFIN = VTTI = 2.5V, FB = SKIP# = OVP/UVP = GND. PGND1 = PGND2 = PHASE = GND, VTTS = VTT, $t_{ON}$ = OPEN, $T_A$ = -40°C to +85°C, Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. (Note 4). **(Continued)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| REF Undervoltage Lockout | $V_{REF}$ rising | | 1.93 | | V |
| | Hysteresis | | 300 | | mV |
| **FAULT DETECTION** | | | | | |
| OVP Trip Threshold (Referenced to Nominal $V_{OUT}$) | UVP/OVP = $AV_{DD}$ | 110 | 114 | 118 | % |
| UVP Trip Level Referred to Nominal $V_{OUT}$ | | 65 | 70 | 75 | % |
| POK1 Trip Level Referred to Nominal $V_{OUT}$ | Lower level, falling edge, 1% hysteresis | 87 | 90 | 93 | % |
| | Upper level, rising edge, 1% hysteresis | 107 | 110 | 113 | % |
| POK2 Trip Level Referred to Nominal VTTS and VTTR | Lower level, falling edge, 1% hysteresis | 87.5 | 90 | 92.5 | % |
| | Upper level, rising edge, 1% hysteresis | 107.5 | 110 | 112.5 | % |
| POK2 Disable Threshold (Measured at REFIN) | $V_{REFIN}$ rising (Hysteresis = 75mV typical) | 0.7 | | 0.9 | V |
| UVP Blanking Time | From rising edge of SHDNA# | 8 | 14 | 25 | ms |
| OVP, UVP, POK_ Propagation Delay | | | 10 | | µs |
| POK_ Output Low Voltage | $I_{SINK}$ = 4mA | | | 0.3 | V |
| POK_ Leakage Current | $V_{POK\_}$ = 5.5V, VFB = 0.8V, VTTS = 1.3V | | | 1 | µA |
| ILIM Adjustment Range | | 0.25 | | 2.00 | V |
| ILIM Input Leakage Current | | | | 0.1 | µA |
| Current Limit Threshold (Fixed) PGND1 to PHASE | ILIM = $AV_{DD}$ | 45 | 50 | 55 | mV |
| Current Limit Threshold (Adjustable) PGND1 to PHASE | $V_{ILIM}$ = 2V | 170 | 200 | 235 | mV |
| Current-Limit Threshold (Negative Direction) PGND1 to PHASE | SKIP# = $AV_{DD}$ | -75 | -60 | -45 | mV |
| Current-Limit Threshold (Negative Direction) PGND1 to PHASE | SKIP# = $AV_{DD}$, ILIM = 2V | | -250 | | mV |
| Current-Limit Threshold (Zero Crossing) PGND1 to PHASE | | | 3 | | mV |
| Thermal Shutdown Threshold | Rising | | 150 | | °C |
| | Hysteresis | | 15 | | °C |
| **INTERNAL BOOT DIODE** | | | | | |
| $V_D$ Forward Voltage | PVCC - $V_{BOOT}$, $I_F$ = 10mA | | 0.60 | 0.70 | V |
| $I_{BOOT\_LEAKAGE}$ Leakage Current | $V_{BOOT}$ = 25V, PHASE = 20V, PVCC = 5V | | 300 | 500 | nA |
| **MOSFET DRIVERS** | | | | | |
| UGATE Gate Driver ON-Resistance | $V_{BOOT}$ - $V_{PHASE}$ = 5V | | 1.5 | 5 | Ω |
| LGATE Gate Driver ON-Resistance in High State | | | 1.5 | 5 | Ω |
| LGATE Gate Driver ON-Resistance in Low State | | | 0.6 | 3 | Ω |
| Dead Time (Additional to Adaptive Delay) | LGATE rising | | 30 | | ns |
| | UGATE rising | | 30 | | ns |
| **INPUTS AND OUTPUTS** | | | | | |
| Logic Input Threshold High (SHDNA#, SKIP#, STBY#) | Rising edge | 1.2 | 1.7 | 2.20 | V |
| | Hysteresis | | 225 | | mV |
| Logic Input Current (SHDNA#, SKIP#, STBY#) | | -1 | | 1 | µA |
| FB Input Logic Level | Low (2.5V output) | | | 0.1 | V |

**Electrical Specifications** $V_{IN}$ = +15V, $V_{DD}$ = $AV_{DD}$ = SHDNA# = STBY# = BOOT = ILIM = 5V, OUT = REFIN = VTTI = 2.5V, FB = SKIP# = OVP/UVP = GND. PGND1 = PGND2 = PHASE = GND, VTTS = VTT, $t_{ON}$ = OPEN, $T_A$ = -40°C to +85°C, Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. (Note 4). **(Continued)**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Bias Current (FB) | | -0.1 | | 0.1 | µA |
| Four-Level Input Logic Levels ($t_{ON}$, OVP/UVP) | High | $AV_{DD}$ - 0.4 | | | V |
| | Floating | 3.15 | | 3.85 | V |
| | REF | 1.65 | | 2.35 | V |
| | Low | | | 0.5 | V |
| Logic Input Current ($t_{ON}$, OVP/UVP, Note 5) | | -3 | | +3 | µA |
| OUT Input Resistance | FB = GND | 125 | 250 | 500 | kΩ |
| | FB Adjustable Mode | 125 | 250 | 500 | kΩ |
| OUT Discharge Mode ON-Resistance | | | 15 | 30 | Ω |
| **LINEAR REGULATORS (VTTR AND VTT)** | | | | | |
| VTTI Input Voltage Range | | 1.0 | | 2.8 | V |
| VTTI Supply Current | $I_{VTT}$ = $I_{VTTR}$ = 0 | | 0.1 | 1 | mA |
| VTTI Shutdown Current | SHDNA# = STBY# = GND | | | 10 | µA |
| REFIN Input Impedance | $V_{REFIN}$ = 2.5V | 17 | 20 | 27 | kΩ |
| REFIN Range | | 1.0 | | 2.8 | V |
| VTT, VTTR UVLO Threshold (Measured at OUT) | | 0.01 | 0.1 | 0.2 | V |
| Soft-Start Charge Current | $V_{SS}$ = 0 | | 4 | | µA |
| VTT internal MOSFET High-Side ON-Resistance | $I_{VTT}$ = -100mA, $V_{VTTI}$ = 1.5V, $AV_{DD}$ = 4.5V ($T_J$ = +125°C) | | 0.10 | 0.28 | Ω |
| VTT internal MOSFET Low-Side ON-Resistance | $I_{VTT}$ = 100mA, $AV_{DD}$ = 4.5V ($T_J$ = +125°C) | | 0.18 | 0.43 | Ω |
| VTT Output Accuracy (Referenced to VTTR) | $V_{REFIN}$ = 1.8V or 2.5V, $I_{VTT}$ = ±5mA | -1.5 | | 1.5 | % |
| VTT Load Regulation | $V_{REFIN}$ = 2.5V, $I_{VTT}$ = 0A to ±1.5A | | 1 | | % |
| | $V_{REFIN}$ = 1.8V, $I_{VTT}$ = 0A to ±1.5A | | 1 | | % |
| VTT Positive Current Limit | VTT = 0 | 2.5 | 3.0 | 4.0 | A |
| VTT Negative Current Limit | VTT = VTTI | -3.5 | -2.5 | -2.0 | A |
| VTTS Input Current | $V_{VTTS}$ = 1.5V, VTT Open | | 0.1 | 1 | µA |
| VTTR Output Error (Referenced to $V_{REFIN}$/2) | $V_{REFIN}$ = 1.8V, $I_{VTTR}$ = 0mA | -1.25 | | 1.25 | % |
| VTTR Current Limit | VTTR = 0 or VTTI | ±20 | ±40 | ±60 | mA |

NOTES:

4. Limits established by characterization and are not production tested.
5. When the inductor is in continuous conduction, the output voltage will have a DC regulation level higher than the error comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage will have a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.
6. On-time and off-time specifications are measured from 50% point to 50% point at the UGATE pin with PHASE = GND, $V_{BOOT}$ = 5V, and a 250pF capacitor connected from UGATE to PHASE. Actual in-circuit times may differ due to MOSFET switching speeds.

## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | TON | $t_{ON}$ On-Time Selection-Control Input. This four-level logic input sets the nominal UGATE on-time. Connect to GND, REF, $AV_{DD}$, or leave $t_{ON}$ unconnected to select the following nominal switching frequencies:<br>$t_{ON}$ = $AV_{DD}$ (200kHz)<br>$t_{ON}$ = OPEN (300kHz)<br>$t_{ON}$ = REF (450kHz)<br>$t_{ON}$ = GND (600kHz) |
| 2 | OVP/UVP | Overvoltage/Undervoltage Protection Control Input. This four-level logic input enables or disables the Overvoltage and/or Undervoltage Protection. The overvoltage limit is 116% of the nominal output voltage. The undervoltage limit is 70% of the nominal output voltage. Discharge mode is enabled when OVP is also enabled. Connect the OVP/UVP pin to the following pins for the desired function:<br>OVP/UVP = $AV_{DD}$ (Enable OVP and discharge mode, enable UVP)<br>OVP/UVP = OPEN (Enable OVP and discharge mode, disable UVP)<br>OVP/UVP = REF (Disable OVP and discharge mode, enable UVP)<br>OVP/UVP = GND (Disable OVP and discharge mode, disable UVP) |
| 3 | REF | +2.0V Reference Voltage Output. Bypass to GND with a 0.1µF (min) bypass capacitor. REF can supply 50µA for external loads. Can be used for setting voltage for ILIM. REF turns off when SHDNA#, STBY# are low. |
| 4 | ILIM | Current-Limit Threshold Adjustment for Buck Regulator. The current-limit threshold across PGND and PHASE is 0.1x the voltage at ILIM. Connect ILIM to a resistive-divider (typically from REF) to set the current-limit threshold between 25mV and 200mV (with 0.25V to 2V at ILIM). Connect to $AV_{DD}$ to select the 50mV default current-limit threshold. |
| 5 | POK1 | Buck Power-Good Open-Drain Output. POK1 is low when the Buck output voltage is more than 10% above or below the normal regulation point or during soft-start. POK1 is high impedance when the output is in regulation and the soft-start circuit has terminated. POK1 is low in shutdown. |
| 6 | POK2 | LDO Power-Good Open-Drain Output. In normal mode, POK2 is low when either VTTR or VTTS is more than 10% above or below the normal regulation point, which is typically REFIN/2. In standby mode, POK2 responds only to VTTR input. POK2 is low in shutdown, and when VREFIN is less than 0.8V. |
| 7 | STBY# | Stand-By Pin. Tie to low for low quiescent mode where the VTT output is disabled with high impedance but the VTTR buffer is kept alive if SHDNA# is high. POK2 takes input from only VTTR in this mode. VTT is discharged to 0V when SHDNA# = GND. PWM output can be on or off depending on the state of SHDNA#. |
| 8 | SS | Soft-Start Control Pin for VTT and VTTR. Connect a capacitor ($C_9$ in "Typical Application Circuit" on page 22) from SS to GND (see Soft-Start capacitor Selection in “LDO Section” on page 1). Leave SS open to disable soft-start. SS discharged to GND when SHDNA# = GND |
| 9 | VTTS | Sensing Pin for Termination Supply Output. Normally tied to VTT pin to allow accurate regulation to ½ the REFIN voltage. Connected to a resistor divider from VTT to GND to regulate VTT to higher than ½ the REFIN voltage. |
| 10 | VTTR | Termination Reference Voltage. VTTR tracks the value of the VTT output. |
| 11 | PGND2 | Power Ground for the VTT and VTTR. |
| 12 | VTT | Termination Power Supply Output. Tie VTT to VTTS to regulate to $V_{REFIN}/2$. |
| 13 | VTTI | Power Supply Input Voltage for VTT. Normally tied to output of buck regulator for DDR application. |
| 14 | REFIN | External Reference Input. This is used to regulate the VTT and VTTR outputs to $V_{REFIN}/2$ |
| 15 | FB | Feedback Input for Buck Output. Connect to GND for a +2.5V fixed output. For an adjustable output (0.7V to 5.5V), connect FB to a resistive-divider from the output voltage. FB regulates to +0.7V. |
| 16 | OUT | Output Voltage Sense Connection. Connect directly to the positive terminal of the buck capacitors. OUT senses the output voltage to determine the on-time for the high-side switching MOSFET (Q1 in the "Typical Application Circuit" on page 22). OUT also serves as the buck output’s feedback input in fixed-output modes. When discharge mode is enabled by OVP/UVP, the output capacitor is discharged through an internal 20Ω resistor connected between OUT and ground. |
| 17 | VIN | Input Voltage Sense Connection. Connect to input power source. $V_{IN}$ is used only to set the PWM on-time one-shot timer. This pin can range from 2V to 25V. |
| 18 | UGATE | High-Side Gate-Driver Output. Swings from PHASE to BOOT. UGATE is low when in shutdown or UVLO. |

## Pin Descriptions (Continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 19 | PHASE | External Inductor Connection. Connect PHASE to the input side of the inductor. PHASE is used for both current limit and the return supply of the UGATE driver. |
| 20 | BOOT | Boost Flying-Capacitor Connection. Connect to an external capacitor according to the "Typical Application Circuit" on page 22 (Figure 29). See “Boost-Supply Capacitor Selection (Buck)” on page 21. |
| 21 | LGATE | Synchronous Rectifier Gate-Driver Output. Swings from PGND to $V_{DD}$. |
| 22 | VDD | Supply Input for the LGATE Gate Drive. Connect to +4.5V to +5.5V system supply voltage. Bypass to PGND1 with a 4.7µF ceramic capacitor. |
| 23 | PGND1 | Power Ground for BUCK Controller. Connect PGND1 externally to the underside of the exposed pad. |
| 24 | GND | Analog Ground for both BUCK and LDO. Connect externally to the underside of the exposed pad. |
| 25 | SKIP# | Pulse-Skipping Control Input. Connect to $AV_{DD}$ for low-noise, forced-PWM mode. Connect to GND to enable pulse-skipping operation. |
| 26 | AVDD | Analog Supply for both BUCK and LDO. Bypass to GND with a 1.0µF ceramic capacitor. A 10Ω internal resistor is connected between $V_{DD}$ and $AV_{DD}$. |
| 27 | SHDNA# | Shutdown Control Input A. Use to control Buck output. A rising edge on SHDNA# clears the overvoltage and undervoltage protection fault latches (see Tables 2 and 3). Connect $AV_{DD}$ for normal operation. |
| 28 | TP0 | Test Pin. Must be connected to GND externally. |

## Typical Operating Characteristics

$V_{IN}$ = 12V, $V_{DDQ}$ = 1.8V, $t_{ON}$ = GND, SKIP# = $AV_{DD}$, circuit of Figure 29, $T_A$ = +25°C, unless otherwise noted.

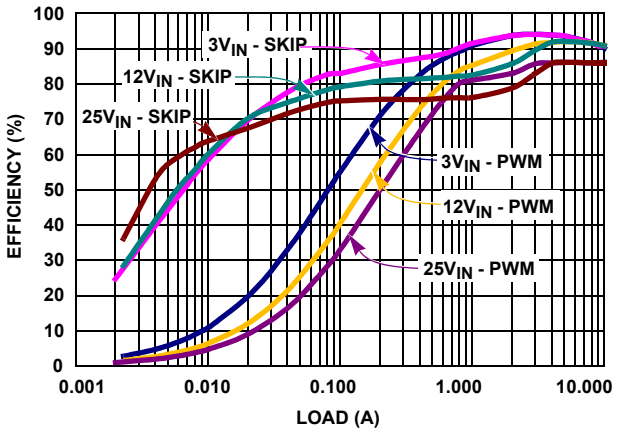



FIGURE 1. EFFICIENCY vs LOAD (1.8V) ($t_{ON}$ = GND)

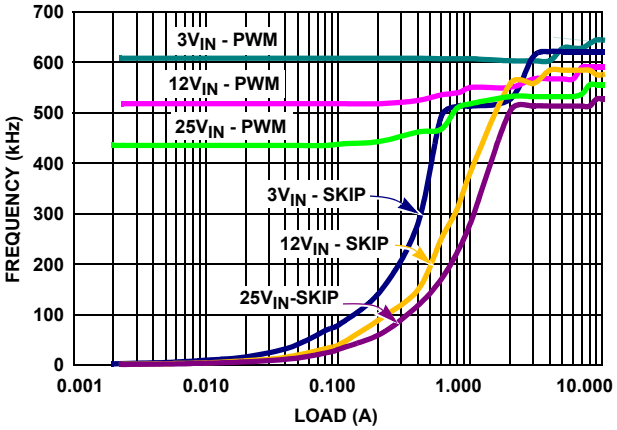



FIGURE 2. SWITCHING FREQUENCY vs LOAD ($t_{ON}$ = GND)

## *Typical Operating Characteristics*

$V_{IN}$ = 12V, $V_{DDQ}$ = 1.8V, $t_{ON}$ = GND, SKIP# = $AV_{DD}$, circuit of Figure 29, $T_A$ = +25°C, unless otherwise noted. **(Continued)**

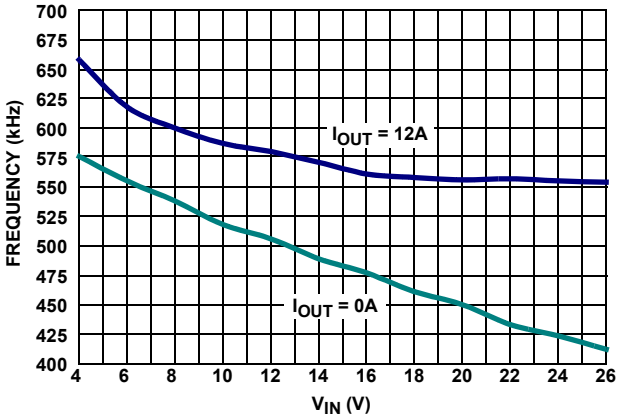



FIGURE 3. SWITCHING FREQUENCY vs INPUT VOLTAGE ($t_{ON}$ = GND)

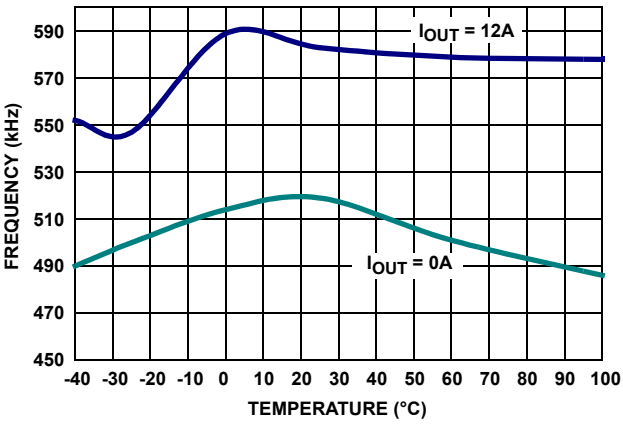



FIGURE 4. SWITCHING FREQUENCY vs TEMPERATURE ($t_{ON}$ = GND)

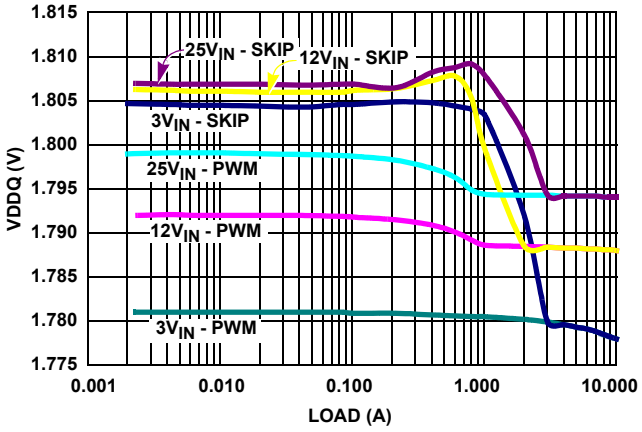



FIGURE 5. VDDQ REGULATION vs LOAD (1.8V)

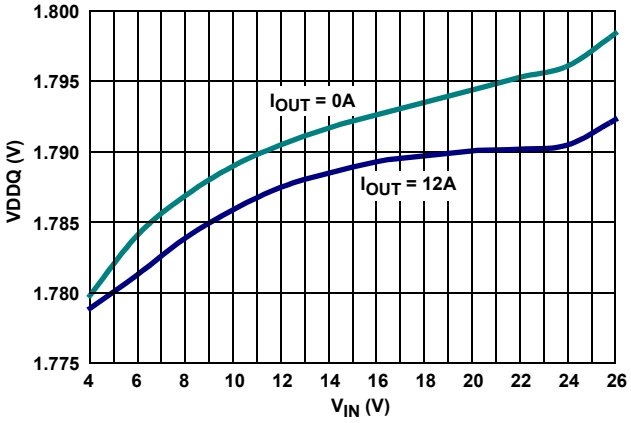



FIGURE 6. VDDQ OUTPUT vs INPUT VOLTAGE (1.8V)

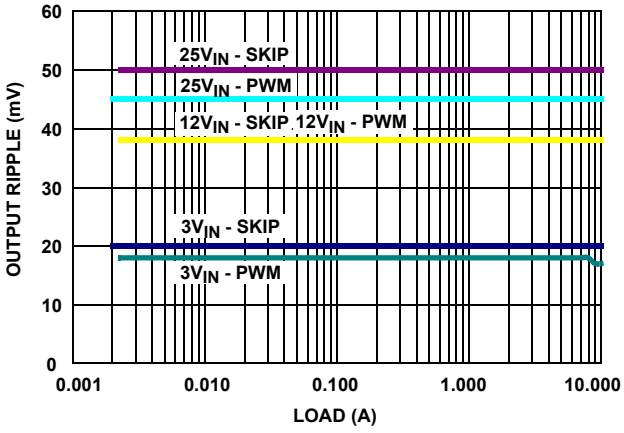



FIGURE 7. OUTPUT RIPPLE vs LOAD (1.8V) ($t_{ON}$ = GND)

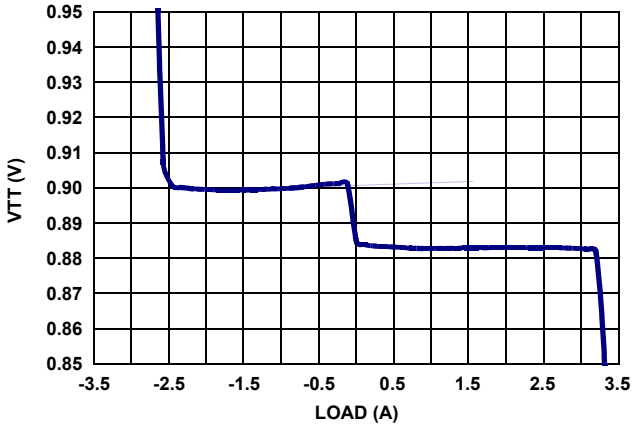



FIGURE 8. VTT REGULATION vs VTT LOAD

## *Typical Operating Characteristics*

$V_{IN}$ = 12V, $V_{DDQ}$ = 1.8V, $t_{ON}$ = GND, SKIP# = $AV_{DD}$, circuit of Figure 29, $T_A$ = +25°C, unless otherwise noted. **(Continued)**

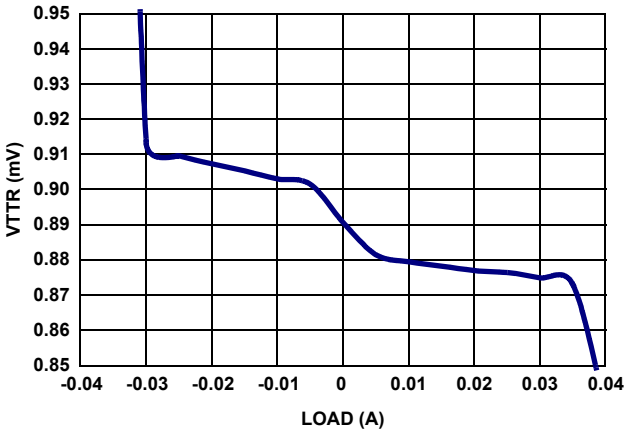
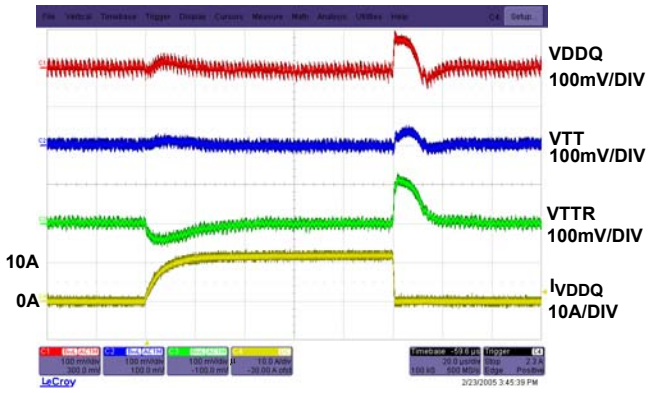



FIGURE 9. VTTR REGULATION vs VTTR LOAD

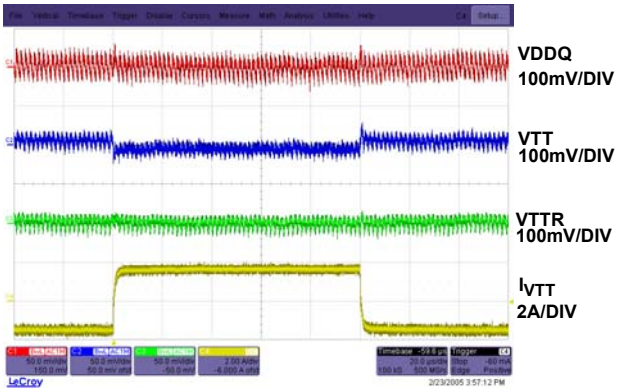
$I_{VTT}$ = 1.5A, $I_{VTTR}$ = 15mA




20µs/DIV

FIGURE 10. LOAD TRANSIENT (VDDQ)

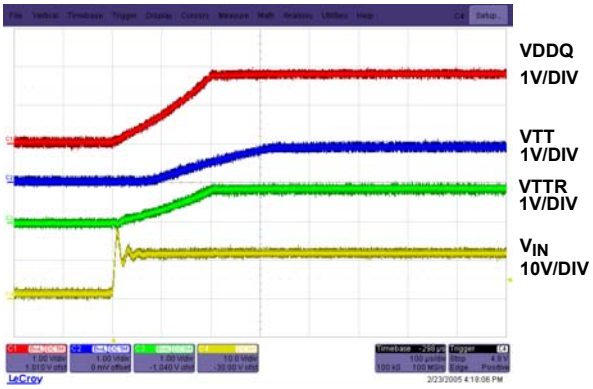
$I_{VDDQ}$ = 12A, $I_{VTTR}$ = 15mA




20µs/DIV

FIGURE 11. LOAD TRANSIENT (VTT -1.5A TO 1.5A)

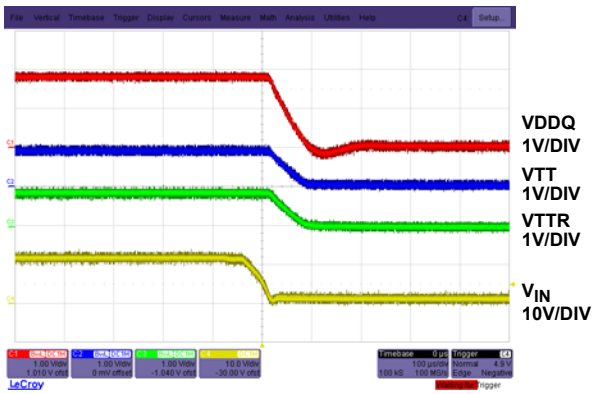
$V_{DD}$ = 5V, $I_{VDDQ}$ = 12A, $I_{VTT}$ = 1.5A, $I_{VTTR}$ = 15mA




100µs/DIV

FIGURE 12. POWER-UP WAVEFORMS

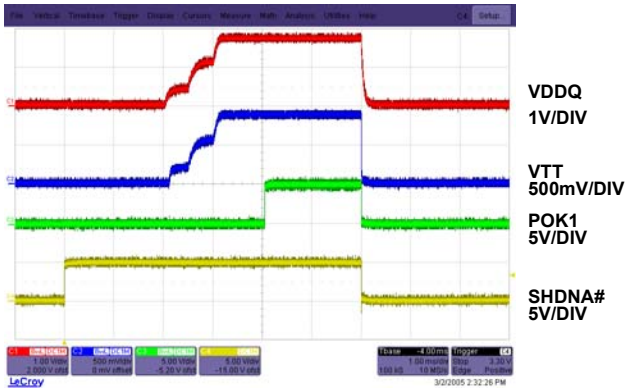
$V_{DD}$ = 5V, $I_{VDDQ}$ = 12A, $I_{VTT}$ = 1.5A, $I_{VTTR}$ = 15mA




100µs/DIV

FIGURE 13. POWER-DOWN WAVEFORMS

$I_{VDDQ}$ = 12A, $I_{VTT}$ = 1.5A




1ms/DIV

FIGURE 14. VDDQ START-UP AND SHUTDOWN INTO HEAVY LOAD, DISCHARGE DISABLED

## *Typical Operating Characteristics*

$V_{IN}$ = 12V, $V_{DDQ}$ = 1.8V, $t_{ON}$ = GND, SKIP# = $AV_{DD}$, circuit of Figure 29, $T_A$ = +25°C, unless otherwise noted. **(Continued)**

$R_{VDDQ}$ = 10Ω, $R_{VTT}$ = 20Ω

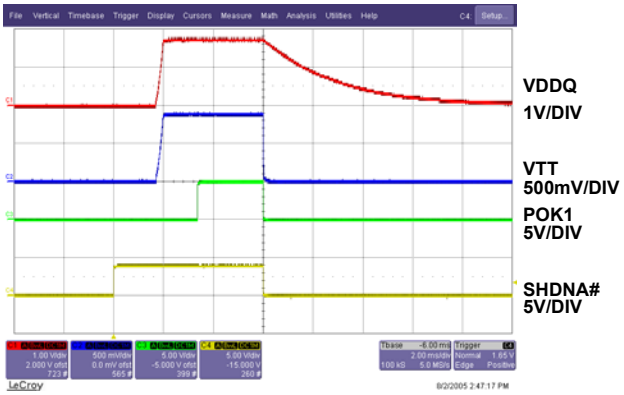



FIGURE 15. VDDQ START-UP AND SHUTDOWN INTO LIGHT LOAD, DISCHARGE ENABLED

$I_{VTT}$ = 1.5A, $I_{VTTR}$ = 15mA

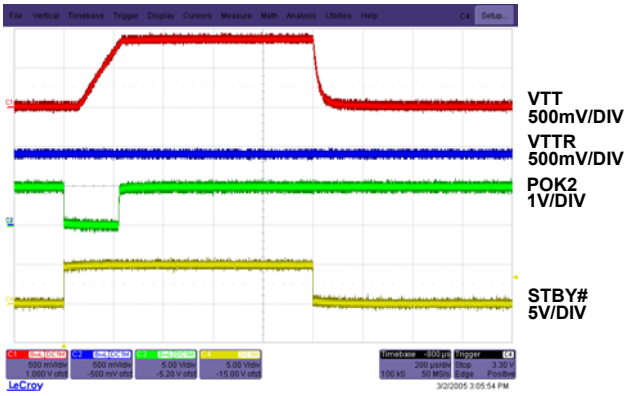



FIGURE 16. VTT, VTTR START-UP AND SHUTDOWN

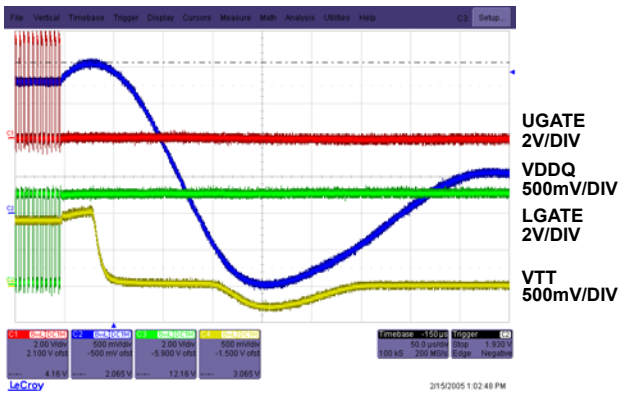



FIGURE 17. OVERVOLTAGE AND TURN-OFF OF BUCK OUTPUT

UVP DISABLE, FOLDBACK CURRENT LIMIT

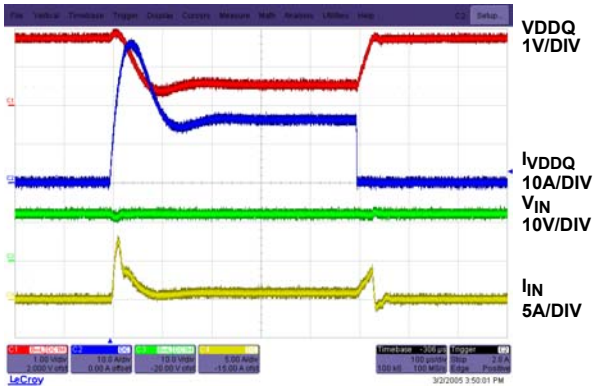



FIGURE 18. SHORT CIRCUIT AND RECOVERY OF VDDQ

UVP ENABLE

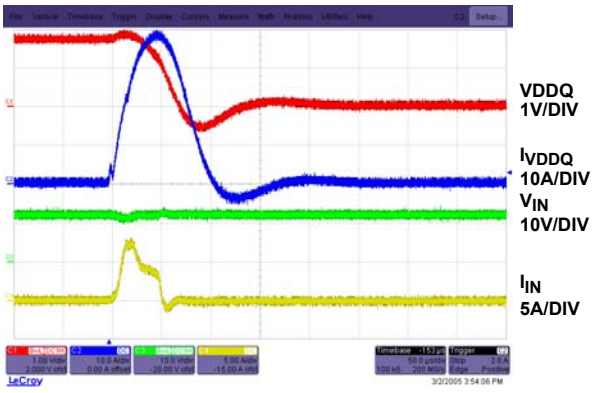



FIGURE 19. SHORT CIRCUIT AND RECOVERY OF VDDQ

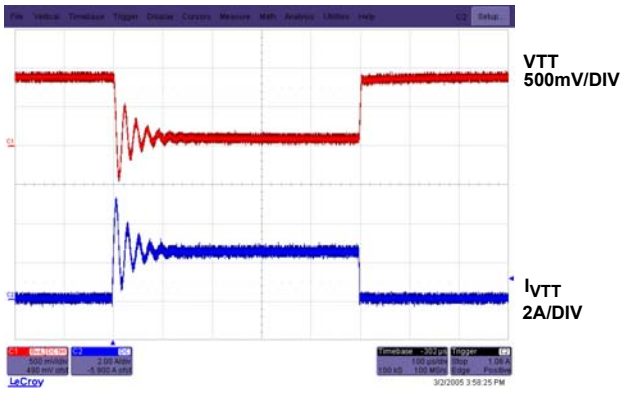



FIGURE 20. SHORT CIRCUIT AND RECOVERY OF VTT

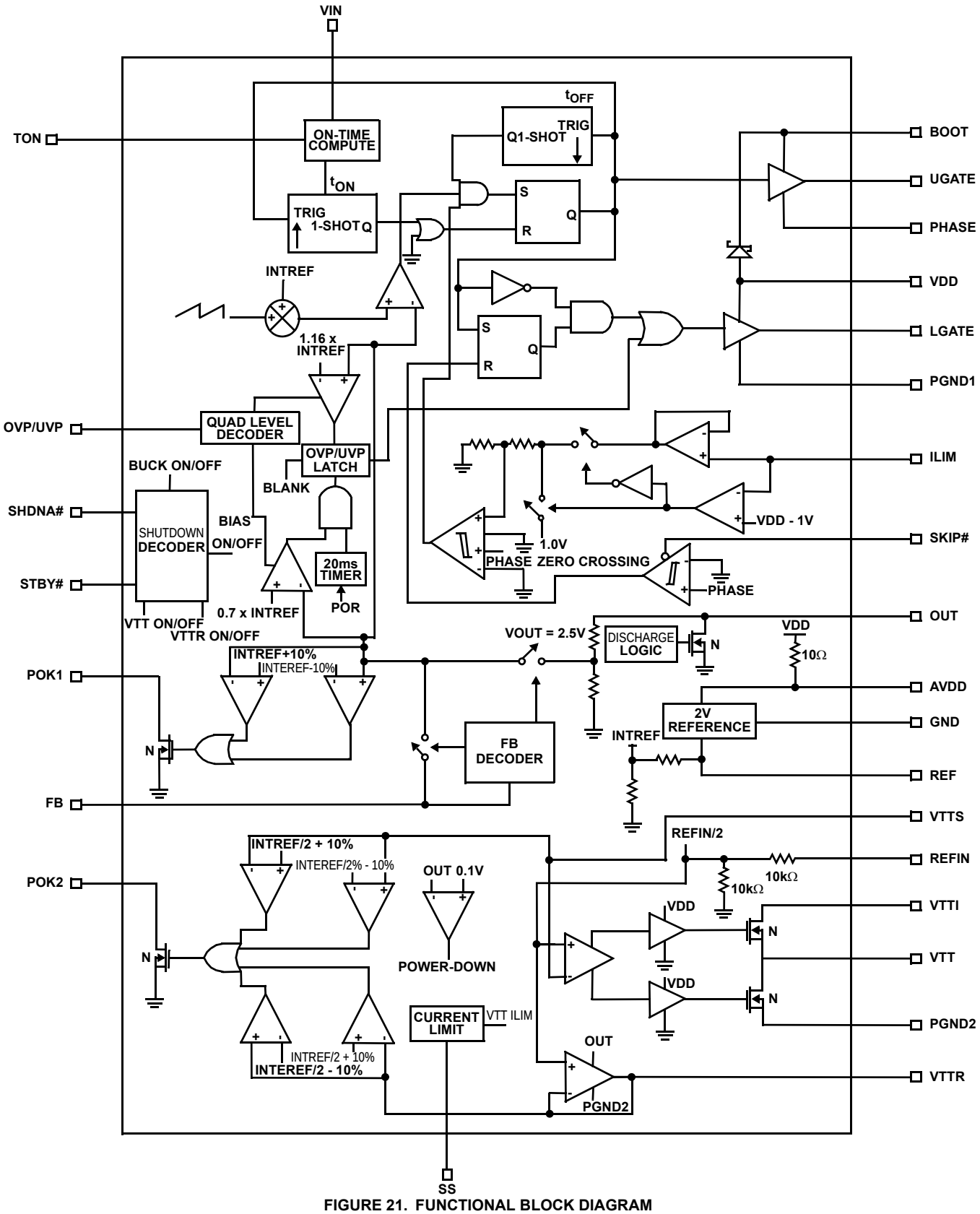



FIGURE 21. FUNCTIONAL BLOCK DIAGRAM

## Detailed Description

The ISL88550A combines a synchronous buck PWM controller, an LDO linear regulator, and a 10mA reference output. The buck controller drives two external N-Channel MOSFETs to deliver load currents up to 15A and generates voltages down to 0.7V from a +2V to +25V input. The LDO Linear Regulator can source up to 2.5A and sink up to -2.0A continuously. These features make the ISL88550A ideally suited for DDR memory application.

The ISL88550A buck regulator is equipped with a fixed switching frequency up to 600kHz constant on-time PWM architecture. This control scheme handles wide input/output voltage ratios with ease, and provides 100ns “instant-on” response to load transients while maintaining high efficiency with relatively constant switching frequency.

The buck controller (LDO) and buffered reference output are provided with independent current limits. Lossless fold-back current limit in the buck regulator is achieved by monitoring the drain to source voltage drop of the low side FET. The ILIM input is used to adjust this current limit. Overvoltage protection is achieved by latching the low side synchronous FET on and the high side FET off when the output voltage is over 116% of its set output. It also features an optional undervoltage protection by latching the MOSFET drivers to the OFF state during an overcurrent condition when the output voltage is lower than 70% of the regulated output. Once the overcurrent condition is removed, the regulator is allowed to soft-start again. This helps minimize power dissipation during a short circuit condition.

The current limit in the LDO and buffered reference output is +3.0A/-2.5A and ±40mA respectively and neither have the overvoltage or undervoltage protection. When the current limit in either output is reached, the output no longer regulates the voltage, but will regulate the current to the value of the current limit.

### +5V Bias Supply ($V_{DD}$ and $AV_{DD}$)

The ISL88550A requires an external +5V bias supply in addition to the input voltage ($V_{IN}$). Keeping the bias supply external to the IC improves the efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and the gate drivers. $V_{DD}$, $AV_{DD}$ and $V_{IN}$ can be connected together if the input source is a fixed +4.5V to +5.5V supply.

$V_{DD}$ is the supply input for the Buck regulator’s MOSFET drivers, and $AV_{DD}$ supplies the power for the rest of the IC. The current from the $AV_{DD}$ and $V_{DD}$ power supply must supply the current for the IC and the gate drive for the MOSFET’s. This maximim current can be estimated in Equation 1:

$$I_{BIAS} = I_{VDD} + I_{AVDD} + f_{SW} x (Q_{G1} + Q_{G2}) \quad \text{(EQ. 1)}$$

Where $I_{VDD}$ + $I_{AVDD}$ are the quiescent supply currents into $V_{DD}$; $AV_{DD}$, $Q_{G1}$ and $Q_{G2}$ are the total gate charges of MOSFETs $Q_1$ and $Q_2$ (at $V_{GS}$ = 5V) in the "Typical Application Circuit" on page 22, and $f_{SW}$ is the switching frequency.

### Free-Running Constant-ON-Time PWM

The constant ON-time PWM control architecture is a pseudo fixed frequency, constant on-time, current-mode regulator with voltage feed forward (Figure 21). This architecture relies on the output filter capacitor’s ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch ON-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to the output voltage. Another one-shot sets a minimum off-time of 300ns typically. The ON-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

### ON-Time One Shot ($t_{ON}$)

The heart of the PWM core is the one-shot that sets the high-side switch ON-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the ON-time in response to input and output voltages. The high-side switch ON-time is inversely proportional to the input voltage ($V_{IN}$) and is proportional to the output voltage, as shown in Equation 2:

$$t_{on} = K \times \frac{\left(V_{OUT} + I_{LOAD} \times r_{DS(ON)Q2}\right)}{V_{IN}} \quad \text{(EQ. 2)}$$

where K (the ON-time scale factor) is set by the $t_{ON}$ input connection (Table 1) and $r_{DS(ON)Q2}$ is the ON-resistance of the synchronous rectifier ($Q_2$) in the "Typical Application Circuit" on page 22. This algorithm results in a nearly constant switching frequency despite the lack of a fixed frequency clock generator. The benefits of a constant switching frequency are two-fold:

1. The frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band.
2. The inductor ripple-current operating point remains relatively constant, resulting in an easy design methodology and predictable output voltage ripple.

The ON-time one-shot has good accuracy at the operating points specified in the “Electrical Specifications” table (approximately ±12.5% at 600kHz and 450kHz and ±10% at 200kHz and 300kHz) on page 3. ON-times at operating points far removed from the conditions specified in the “Electrical Specifications” table on page 3 can vary over a wider range. For example, the 600kHz setting typically runs approximately 10% slower with inputs much greater than 5V due to the very short ON-times required.

The constant ON-time translates only roughly to a constant switching frequency. The ON-times guaranteed in the “Electrical Specifications” table on page 3 are influenced by resistive losses and by switching delays in the high-side MOSFET. Resistive losses, which include the inductor, both MOSFETs, the output capacitors ESR, and any PC board

copper losses in the output and ground, tend to raise the switching frequency as the load increases. The dead-time effect increases the effective ON-time, reducing the switching frequency as one or both dead times are added to the effective ON-time. The dead time occurs only in PWM mode (SKIP# = $V_{DD}$) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes PHASE to go high earlier than normal, extending the ON-time by a period equal to the UGATE-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is shown in Equation 3:

$$f_{SW} = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})} \quad \text{(EQ. 3)}$$

where $V_{DROP1}$ is the sum of the parasitic voltage drops in the inductor discharge path, including the synchronous rectifier, the inductor, and any PC board resistances; $V_{DROP2}$ is the sum of the resistances in the charging path, including the high-side switch ($Q_1$ in "Typical Application Circuit" on page 22), the inductor and any PC board resistances, and $t_{ON}$ is the one-shot on-time (see "ON-Time One Shot ($t_{ON}$)" on page 12).

### *Automatic Pulse-Skipping Mode (SKIP# = GND)*

In skip mode, (SKIP# = GND), an inherent automatic switchover to PFM takes place at light loads (Figure 22). This switchover is affected by a comparator that truncates the low-side switch ON-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the synchronous rectifier MOSFET ($Q_2$ in "Typical Application Circuit" on page 22). Once $V_{PGND}$ - PHASE drops below 5% of the current-limit threshold (3mV for the default 50mV current-limit threshold), the comparator forces LGATE low (see "Functional Block Diagram" on page 11, Figure 21). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to one-half the peak-to-peak ripple current, which is a function of the inductor value (see Figure 22). This threshold is relatively constant, with only a minor dependence on the input voltage ($V_{IN}$).

$$I_{LOAD(SKIP)} = \left(\frac{V_{OUT} \times K}{2L}\right)\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \quad \text{(EQ. 4)}$$

where K is the ON-time scale factor (see Table 1). For example, in the "Typical Applications Circuit" on page 22 (K =1.7µs, $V_{OUT}$ = 2.5V, $V_{IN}$ = 12V, and L = 1µH), the pulse-skipping switchover occurs in Equation 5:

$$\left(\frac{2.5V \times 1.7\mu s}{2 \times 1\mu H}\right)\left(\frac{12V - 2.5V}{12V}\right) = 1.68A \quad \text{(EQ. 5)}$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used. The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs light-load efficiency are made by selection of inductor value. Generally, low inductor values produce a broader efficiency vs load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed), and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input voltage levels.

DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the ISL88550A regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction (SKIP# = GND and $I_{LOAD} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error comparator threshold by approximately 1.5% due to slope compensation.

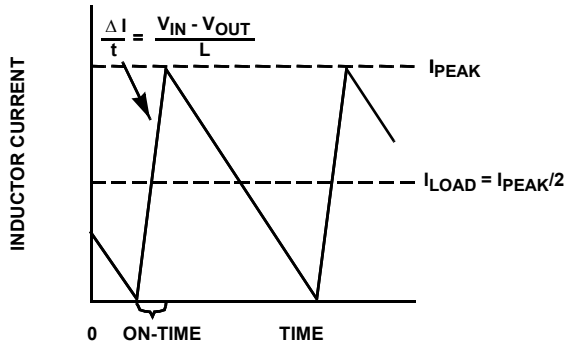



**FIGURE 22. PULSE SKIPPING/DISCONTINUOUS CROSSOVER POINT**

**TABLE 1. APPROXIMATE K-FACTOR ERRORS**

| $t_{ON}$ SETTING | TYPICAL K FACTOR (µs) | K-FACTOR ERROR (10%) | MINIMUM $V_{IN}$ AT $V_{OUT}$ = 2.5V (h = 1.5, SEE DROPOUT PERFORMANCE SECTION) | TYPICAL APPLICATION | COMMENTS |
|---|---|---|---|---|---|
| 200kHz ($t_{ON}$ = $AV_{DD}$) | 5.0 | ±10 | 3.15 | 4-Cell Li+ Notebook | Use for absolute best efficiency |
| 300kHz ($t_{ON}$ = OPEN) | 3.3 | ±10 | 3.47 | 4-Cell Li+ Notebook | Considered mainstream by current standards |
| 450kHz ($t_{ON}$ = REF) | 2.2 | ±12.5 | 4.13 | 3-Cell Li+ Notebook | Useful in 3-cell systems for lighter loads |
| 600kHz ($t_{ON}$ = GND) | 1.7 | ±12.5 | 5.61 | +5V input | Good operating point for compound buck designs or desktop circuits. |

### *Force PWM Mode (SKIP# = $AV_{DD}$)*

The low-noise forced-PWM mode (SKIP# = $AV_{DD}$) disables the zero-crossing comparator, which controls the low-side switch ON-time. This forces the low-side gate drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while UGATE maintains a duty factor of $V_{OUT}/V_{IN}$. Forced-PWM mode keeps the switching frequency fairly constant. However, forced-PWM operation comes at a cost where the no-load $V_{DD}$ bias current remains between 2mA and 20mA due to the external MOSFETs gate charge and switching frequency. Forced-PWM mode is most useful for reducing audio frequency noise, improving load-transient response, and providing sink current capability for dynamic output voltage adjustment.

### *Current Limit Buck Regulator (ILIM)*

#### VALLEY CURRENT LIMIT

The current-limit circuit for the Buck Regulator portion of the ISL88550A employs a unique “valley” current sensing algorithm that senses the voltage drop across PHASE and PGND1 and uses the ON-resistance of the rectifying MOSFET ($Q_2$ in the "Typical Application Circuit" on page 22) as the current sensing element. If the magnitude of the current sense signal is above the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle (Figure 23). With Valley Current Limit sensing, the actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor current ripple. Therefore, the exact current limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value and input voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the ISL88550A also implements a negative current limit to prevent excessive reverse inductor currents when the Buck Regulator output is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when $V_{ILIM}$ is adjusted. The current-limit threshold is adjusted with an external resistor-divider at ILIM. A 2µA to 20µA divider current is recommended for accuracy and noise immunity.

The current-limit threshold adjustment range is from 25mV to 200mV. In the adjustable mode, the current limit threshold voltage (from PHASE to PGND1) is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 50mV when ILIM is connected to $AV_{DD}$. The logic threshold for switchover to the 50mV default value is approximately $AV_{DD}$ - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen between PHASE and PGND1.

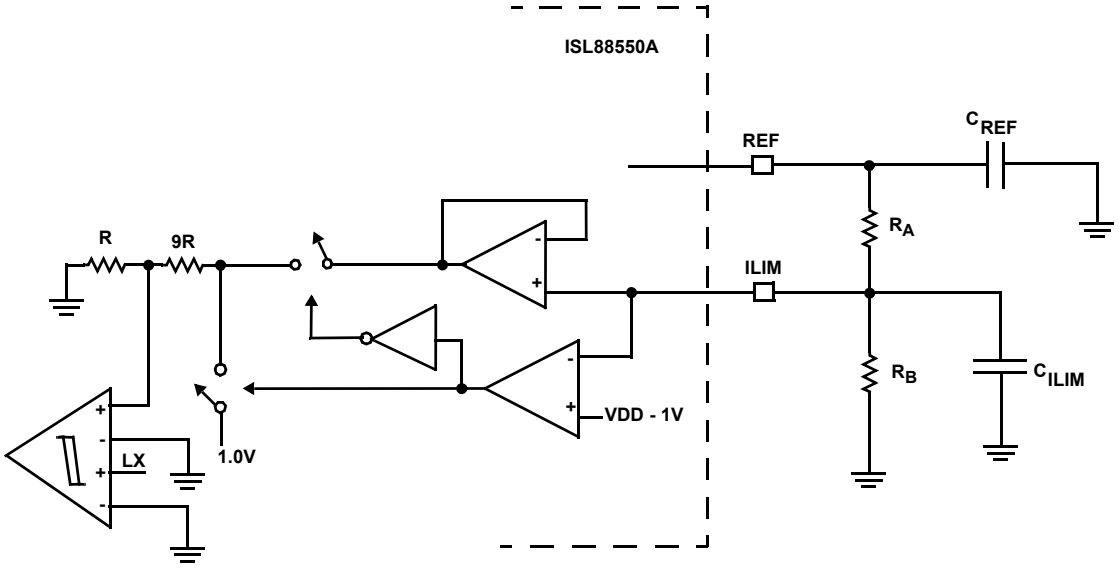



FIGURE 23. ADJUSTABLE CURRENT LIMIT THRESHOLD

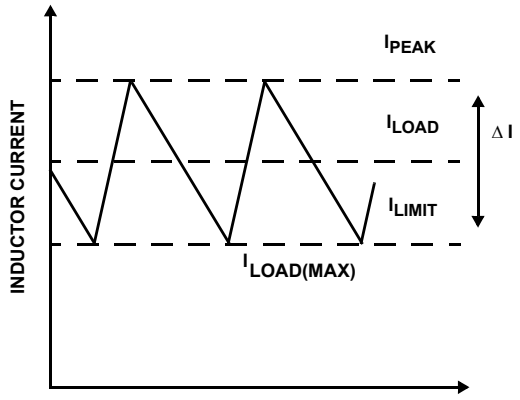



FIGURE 24. VALLEY CURRENT-LIMIT THRESHOLD

### *POR, UVLO and Soft-Start*

Internal Power-on reset (POR) occurs when $AV_{DD}$ rises above approximately 2V, resetting the fault latch and the soft-start counter, powering up the reference and preparing the Buck Regulator for operation. Until $AV_{DD}$ reaches 4.25V (typical), $AV_{DD}$ undervoltage lockout (UVLO) circuitry inhibits switching. The controller inhibits switching by pulling UGATE low and holding LGATE low when OVP and shutdown discharge are disabled (OVP/UVP = REF or GND) or forcing LGATE high when OVP and shutdown discharge are enabled (OVP/UVP = $AV_{DD}$ or OPEN). See Table 3 for detailed truth table for OVP/UVP and Shutdown settings.

When $AV_{DD}$ rises above 4.25V, the controller activates the Buck Regulator and initializes the internal soft-start. The Buck Regulator's internal soft-start allows a gradual increase of the current limit level during start-up to reduce the input surge currents. The ISL88550A divides the soft-start period into five phases. During the first phase, the controller limits the current limit to only 20% of the full current limit. If the output does not reach regulation within 425µs, soft-start enters the second phase and the current limit is increased by another 20%. This process repeats until the maximum current limit is reached after 1.7ms, or when the output reaches the nominal regulation voltage, whichever occurs first. Adding a capacitor in parallel with the external ILIM resistors creates a continuously adjustable analog soft-start function for the Buck Regulator's output.

For most applications, LDO soft-start is not necessary because output charging current is limited to approximately 3.0A. For 20µF LDO output capacitors, the minimum rise time is about 30µs. However, soft-start in the LDO section can be realized by tying a capacitor between the SS pin and GND. When STBY# is driven low, or during thermal shutdown of the LDO's, the SS capacitor is discharged. When STBY# is driven high or when the thermal limit is removed, an internal 4µA (typical) current charges the SS capacitor. The resulting linear ramp voltage on SS linearly increases the current-limit comparator thresholds to both the VTT and VTTR outputs until full current limit is attained when SS reaches approximately 1.6V. This lowering of the current limit during start-up limits the initial in-rush current peaks, particularly when driving higher output capacitances. For good tracking, choose the value of the SS capacitor less than 390pF. Leave SS floating to disable the soft-start feature.

### *Power OK (POK1)*

POK1 is an open-drain output for a window comparator that continuously monitors $V_{OUT}$. POK1 is actively held low when SHDNA# is low and during the Buck Regulator outputs soft-start. After the digital soft-start terminates, POK1 becomes high impedance as long as the output voltage is within ±10% of the nominal regulation voltage set by FB. When $V_{OUT}$ drops 10% below or rises 10% above the nominal regulation voltage, the ISL88550A pulls POK1 low. Any fault condition forces

POK1 low until the fault latch is cleared by toggling SHDNA# or cycling $AV_{DD}$ power below 1V. For logic level output voltages, connect an external pull-up resistor between POK1 and $AV_{DD}$. A 100kΩ resistor works well in most applications. Note that the POK1 window detector is completely independent of the overvoltage and undervoltage protection fault detectors and the state of VTTS and VTTR.

### *SHDNA# and Output Discharge*

The SHDNA# input corresponds to the Buck Regulator and places the Buck Regulator's portion of the IC in a low power mode (see "Electrical Specifications" table on page 3). SHDNA# is also used to reset a fault signal such as an overvoltage or undervoltage fault.

When output discharge is enabled (OVP/UVP = $AV_{DD}$ or open) and SHDNA# is pulled low, or if UVP is enabled (OVP/UVP = $AV_{DD}$) and $V_{OUT}$ falls to 70% of its regulation set point, the ISL88550A discharges the Buck Regulator output (via the OUT input) through an internal 15Ω switch to ground. While the output is discharging, the PWM controller is disabled, but the reference remains active to provide an accurate threshold.

When output discharge is disabled (OVP/UVP = REF or GND), the controller does not actively discharge the Buck Output. Under these conditions, the Buck Output discharge rate is determined by the load current and its output capacitance. The Buck Regulator detects and latches the discharge mode state set by OVP/UVP setting on start-up.

### *STBY#*

The STBY# input is an active low input that is used to shutdown only the VTT output. When STBY# is low, VTT is high impedance, but the VTTR output is still active if SHDNA# is high. VTT and VTTR are pulled to 0V when SHDNA is low.

**TABLE 2. SHUTDOWN AND STANDBY CONTROL LOGIC**

| SHDNA# | STBY# | BUCK OUTPUT | VTT | VTTR |
|---|---|---|---|---|
| GND | X | OFF | OFF (Discharge to 0V) | OFF (Tracking ½ REFIN) |
| $AV_{DD}$ | GND | ON | OFF (High Impedance) | ON |
| $AV_{DD}$ | $AV_{DD}$ | ON | ON | ON |

### *Power OK (POK2)*

POK2 is the open-drain output for a window comparator that continuously monitors the VTTS input and VTTR output. POK2 is high impedance as long as the output voltage is within ±10% of the nominal regulation voltage as set by REFIN. When $V_{VTTS}$ or $V_{VTTR}$ rise 10% above or 10% below their nominal regulation voltage, the ISL88550A pulls POK2 low. For logic level output voltages, connect an external pull-up resistor between POK2 and $AV_{DD}$. A 100kΩ resistor works well in most applications. Note that the POK2 window detector is completely independent of the overvoltage and undervoltage protection fault detectors and the state of VDDQ.

### *Current Limit (LDO for VTT and VTTR Buffer)*

The VTT output is a linear regulator that regulates the input (VTTI) to ½ the $V_{REFIN}$ voltage. The feedback point for VTT is at the VTTS input (see Figure 21). VTT is capable of sourcing up to 2.5A and sinking up to -2.0A continuously. The current limit for VTT and VTTR is typically +3.0A/-2.5A and ±40mA respectively. When the current limit for either output is reached, the outputs regulate the current not the voltage. The current limits for both VTT and VTTR can be reduced from their full values by forcing the voltage at the SS pin below 1.6V (typical), or by tying a resistor ($R_{SS}$) between the SS pin and ground such that $4\mu A * R_{SS}$ is less than 1.6V. POK2 is pulled low when REFIN is <0.8V.

## *Fault Protection*

The ISL88550A provides overvoltage/undervoltage fault protection in the buck controller. Select OVP/UVP to enable and disable fault protection as shown in Table 3. Once activated, the controller continuously monitors the output for undervoltage and overvoltage fault conditions. Any VDDQ shutdown due to OVP, UVP, OTP or SHDNA# = 0 should also discharge VTT to 0V.

### *Overvoltage Protection (OVP)*

When the output voltage rises above 114% of the nominal regulation voltage and OVP is enabled (OVP/UVP = AVDD or open), the OVP circuit sets the fault latch, shuts down the PWM controller and immediately pulls UGATE low and forces LGATE high. This turns on the synchronous rectifier MOSFET with 100% duty cycle, rapidly discharging the output capacitor and clamping the output to ground. Note that immediately latching LGATE high can cause the output voltage to go slightly negative due to energy stored in the output LC circuit at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp. Toggle SHDNA# or cycle AVDD power below 1V to clear the fault latch and restart the controller. OVP is disabled when OVP/UVP is connected to REF or GND (see Table 3). OVP only applies to the Buck Output. The VTT and VTTR Outputs do not have overvoltage protection. When VDDQ is discharged to 0V due to OVP, VTT is also discharged to 0V.

**TABLE 3. OVP/UVP FAULT PROTECTION**

| OVP/UVP | DISCHARGE | UVP PROTECTION | OVP PROTECTION |
|---|---|---|---|
| $AV_{DD}$ | 15Ω internal switch ON<br>UGATE/LGATE is low when SHDNA# = low for normal shutdown | Enabled | Enabled.<br>UGATE pulled low and LGATE forced high if OVP detected |

**TABLE 3. OVP/UVP FAULT PROTECTION**

| OVP/UVP | DISCHARGE | UVP PROTECTION | OVP PROTECTION |
|---|---|---|---|
| OPEN | 15Ω internal switch ON<br>UGATE/LGATE is low when SHDNA# = low for normal shutdown | Disabled | Enabled.<br>UGATE pulled low and LGATE forced high if OVP detected |
| REF | 15Ω internal switch OFF<br>UGATE/LGATE is low when SHDNA# = low | Enabled | Disabled |
| GND | 15Ω internal switch OFF<br>UGATE/LGATE is low when SHDNA# = low | Disabled | Disabled |

### *Undervoltage Protection (UVP)*

When the output voltage drops below 70% of its regulation voltage and UVP is enabled (OVP/UVP = $AV_{DD}$ or REF), the controller sets the fault latch and begins the discharge mode (see “SHDNA# and Output Discharge” on page 16). UVP is ignored for 14ms (minimum) after start-up or after a rising edge on SHDNA#. Toggle SHDNA# or cycle $AV_{DD}$ power below 1V to clear the fault latch and restart the controller. UVP is disabled when OVP/UVP is left open or connected to GND (see Table 3). UVP only applies to the Buck Output. The VTT and VTTR Outputs do not have undervoltage protection. When VDDQ is discharged to 0V due to UVP, VTT is also discharged to 0V.

### *Thermal Fault Protection*

The ISL88550A features a thermal fault protection circuit, which monitors the Buck Regulator of the IC, the Linear Regulator (VTT) and the buffered output (VTTR). When the junction temperature of the ISL88550A rises above +150°C, a thermal sensor activates the fault latch, pulls POK1 low and shuts down the buck converter using discharge mode regardless of the OVP/UVP setting, and VTT is also discharged to 0V. Toggle SHDNA# or cycle $AV_{DD}$ power below 1V to reactivate the controller after the junction temperature cools by +15°C.

## *Design Procedure*

Firmly establish the input voltage range ($V_{IN}$) and maximum load current in the buck regulator before choosing a switching frequency and inductor operating point (ripple-current ratio or LIR). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design.

### *Input Voltage Range*

The maximum value (VIN (MAX)) must accommodate the worst-case, high AC adapter voltage. The minimum value (VIN (MIN)) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice, lower input voltages result in better efficiency.

### *Maximum Load Current*

There are two values to consider. The peak load current ($I_{PEAK}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current ($I_{LOAD}$) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

### *Switching Frequency*

This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses proportional to frequency and $VIN^2$. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

### *Inductor Operating Point*

This choice provides trade-offs: size vs efficiency and transient response vs output ripple. Low inductor values provide better transient response and smaller physical size but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping (SKIP# = low at light loads), the inductor value also determines the load current value at which PFM/PWM switchover occurs.

## *Setting the Output Voltage (Buck)*

### *Preset Output Voltages*

The ISL88550A allows the selection of common voltages without requiring external components (Figure 25). Connect FB to GND for a fixed 2.5V output, or connect FB directly to OUT for a fixed 0.7V output.

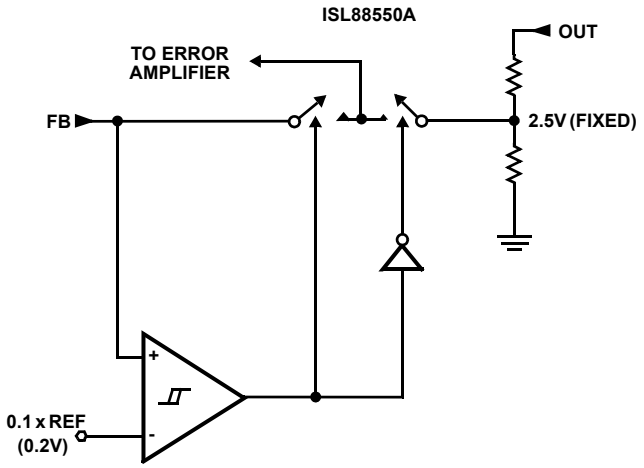



FIGURE 25. DUAL-MODE FEEDBACK DECODER

### *Setting the Buck Regulator Output ($V_{OUT}$) with a Resistive Voltage-Divider at FB*

The Buck Regulator output voltage can be adjusted from 0.7V to 3.5V using a resistive voltage-divider (Figure 26). The ISL88550A regulates FB to a fixed reference voltage (0.7V). The adjusted output voltage is shown in Equation 6:

$$V_{OUT} = V_{FB}\left(1+\frac{R_C}{R_D}\right)+\frac{V_{RIPPLE}}{2} \quad \text{(EQ. 6)}$$

Where VFB is 0.7V and Equation 7 is:

$$V_{RIPPLE} = LIR \times I_{LOAD} \times R_{ESR} \quad \text{(EQ. 7)}$$

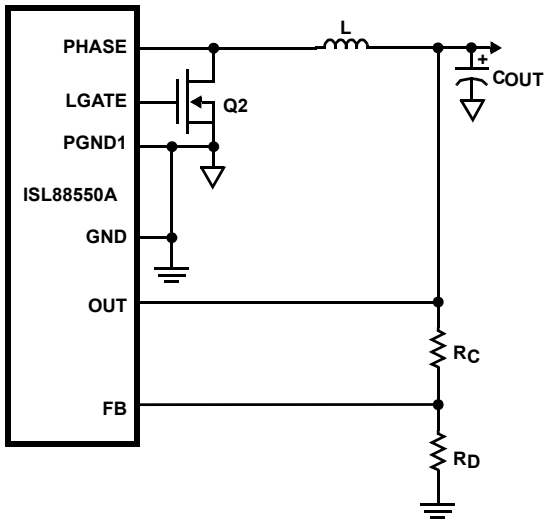



FIGURE 26. SETTING $V_{OUT}$ WTH A RESISTIVE VOLTAGE DIVIDER

### *Setting the VTT and VTTR Voltages (LDO)*

The Termination Power Supply Output (VTT) can be set by two different methods. First, the VTT output can be connected directly to the VTTS input to force VTT to regulate to $V_{REFIN}/2$. Second, VTT can be forced to regulate higher than $V_{REFIN}/2$ by connecting a resistive divider from VTT to VTTS.

For cases where resistor divider programming is desired, a special set of equations must be used to determine the proper resistance values:

$$R_1 = \frac{V_{TT} \cdot K_{VTOL}}{6\times10^{-4}} \quad \text{(EQ. 8)}$$

$$R_2 = R_1 \cdot \frac{\frac{REFIN}{2}}{(2\times10^{-5} \cdot R_1) + V_{TT} - \frac{REFIN}{2}} \quad \text{(EQ. 9)}$$

Where KVTOL is the desired accuracy of the VTT voltage in percent (e.g. - for 0.5%, KVTOL = 0.5).

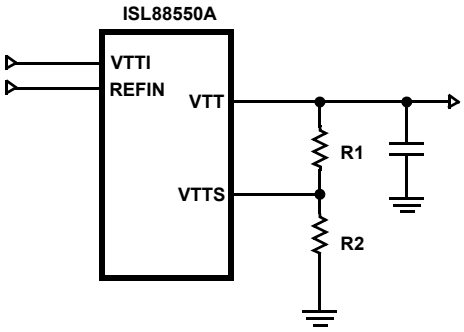



FIGURE 27. RESISTOR DIVIDER PROGRAMMING OF VTT LDO

The maximum value for VTT will be the $V_{VTTI}$ - $V_{DROPOUT}$ where $V_{DROPOUT} = I_{VTT} \times 0.3$ typically.

The Termination Reference Voltage (VTTR) will follow ½ $V_{REFIN}$.

### *Inductor Selection (Buck)*

The switching frequency and inductor operating point determine the inductor value, as shown in Equation 10:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR} \quad \text{(EQ. 10)}$$

For example: $I_{LOAD(MAX)}$ = 12A, $V_{IN}$ = 12V, $V_{OUT}$ = 2.5V, $f_{SW}$ = 300kHz, 30% ripple current or LIR = 0.3, as shown in Equation 11.

$$L = \frac{2.5V(12V - 2.5V)}{12V \times 300kHz \times 12A \times 0.3} = 1.8\mu H \quad \text{(EQ. 11)}$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current ($I_{PEAK}$) as shown in Equation 12:

$$I_{PEAK} = I_{LOAD(MAX)}\left(1+\frac{LIR}{2}\right) \quad \text{(EQ. 12)}$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

### *Input Capacitor Selection (Buck)*

The input capacitor must meet the ripple current requirement ($I_{RMS}$) imposed by the switching currents in Equation 13:

$$I_{RMS} = I_{LOAD}\sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad \text{(EQ. 13)}$$

For most applications, non-tantalum chemistry capacitors (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the ISL88550A are operated as the second stage of a two-stage power conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than +10°C temperature rise at the RMS input current for optimal reliability and lifetime.

### *Output Capacitor Selection (Buck)*

The output filter capacitor must have low enough equivalent series resistance ($R_{ESR}$) to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. For processor core voltage converters and other applications in which the output is subject to violent load transients, the output capacitor's size depends on how much $R_{ESR}$ is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance in Equation 14:

$$R_{ESR} \leq \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}} \quad \text{(EQ. 14)}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much $R_{ESR}$ is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller is approximately equal to the total inductor ripple current multiplied by the output capacitor's $R_{ESR}$. Therefore, the maximum $R_{ESR}$ required to meet ripple specifications is shown in Equation 15:

$$R_{ESR} \leq \frac{V_{RIPPLE}}{I_{LOAD(MAX)} \times LIR} \quad \text{(EQ. 15)}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OSCONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent $V_{SAG}$ and $V_{SOAR}$ from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the $V_{SAG}$ and $V_{SOAR}$ equations in "Transient Response (Buck)" on page 22).

### *VTT Output Capacitor Selection (LDO)*

Place 2µFx10µF 0805 ceramic capacitor as close to VTT output as possible for optimum performance of output loading up to +2.5A/-2.0A. In most applications, it is not necessary to add more capacitance. However, optional additional capacitances can be added further away (>1.5") from VTT output.

### *VTTR Output Capacitor Selection (LDO)*

The VTTR buffer is a scaled down version of the VTT regulator with much smaller output transconductance. Its compensation capacitor can therefore be smaller, and its ESR larger than what is required for its larger counterpart. For typical applications requiring load current up to ±20mA, a ceramic capacitor with a minimum value of 1µF is recommended (ESR <0.3Ω). Tie this capacitor between VTTR and analog ground plane.

### *VTTI Input Capacitor Selection (LDO)*

Both the VTT and VTTR output stages are powered from the same VTTI input. Their output voltages are referenced to the same REFIN input. The value of the VTTI bypass capacitor is chosen to limit the amount of ripple/noise at VTTI, or the amount of voltage dip during a load transient. Typically, a ceramic capacitor of at least 10µF should be used. This value is to be increased with larger load current, or if the trace from the VTTI pin to the power source is long and has significant impedance. Furthermore, to prevent undesirable VTTI bounce from coupling back to the REFIN input and possibly causing instability in the loop, the REFIN pin should ideally tap its signal from a separate low impedance DC source rather than directly to the VTTI input. If the latter is unavoidable, increase the amount of bypass at the VTTI input and add additional bypass at the REFIN pin.

### *MOSFET Selection (Buck)*

The ISL88550A drive external, logic-level, N-Channel MOSFETs as the circuit-switch elements. The key selection parameters are as follows:

**Maximum Drain-To-Source Voltage ($V_{DSS}$):** Should be at least 20% higher than input supply rail at the high side MOSFET's drain.

Choose the MOSFETs with rated $r_{DS(ON)}$ at $V_{GS}$ = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has a conduction loss equal to switching loss at nominal input voltage and maximum output current. For low-side MOSFET, make sure that it does not spuriously turn on because of dV/dt caused by high-side MOSFET turning on, as this would result in shoot through

current degrading the efficiency. MOSFETs with a lower $Q_{GD}$ to $Q_{GS}$ ratio have higher immunity to dV/dt.

For proper thermal-management design, calculate the power dissipation at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for low-side MOSFET, worst case is at $V_{IN(MAX)}$; for high-side MOSFET, it could be either at $V_{IN(MIN)}$ or $V_{IN(MAX)}$). The high-side MOSFET and low-side MOSFET have different loss components due to the circuit operation. The low-side MOSFET operates as a zero voltage switch; therefore, major losses are:

1. The channel conduction loss ($P_{LSCC}$)
2. The body diode conduction loss ($P_{LSDC}$)
3. The gate-drive loss ($P_{LSDR}$)

$$P_{LSCC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{LOAD}{}^2 \times r_{DS(ON)} \quad \text{(EQ. 16)}$$

$$P_{LSDC} = 2I_{LOAD} \times V_F \times t_{DT} \times f_{SW} \quad \text{(EQ. 17)}$$

where VF is the body-diode forward-voltage drop, $t_{DT}$ is the dead time (~30ns), and $f_{SW}$ is the switching frequency. Because of the zero-voltage switch operation, the low-side MOSFET gate-drive loss occurs as a result of charging and discharging the input capacitance, (CISS). This loss is distributed among the average LGATE driver's pull-up and pull-down resistance, RLGATE (1Ω), and the internal gate resistance (RGATE) of the MOSFET (~2Ω). The driver power dissipated is given by Equation 18:

$$P_{LSDR} = C_{ISS} \times V_{GS}{}^2 \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{LGATE}} \quad \text{(EQ. 18)}$$

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel conduction loss ($P_{HSCC}$), the VI overlapping switching loss ($P_{HSSW}$), and the drive loss ($P_{HSDR}$). The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current:

$$P_{HSCC} = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}{}^2 \times r_{DS(ON)} \quad \text{(EQ. 19)}$$

Use $r_{DS(ON)}$ at $T_{J(MAX)}$.

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_{SW} \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}} \quad \text{(EQ. 20)}$$

where $I_{GATE}$ is the average UGATE driver output-current determined by Equation 21:

$$I_{GATE(ON)} = \frac{2.5V}{R_{UGATE} + R_{GATE}} \quad \text{(EQ. 21)}$$

where $R_{UGATE}$ is the high-side MOSFET driver's ON-resistance (1.5Ω typical) and $R_{GATE}$ is the internal gate resistance of the MOSFET (~2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_{SW} \times \frac{R_{GATE}}{R_{GATE} + R_{UGATE}} \quad \text{(EQ. 22)}$$

where $V_{GS} = V_{DD} = 5V$. In addition to the losses in Equation 22, allow about 20% more for additional losses because of MOSFET output capacitances and low-side MOSFET body-diode reverse recovery charge dissipated in the high-side MOSFET that is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specifications to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipations. To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source, or add resistors in series with UGATE and LGATE to slow down the switching transitions. Adding series resistors increases the power dissipation of the MOSFET, so ensure that this does not overheat the MOSFET.

### *MOSFET Snubber Circuit (Buck)*

Fast switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at PHASE's rising and falling transitions and can interfere with circuit performance and generate EMI. A series R-C snubber may be added across the lower MOSFET to dampen this ringing. Following is the procedure for selecting the value of the series RC circuit:

1. Connect a scope probe to measure PHASE to GND, and observe the ringing frequency, $f_R$.
2. Find the capacitor value (connected from PHASE to GND) that reduces the ringing frequency by half.

The circuit parasitic capacitance ($C_{PAR}$) at PHASE is then equal to 1/3 the value of the added capacitance above. The circuit parasitic inductance ($L_{PAR}$) is calculated using Equation 23:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}} \quad \text{(EQ. 23)}$$

The resistor for critical dampening ($R_{SNUB}$) is equal to $2\pi \times fR \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion. The capacitor ($C_{SNUB}$) should be at least 2x to 4x the value of the $C_{PAR}$ in order to be effective. The power loss of the snubber circuit ($P_{RSNUB}$) is dissipated in the resistor and can be calculated as shown in Equation 24:

$$P_{RSNUB} = C_{SNUB} \times V_{IN}{}^2 \times f_{SW} \quad \text{(EQ. 24)}$$

where $V_{IN}$ is the input voltage and $f_{SW}$ is the switching frequency. Choose an $R_{SNUB}$ power rating that meets the specific application's derating rule for the power dissipation calculated.

### Setting the Current Limit (Buck)

The current-sense method used in the ISL88550A makes use of the ON-resistance ($r_{DS(ON)}$) of the low side MOSFET ($Q_2$ in "Typical Application Circuit" on page 22). When calculating the current limit, use the worst-case maximum value for $r_{DS(ON)}$ from the MOSFET data sheet, and add some margin for the rise in $r_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each +1°C of temperature rise.

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current, as shown in Equation 25:

$$I_{LIM(VAL)} > I_{LOAD(MAX)} - \left(\frac{I_{LOAD(MAX)} \times LIR}{2}\right) \quad \text{(EQ. 25)}$$

where $I_{LIM(VAL)}$ equals the minimum valley current-limit threshold voltage divided by the ON-resistance of $Q_2$ ($r_{DS(ON)Q2}$). For the 50mV default setting, the minimum valley current-limit threshold is 40mV. Connect $I_{LIM}$ to $AV_{DD}$ for a default 50mV valley current limit threshold. In adjustable mode, the valley current limit threshold is precisely 1/10th the voltage seen at $I_{LIM}$. For an adjustable threshold, connect a resistive divider from REF to GND with $I_{LIM}$ connected to the center tap. The external 250mV to 2V adjustment range corresponds to a 25mV to 200mV valley current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the valley current limit tolerance.

### Setting the Foldback Current Limit (Buck)

Alternately, foldback current limit can be implemented if UVP is disabled. Foldback current limit reduces the power dissipation of external components so they can withstand indefinite output overload or short circuit. With automatic recovery after the fault condition is removed. To implement foldback current limit, connect a resistor from $V_{OUT}$ to $I_{LIM}$ ($R_1$ in the "Typical Application Circuit" on page 22), in addition to the resistor-divider network ($R_4$ and $R_5$) used for setting the adjustable current limit.

Equations 26 through 31 demonstrate how to calculate the values of $R_1$, $R_4$, and $R_5$:

1. Calculate the voltage, $V_{ILIM}$

$$V_{ILIM} = 10 \times I_{LOAD(MAX)} \times \left[1 - \frac{LIR}{2}\right] \times r_{DSON(Q2)} \quad \text{(EQ. 26)}$$

2. Pick a percentage of foldback, $P_{FB}$, from 15% to 40%.

3. Calculate the voltage,$V_{VILIM(0V)}$, when the output is shorted (0V).

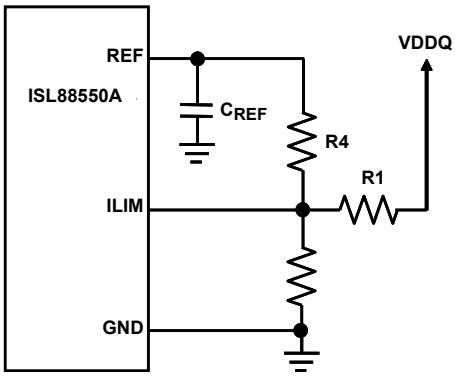



**FIGURE 28. FOLDBACK CURRENT LIMIT**

$$V_{ILIM(0V)} = P_{FB} \times V_{ILIM} \quad \text{(EQ. 27)}$$

4. The value of $R_4$ can be calculated using Equation 28:

$$R_4 = \frac{2V - V_{ILIM(0V)}}{10\mu A} \quad \text{(EQ. 28)}$$

5. The parallel combination of $R_1$ and $R_5$ is calculated using Equation 29:

$$R_{R1 // R5} = \frac{2V}{10\mu A} - R_4 \quad \text{(EQ. 29)}$$

6. Then $R_5$ can be calculated as:

$$R5 = \frac{VDDQ \times R4 \times R_{R1//R5}}{\left[\left(VDDQ - \left(V_{ILIM} - V_{ILIM(0V)}\right)\right) \times R4 - \left(V_{ILIM} - V_{ILIM(0V)}\right) \times R_{R1//R5}\right]} \quad \text{(EQ. 30)}$$

7. Then $R_1$ is calculated as shown in Equation 31:

$$R1 = \frac{R5 \times R_{R1//R5}}{\left[R5 - R_{R1//R5}\right]} \quad \text{(EQ. 31)}$$

### Boost-Supply Capacitor Selection (Buck)

The boost capacitor should be 0.1µF to 4.7µF, depending on the input and output voltages, external components, and PC board layout. The boost capacitance should be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET conduction time, which happens at maximum operating duty cycle (this occurs at minimum input voltage). In addition, ensure that the boost capacitor does not discharge to below the minimum gate-to-source voltage required to keep the high-side MOSFET fully enhanced for lowest ON-resistance. This minimum gate to source voltage ($V_{GS(MIN)}$) is determined using Equation 32:

$$V_{GS(MIN)} = V_{DD} \times \frac{Q_G}{C_{BOOST}} \quad \text{(EQ. 32)}$$

where $V_{DD}$ is 5V, $Q_G$ is the total gate charge of the high-side MOSFET, and $C_{BOOST}$ is the boost capacitor value where $C_{BOOST}$ is $C_7$ in the "Typical Application Circuit" on page 22.

### *Transient Response (Buck)*

The inductor ripple current also affects transient response performance, especially at low $V_{IN}$ - $V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The output sag is also a function of the maximum duty factor, which can be calculated from the ON-time and minimum off-time as shown in Equation 33:

$$V_{SAG} = \frac{L \times \Delta I_{LOAD(MAX)}^2 \left[\frac{V_{OUT} \times K}{V_{IN}} + t_{OFF(MIN)}\right]}{2C_{OUT} \times V_{OUT}\left[\frac{(V_{IN} - V_{OUT}) \times K}{V_{IN}} + t_{OFF(MIN)}\right]} \quad \text{(EQ. 33)}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the "Electrical Specifications" on page 3) and K is from Table 1.

The overshoot during a full-load to no-load transient due to stored inductor energy can be calculated using Equation 34:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}^2 \times L}{2 \times C_{OUT} \times V_{OUT}} \quad \text{(EQ. 34)}$$

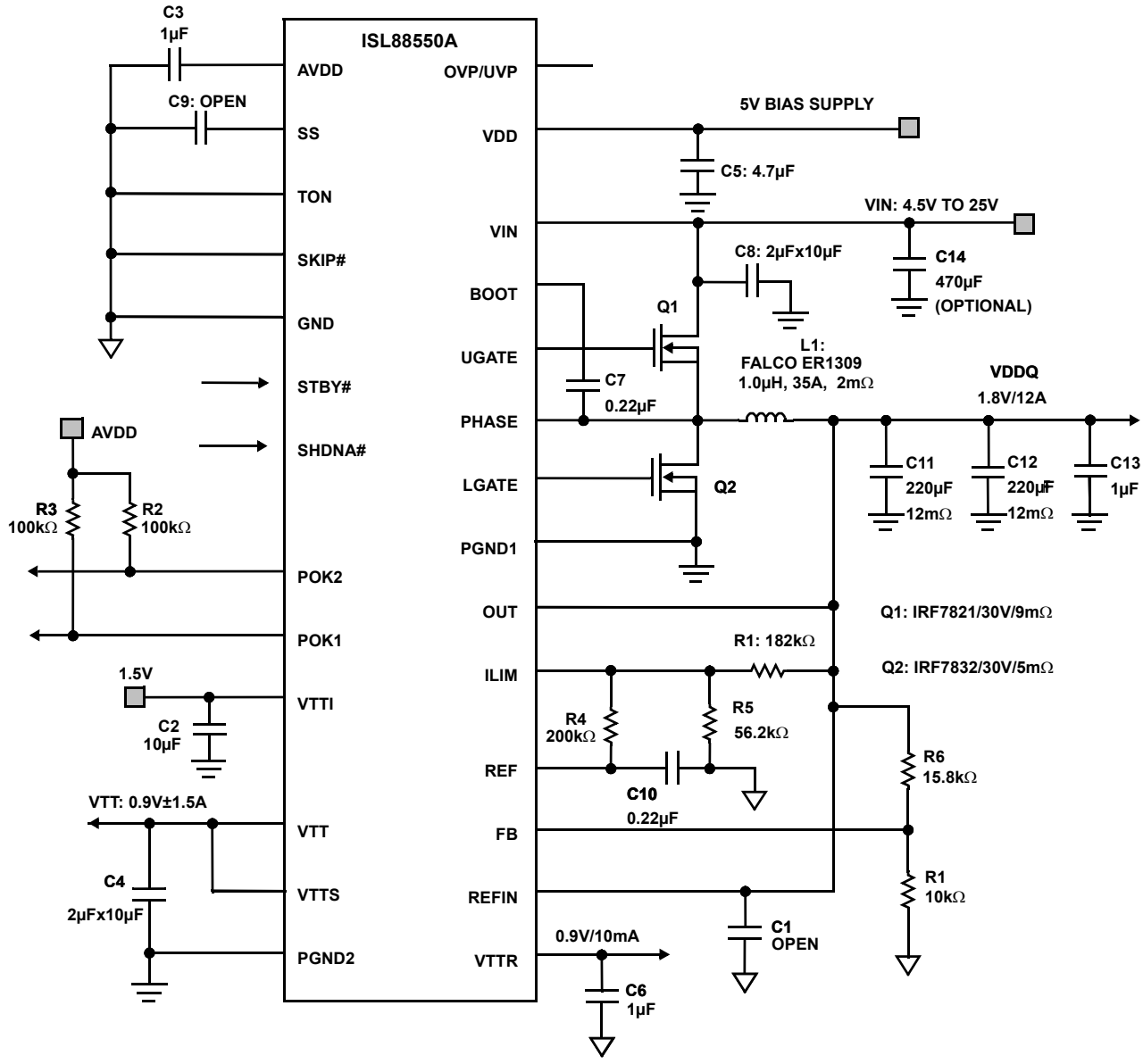



FIGURE 29. TYPICAL DDR II APPLICATIONS CIRCUIT

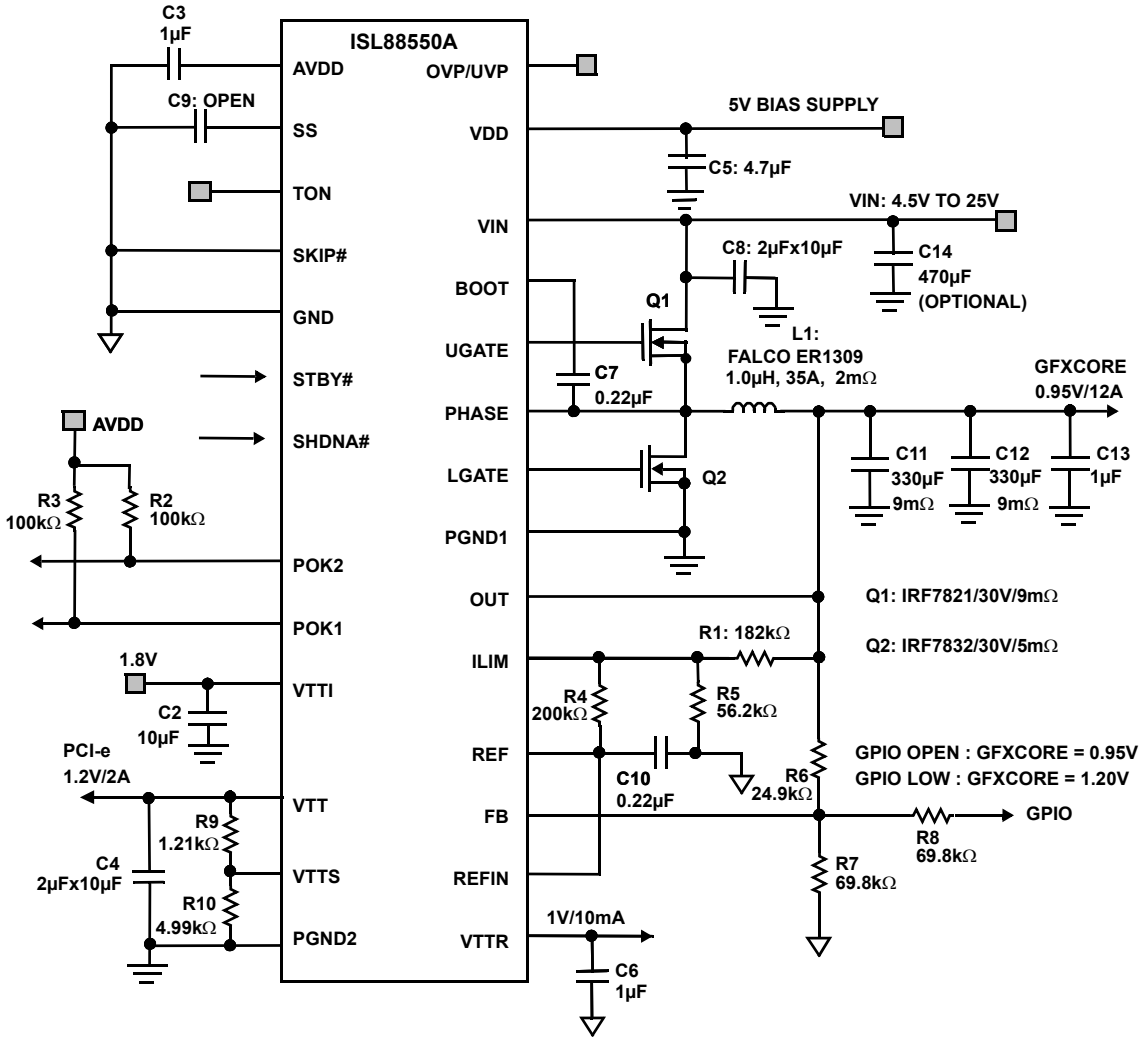



FIGURE 30. TYPICAL GFX APPLICATION CIRCUIT

## Applications Information

### Dropout Performance (Buck)

The output voltage adjustable range for continuous conduction operation is restricted by the non-adjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) ON-time setting. When working with low input voltages, the duty-factor limit must be calculated using the worse case values for on and off times. Manufacturing tolerances and internal propagation delays introduce an error to the $t_{ON}$ K-factor. This error is greater at higher frequencies (see Table 1). Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the $V_{SAG}$ equation in “Transient Response (Buck)” on page 22).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time ($I_{DOWN}$) as much as it ramps up during the on-time ($I_{UP}$). The ratio $h = I_{UP}/I_{DOWN}$ indicates the controller’s ability to slew the inductor current higher in response to increased load, and must always be >1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and $V_{SAG}$ greatly increases, unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between $V_{SAG}$, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated using Equation 35:

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{1-\left(\frac{h \times t_{OFF(MIN)}}{K}\right)}\right] + V_{DROP2} - V_{DROP1} \quad \text{(EQ. 35)}$$

where $V_{DROP1}$ and $V_{DROP2}$ are the parasitic voltage drops in the discharge and charge paths (see “ON-Time One Shot ($t_{ON}$)” on page 12), $t_{OFF(MIN)}$ is from the “Electrical Specifications” Table on page 3, and K is taken from Table 1. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable $V_{SAG}$. If operation near dropout is anticipated, calculate $V_{SAG}$ to be sure of adequate transient response.

A dropout design example is shown in Equation 36:

- $V_{OUT}$ = 2.5V
- $f_{SW}$ = 600kHz
- K = 1.7µs
- $t_{OFF(MIN)}$ = 450ns
- $V_{DROP1}$ = $V_{DROP2}$ = 100mV
- h = 1.5

$$V_{IN(MIN)} = \left[\frac{2.5V + 0.1V}{1 - \left(\frac{1.5 \times 450ns}{1.7\mu s}\right)}\right] + 0.1V - 0.1V = 4.3V \quad \text{(EQ. 36)}$$

## PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the topside of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single m of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSP and CSN directly across the current-sense resistor ($R_{SENSE}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BOOT, PHASE, UGATE, and LGATE) away from sensitive analog areas (REF, FB, and ILIM).

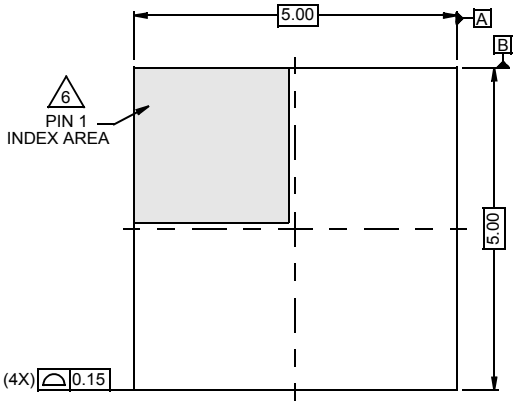
## Special Layout Considerations for LDO Section

The 20µF output capacitor (or capacitors) at VTT should be placed as close to the VTT and PGND2 pins (pins 12 and 11) as possible to minimize the series resistance/inductance in the trace. The PGND2 side of the capacitor should be shorted with the lowest impedance path to the ground slug underneath the IC, which should also be star-connected to the GND (pin 24) of the IC. A narrower trace can be used to tie the output voltage on the VTT side of the capacitor back to the VTTS pin (pin 9). However, keep this trace well away from noisy signals such as the PGND or PGND2 to prevent noise from being injected into the error amplifier's input. For best performance, the VTTI bypass capacitor should also be placed as close to the VTTI pin (pin 13) as possible. A short low impedance connection should also be made to tie the other side of the capacitor to the PGND2 pin. The REFIN pin (pin 14) should be separately routed with a clean trace and adequately bypass to AGND. A suggested layout of the board can be found in the Evaluation Board Kit of ISL88550A.

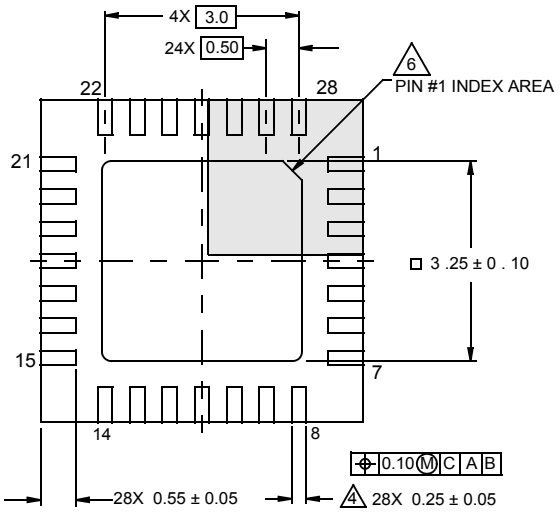
# Package Outline Drawing

## L28.5x5B

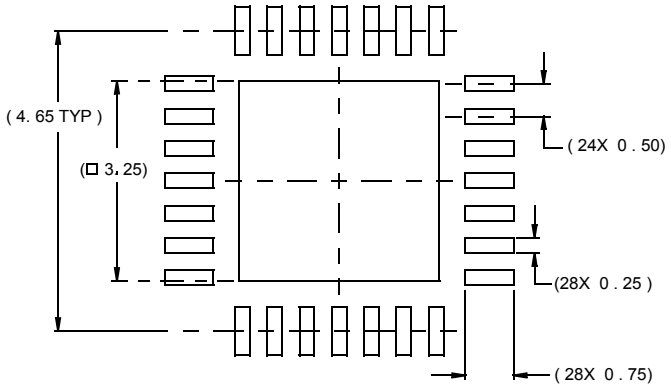
**28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 1, 10/07**



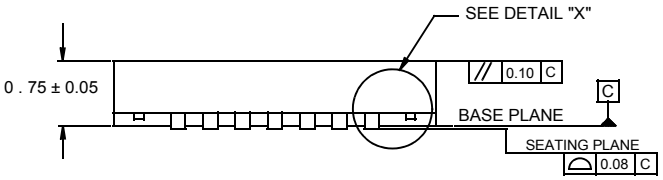

TOP VIEW



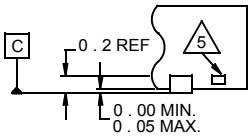

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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