ISL9001A

LDO with Low ISUPPLY, High PSRR

FN6433
Rev 3.00
December 10, 2015

ISL9001A is a high performance Low Dropout linear regulator capable of sourcing 300mA current. It has a low standby current and high-PSRR and is stable with output capacitance of 1µF to 10µF with ESR of up to 200mΩ.

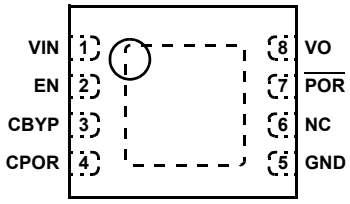
The ISL9001A has a very high PSRR of 90dB and output noise less than 30µV_{RMS}. A reference bypass pin allows connection of a noise-filtering capacitor for low-noise and high-PSRR applications. When coupled with a no load quiescent current of 25µA (typical), and 0.1µA shutdown current, the ISL9001A is an ideal choice for portable wireless equipment.

The ISL9001A provides a P_{GOOD} signal with delay time programmable through an external capacitor.

Several different fixed voltage outputs are standard. Output voltage options for each LDO range from 1.5V to 3.3V. Other output voltage options may be available upon request.

Pinout

ISL9001A
(8 LD DFN)
TOP VIEW



Features

- 300mA high performance LDO
- Excellent transient response to large current steps
- Excellent load regulation: <0.1% voltage change across full range of load current
- High PSRR: 90dB @ 1kHz
- Wide input voltage capability: 2.3V to 6.5V
- Extremely low quiescent current: 25µA
- Low dropout voltage: typically 200mV @ 300mA
- Low output noise: typically 30µV_{RMS} @ 100µA (1.5V)
- Stable with 1µF to 10µF ceramic capacitors
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- Delayed POR, programmable with external capacitor
- ±1.8% accuracy over all operating conditions
- Tiny 2mmx3mm 8 Ld DFN package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, cell phones and smart phones
- Portable instruments, MP3 players
- Handheld devices, including medical handhelds

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	VO VOLTAGE (V) (Note 3)	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL9001AIRBZ-T	EBB	1.5	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRCZ-T	EBC	1.8	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRFZ-T	EBD	2.5	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRJZ-T	EBE	2.8	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRKZ-T	EBF	2.85	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRLZ-T (**No longer available or supported, recommended part: ISL9005AIRKZ-T**)	EBG	2.9	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL9001AIRNZ-T	EBJ	3.3	-40 to +85	8 Ld 2x3 DFN	L8.2x3

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Please refer to TB347 for details on reel specifications
3. For other output voltages, contact Intersil Marketing.

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . +7.1V
VO Pin . . . . . +3.6V
All Other Pins . . . . . -0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +85°C
Supply Voltage (VIN) . . . . . 2.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld 2x3 DFN Package	69	10

Junction Temperature Range . . . . . -40°C to +125°C
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 5.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		2.3		6.5	V
Ground Current		Quiescent condition: I_O = 0µA				
	I_{DD}	LDO active		25	32	µA
Shutdown Current	I_{DDS}	LDO disabled @ +25°C		0.1	1.0	µA
UVLO Threshold	V_{UV+}		1.9	2.1	2.3	V
	V_{UV-}		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at V_{IN} = V_O + 0.5V, I_O = 10mA, T_J = +25°C	-0.7		+0.7	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = +25°C	-0.8		+0.8	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Continuous	300			mA
Internal Current Limit	I_{LIM}		350	475	600	mA
Dropout Voltage (Note 6)	V_{DO1}	I_O = 300mA; V_O < 2.5V		300	500	mV
	V_{DO2}	I_O = 300mA; 2.5V ≤ V_O ≤ 2.8V		250	400	mV
	V_{DO3}	I_O = 300mA; V_O > 2.8V		200	325	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection		I_O = 10mA, V_{IN} = 2.8V (min), V_O = 1.8V, C_{BYP} = 0.1µF				
		@ 1kHz		90		dB
		@ 10kHz		70		dB
		@ 100kHz		50		dB
Output Noise Voltage		I_O = 100µA, V_O = 1.5V, T_A = +25°C, C_{BYP} = 0.1µF BW = 10Hz to 100kHz		30		μV_{RMS}

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 5.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	500	µs
LDO Soft-Start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V
EN PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.5	V
Input High Voltage	V_{IH}		1.4		V_{IN} + 0.3	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA
Pin Capacitance	C_{PIN}	Informative		5		pF
$\overline{\text{POR}}$ PIN CHARACTERISTICS						
$\overline{\text{POR}}$ Thresholds	V_{POR+}	As a percentage of nominal output voltage	91	94	97	%
	V_{POR-}		87	90	93	%
$\overline{\text{POR}}$ Delay	t_{PLH}	C_{POR} = 0.01µF	100	200	300	ms
	t_{PHL}			25		µs
$\overline{\text{POR}}$ Pin Output Low Voltage	V_{OL}	@ I_{OL} = 1.0mA			0.2	V
$\overline{\text{POR}}$ Pin Internal Pull-up Resistance	R_{POR}		78	100	180	kΩ

NOTES:

6. VOx = 0.98*VOx(NOM); Valid for VOx greater than 1.85V.
7. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

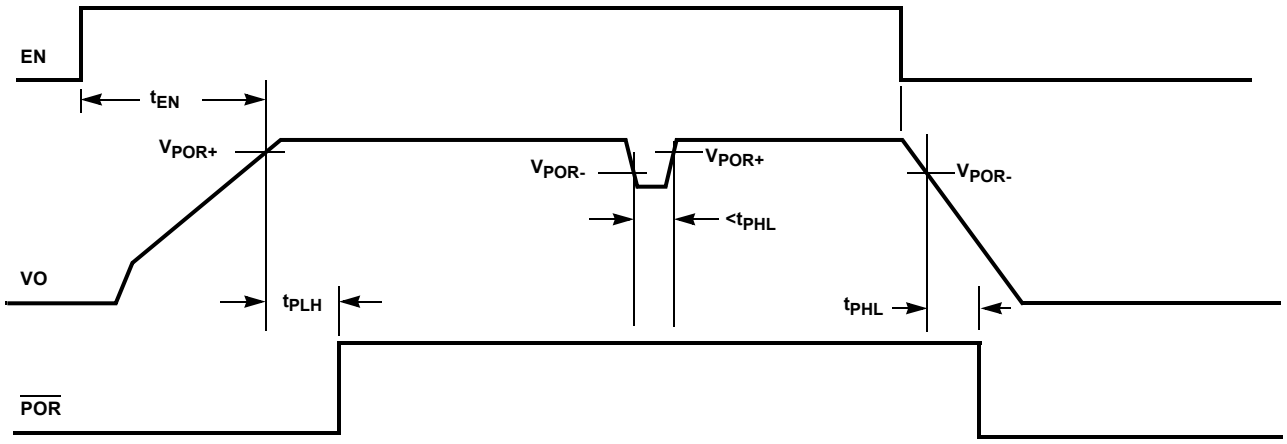


FIGURE 1. TIMING PARAMETER DEFINITION

Typical Performance Curves

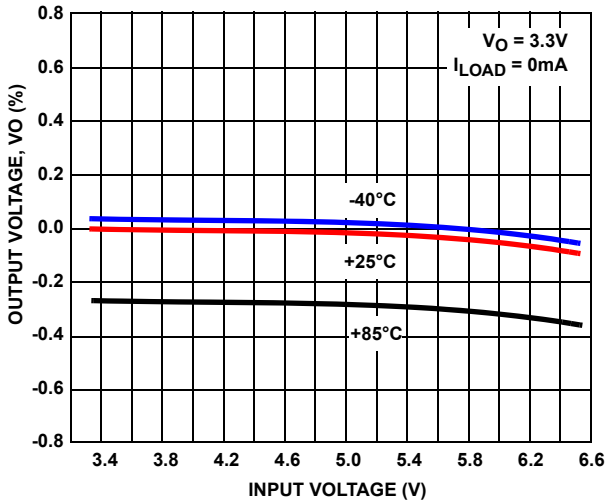


FIGURE 2. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

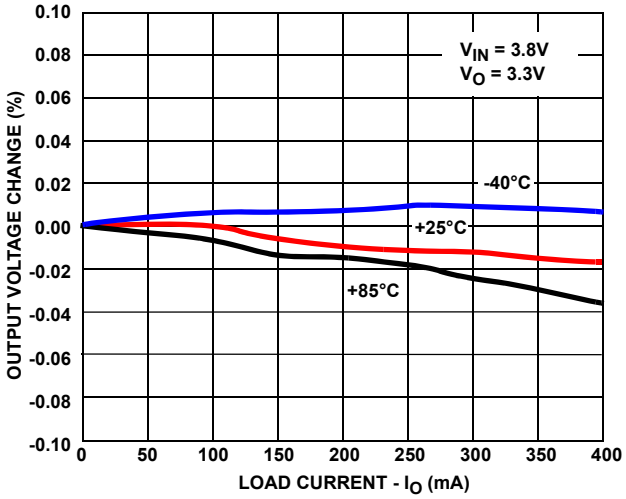


FIGURE 3. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

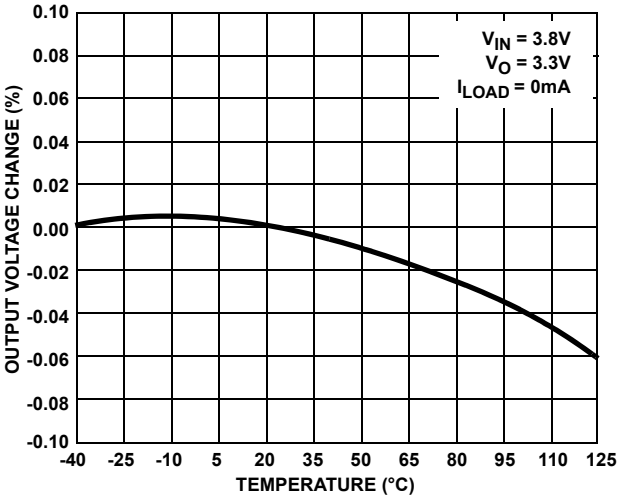


FIGURE 4. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

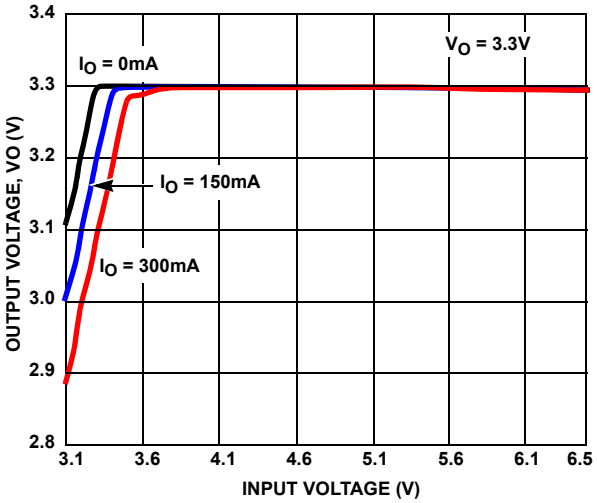


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

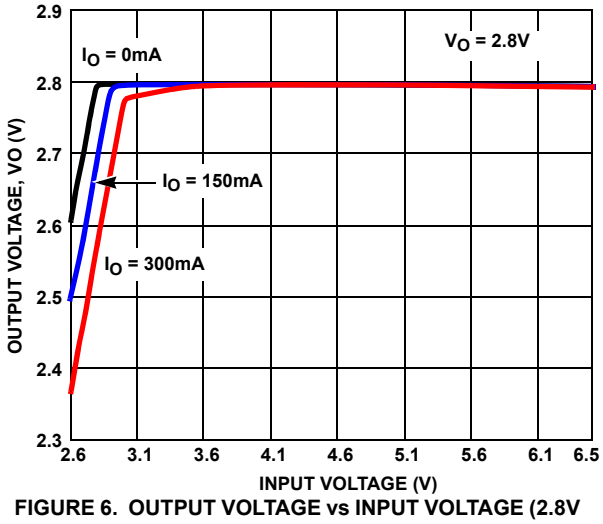


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

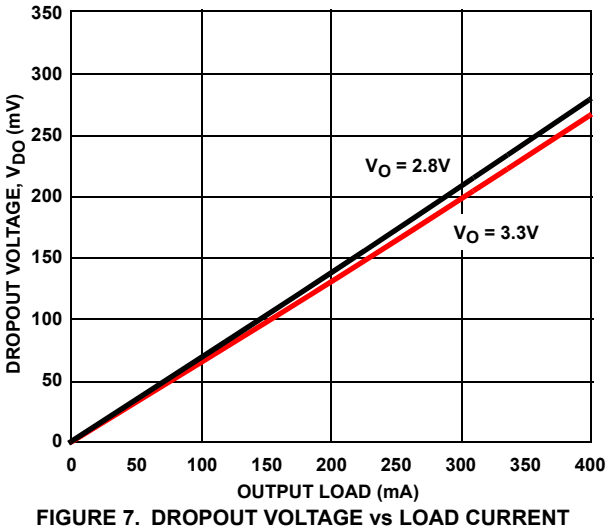


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

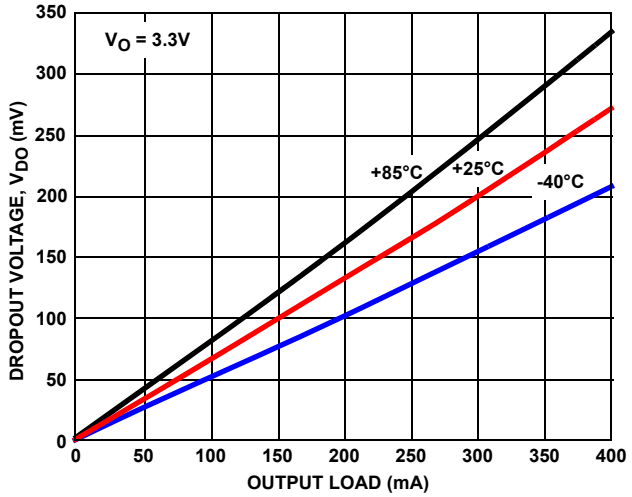


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

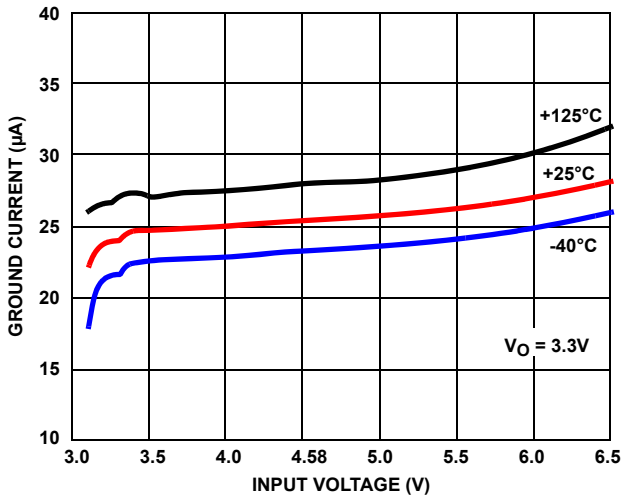


FIGURE 9. GROUND CURRENT vs INPUT VOLTAGE

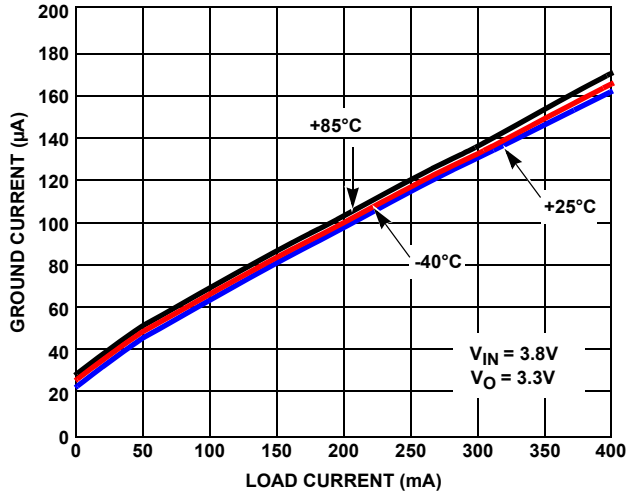


FIGURE 10. GROUND CURRENT vs LOAD

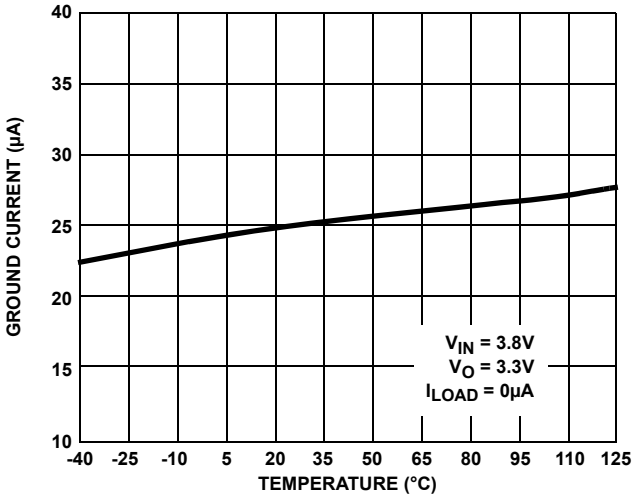


FIGURE 11. GROUND CURRENT vs TEMPERATURE

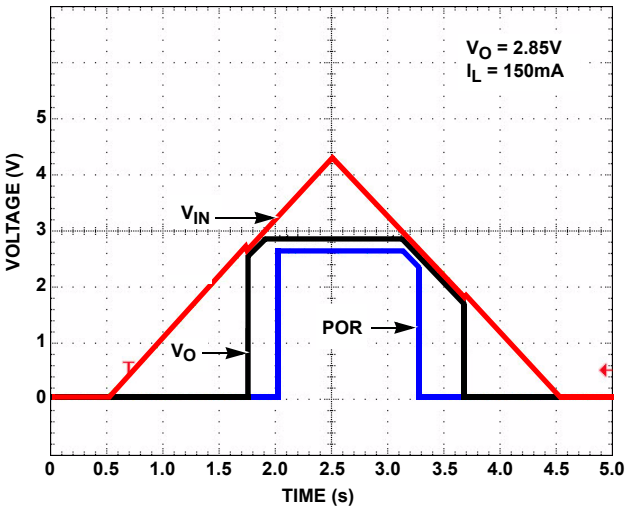


FIGURE 12. POWER-UP/POWER-DOWN

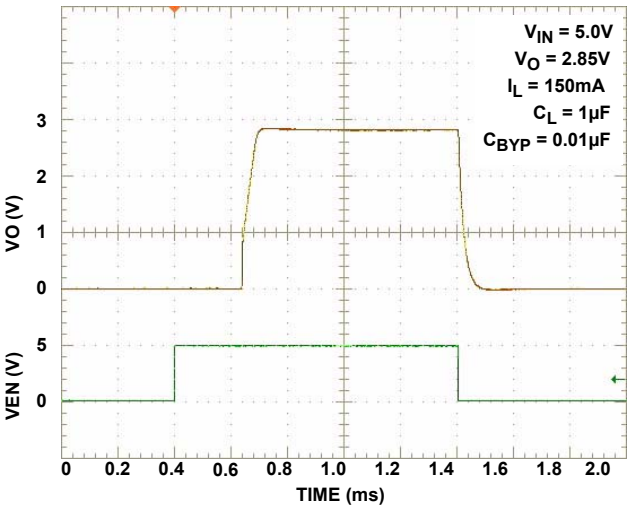


FIGURE 13. TURN-ON/TURN-OFF RESPONSE

Typical Performance Curves (Continued)

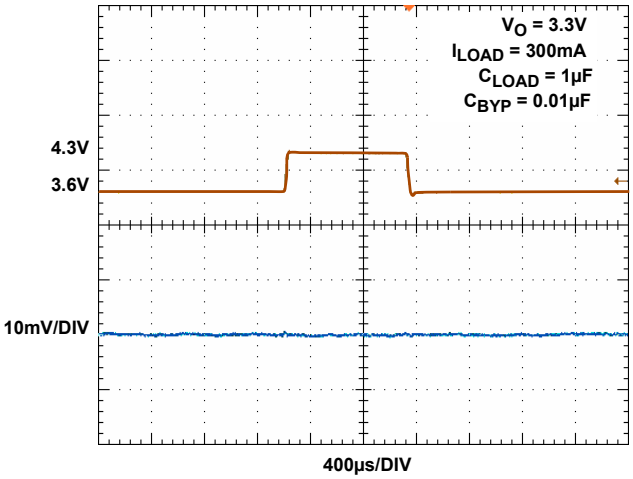


FIGURE 14. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

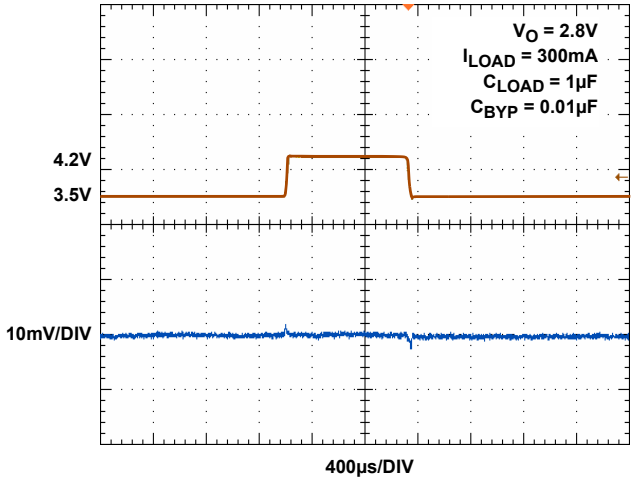


FIGURE 15. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

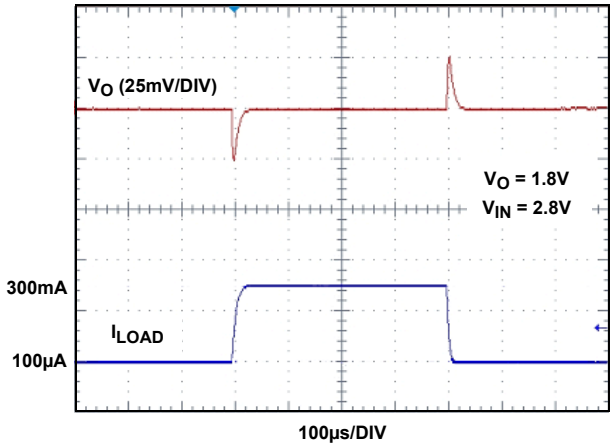


FIGURE 16. LOAD TRANSIENT RESPONSE

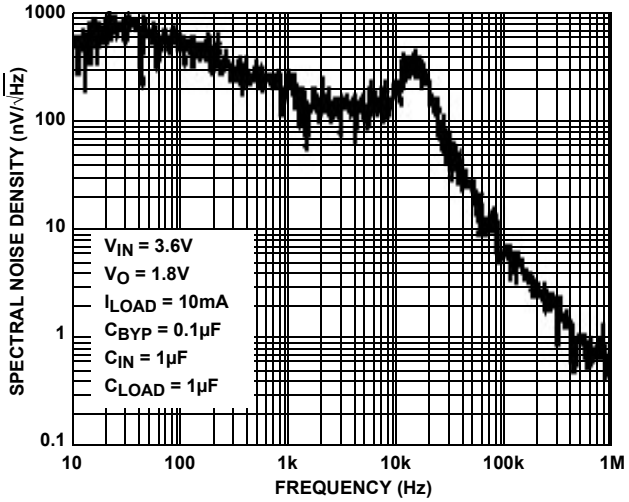


FIGURE 17. SPECTRAL NOISE DENSITY vs FREQUENCY

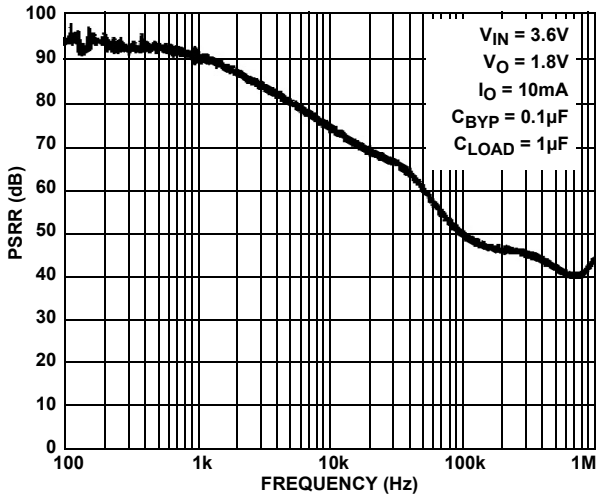
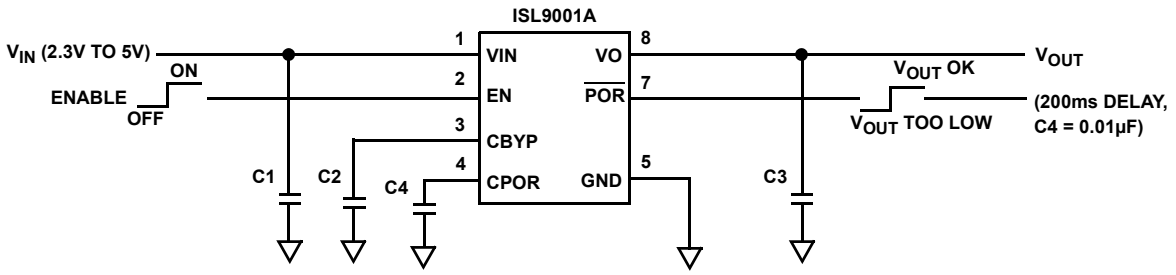


FIGURE 18. PSRR vs FREQUENCY

Pin Description

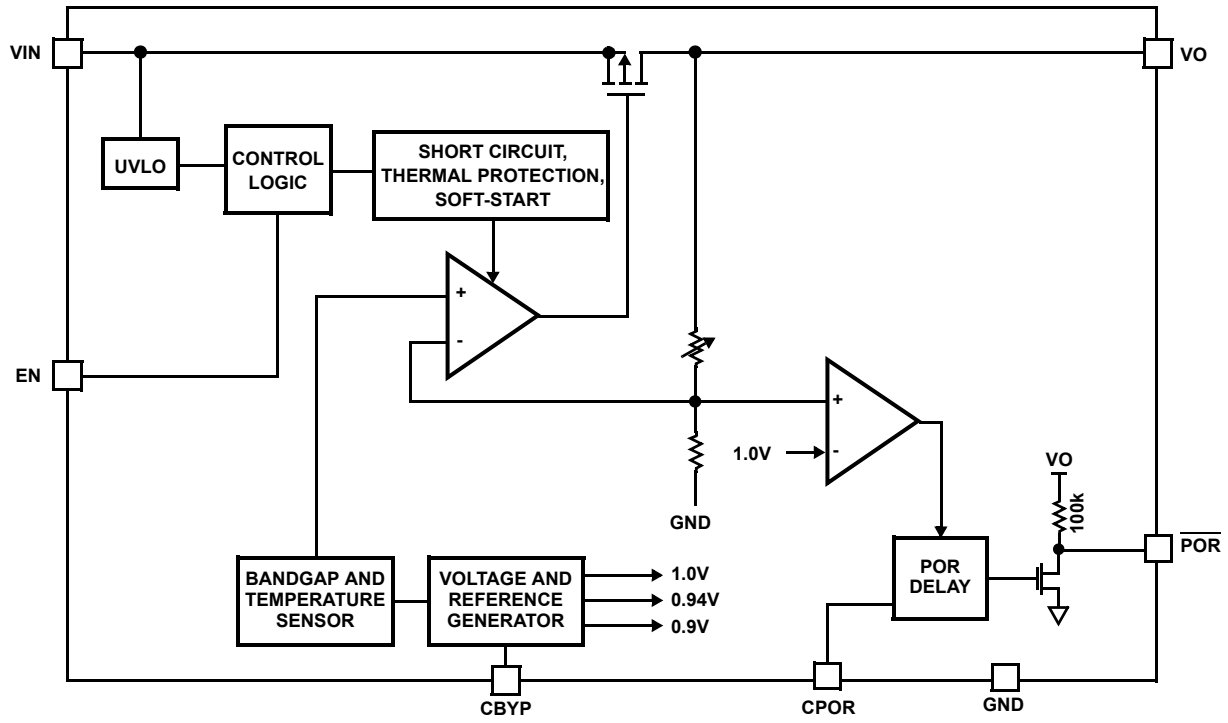
PIN NUMBER	PIN NAME	DESCRIPTION
1	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.
2	EN	LDO Enable.
3	CBYP	Reference Bypass Capacitor Pin: Optionally connect capacitor of value 0.01µF to 0.1µF between this pin and GND to achieve lowest noise and highest PSRR.
4	CPOR	POR Delay Setting Capacitor Pin: Connect a capacitor between this pin and GND to delay the $\overline{POR}$ output release after the output reaches 94% of its specified voltage level. (200ms delay per 0.01µF).
5	GND	GND is the connection to system ground. Connect to PCB Ground plane.
6	NC	Do not connect.
7	$\overline{POR}$	Open-drain POR Output (active-low): Internally connected to VO through 100kΩ resistor.
8	VO	LDO Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended).

Typical Application



C1, C3: 1µF X5R CERAMIC CAPACITOR
C2: 0.1µF X7R CERAMIC CAPACITOR
C4: 0.01µF X7R CERAMIC CAPACITOR

Block Diagram



Functional Description

The ISL9001A contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9001A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart thermal shutdown protects the device against overheating.

Power Control

The ISL9001A has an enable pin (EN) to control power to the LDO output. When EN is low, the device is in shutdown mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1µA. When the enable pin is asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. Once the bypass capacitor has been charged, the LDO powers up.

During operation, whenever the VIN voltage drops below about 1.84V, the ISL9001A immediately disables the LDO output. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01µF capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1µF CBYP capacitor should be used. This filters the reference noise to below the 10Hz to 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator outputs references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9001A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not recommended as LDO performance improvement is minimal.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge. The ISL9001A provides short-circuit protection by limiting the output current to about 425mA.

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory.

Power-On Reset Generation

The ISL9001A has a Power-on Reset signal generation circuit, which indicates that output power is good. The POR signal is generated as follows.

A POR comparator continuously monitors the output of the LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time (see the following). In the power-good state, the open-drain $\overline{\text{POR}}$ output is in a high-impedance state. An internal 100kΩ pull-up resistor pulls the pin up to the LDO output voltage. An external resistor can be added between the $\overline{\text{POR}}$ output and the LDO output for a faster rise time, however, the $\overline{\text{POR}}$ output should not connect through an external resistor to a supply greater than the LDO voltage.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL9001A pulls the POR pin low.

The PGOOD entry and exit delays are determined by the value of an external capacitor connected to the CPOR pin. For a 0.01µF capacitor, the entry and exit delays are 200ms and 25µs respectively. Larger or smaller capacitor values will yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10µs to ensure sufficient immunity against transient induced false POR triggering.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +140°C, if the LDO is sourcing more than 50mA, it shuts down until the die cools sufficiently. Once the die temperature falls back below about +110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 10, 2015	FN6433.3	Added Rev History and About Intersil Verbiage. Updated Ordering Information on page 2 Updated POD L8.2x3 to most current version. Rev changes are as follows: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). Bottom View: Changed exposed pad height from 1.80 +/-0.10 to 1.80 +0.10/-0.15 Changed exposed pad width from 1.65 +/-0.10 to 1.65 +0.10/-0.15 Side View: Changed 0.05 to 0.05 MAX Converted to new POD standards by adding land pattern and moving dimensions from table onto drawing.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

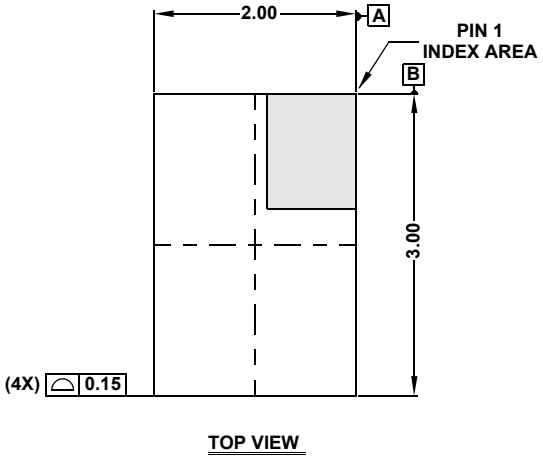
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

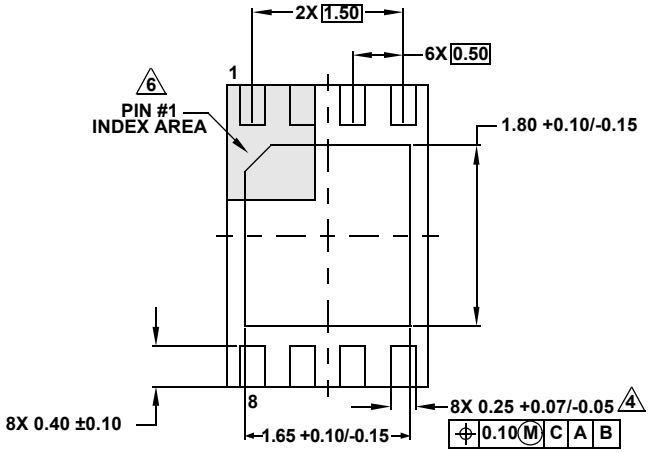
Package Outline Drawing

L8.2x3

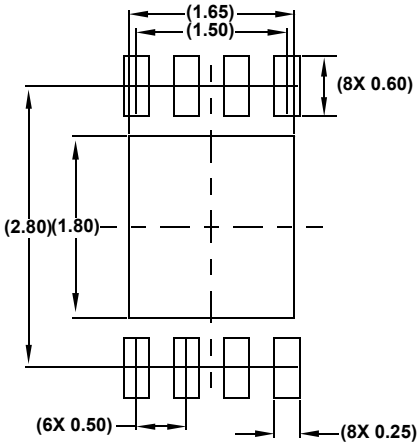
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 3/15



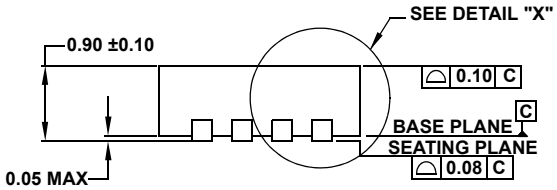
TOP VIEW



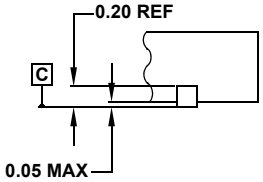
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compies to JEDEC MO-229 VCED-2.

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