ISL9492

Single Output LNB Supply and Control Voltage Regulator with I^{2}C Interface for Satellite Set-Top Box Designs

FN6547
Rev 1.00
March 17, 2011

The ISL9492 is a highly integrated voltage regulator and interface IC specifically designed for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNB) of a single antenna port. It also supports DiSEqC tone generation and modulation with diagnostic status read-back. Controlling the ISL9492 is simple via the I^{2}C bus by writing 8 bit words onto the System Registers (SR).

The device design makes the total LNB supply design simple, efficient and compact with low external component count by integrating Boost power MOSFET, current-mode boost PWM and a low-noise linear regulator. The current-mode boost converters provide the linear regulator with input voltage that is set to the final output voltages, plus typically 0.9V to insure minimum power dissipation across each linear regulator.

The LNB output voltage can be controlled in two ways; by full control from I^{2}C using the VTOP and VBOT bits or by setting the I^{2}C to the lower range and switching to higher range with the select VTOP pin.

The External modulation input EXTM accepts a modulated DISEqC command and transfers it symmetrically to the output. The EXTM pin can be used to modulate the continuous internal tone. The fault signal serves as an interrupt for the processor when any condition turns OFF the LNB controller (over-temperature, overcurrent, disable). The states of these flags to the faults can be thoroughly examined through the I^{2}C registers.

Features

- Single-Chip Power Solution
  - Operation for 1-Tuner/1-Dish Applications
  - Integrated DC/DC Converter and I^{2}C Interface
- Integrated Boost MOSFET
- Switch-Mode Power Converter for Lowest Dissipation
  - 490kHz Boost Switching Frequency
  - Boost PWMs with > 92% Efficiency
  - Selectable 13.5V or 18.5V Outputs
  - I^{2}C and Pin Controllable Output
- 31V Output Back-Bias Capability
- Built-in Tone Oscillator Factory
  - Facilitates DiSEqC (EUTELSAT) Encoding
  - Trimmed to 22kHz
  - External Modulation Input
- DiSEqC 2.0 Support and Diagnostics
- Internal Overvoltage, Undervoltage, Overcurrent Protection, Over-Temperature Flags Accessible through the I^{2}C Interface and Fault Signal Status Pin
- Short-Circuit Protection

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

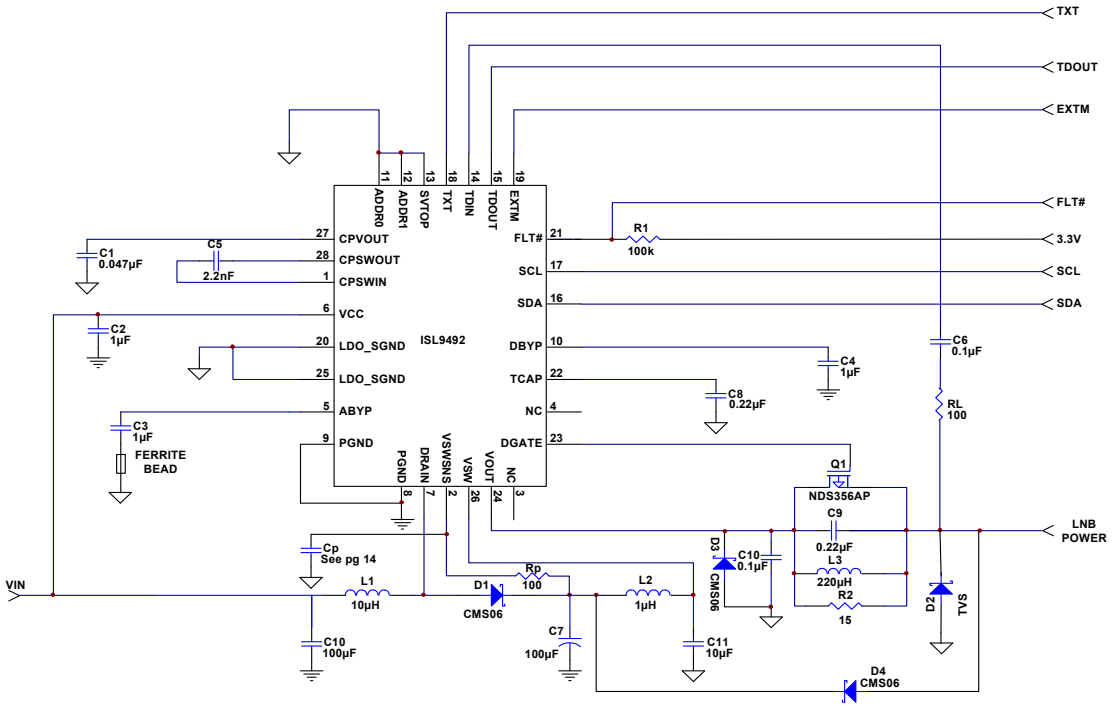


FIGURE 1. TYPICAL APPLICATION

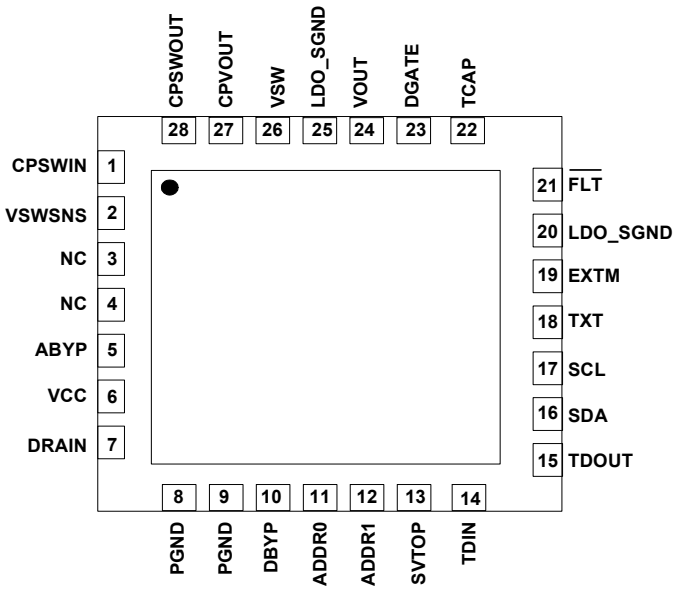
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9492ERZ	94 92ERZ	-20 to +85	28 Ld 4x4 TQFN	L28.4x4A
ISL9492QFNEVAL1	Evaluation Board			

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9492. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL9492
(28 LD TQFN)
TOP VIEW



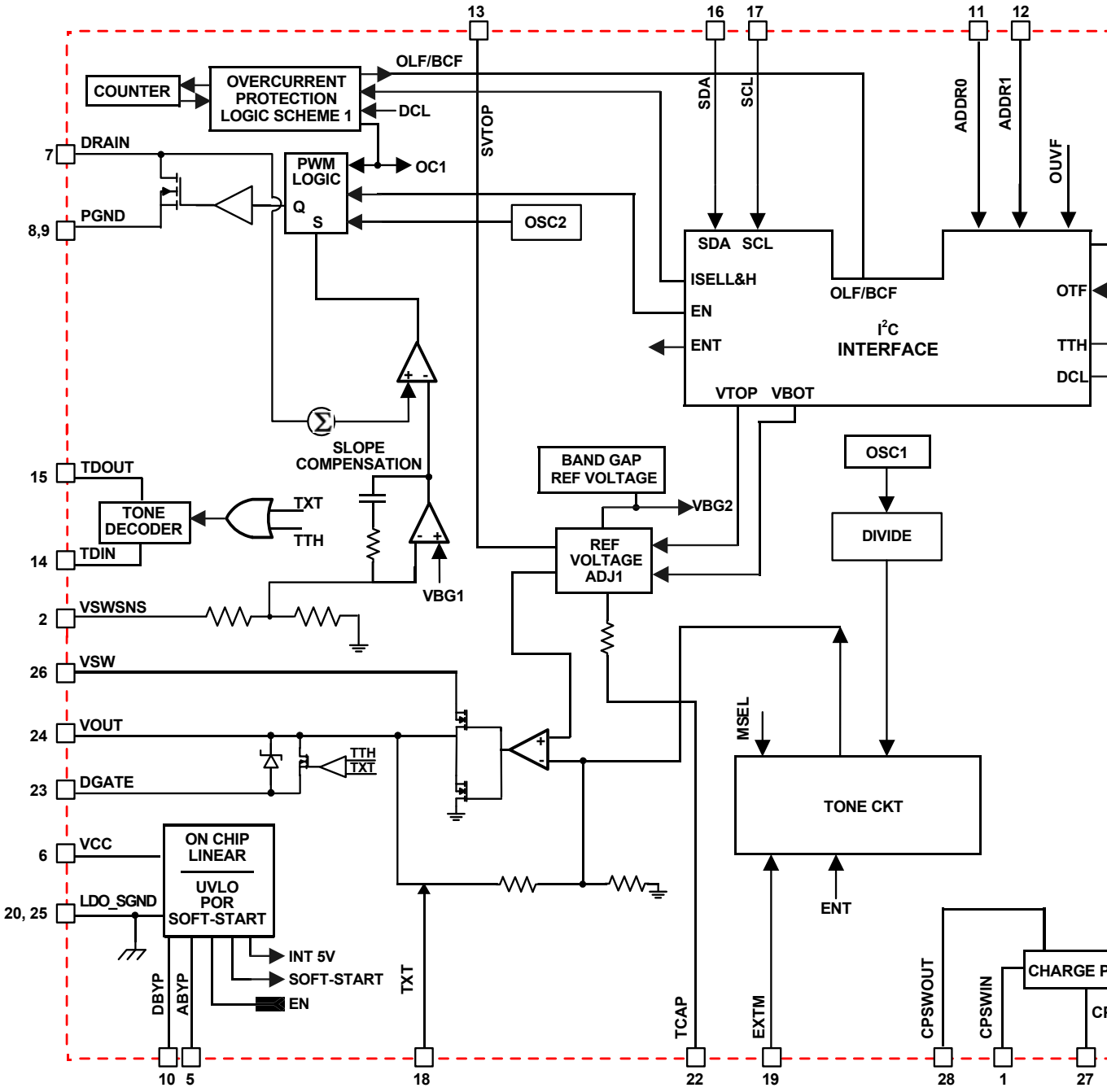
Functional Pin Descriptions

PIN	SYMBOL	FUNCTION
1	CPSWIN	Charge pump connection 1
2	VSWSNS	Boost regulator sense line. Connect to boost output capacitor.
3, 4	NC	No connect pins
5	ABYP	Analog 5V supply. Decouple with 1µF ceramic capacitor and a ferrite bead (see “ABYP” on page 14 for more detail).
6	VCC	Main power supply to the chip.
7	DRAIN	This is the Drain of the Boost MOSFET. The Boost inductor will be connected to this pin.
8,9	PGND	Power gound for the Internal Boost MOSFET.
10	DBYP	Digital 5V supply. Decouple with 1µF ceramic capacitor.
11, 12	ADDR0, ADDR1	Logic combination at the ADD0 and ADD1 can select four different chip select addresses.
13	SVTOP	External control of output voltage selection.
14	TDIN	Tone detector input.
15	TDOUT	The envelope of the actually detected external tone signal. It is an open-drain output.

Functional Pin Descriptions (Continued)

PIN	SYMBOL	FUNCTION
16	SDA	Bidirectional data from/to I^2C bus.
17	SCL	Clock from I^2C bus.
18	TXT	Tx, Rx switch control
19	EXTM	This pin can be used in two ways: 1. To drive TONE with the actual tone signal directly. 2. To drive TONE with the envelope of the actual tone signal to be generate by this device.
20, 25	LDO_SGND	Small signal ground for the internal LDO.
21	$\overline{FLT}$	This is an open drain output from the controller. It will go LOW when any of the fault flags is set.
22	TCAP	Capacitor for setting rise and fall time of the output voltage. Typical value is 0.1µF.
23	DGATE	Connect to an external PMOS gate to short the RLC tank circuit during 22kHz tone transmission.
24	VOUT	Linear regulator output provides the LNB power.
26	VSW	Input to the linear regulator that actually provides the LNB output voltage.
27	CPVOUT	Output of charge pump.
28	CPSWOUT	Charge pump connection 2.
-	Pad	There is no connection with this pin. EPAD also has no connection and should be connected to GND plane with multiple vias.

Block Diagram



Typical Application Schematic

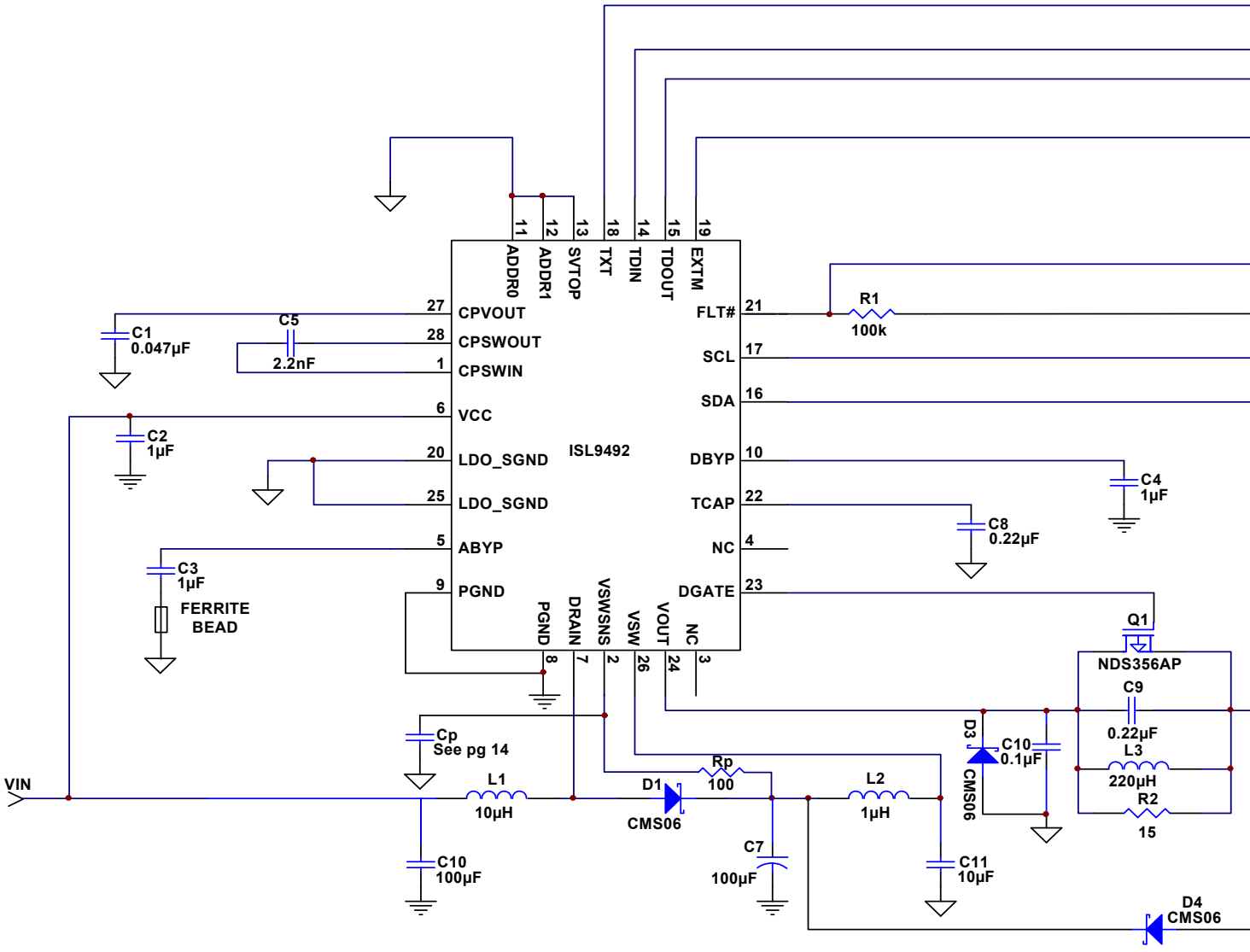


Table of Contents

Absolute Maximum Ratings

V_{CC} (Supply Voltage) . . . . . 8V to 18V
V_{OUT} . . . . . -0.3V to 36V
VSW, Drain . . . . . -0.3V to 24V
All Other Pins . . . . . -0.3V to 5.5V
All Pins Referenced to Ground
ESD Rating
  Human Body Model (Tested per JESD22-A114E) 3kV
  Machine Model (Tested per JESD22-A115-A) 200V
  Charged Device Model 2kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TQFN Package (Notes 4, 5)	38	3

Maximum Junction Temperature (Note 6) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature . . . . . -20°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. The device junction temperature should be kept below +150°C. Thermal shutdown circuitry turns off the device if junction temperature exceeds +150°C typically.

Electrical Specifications

V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN = 1, VTOP = 0, VBOT = 0, ENT = 0, V_{OUT} Load = 100mA, unless otherwise noted. See “ISL9492 Software Description” on page 16 for I^2C access to the system. **Boldface limits apply over the operating temperature range, -20°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	(Note 7)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Operating Supply Voltage Range			F	**8**	12	**14**	V
Standby Supply Current		EN = 0	F	-	3.6	-	mA
Supply Current	I_{IN}	VTOP = VBOT = EN = 1, DLIN = 0, V_{OUT} = No load	F	-	6	**10**	mA
Supply Current	I_{VSW}	VTOP = VBOT = EN = DLIN = 1, No load	F	-	-	**20**	mA
Temperature Shutdown Threshold			F	-	150	-	°C
Temperature Shutdown Hysteresis			F	-	20	-	°C
UNDERVOLTAGE LOCKOUT BOOST							
Falling Threshold	OUVL	V_{CC} Falling from above 8V (Note 9)	F	-	6.8	-	V
Rising Threshold	OUVL	V_{CC} Rising from 0V	F	-	7.35	-	V
BOOST CONVERTER							
Boost MOSFET Drain Current Limit			F	-	4	-	A
Boost MOSFET ON-Resistance			F	-	520	-	mΩ
LINEAR REGULATOR							
Output Voltage		13V (see Table 1)	P	**13.2**	13.5	**13.8**	V
		14V (see Table 1)	P	**13.9**	14.2	**14.5**	V
		18V (see Table 1)	P	**18.2**	18.5	**18.8**	V
		20V (see Table 1)	P	**19.7**	20	**20.3**	V
Dropout Voltage	V_{DROP}	V_{OUT} Load = 750mA (Note 9)	F	-	0.4	-	V
T_{CAP} Current (Output Soft-start Control)		T_{CAP} = 0V	F	**8**	10	**12**	µA
Output Undervoltage (Asserted High During Soft-start)		OUVF bit is asserted high, Measured from the typical output set value	P	**-12**	-	**-2**	%
Output Overvoltage (Asserted High During Soft-start)		OUVF bit is asserted high, Measured from the typical output set value	P	**+2**	-	**+12**	%

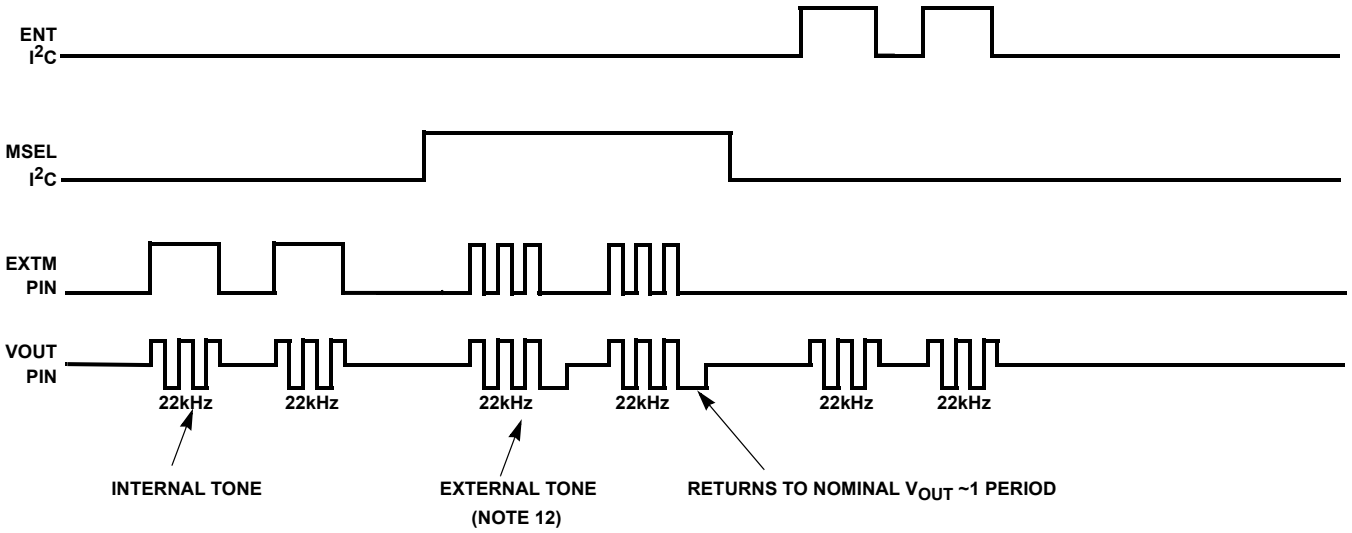
Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN = 1, VTOP = 0, VBOT = 0, ENT = 0, V_{OUT} Load = 100mA, unless otherwise noted. See "ISL9492 Software Description" on page 16 for I^2C access to the system. **Boldface limits apply over the operating temperature range, -20°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	(Note 7)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Line Regulation		V_{CC} = 8V to 14V; V_{OUT} = 13V @ 350mA	P	-	4	**40**	mV
		V_{CC} = 8V to 14V; V_{OUT} = 18V @ 350mA	P	-	4	**60**	mV
Load Regulation		V_{OUT} Load = 0mA to 350mA	P	-	50	**80**	mV
		V_{OUT} Load = 0mA to 750mA	P	-	100	**200**	mV
Current Limiting	I_{MAX}	ISELH = 0, ISELL = 0, DCL bit = 0 (Note 10)	P	**850**	950	**1050**	mA
		ISELH = 1, ISELL = 0, DCL bit = 0 (Note 10)	P	**600**	670	**740**	mA
		ISELH = 0, ISELL = 1, DCL bit = 0 (Note 10)	P	**710**	790	**870**	mA
		ISELH = 1, ISELL = 1, DCL bit = 0 (Note 10)	P	**370**	400	**450**	mA
Cable Fault CABF Threshold	I_{CAB}	V_{OUT} = 20V, No Tone	P	**2**	20	**50**	mA
Back-Biased Current		V_{OUT} = 21V from External Source	P	-	-	**10**	mA
TONE OSCILLATOR (TONE) (Note 8)							
Tone Frequency	f_{tone}	ENT = 1	P	**20**	22	**24**	kHz
Tone Amplitude	V_{tone}	ENT = 1, with Proper DiSEqC Tank Circuit	P	**500**	680	**800**	mV
Tone Duty Cycle	dc_{tone}	ENT = 1	P	**-**	50	**-**	%
Tone Rise or Fall Time	t_r, t_f	ENT = 1	P	**5**	10	**14**	µs
TONE DECODER (TDIN, TDOUT)							
Frequency Capture Range	Ftdin		P	**18**	-	**26**	kHz
Input Impedance	Zdet		F	-	8.6	**-**	kΩ
Detector Output Voltage	V_{tdout_L}	Tone Present, Sink Current = 3mA	P	-	-	**0.4**	V
Detector Output Leakage (Open Drain)	I_{tdout_H}	Tone Absent	P	-	-	**10**	µA
Tone Decoder Rx Threshold (Note 10)	V_{RXth}	TTH bit = 0 and TXT pin = 0	P	**200**	-	-	mV_{P-P}
Tone Decoder Tx Threshold (Note 10)	V_{TXth}	TTH bit= 1 or TXT pin = 1	P	**400**	-	-	mV_{P-P}
LOGIC INTERFACE (INPUT = EXTM, SVTOP, ADD0, ADD1, TXT, SCL, SDA, OUTPUT = $\overline{FLT}$)							
Input Logic LOW			F	-	-	**0.8**	V
Input Logic HIGH			F	**2.0**	-	-	V
Input Current			F	-	25	-	µA
Input Pull-down Resistance			F	-	200	-	kΩ
Output Logic LOW		Fault Detected, Sink Current = 3mA	F	-	-	**0.4**	V
Output Logic High Leakage (Open Drain)		No Fault	F	-	-	**10**	µA

NOTES:

7. F = Functional check; P = Probe or final test
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. Output voltage can only be maintained in regulation if the input voltage is within the specified range.

Tone Waveform



NOTES:

10. TTH allows threshold control through the I^2C Interface.
11. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
12. The tone rise and fall times are not shown due to resolution of graphics.

FIGURE 2. TONE WAVEFORM

Typical Performance Curves

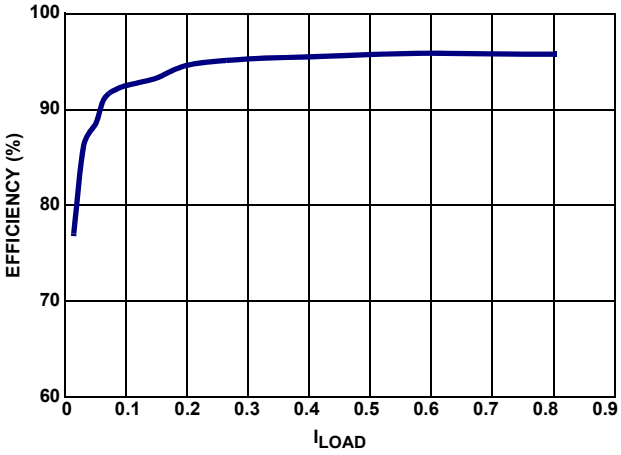


FIGURE 3. BOOST EFFICIENCY FOR 12V_{IN} TO 14.3V_{OUT}

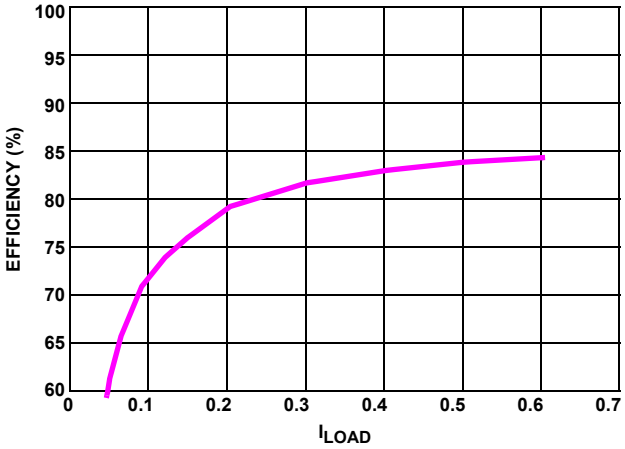


FIGURE 4. SYSTEM EFFICIENCY (BOOST + LDO) FOR 12V_{IN} TO 13.3V_{OUT}

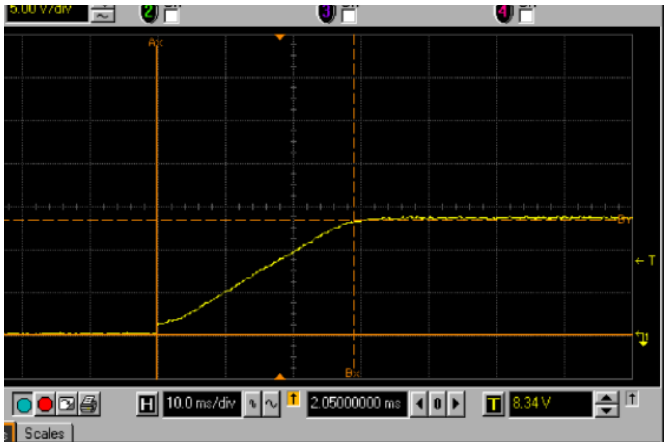


FIGURE 5. VLNB RISE TIME = 29ms, T_{CAP} = 0.22µF

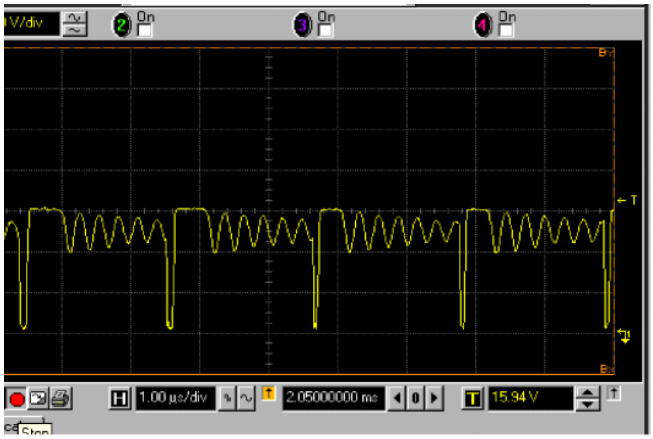


FIGURE 6. BOOST SWITCH NODE AT 0A (DISCONTINUOUS)

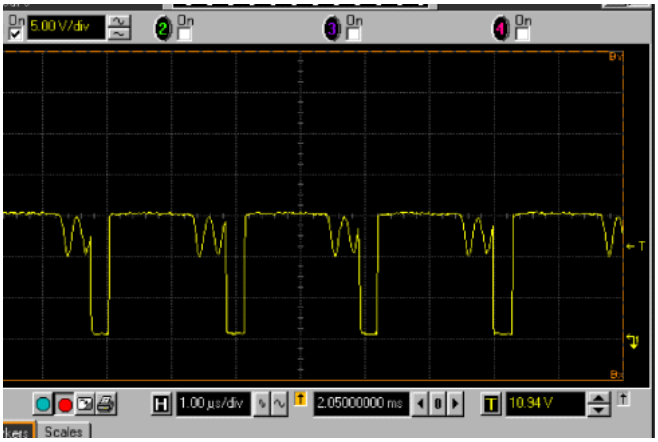


FIGURE 7. BOOST SWITCH NODE AT 100mA (PARTIAL DISCONTINUOUS)

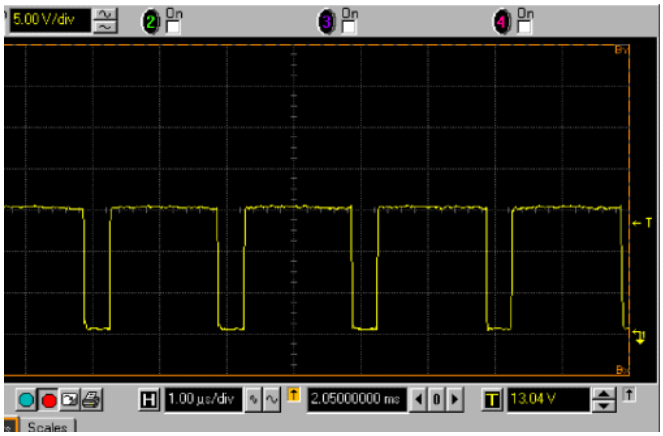


FIGURE 8. BOOST SWITCH NODE AT 300mA (CONTINUOUS MODE)

Typical Performance Curves (Continued)

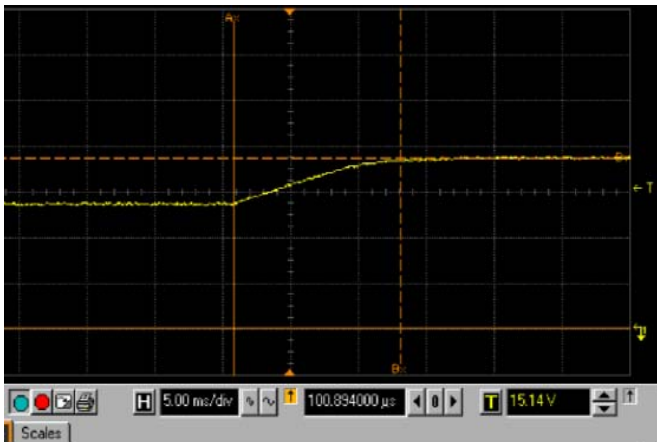


FIGURE 9. VLNB TRANSITIONS FROM 13.3V TO 18.3V

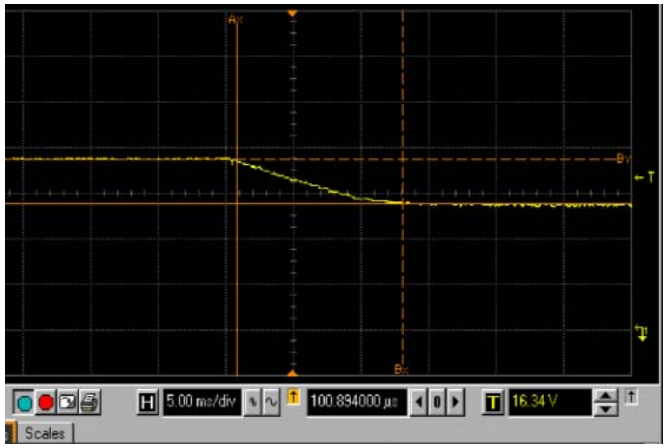


FIGURE 10. VLNB TRANSITIONS FROM 18.3V TO 13.3V

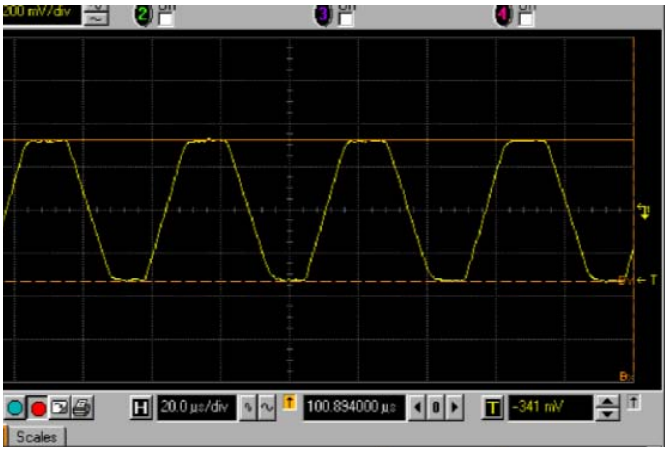


FIGURE 11. 22kHz TONE AT NO-LOAD

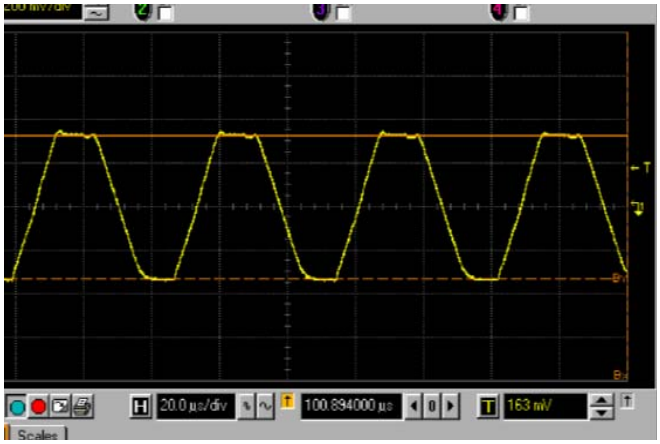


FIGURE 12. 22kHz TONE AT 700mA

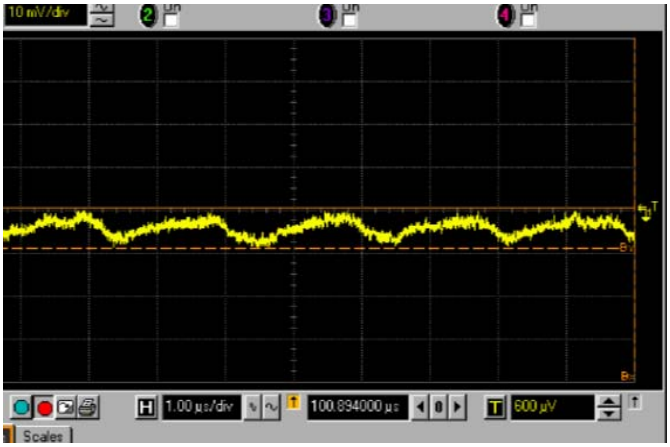


FIGURE 13. AC NOISE ON 13.3V_{OUT} AT 700mA IS ~ 10mV

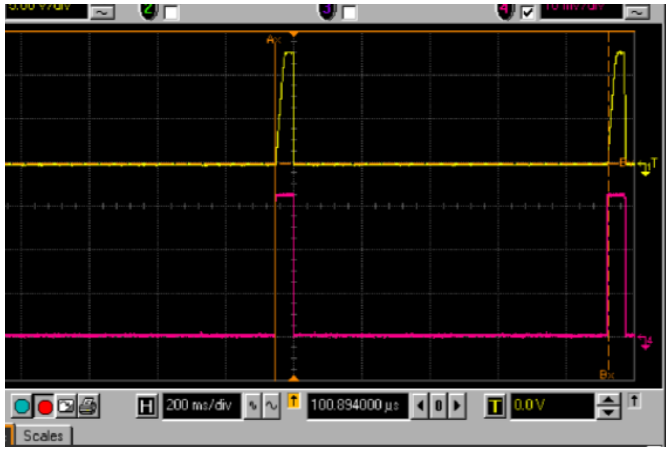


FIGURE 14. DYNAMIC CURRENT LOOP STARTED TO ENABLE. TOP IS VLNB AND BOTTOM IS LOAD CURRENT WAVEFORM (200mA/DIV)

Typical Performance Curves (Continued)

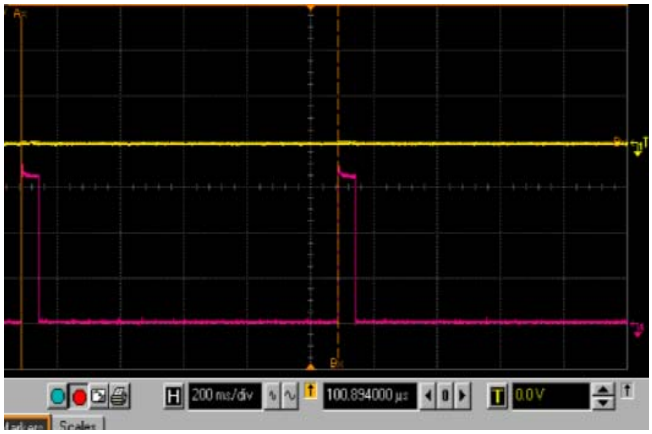


FIGURE 15. ISL9492 SHORTED TO GND IN DYNAMIC MODE. TOP IS VLNB AND BOTTOM IS LOAD CURRENT WAVEFORM (200mA/DIV)

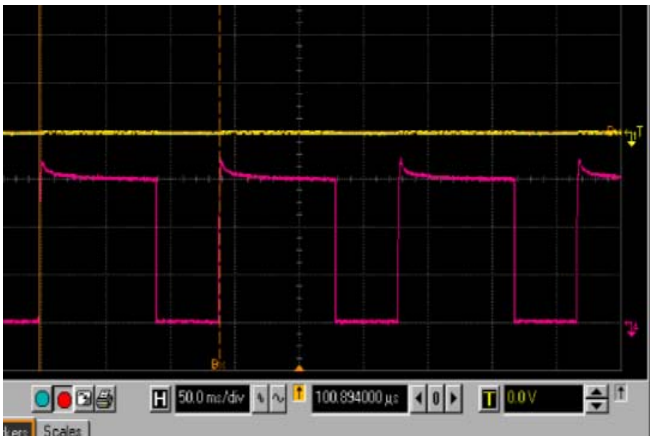


FIGURE 16. ISL9492 SHORTED TO GND IN STATIC MODE CAUSES THERMAL SHUTDOWN. TOP IS VLNB AND BOTTOM IS LOAD CURRENT WAVEFORM (200mA/DIV)

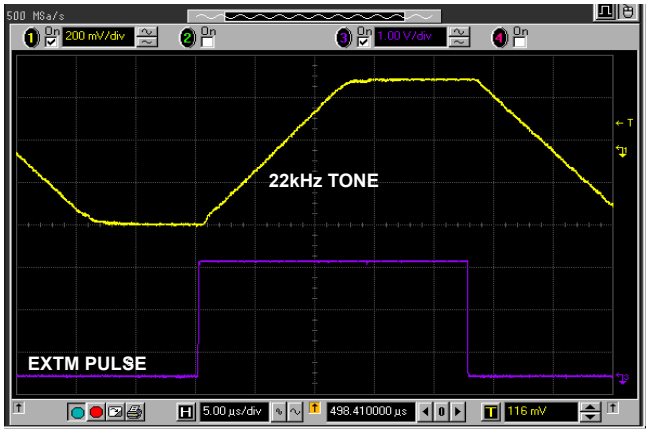


FIGURE 17. ISL9492 EXTM SIGNAL GOING LOW TO HIGH AND HIGH TO LOW vs TONE ENABLED ON OUTPUT DELAY

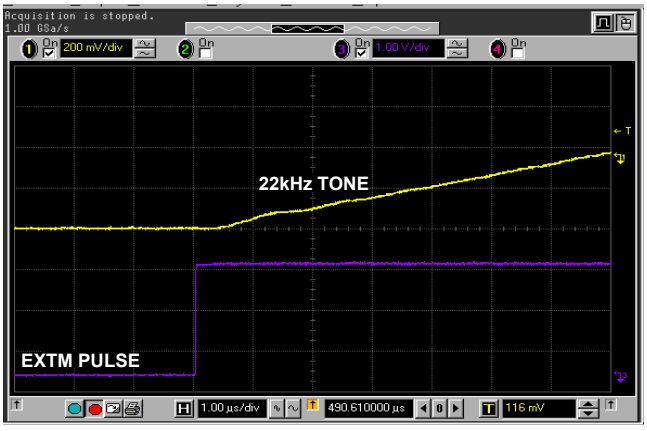


FIGURE 18. EXTM GOING HIGH TO TONE ENABLED ON THE OUTPUT DELAY IS ~500ns

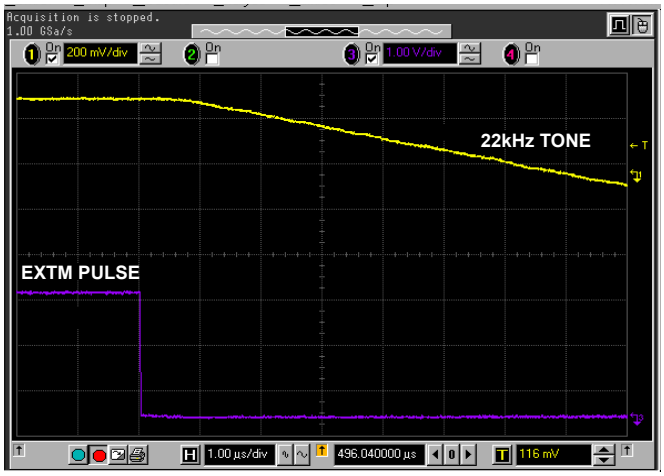


FIGURE 19. EXTM GOING LOW TO TONE DISABLED ON THE OUTPUT DELAY IS ~750ns

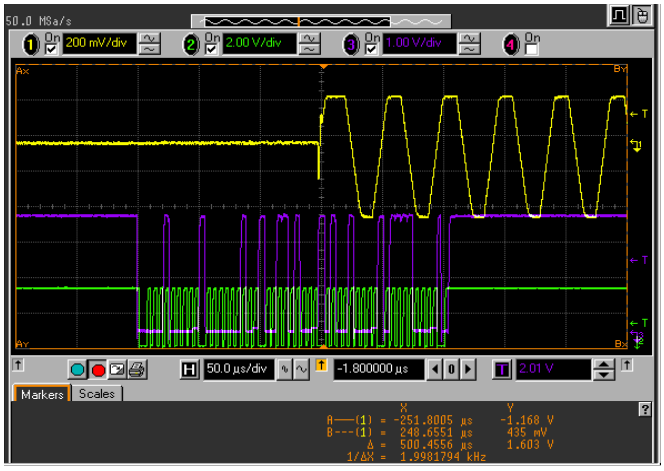


FIGURE 20. ISL9492 ENT BIT GOING HIGH TO TONE ENABLED ON THE OUTPUT DELAY

Typical Performance Curves (Continued)

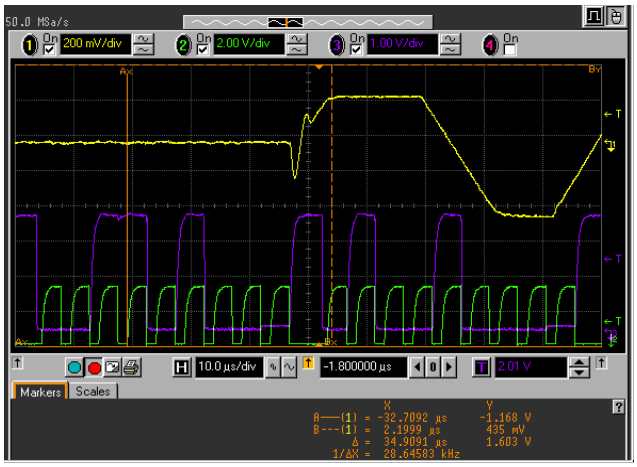


FIGURE 21. ENT BIT GOING HIGH TO TONE ENABLED ON THE OUTPUT DELAY IS ~34µs

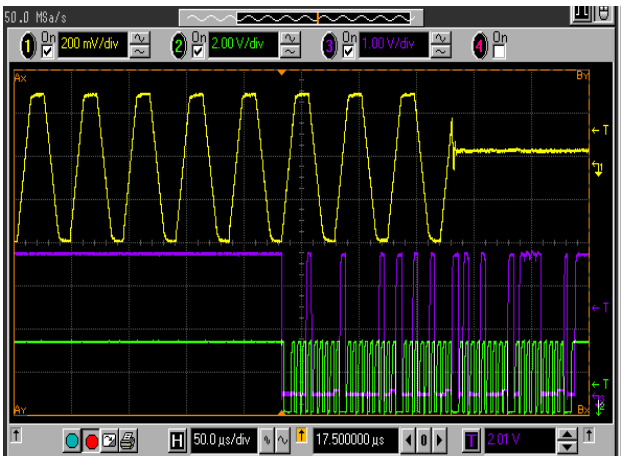


FIGURE 22. ISL9492 ENT BIT GOING LOW TO TONE DISABLED ON THE OUTPUT DELAY

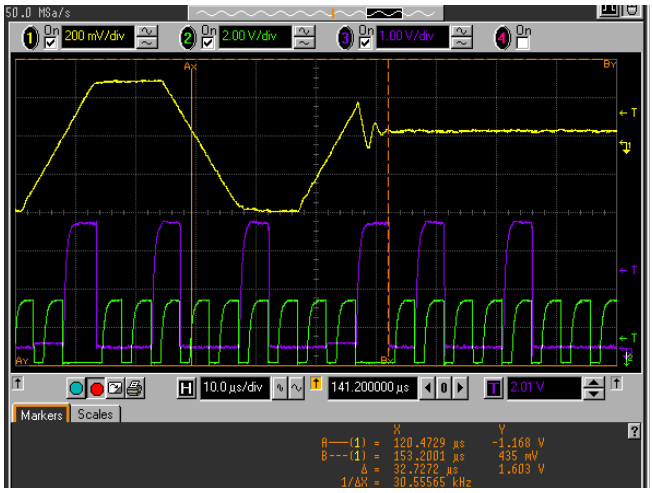


FIGURE 23. ENT BIT GOING LOW TO TONE DISABLED ON THE OUTPUT DELAY IS ~32µs

Derated Performance Curve

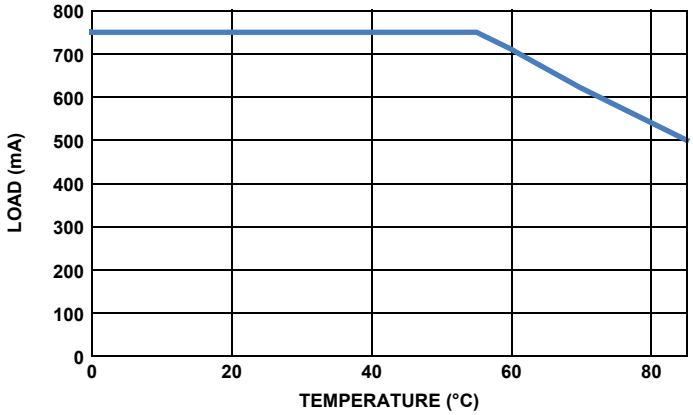


FIGURE 24. OUTPUT CURRENT DERATING

Functional Description

The ISL9492 single output voltage regulator is an ideal choice for advanced satellite set-top box and personal video recorder applications. The device utilizes built-in DC/DC step-up converters that generate a voltage for the linear regulator with minimal power dissipation. An undervoltage lockout circuit disables the device when V_{CC} drops below a fixed threshold.

DiSEqC Encoding

The tone signal can be generated in many different ways. External tone on the EXTM pin can be used when the ENT bit is low and the MSEL bit is high. The ISL9492 will inject an internal tone on V_{OUT} as long as:

- The EXTM pin is low, the ENT bit is high and the MSEL bit is low
- The ENT and MSEL bits are low and the EXTM pin is high

DiSEqC Decoder

If a tone signal is detected within the specified frequency range on TDIN thru a 10nF from V_{OUT}, the open drain pin TDOUT is asserted low. The detector threshold is 200mV (TTH bit = 0 and TXT pin is 0) in the Receive mode and 400mV (TTH = 1 or TXT = 1) in the Transmit mode.

ABYP

The ABYP pin provides 5V bias to the internal analog circuitry and the digital I^2C block and is susceptible to noise pickup due to integrated high power boost MOSFET. In order to minimize any disturbance preventing the normal operation of the chip, it is recommended to add a ferrite bead (TDK part # MMZ1608S102A) in series with the decoupling capacitor.

Device Enable

The device can be enabled or disabled through the EN and DLIN bits. When both the EN and DLIN bits are LOW (default state), both the boost converter and the linear regulator are shut down, in which case, the boost output voltage will be Vin - Vdiode and the linear regulator will be at 0V. When both the EN and DLIN bits are HIGH, both power blocks are enabled. When the EN bit is high and the DLIN bit is low, the boost circuit is enabled and the linear regulator will be disabled.

DiSEqC External MOSFET

To transmit DiSEqC tone to the outside world, the external MOSFET Q1 in the “Typical Application Schematic” on page 5 has to be turned on by pulling the TXT pin or the TTh bit high. In order to receive tone from the LNB, the TXT pin or TTH bit should be pulled low.

Linear Regulator

In order to minimize the power dissipation, the output voltage of the boost converter is regulated to a voltage slightly higher than the desired LNB output voltage. The linear regulator has the capability to sink and source current from the LNB where this highly desirable feature allows full modulation capability into capacitive loads as high as 0.75µF.

Boost Regulator Inductor and Output Capacitor Selection

The ISL9492 boost regulator is internally compensated and relies on the inductor and output capacitor value for overall loop stability. It is recommended that the boost inductor be in the 8µH to 15µH range and the output capacitor in the 50µF to 200µF range with a worst case ESR of 40mΩ to 125mΩ. In case if the output capacitor is an Aluminum Electrolytic type, special attention should be paid to the increased ESR at low temperature due to freezing liquid electrolyte at around 0°C. The increased ESR can interfere with the overall stability by introducing a zero much sooner than anticipated at $1/2\ \pi * R\_ESR * C_{OUT}$. The following are some recommended part numbers which meet the above mentioned criteria:

- L = 10µH inductor - Sumida # CDR7D43MN-100
- C_{OUT} = 180µF capacitor - Panasonic # EKZE500ELL181MH20D

In case the output capacitor ESR is outside the recommended range, an additional external pole comprised of Rp and Cp needs to be inserted on VSWSNS as shown in Figure 25 so that it cancels the ESR zero. Assuming C_{OUT}_ESR = 230mΩ, C_{OUT} = 100µF and Rp = 100Ω, then Cp is calculated to be 0.22µF, as shown in Equation 1. The voltage rating on this capacitor should be in the 25V to 35V range since it is connected to the boost V_{OUT} rail.

$$Cp = \frac{ESR \times Cout}{100} \quad \text{(EQ. 1)}$$

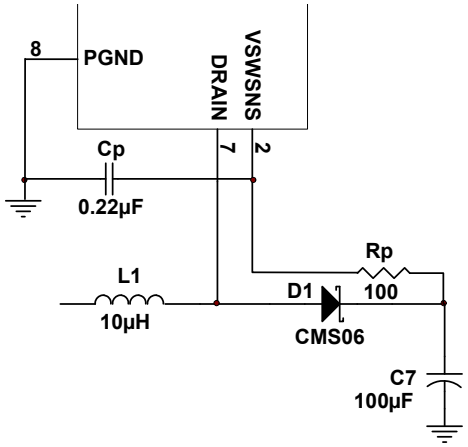


FIGURE 25. ADDITIONAL POLE ADDED BY RP AND CPD CND CP TO COMPENSATE HIGH ESR ZERO

Output Timing

The output voltage rise and fall times can be set by an the external capacitor on the TCAP pin. The output rise and fall times is given by Equation 2:

$$C = \frac{10T}{\Delta V} \quad \text{(EQ. 2)}$$

Where C is the TCAP value in nF, T is the required transition time in ms and ΔV is the differential transition voltage from low output voltage range to the high output range in Volts. Too large a value of TCAP prevents the output from rising to the nominal value, within the soft-start time when the error amplifier is released. Too small a value of the TCAP can cause high peak currents in the boost circuit. For example, a 10V/ms slew on a 80µF VSW

capacitor with an inductor of 15µH can cause a peak inductor current of approximately 1A.

Output Voltage Selection

The device offers a flexible means to select the output voltage. When VSPEN is LOW, the output voltage can be selected by the SVTOP pin. In this case, when the SVTOP pin is LOW, the output voltage is either 13V or 14V, depending on the VBOT bit. When the SVTOP pin is HIGH, the output voltage is either 18V or 20V depending on the VTOP bit. When VSPEN is HIGH, the SVTOP pin is ignored, and the output is selected by both the VTOP and the VBOT bits. See Table 1.

TABLE 1.

VSPEN	VTOP	VBOT	SVTOP	VOUT
0	X	0	0	13.5V
0	X	1	0	14.2V
0	0	X	1	18.5V
0	1	X	1	20V
1	0	0	X	13.5V
1	0	1	X	14.2V
1	1	0	X	18.5V
1	1	1	X	20V

Current Limiting

Both the boost converter and the linear regulator have independent current limit. In the boost converter, this is achieved through cycle-by-cycle internal current limit. In the linear regulator, current limit threshold is set by the ISELH and ISELL bits (see Table 9). At any time, when the linear regulator goes into current limit and the DCL bit is high, the OLF bit is set. OLF bit is not affected by current limit occurred through the boost converter. In this mode, the part will deliver the full specified current for 50ms. During this time, if the current limit condition disappears, the OLF bit will be cleared and the part restarts. If the part is still in current limit after this time period, the linear regulator and boost converter will automatically disable for 900ms to prevent the part from overheating. After this shutdown period, the ISL9492 will automatically re-enable itself and the above described sequence will repeat. This current limit method is also called “Dynamic current limit”. The ISL9492 can also be configured so when a current limit is detected, the part rather than disabling the linear regulator after 50ms stays powered up and delivers the programmed load current in a constant current mode. This mode can be enabled by writing a “0” in the DCL bit. In this mode, the OLF bit is set high to indicate an overcurrent condition. This current limiting method is also called “Static Current Limit”. This method can be used to enable any loads which are highly capacitive during start-up.

Thermal Protection and Fault Indicator

When the junction temperature reaches the critical temperature, the boost converter and the linear regulator are immediately disabled with the OTF bit set. Only when the junction temperature cools down to a lower temperature threshold specified will this bit will be cleared and the part be allowed to restart.

When any of the fault handling flags (OTF, CABF, OUVF, OLF, BCF) are set, the fault indicator pin $\overline{FLT}$ will go LOW. This status output can serve as an interrupt signal to a microcontroller. The OUVF bit will be low indicating the output voltage is good and within 90% of final steady-state DC value, so during output voltage transitions, this bit will go high indicating output voltage is out of regulation followed by going low; see Figure 4. This bit can be used as an output for the system to know that the LNB output voltage is in regulation and it can start communicating with the LNB by transmitting the 22kHz tone. The system will be able to apply internal or external tone only after the OUVF bit is pulled low and during tone application, the bit will stay latched low. BCF bit is set when back bias is detected; OLF bit is set when an overcurrent is detected; CABF bit is set low when there is maximum of 50mA of load current; OTF bit is set when the die junction temperature reaches +150°C; all these registers are activated after the LDO is enabled by the DLIN bit in SR4 register.

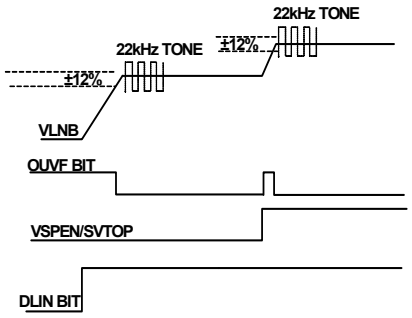


FIGURE 26. OUTPUT POWER SEQUENCE

I²C Bus Interface for ISL9492

(Refer to Philips I²C Specification, Rev. 2.1)

Data transmission from main microprocessor to the ISL9492 and vice versa takes place through the two-wire I²C bus interface, consisting of the two lines SDA and SCL. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. (Pull-up resistors to positive supply voltage must be externally connected). When the bus is free, both lines are HIGH. The output stages of ISL9492 will have an open drain/open collector in order to perform the wired-AND function. Data on the I²C bus can be transferred up to 100kbps in the standard-mode or up to 400kbps in the fast-mode. The level of logic “0” and logic “1” is defined in the “Electrical Specifications” table on page 8. One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 27.

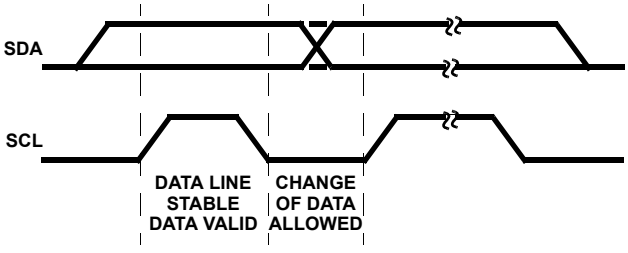


FIGURE 27. DATA VALIDITY

START and STOP Conditions

As shown in Figure 28, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

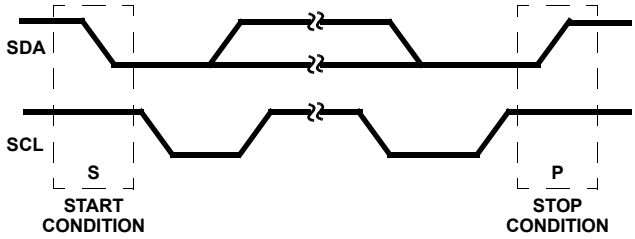


FIGURE 28. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (Figure 29). The peripheral that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Note that set-up and hold times must also be taken into account.)

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer. The ISL9492 will not generate the acknowledge if the POWER OK signal from the UVLO is LOW.

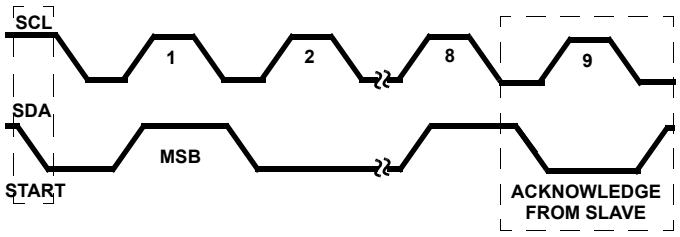


FIGURE 29. ACKNOWLEDGE ON THE I^2C BUS

Transmission Without Acknowledge

Avoiding detection of the acknowledgement, the microprocessor can use a simpler transmission; it waits one clock without checking the slave acknowledging, and sends the new data.

This approach, however, is less protected from error and decreases the noise immunity.

ISL9492 Software Description

Interface Protocol

The interface protocol is comprised of the following, as shown in Table 2:

- A start condition (S)
- A chip address byte (MSB on left; the LSB bit determines read (1) or write (0) transmission) (the assigned I^2C slave address for the ISL9492 is 0001 0XX)
- A sequence of data (1 byte + Acknowledge)
- A stop condition (P)

TABLE 2. INTERFACE PROTOCOL

S	0	0	0	1	0	A1	A0	R/W	ACK	Data (8 bits)	ACK	P

System Register Format

- R, W = Read and Write bit
- R = Read-only bit

All bits reset to 0 at Power-On

TABLE 3. STATUS REGISTER (SR1)

R, W	R, W	R, W	R	R	R	R	R
SR1H	SR1M	SR1L	OTF	CABF	OUVF	OLF	BCF

TABLE 4. TONE REGISTER (SR2)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR2H	SR2M	SR2L	ENT	MSEL	TTH	Res*	Res*

TABLE 5. COMMAND REGISTER (SR3)

R, W	R, W	R, W	R,W	R, W	R,W	R, W	R, W
SR3H	SR3M	SR3L	Res*	VSPEN	DCL	ISELH	ISELL

TABLE 6. CONTROL REGISTER (SR4)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR4H	SR4M	SR4L	EN	DLIN	Res*	VTOP	VBOT

Transmitted Data (I^2C Bus WRITE Mode)

When the R/W bit in the chip is set to 0, the main microprocessor can write on the system registers (SR2 thru SR4) of the ISL9492 via I^2C bus. These will be written by the microprocessor as shown in Table 7. The spare bits of registers are reserved for further use.

TABLE 7. STATUS REGISTER SR1 CONFIGURATION

SR1H	SR1M	SR1L	OTF	CABF	OUVF	OLF	BCF	FUNCTION
0	0	0	X	X	X	X	X	SR1 selected
0	0	0	X	X	X	0	X	No current limit detected
0	0	0	X	X	X	1	X	Current limit detected in the linear regulator
0	0	0	X	X	X	X	0	No back-bias detected
0	0	0	X	X	X	X	1	Back-bias detected
0	0	0	X	X	0	X	X	V_{OUT} within specified range
0	0	0	X	X	1	X	X	V_{OUT} not within specified range
0	0	0	X	0	X	X	X	Cable connected
0	0	0	X	1	X	X	X	Cable open
0	0	0	0	X	X	X	X	Junction normal temperature
0	0	0	1	X	X	X	X	Junction over-temperature reached

TABLE 8. TONE REGISTER SR2 CONFIGURATION

SR2H	SR2M	SR2L	ENT	MSEL	TTH	Res*	Res*	FUNCTION
0	0	1	X	X	X	0	0	SR2 selected
0	0	1	0	0	X	0	0	Tone generated internally according to the state of the EXTMpin
0	0	1	0	1	X	0	0	Tone supplied by EXTM pin
0	0	1	1	0	X	0	0	Tone generated internally regardless of the EXTM pin
0	0	1	X	X	0	0	0	Decoder Rx threshold set
0	0	1	X	X	1	0	0	Decoder Tx threshold set

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode. Res* is a reserved bit and should be “0”

TABLE 9. COMMAND REGISTER SR3 CONFIGURATION

SR3H	SR3M	SR3L	Res*	VSPEN	DCL	ISELH	ISELL	FUNCTION
0	1	0	0	X	X	X	X	SR3 selected
0	1	0	0	X	1	X	X	Dynamic current limit
0	1	0	0	X	0	X	X	Static Current limit
0	1	0	0	X	X	1	1	VOUT current limit set to 400mA
0	1	0	0	X	X	1	0	VOUT current limit set to 670mA
0	1	0	0	X	X	0	1	VOUT current limit set to 790mA
0	1	0	0	X	X	0	0	VOUT current limit set to 950mA
0	1	0	0	0	X	X	X	SVTOP pin enabled
0	1	0	0	1	X	X	X	SVTOP pin disabled

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode. Res* is a reserved bit and should be “0”

TABLE 10. CONTROL REGISTER SR4 CONFIGURATION

SR4H	SR4M	SR4L	EN	DLIN	Res*	VTOP	VBOT	FUNCTION
0	1	1	X	X	0	X	X	SR4 selected
0	1	1	0	X	0	X	X	Device disabled
0	1	1	1	X	0	X	0	V_{OUT} = 13.4V if VSPEN = 0 and SVTOP = 0
0	1	1	1	X	0	X	1	V_{OUT} = 14.4V if VSPEN = 0 and SVTOP = 0
0	1	1	1	X	0	0	X	V_{OUT} = 18.7V if VSPEN = 0 and SVTOP = 1
0	1	1	1	X	0	1	X	V_{OUT} = 20V if VSPEN = 0 and SVTOP = 1
0	1	1	1	X	0	0	0	V_{OUT} = 13.4V if VSPEN = 1 and SVTOP = X
0	1	1	1	X	0	0	1	V_{OUT} = 14.4V if VSPEN = 1 and SVTOP = X
0	1	1	1	X	0	1	0	V_{OUT} = 18.7V if VSPEN = 1 and SVTOP = X
0	1	1	1	X	0	1	1	V_{OUT} = 20V if VSPEN = 1 and SVTOP = X
0	1	1	1	0	0	X	X	Internal linear regulator is turned-off but boost circuit is on
0	1	1	1	1	0	X	X	Internal linear regulator is turned-on and boost circuit is on

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode.Res* is a reserved bit and should be “0”

Received Data (I²c bus READ MODE)

The ISL9492 can provide to the master a copy of the system register information via the I^2C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following Master generated clock bits, the ISL9492 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the ISL9492.
- Not acknowledge, stopping the read mode communication.

The read only bits of the register SR1 convey diagnostic information about the ISL9492, as indicated in Table 7.

Power–On I^2C Interface Reset

The I^2C interface built into the ISL9492 is automatically reset at power-on. The I^2C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I^2C commands and the system register SR1 thru SR4 are all initialized to all zero, thus keeping the power blocks disabled. Once the V_{CC} rises above UVLO, the POWER OK signal to the I^2C is asserted high, and the I^2C interface becomes operative and the SR’s can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the Power-On reset circuit. (I^2C comes up with EN = 0; EN goes HIGH at the same time as (or later than) all other I^2C data for that PWM becomes valid).

ADD0 and ADD1 Pins

Connecting these pins to GND, the chip I^2C interface address is 0001000, but, it is possible to choose between four different addresses by setting these pins to the logic levels indicated in Table 11.

TABLE 11. ADDRESS PIN CHARACTERISTICS

V_{ADDR}	ADD1	ADD0
V_{ADDR}-1 “0001000”	0	0
V_{ADDR}-2 “0001001”	0	1
V_{ADDR}-3 “0001010”	1	0
V_{ADDR}-4 “0001011”	1	1

Layout Guidelines

It is highly recommended to connect GND of C1, C6, C14, C2, C15, pins 8 and 9 in a tight formation on the top layer as shown in red circles in Figure 30 and needs to be returned back to the input power supply GND post, which is on the bottom left of the ISL9492QFNEVAL1 evaluation board. The ground side of the components in green circles along with the epad can be dropped to the internal ground plane which connects to the top ground plane with 8-10 vias near C1 to form a star ground connection. Refer to AN1629 “ISL9492 Quick Start Guide”

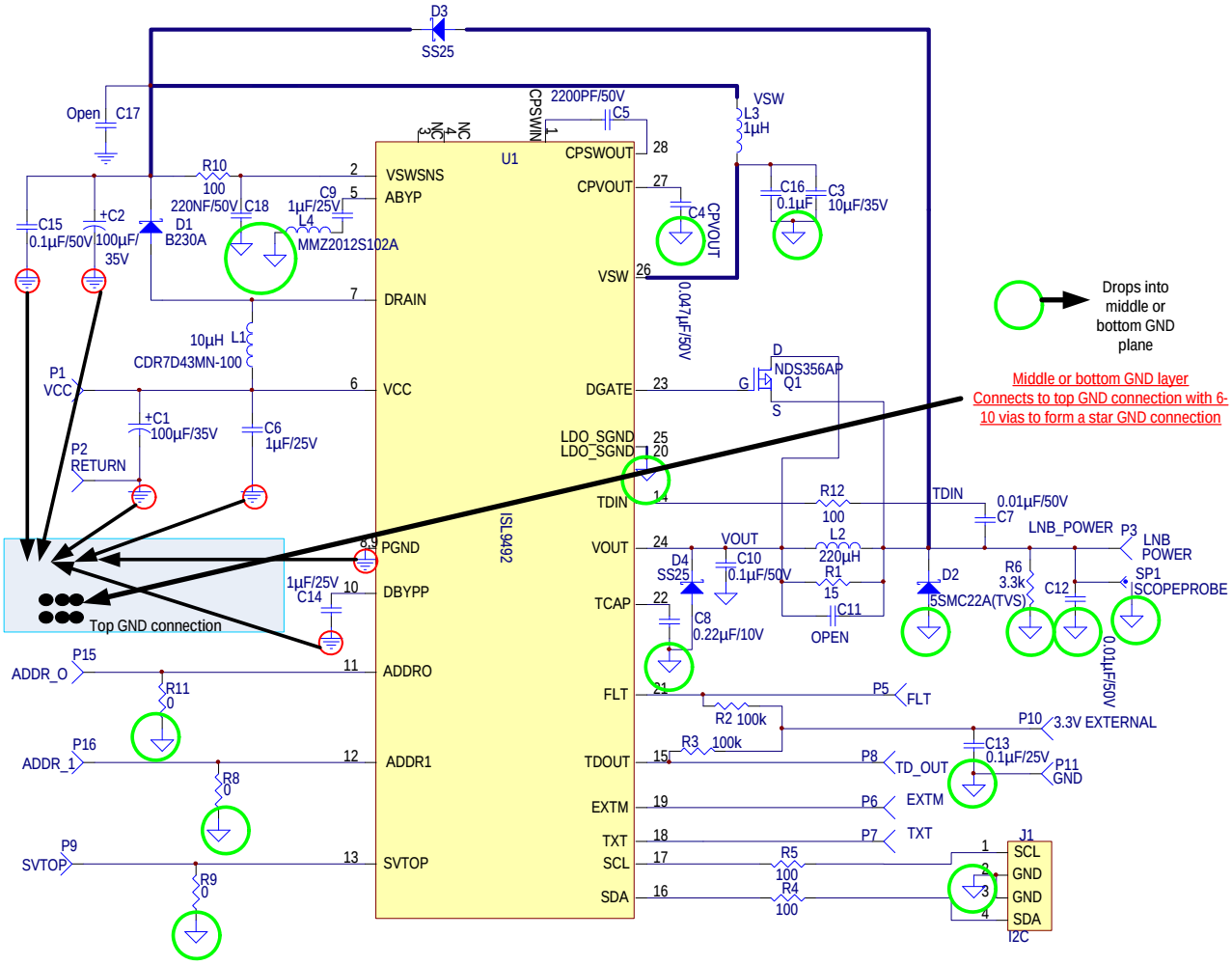


FIGURE 30. ISL9492 STAR GROUND CONNECTION ILLUSTRATION

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/4/11	FN6547.1	Changed in Typical Application Schematic on page 1 and page 5 bottom D3 which was duplicated to D4.
3/2/11		Added Layout Guidelines on page 19.
1/28/11	FN6547.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL9492

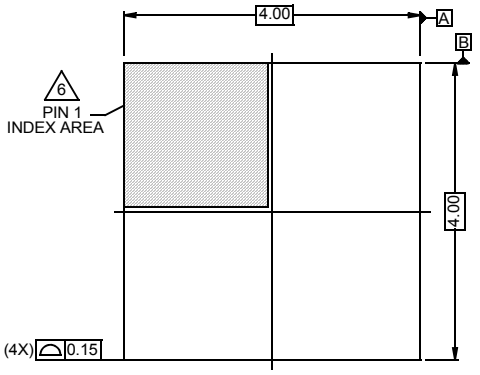
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

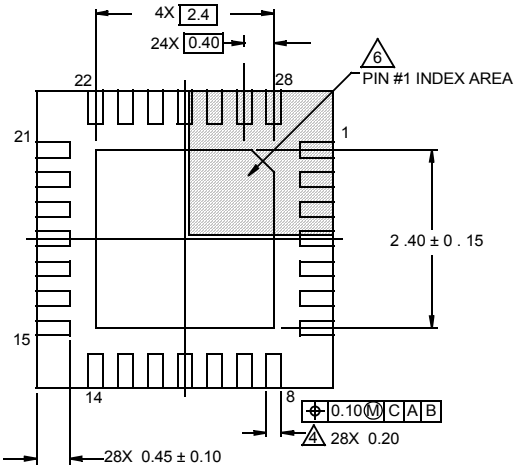
Package Outline Drawing

L28.4x4A

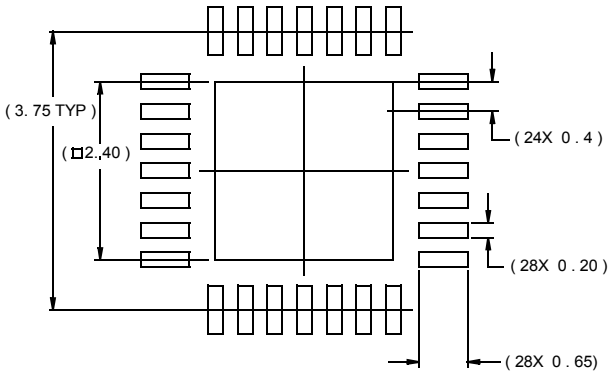
28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 12/08



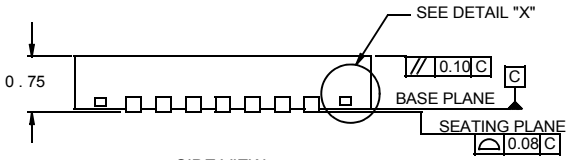
TOP VIEW



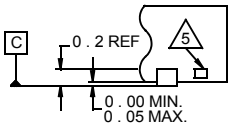
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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