NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL98603

5-Channel Integrated LCD Supply

The ISL97653A represents a fully integrated supply IC for LCD-TV applications. With an input operating range of 4V to 14V, both commonly used LCD-TV input supplies, 5V and 12V, are supported. An A_{VDD} supply up to 20V is generated by a high-performance PWM BOOST converter with an integrated 4.4A FET. V_{ON} is generated using an integrated charge pump with on-chip diodes and can be modulated using an on-chip V_{ON} slice control circuit. V_{OFF} is generated using an integrated charge pump controller. Additionally, the chip allows for two logic supplies. A buck regulator with an included 2.5A high side switch is used for the main logic output and an internal LDO controller can be used to generate a second logic LDO output.

To facilitate production test, an integrated HVS circuit is included which can provide high voltage stress of the LCD panel.

An on-board temperature sensor is also provided for system thermal management control.

The ISL97653A is packaged in a 40 Ld 6mmx6mm QFN package and is specified for operation over the -40°C to +105°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97653AIRZ	97653A IRZ	40 Ld 6X6 QFN	L40.6X6
ISL97653AIRZ-T*	97653A IRZ	40 Ld 6X6 QFN (Tape and Reel)	L40.6X6
ISL97653AIRZ-TK*	97653A IRZ	40 Ld 6X6 QFN (Tape and Reel)	L40.6X6

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

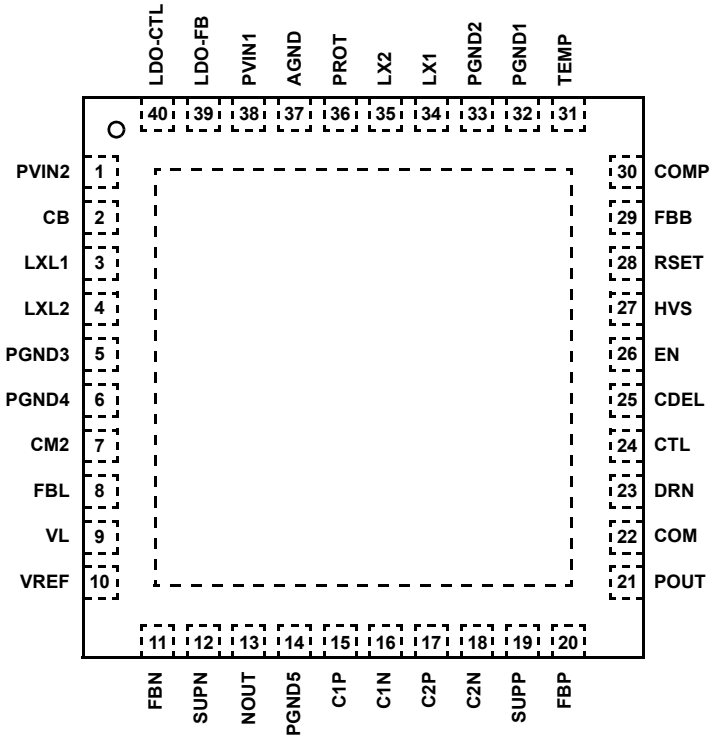
- 5V to 14V Input Supply
- Integrated 4.4A Boost Converter
- Integrated V_{ON} Charge Pump and V_{ON} Slice Circuit
- Integrated V_{OFF} Charge Pump Output
- Integrated 2.5A Buck Converter
- LDO Controller for an Additional Logic Supply
- High Voltage Stress (HVS) Test Mode
- Thermal Shutdown
- 40 Ld QFN (6mmx6mm) Package
- Pb-Free (RoHS Compliant)

Applications

- LCD-TVs
- Industrial/Medical LCD Displays

Pinout

ISL97653A
(40 LD 6X6 QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Maximum Pin Voltages, All Pins Except Below 6.5V
LX1, LX2, SUPP, SUPN, NOUT, PROT, C1N, C2N 24V
PVIN1, PVIN2, LXL1, LXL2 . . . . . 16.8V
EN, CTL 16.5V
DRN, POUT, COM, C1P, C2P. 33V
CB 21V

Recommended Operating Conditions

Input Voltage Range, VIN . . . . . 4V to 14V
Input Capacitance, C_{IN} 2x10µF
Boost Output Voltage Range, A_{VDD} . . . . . +20V
Output Capacitance, C_{OUT} 3x22µF
Boost Inductor, L1 . . . . . 3.3µH-10µH
V_{ON} Output Range, V_{ON} . . . . . .+15V to +30V
V_{OFF} Output Range, V_{OFF} . . . . . .-15V to -5V
Logic Output Voltage Range, V_{LOGIC} . . . . . .+1.5V to +3.3V
Buck Inductor, L2 . . . . . 3.3µH to 10µH

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6x6 QFN Package (Notes 1, 2)	29	1

Operating Ambient Temperature Range . . . . . -40°C to +105°C
Operating Junction Temperature . . . . . -40°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = 12V, V_{BOOST} = V_{SUPN} = V_{SUPP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
SUPPLY PINS						
V_{IN}	Supply Voltage		4		14	V
I_S	Quiescent Current	Enabled, no switching		4	5	mA
		Disabled		2.7	3.5	mA
F_{SW}	Switching Frequency		580	680	780	kHz
V_{REF}	Reference Voltage	T_A = +25°C	1.190	1.215	1.240	V
			1.187	1.215	1.243	V
VLOR	Undervoltage Lockout Threshold	V_L rising	3.4	3.55	3.7	V
VLOF	Undervoltage Lockout Threshold	V_L falling	2.9	3.0	3.2	V
	Thermal Shutdown	Temperature rising		150		°C
	Thermal Shutdown Hysteresis			20		°C
LOGIC SIGNALS HVS, EN, CTL						
Logic Input High			2.0			V
Logic Input Low					0.4	V
Pull-down Resistance			115	174	250	kΩ
HVS, RSET						
RSET	RSET Pull-down Resistance	HVS = HIGH		200		Ω
I_{RSET}	RSET Leakage Current	HVS = LOW, V_{RSET} = 1.2V			0.4	µA
A_{VDD} BOOST						
DLIM	Min Duty Cycle			8.5	12	%
	Max Duty Cycle			90		%

Electrical Specifications V_{IN} = 12V, V_{BOOST} = V_{SUPN} = V_{SUPP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
V_{BOOST}	Boost Output Range			20		V
EFF_{BOOST}	Boost Efficiency	VIN = 12V, V_{BOOST} = 15V		90+		%
V_{FB}	Boost Feedback Voltage	T_A = +25°C	1.203	1.215	1.227	V
			1.198	1.215	1.232	V
I_{BOOST}	Boost FET Current Limit		3.7	4.4	5.1	A
$r_{DS(ON)-BOOST}$	Switch ON-Resistance			93	200	mΩ
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation - Boost			0.08	0.15	%
$\Delta V_{BOOST}/\Delta I_{OUT}$	Load Regulation - Boost	Load 100mA to 200mA		0.004	1	%
LOGIC BUCK						
EFF_{BUCK}	Buck Efficiency	VIN = 5V, V_{LOGIC} = 3.3V		90+		%
I_{BUCK}	Buck FET Current Limit		2.6		4.7	A
$r_{DS(ON)-BUCK}$	Switch On Resistance			150	210	mΩ
$\Delta V_{LDO}/\Delta I_{OUT}$	Load Regulation - Buck	Load 100mA to 500mA		0.5	1	%
V_{FL}	Feedback Voltage	T_A = +25°C	1.195	1.215	1.235	V
			1.189	1.215	1.241	V
V_{ON} CHARGE PUMP						
ILoad_PCP_min	External Load Driving Capability	V_{ON} = 24V (2X Charge Pump)	40			mA
		V_{ON} = 28V (3X Charge Pump)	40			mA
V_{FBP}	Feedback Voltage, I_{ON} = 1mA	T_A = +25°C	1.195	1.215	1.235	V
			1.189	1.215	1.241	V
r_{ON} (VSUP_SW)	ON Resistance of V_{SUP} Input Switch	I(switch) = +40mA		10	17	Ω
r_{ON} (C1/2-)H	High-Side Driver ON-Resistance at C1- and C2-	I(C1/2-) = +40mA			30	Ω
r_{ON} (C1/2-)L	Low-Side Driver ON-Resistance at C1- and C2-	I(C1/2-) = -40mA		4	10	Ω
V_{ON} Load Reg	V_{ON} Output Load Regulation	I_{ON} = 10mA to 40mA		0.3		%
V(diode)	Internal Schottky Diode Forward Voltage Drop	I(diode) = +40mA		700	800	mV
V_{OFF} CHARGE PUMP						
ILoad_NCP_min	External Load Driving Capability	SUPN > 13.5V VOFF = -8V	100	120		mA
V_{FBN}	Feedback Voltage, I_{OFF} = 10mA	T_A = +25°C	0.173	0.203	0.233	V
			0.171	0.203	0.235	V
r_{ON} (NOUT)H	High-Side Driver ON-Resistance at NOUT	I(NOUT) = +60mA			10	Ω
r_{ON} (NOUT)L	Low-Side Driver ON-Resistance at NOUT	I(NOUT) = -60mA			5	Ω
V_{OFF} Load Reg	V_{OFF} Output Load Reg	I_{OFF} = 10mA to 100mA, T_A = +25°C			2.4	%
LDO Controller						
I_{DRVP}	Sink Current	V_{FBP} = 1.1V, V_{LDO_CTL} = 10V	12	15		mA

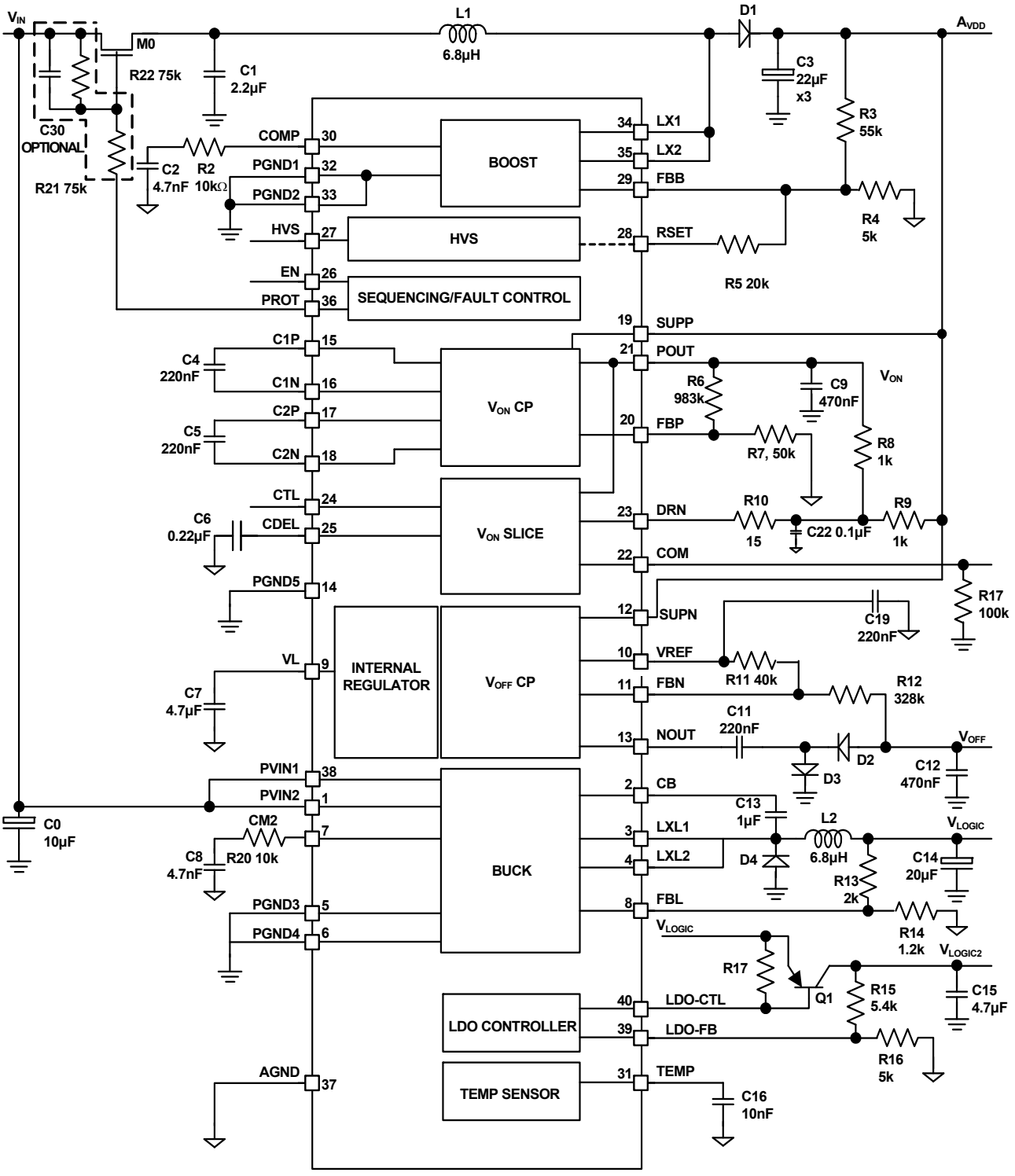
Electrical Specifications V_{IN} = 12V, V_{BOOST} = V_{SUPN} = V_{SUPP} = 15V, V_{ON} = 25V, V_{OFF} = -8V, over-temperature from -40°C to +105°C, unless otherwise stated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
LDO-FB	Feedback Voltage w/transistor load 1mA	T_A = +25°C	1.191	1.215	1.239	V
			1.189	1.215	1.241	V
FAULT DETECTION THRESHOLDS						
T_off	Thermal Shut-Down (latched and reset by power cycle or EN cycle)	Temperature rising		150		°C
Vth_A_{VDD}(FBB)	A_{VDD} Boost Short Detection	V(FBB) falling less than		0.9		V
Vth_POUT (FBP)	P_{OUT} Charge Pump Short Detection	V(FBP) falling less than		0.9		V
Vth_NOUT (FBN)	N_{OUT} Charge Pump Short Detection	V(FBN) rising more than		0.4		V
V_{ON} Slice POSITIVE SUPPLY = V(POUT)						
I(POUT)_slice	V_{ON} Slice Current from POUT Supply	CTL = VDD, sequence complete		400	500	µA
		CTL = AGND, sequence complete		150	200	µA
r_{ON} (POUT-COM)	ON-Resistance between POUT-COM	CTL = VDD, sequence complete		5	10	Ω
r_{ON} (DRN-COM)	ON-Resistance between DRN-COM	CTL = AGND, sequence complete		30	60	Ω
rON_COM	ON-Resistance between DRN-COM and PGND		200	260	400	Ω
PROT						
I_{PROT_ON}	PROT Pull-Down Current or Resistance when Enabled by the Start-U	V_{PROT} > 0.9V	38	50	60	µA
		V_{PROT} < 0.9V	500	760	1000	Ω
I_{PROT_OFF}	PROT Pull-Up Current when Disabled	V_{PROT} < 20V	2	3	4.5	mA

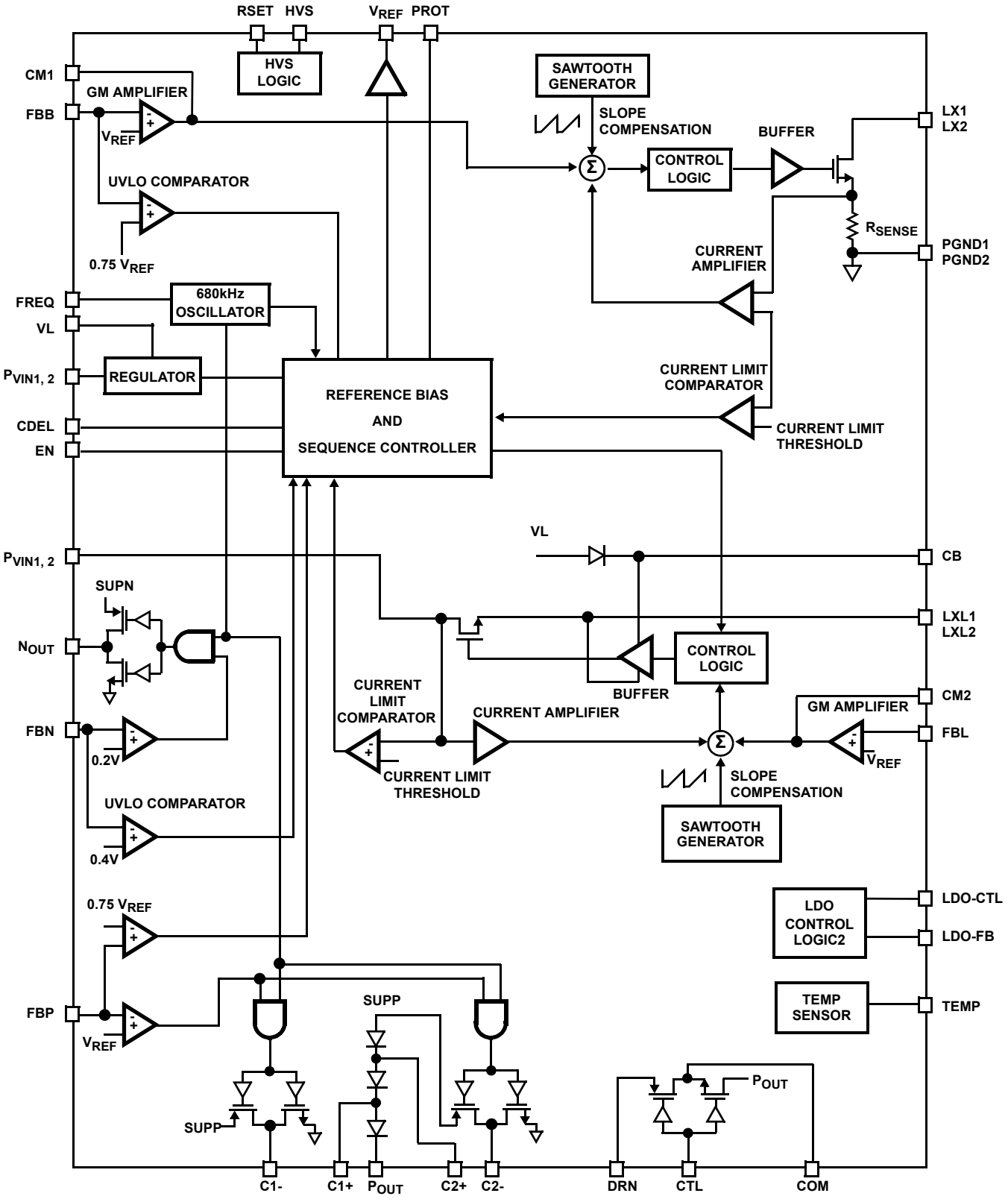
NOTE:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application Diagram



Typical Application Diagram (Continued)



Typical Performance Curves

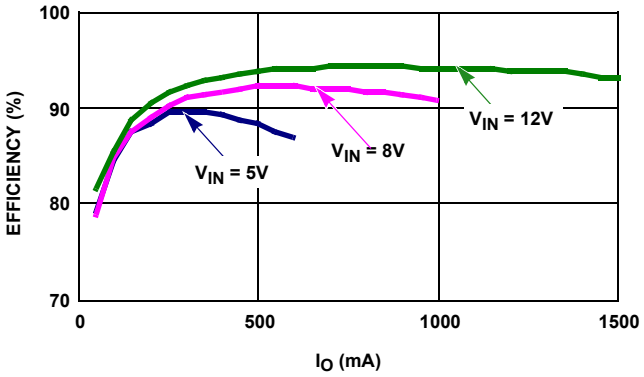


FIGURE 1. BOOST EFFICIENCY

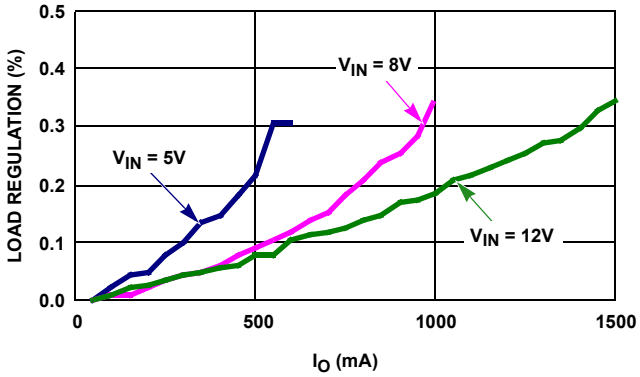


FIGURE 2. BOOST LOAD REGULATION

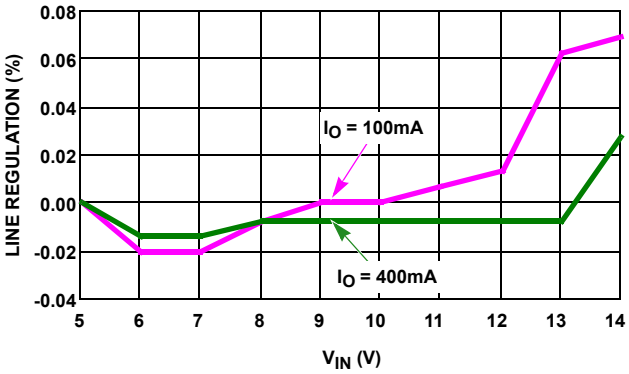


FIGURE 3. BOOST LINE REGULATION

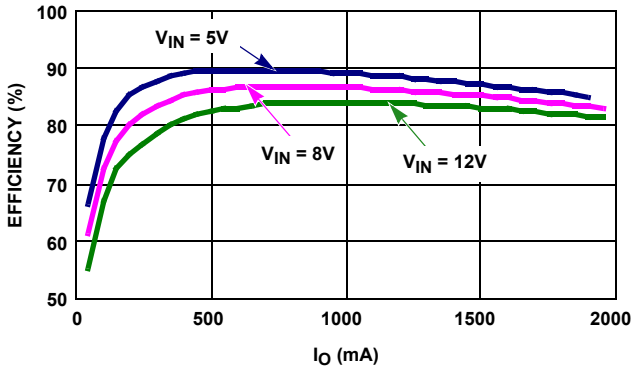


FIGURE 4. BUCK EFFICIENCY

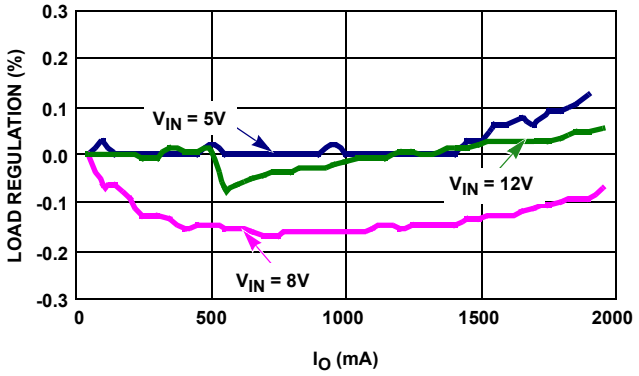


FIGURE 5. BUCK LOAD REGULATION

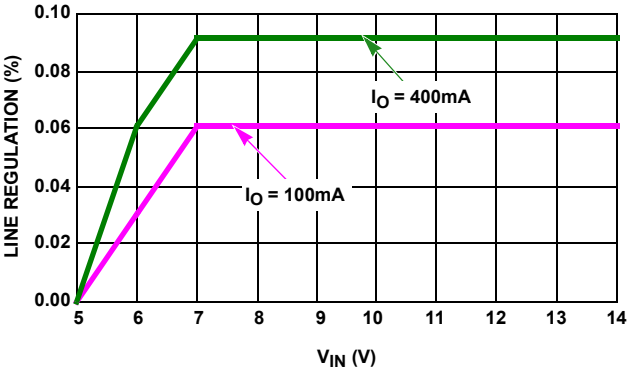


FIGURE 6. BUCK LINE REGULATION

Typical Performance Curves (Continued)

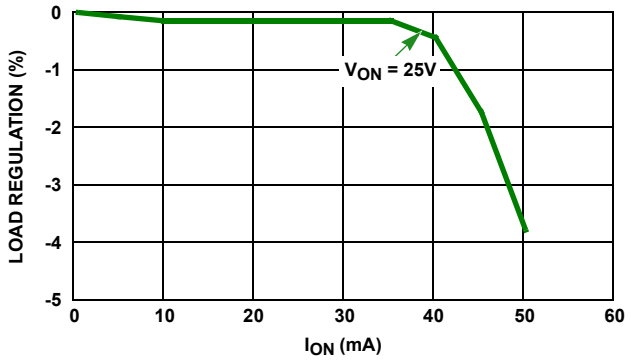


FIGURE 7. V_{ON} LOAD REGULATION

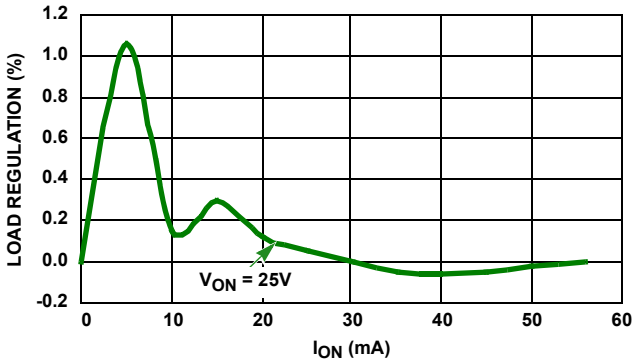


FIGURE 8. V_{OFF} LOAD REGULATION

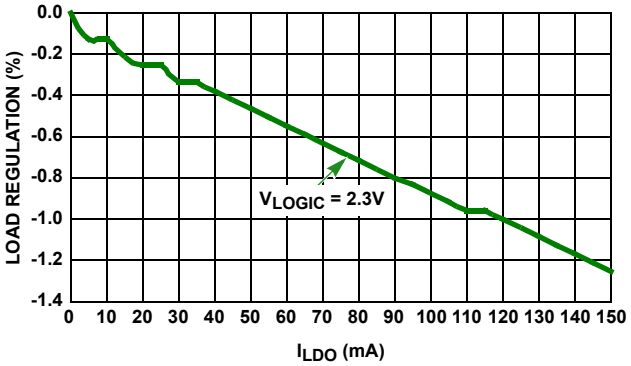


FIGURE 9. LOGIC LDO LOAD REGULATION

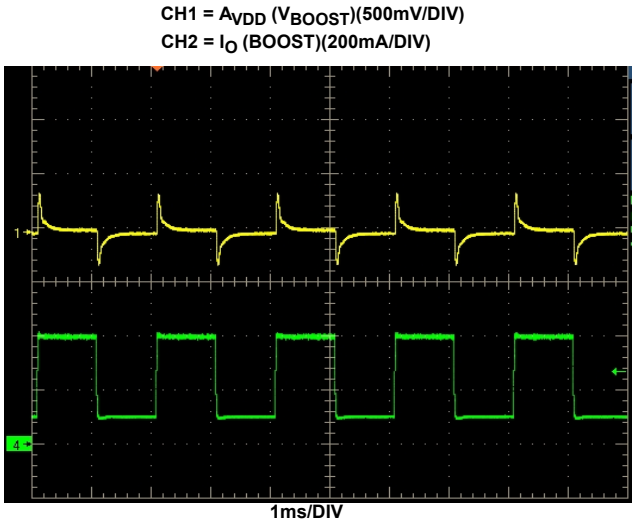


FIGURE 10. BOOST TRANSIENT RESPONSE

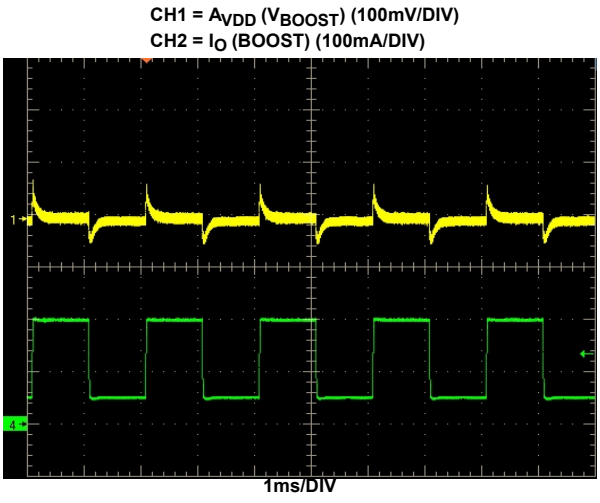


FIGURE 11. BUCK TRANSIENT RESPONSE

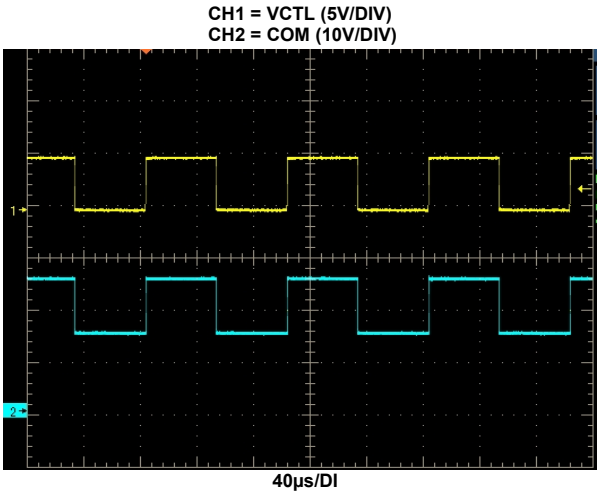


FIGURE 12. VON SLICE OPERATION

Typical Performance Curves (Continued)

Ch1 = LXL (400ns/DIV)
Ch2 = ILXL (400ns/DIV)

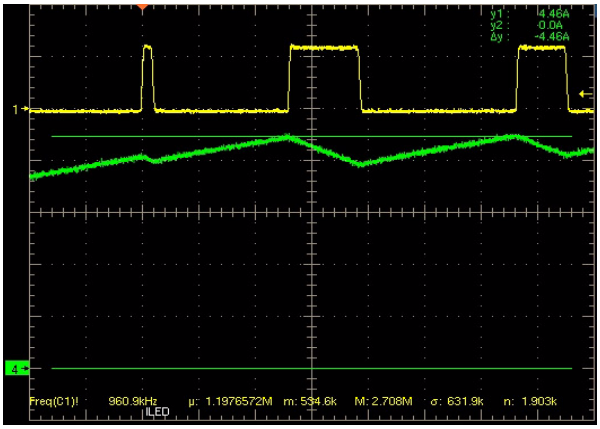


FIGURE 13. BOOST CURRENT LIMIT

Ch1 = LXL (400ns/DIV)
Ch2 = ILXL (400ns/DIV)

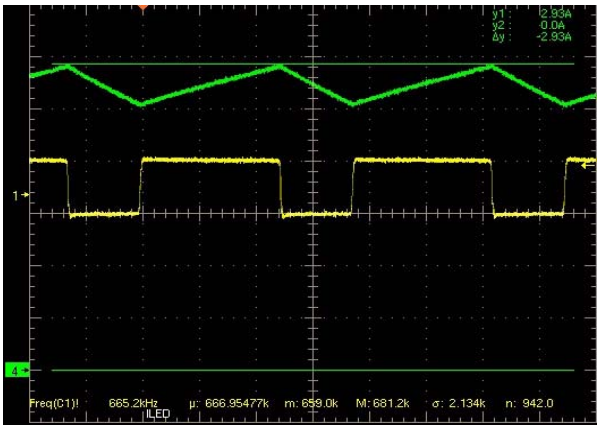


FIGURE 14. BUCK CURRENT LIMIT

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	PVIN2	Logic buck supply voltage. This is also the analog supply from which the VL is generated. Needs at least 1µF bypassing.
2	CB	Logic buck boot strap pin. Generate the gate drive voltage for the N-Channel MOSFET by connecting a 1µF cap to the switching node LXL1, 2.
3, 4	LXL1, LXL2	Logic buck switching node. Source of the high side internal power N-Channel MOSFET for the Buck.
5, 6	PGND3, PGND4	Logic buck ground pin.
7	CM2	Buck compensation pin. An RC network is recommended. Increase R for better transient response at the expense of stability.
8	FBL	Logic buck feedback pin. High impedance input to regulate at 1.215V.
9	VL	5.25V internal regulator output. Bypass with a 4.7µF capacitor. Ref voltage is generated from VL.
10	VREF	Reference voltage output. Bypass with a low valued capacitor for transients - recommend 220nF. Should not be greater than 5 times CDEL capacitor to ensure correct start-up sequence.
11	FBN	Negative charge pump feedback pin. High impedance input to regulate to 0.203V.
12	SUPN	Negative charge pump supply voltage. Can be the same as or different from A_{VDD}.
13	NOUT	Negative charge pump driver output.
14	PGND5	Charge pump ground pin.
15	C1P	Charge pump capacitor 1, positive connection.
16	C1N	Charge pump capacitor 1, negative connection.
17	C2P	Charge pump capacitor 2, positive connection.
18	C2N	Charge pump capacitor 2, negative connection.
19	SUPP	Positive charge pump supply. Can be the same as or different from A_{VDD}.
20	FBP	Positive charge pump feedback pin. High impedance input to regulate at 1.215V
21	POUT	V_{ON} charge pump output.
22	COM	High voltage switch control output. V_{ON} slice output.
23	DRN	Lower reference voltage for V_{ON} slice output. Usually connected to A_{VDD}.
24	CTL	Input control pin for V_{ON} slice output.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
25	CDEL	V_{ON} slice control delay input. Minimum 47nF. Recommend 220nF but is only limited by leakage in the cap reaching µA levels.
26	EN	Chip enable (active high). Can be driven to VIN levels.
27	HVS	High-voltage stress input select pin. High selects high voltage mode.
28	RSET	Voltage set pin for HVS test. RSET connects to ground in the high voltage mode - RSET high.
29	FBB	A_{VDD} boost feedback pin. High impedance input to regulate at 1.215V.
30	COMP	Boost compensation network pin. An RC network is recommended. Increase R for better transient response at the expense of stability. R = 0Ω is recommended for 4.4A Boost requirements.
31	TEMP	Temperature sensor output voltage. An analog voltage from 0V to 3V for temperatures of -40°C to +150°C.
32, 33	PGND1, PGND2	Boost ground pins.
34, 35	LX1, LX2	Boost switch output. Drain of the internal power NMOS for the Boost.
36	PROT	Gate driver of the Input protection switch. Goes low when EN is high. Can be used to modulate the passive input inrush current as shown by R_{21},R_{22}, and C_{30} in the “Typical Application Diagram” on page 5.
37	AGND	Analog ground. Separate from PGND’s and star under the chip.
38	PVIN1	Logic buck supply voltage.This is also the analog supply from which the VL is generated. Needs at least 1µF bypassing.
39	LDO-FB	LDO controller feedback. High impedance input to regulate at 1.215V.
40	LDO-CTL	LDO control pin. Gate drive for the external PNP BJT.

Application Information

A_{VDD} Boost Converter

The A_{VDD} boost converter features a fully integrated 4.4A boost FET. The regulator uses a current mode PI control scheme which provides good line regulation and good transient response. It can operate in both discontinuous conduction mode (DCM) at light loads and continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{boost}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

where D is the duty cycle of the switching MOSFET.

The boost soft-start function is digitally controlled within a fixed 10ms time frame during which the current limit is increased in eight linear steps.

The boost converter uses a summing amplifier architecture for voltage feedback, current feedback, and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is triggered. Since this comparison is cycle based, the PWM output will be released after the peak current goes below the current limit threshold.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$A_{VDD} = \frac{R_3 + R_4}{R_4} \times V_{FBB} \quad \text{(EQ. 2)}$$

where R_3 and R_4 are in the “Typical Application Diagram” on page 5. Unless otherwise stated, component variables referred to in equations refer to the Typical Application Diagram.

The current through the MOSFET is limited to 4.4A peak. This restricts the maximum output current (average) based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔIL is peak to peak inductor ripple current, and is set by Equation 4. f_s is the switching frequency (680kHz).

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 4)}$$

Table 1 gives typical values (worst case margins are considered 10%, 3%, 20%, 10% and 15% on V_{IN}, V_O, L, F_{SW} and I_{OMAX}):

TABLE 1. MAXIMUM OUTPUT CURRENT CALCULATION

V_{IN} (V)	V_O (V)	L (µH)	I_{OMAX} (mA)
5	9	6.8	2215
5	12	6.8	1673
5	15	6.8	1344
12	15	6.8	3254
12	18	6.8	2670

Boost Converter Input Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage. Some capacitors are recommended in Table 2 for input capacitor.

TABLE 2. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Boost Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are recommended to match the internal slope compensation as well as to maintain a good transient response performance. The inductor must be able to handle the average and peak currents expressed in Equations 5 and 6:

$$I_{LAVG} = \frac{I_O}{1-D} \quad \text{(EQ. 5)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 6)}$$

Some inductors are recommended in Table 3.

TABLE 3. BOOST INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
10µH/ $5.1A_{PEAK}$	13x13x4.5	TDK	RLF12545T-100M5R1
5.9µH/ $6A_{PEAK}$	12.9X12.9X4	Sumida	CDEP12D38NP-5R9MB-120

Rectifier Diode (Boost Converter)

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. The following table lists two recommendations for boost converter diode.

TABLE 4. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
FYD0504SA	50V/2A	DPAK	Fairchild Semiconductor
30WQ04FN	40V/3.5A	DPAK	International Rectifier

Output Capacitor

Integrating output capacitors supply the load directly and reduce the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \quad \text{(EQ. 7)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 7 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

Table 5 shows some selections of output capacitors.

TABLE 5. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

PI Loop Compensation (Boost Converter)

The boost converter of ISL97653A can be compensated by a RC network connected from COMP pin to ground. C_2 = 4.7nF and R_2 = 0Ω to 10Ω. A RC network is used in the demo board. A higher capacitor value can be used to increase system stability.

Stability can be examined by repeatedly changing the load between 100mA and a max level that is likely to be used in the system being used. The A_{VDD} voltage should be examined with an oscilloscope set to AC 100mV/DIV and the amount of ringing observed when the load current changes. Reduce excessive ringing by reducing the value of the resistor in series with the CM1 pin capacitor.

Cascaded MOSFET Application

A 20V N-Channel MOSFET is integrated in the boost regulator. For applications requiring output voltages greater than 20V, an external cascaded MOSFET is needed as shown in Figure 15. The voltage rating of the external MOSFET should be greater than A_{VDD}.

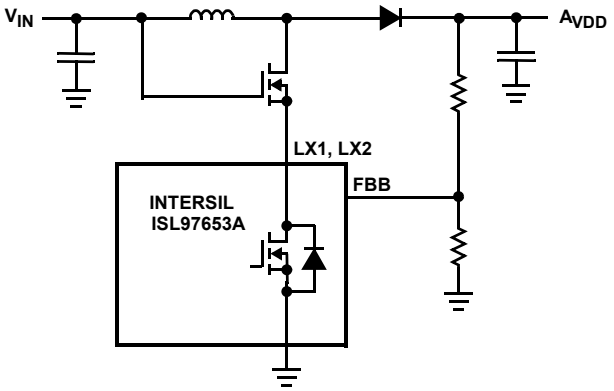


FIGURE 15. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

V_{IN} Protection

A series external P-FET can be used to prevent passive power-up inrush current from the Boost output capacitors charging to V_{IN} - $V_{SCHOTTKY}$ via the boost inductor and Schottky diode. This FET also adds protection in the event of a short circuit on A_{VDD}. The gate of the PFET (shown as M0 in the “Typical Application Diagram” on page 5) is controlled by PROT. When EN is low, PROT is pulled internally to PVIN1, thus M0 is switched off. When EN goes high, PROT is pulled down slowly via a 50µA current source, switching M0 on.

If the device is powered up with EN tied to high, M0 will remain switched off until the voltage on VL exceeds the VLOR threshold. Once the voltage on PROT falls below 0.6V and the step-up regulator is within 90% of its target voltage, PROT is pulled down to ground via a 1.3kΩ impedance. If A_{VDD} falls 10% below regulation, the drive to PROT reverts to a 50µA current source. If a timed fault is detected, M0 is actively switched off.

Several additional external components can optionally be used to fine-tune the function of pin PROT (shown in the dashed box near M0 in the application diagram). PROT ramp rate can be controlled by adding a capacitor C30 between gate and source of M0. M0 gate voltage can be

limited during soft-start by adding a resistor (~75kΩ) between gate and source of M0. In addition, a resistor can be connected between PROT and the gate of M0, in order to limit the maximum V_{GS} of M0 at all times.

Buck Converter

The buck converter is a step down converter supplying power to the logic circuit of the LCD system. The ISL97653A integrates a high voltage N-channel MOSFET to save costs and reduce external component count. In the continuous current mode, the relationship between input voltage and output voltage as expressed in Equation 8:

$$\frac{V_{LOGIC}}{V_{IN}} = D \quad \text{(EQ. 8)}$$

Where D is the duty cycle of the switching MOSFET. Because D is always less than 1, the output voltage of a buck converter is lower than input voltage.

The peak current limit of buck converter is set to 2.5A, which restricts the maximum output current (average) based on Equation 9:

$$I_{OMAX} = 2.5A - \Delta I_{P-P} \quad \text{(EQ. 9)}$$

Where ΔI_{P-P} is the ripple current in the buck inductor as shown in Equation 10:

$$\Delta I_{pp} = \frac{V_{LOGIC}}{L \cdot f_s} \cdot (1 - D) \quad \text{(EQ. 10)}$$

Where L is the buck inductor, f_s is the switching frequency (680kHz).

Feedback Resistors

The buck converter output voltage is determined by Equation 11:

$$V_{LOGIC} = \frac{R_{14} + R_{13}}{R_{14}} \times V_{FBL} \quad \text{(EQ. 11)}$$

Where R_{13} and R_{14} are the feedback resistors in the buck converter loop to set the output voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 1kΩ is recommended.

Buck Converter Input Capacitor

Input capacitance should support the maximum AC RMS current which occurs at D = 0.5 and maximum output current.

$$I_{acrms}(C_{IN}) = \sqrt{D \cdot (1 - D)} \cdot I_O \quad \text{(EQ. 12)}$$

Where I_o is the output current of the buck converter. Table 6 shows some recommendations for the input capacitor.

TABLE 6. INPUT CAPACITOR (BUCK) RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/16V	1210	Murata	C3225X7R1C226M

Buck Inductor

A 3.3µH to 10µH inductor range is recommended for the buck converter. Besides the inductance, the DC resistance and the saturation current are also factors that need to be considered when choosing a buck inductor. Low DC resistance can help maintain high efficiency. Saturation current rating should be higher than 2A. Here are some recommendations for the buck inductor.

TABLE 7. BUCK INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
4.7µH/ $2.7A_{PEAK}$	5.7x5.0x4.7	Murata	LQH55DN4R7M01K
6.8µH/ $3A_{PEAK}$	7.3x6.8x3.2	TDK	RLF7030T-6R8M2R8

Rectifier Diode (Buck Converter)

A Schottky diode is recommended for fast recovery and low forward voltage. The reverse voltage rating should be higher than the maximum input voltage. The peak current rating is 2.5A, and the average current is given by Equation 13:

$$I_{avg} = (1 - D) * I_o \quad \text{(EQ. 13)}$$

Where I_o is the output current of buck converter. The following table shows some diode recommended.

TABLE 8. BUCK RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
PMEG2020EJ	20V/2A	SOD323F	Philips Semiconductors
SS22	20V/2A	SMB	Fairchild Semiconductor

Output Capacitor (Buck Converter)

Four 10µF or two 22µF ceramic capacitors are recommended for this part. The overshoot and undershoot will be reduced with more capacitance, but the recovery time will be longer.

TABLE 9. BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/6.3V	0805	TDK	C2012X5R0J106M
10µF/6.3V	0805	Murata	GRM21BR60J106K
22µF/6.3V	1210	TDK	C3216X5R0J226M
100µF/6.3V	1206	Murata	GRM31CR60J107M

PI Loop Compensation (Buck Converter)

The buck converter of ISL97653A can be compensated by a RC network connected from CM2 pin to ground. C_8 = 4.7nF and R_{20} = 10k RC network is used in the demo board. A larger value resistor can lower the transient overshoot, however, at the expense of stability of the loop.

The stability can be optimized in a similar manner to that described in "PI Loop Compensation (Boost Converter)" on page 12.

Bootstrap Capacitor (C_{13})

This capacitor provides the supply to the high driver circuitry for the buck MOSFET. The bootstrap supply is formed by an internal diode and capacitor combination. A 1µF is recommended for ISL97653A. A low value capacitor can lead to overcharging and in turn damage the part.

During very light loads, the on-time of the low side diode may be insufficient to replenish the bootstrap capacitor voltage. Additionally, if V_{IN} - V_{BUCK} < 1.5V, the internal MOSFET pull-up device may be unable to turn-on until V_{LOGIC} falls. Hence, there is a minimum load requirement in this case. The minimum load can be adjusted by the feedback resistors to FBL.

Charge Pump Controllers (V_{ON} and V_{OFF})

The ISL97653A includes 2 independent charge pumps (see charge pump block and connection diagram). The negative charge pump inverts the SUPN voltage and provides a regulated negative output voltage. The positive charge pump doubles or triples the SUPP voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is controlled by internal comparators that sense the output voltage. These sensed voltages are then compared to scaled internal reference voltages.

Charge pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps can provide 100mA for V_{OFF} and 40mA for V_{ON}.

Positive Charge Pump Design Consideration

All positive charge pump diodes (D1, D2 and D3 shown in the "NEGATIVE CHARGE PUMP BLOCK DIAGRAM" on page 16) for x2 (doubler) and x3 (Tripler) modes of operation are included in the ISL97653A. During the chip start-up sequence the mode of operation is automatically detected when the charge pump is enabled. With both C_7 and C_8 present, the x3 mode of operation is detected. With C_7 present, C_8 open and with C_1+ shorted to C_2+, the x2 mode of operation will be detected.

Internal switches M1, M2 and M3 isolate P_{OUT} from SUPP until the charge pump is enabled. This is important for TFT applications that require the negative charge pump output (V_{OFF}) and A_{VDD} supplies to be established prior to P_{OUT}.

The maximum P_{OUT} charge pump current can be estimated from the following equations assuming a 50% switching duty:

$$I_{MAX}(2x) \sim \text{min of 40mA or}$$

$$\frac{2 \bullet V_{SUPP} - 2 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{(2 \bullet (2 \bullet R_{ONH} + R_{ONL}))} \bullet 0.95A$$

$$I_{MAX}(3x) \sim \text{min of 40mA or}$$

$$\frac{3 \bullet V_{SUPP} - 3 \bullet V_{DIODE}(2 \bullet I_{MAX}) - V(V_{ON})}{(2 \bullet (3 \bullet R_{ONH} + 2 \bullet R_{ONL}))} \bullet 0.95V \quad \text{(EQ. 14)}$$

Note: V_{DIODE} (2 • I_{MAX}) is the on-chip diode voltage as a function of I_{MAX} and V_{DIODE} (40mA) < 0.7V.

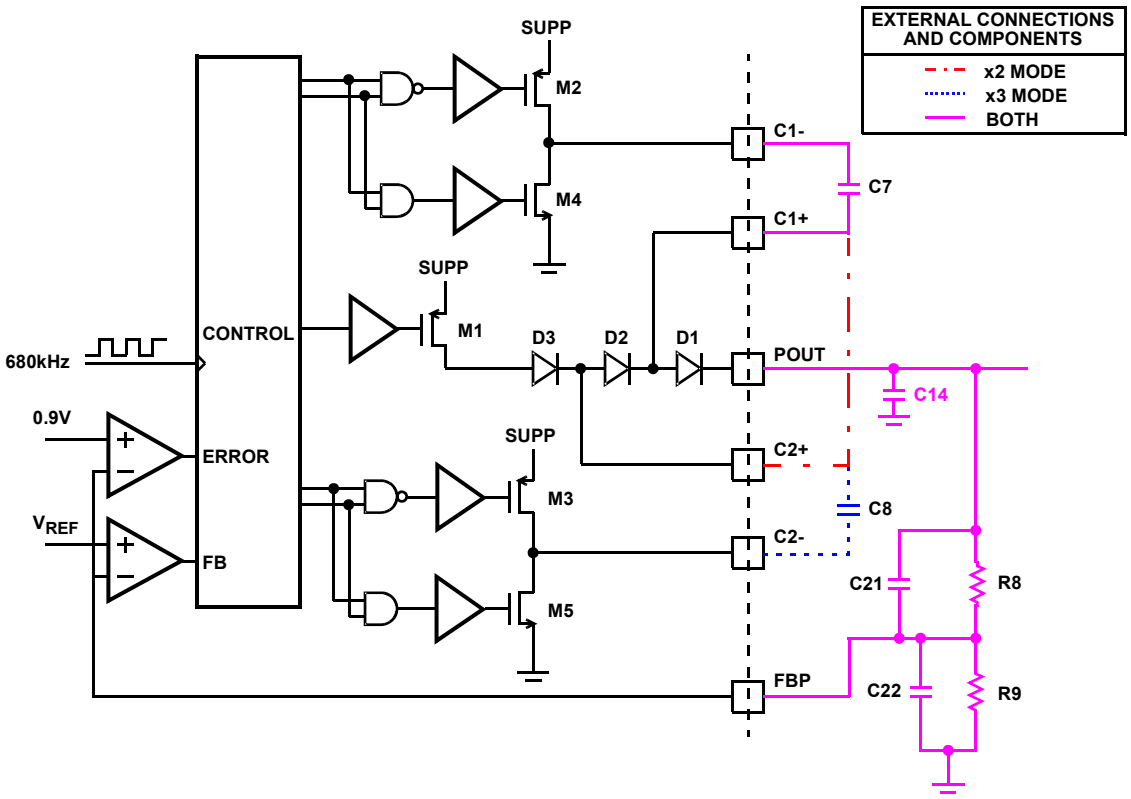


FIGURE 16. V_{ON} FUNCTION DIAGRAM

In voltage doubler configuration, the maximum V_{ON} is as given by the following equation:

$$V_{ON\_MAX(2x)} = 2 \bullet (V_{SUPP} - V_{DIODE}) - 2 \bullet I_{OUT} \bullet (2 \bullet R_{ONH} + R_{ONL}) \quad \text{(EQ. 15)}$$

For Voltage Tripler:

$$V_{ON\_MAX(3x)} = 3 \bullet (V_{SUPP} - V_{DIODE}) - 2 \bullet I_{OUT} \bullet (3 \bullet R_{ONH} + 2 \bullet R_{ONL} \quad \text{(EQ. 16)}$$

V_{ON} output voltage is determined by the following equation:

$$V_{ON} = V_{FBP} \bullet \left(1 + \frac{R_8}{R_9}\right) \quad \text{(EQ. 17)}$$

Negative Charge Pump Design Consideration

The negative charge pump consists of an internal switcher M1, M2 which drives external steering diodes D2 and D3 via a pump capacitor (C_{12}) to generate the negative V_{OFF} supply. An internal comparator (A1) senses the feedback voltage on FBN and turns on M1 for a period up to half a CLK period to maintain $V_{(FBN)}$ in regulated operation at 0.2V. External feedback resistor R_6 is referenced to V_{REF}.

Faults on V_{OFF} which cause V_{FBN} to rise to more than 0.4V, are detected by comparator (A2) and cause the fault detection system to start the internal fault timer which will cause the chip to power down if the fault persists.

The maximum V_{OFF} output voltage of a single stage charge pump is:

$$V_{OFF\_MAX}(2x) = -V_{SUPP} + V_{DIODE} + 2 \bullet I_{OUT} \bullet (R_{ON}(NOUT)H + R_{ON}(NOUT)L) \quad \text{(EQ. 18)}$$

R_6 and R_7 in the “Typical Application Diagram” on page 5 determine V_{OFF} output voltage.

$$V_{OFF} = V_{FBN} \bullet \left(1 + \frac{R7}{R6}\right) - V_{REF} \bullet \left(\frac{R7}{R6}\right) \quad \text{(EQ. 19)}$$

**Although in the given typical application diagram, SUPP and SUPN are connected to A_{VDD}, depending on a specific application, SUPN and/or SUPP could be connected to either A_{VDD} or V_{IN}.*

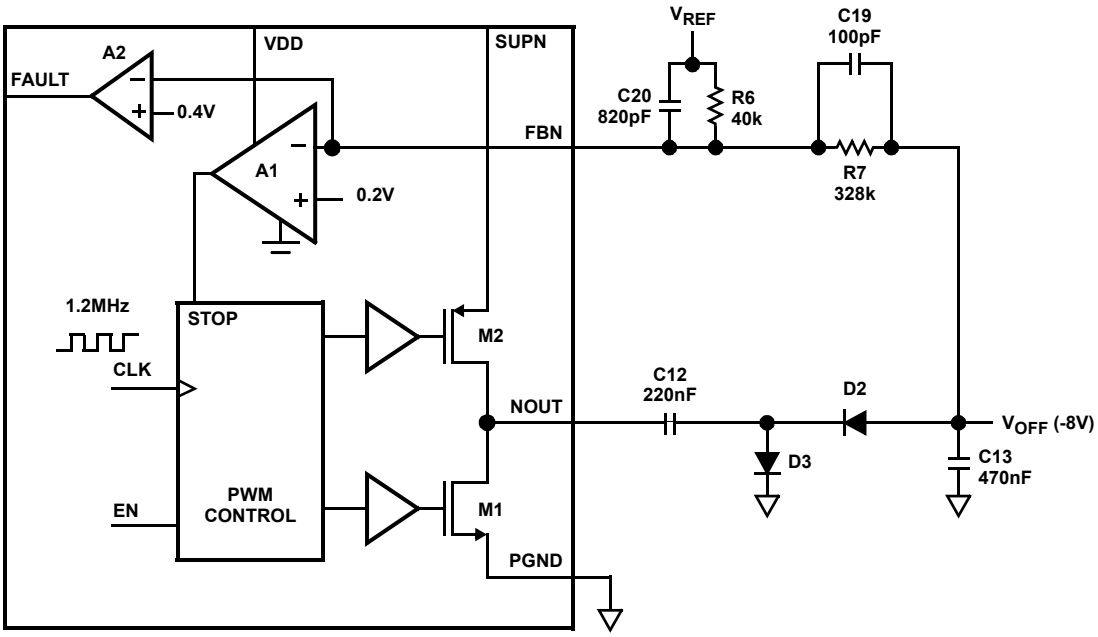


FIGURE 17. NEGATIVE CHARGE PUMP BLOCK DIAGRAM

V_{ON} Slice Circuit

The V_{ON} slice circuit functions as a three way multiplexer, switching the voltage on COM between ground, DRN and POUT, under control of the start-up sequence and the CTL pin.

During the start-up sequence, COM is pulled to ground via an NDMOS FET with $r_{DS(ON)}$ of 260Ω. After the start-up sequence has completed, CTL is enabled and acts as a multiplexer control such that if CTL is low, COM connects to DRN through a 30Ω internal MOSFET, and if CTL is high, COM connects to P_{OUT} internally via a 5Ω MOSFET.

The slew rate of the switch control circuit is mainly restricted by the load capacitance at COM pin and is given by Equation 20:

$$\frac{\Delta V}{\Delta t} = \frac{V_g}{(R_i \parallel R_L) \times C_L} \quad \text{(EQ. 20)}$$

Where V_g is the supply voltage applied to DRN or voltage at P_{OUT}, which range is from 0V to 30V. R_i is the resistance between COM and DRN or P_{OUT} including the internal MOSFET $r_{DS(on)}$, the trace resistance and the resistor inserted, R_L is the load resistance of VON slice circuit, and C_L is the load capacitance of switch control circuit.

In the Typical Application Circuit, R_8, R_9 and C_{22} give the bias to DRN based on Equation 21:

$$V_{DRN} = \frac{V_{ON} \cdot R_9 + AVDD \cdot R_8}{R_9 + R_8} \quad \text{(EQ. 21)}$$

And R_{10} can be adjusted to adjust the slew rate.

V_{LOGIC2} LDO

An LDO controller is also integrated to provide a second logic supply. The LDO-CTL pin drives the base of an external transistor which should be sized for the current required. A resistor divider is used to set the output voltage by feeding back a reference voltage to LDO-FB. The internal feedback reference is 1.215V.

HVS Operation

When the HVS input is taken high, the ISL97653A enters HVS test mode. In this mode, the output of A_{VDD} is increased by switching RSET to ground, and the AVDD is set to:

$$A_{VDD} = \frac{R_3 + R_x}{R_x} \times V_{FBB} \quad \text{(EQ. 22)}$$

Where R_x is the value of R_4 in parallel with R_5. AVDD voltage higher than the maximum rating of the boost MOSFET may damage the part.

Fault Protection

The ISL97653A incorporates a number of fault protection schemes. AVDD, VON, and VOFF are constantly monitored. If fault conditions are detected for longer than 1ms on these FB inputs, the device stops switching and the outputs are disconnected. The ISL97653A also integrates over-temp and over current protection.

Supply Sequencing

When the input voltage V_{IN} is higher than 4V(UVLO), V_{REF}, V_{LOGIC}, and V_{LOGIC2} are turned on. V_{LOGIC} has a 9ms fixed soft-start at start-up. A_{VDD}, V_{ON}, and V_{OFF} are dependant on the EN pin.

When EN is taken high, voltage of pin PROT and V_{OFF} start ramping down. Once the PROT voltage falls below 0.9V, A_{VDD} starts up with a 9ms fixed soft-start time. Please note if V_{OFF} is to start earlier than A_{VDD}, then the SUPN needs to connect to V_{IN}, and V_{IN} voltage should be larger than V_{OFF} absolute value. The delay between V_{OFF} and A_{VDD} can be controlled by C30 in the “Typical Application Diagram” on page 5m and is given by Equation 23:

$$t_{DELAY} = (V_{IN} - 0.9V) \times C_{30} / (50\mu A) \quad \text{(EQ. 23)}$$

The successful completion of the A_{VDD} soft-start cycle triggers two simultaneous events. V_{ON} begins to ramp up and the voltage on CDEL starts ramping up. When the voltage reaches 1.215V, V_{ON} slice starts.

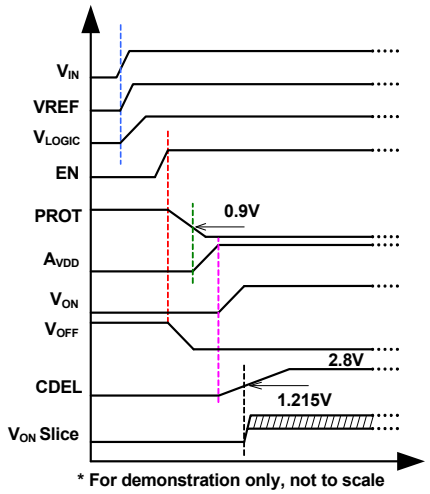


FIGURE 18.

Temperature Sensor

The ISL97653A also includes a temperature output for use in system thermal management control. The integrated sensor measures the die temperature over the -40°C to +150°C range. Output is in the form of an analog voltage on the TEMP pin in the range of 0V to 3V, which is proportional to the sensed die temperature. Temperature accuracy is ±8.5°C over the -40°C to +150°C temperature range.

The device should be disabled by the user when the TEMP pin output reaches 3V (= +150°C die junction). Operation of the device between +125°C and +150°C can be tolerated for short periods, however in order to maximize the life of the IC, it is recommended that the effective continuous operating junction temperature of the die should not exceed +125°C.

Fault Sequencing

The ISL97653A has advanced overall fault detection systems including Overcurrent Protection (OCP) for both boost and buck converters, Undervoltage Lockout Protection (UVLP) and Over-Temperature Protection.

Once the peak current flowing through the switching MOSFET of the boost and buck converters triggers the current limit threshold, the PWM comparator will disable the output, cycle by cycle, until the current is back to normal.

Layout Recommendation

The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

There are some general guidelines for layout:

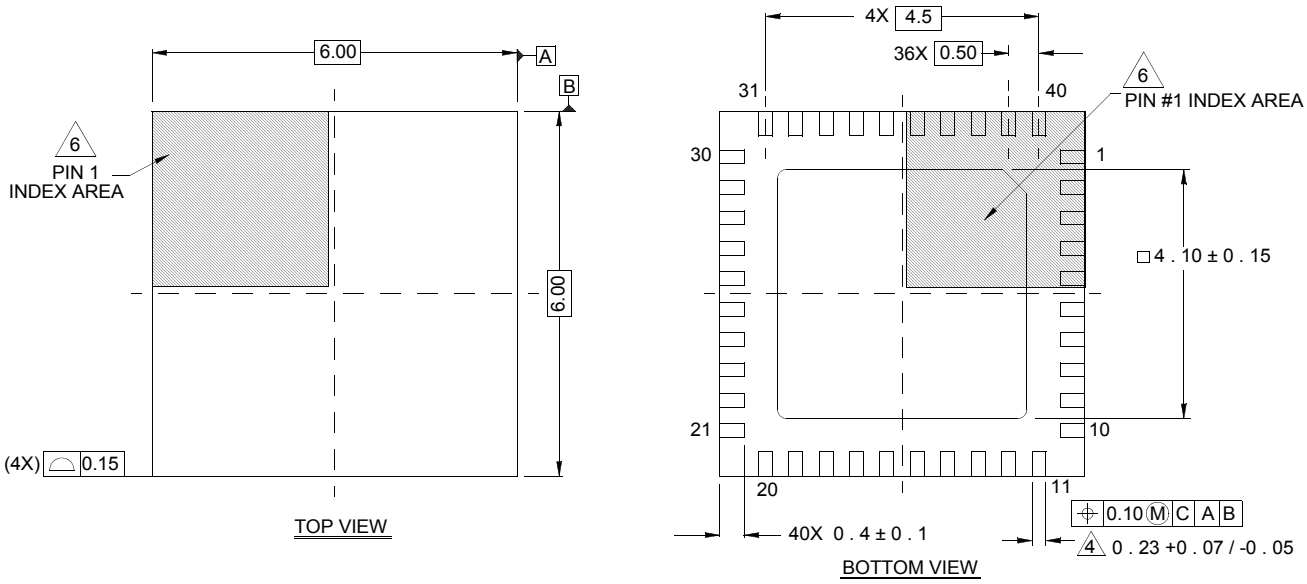
1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF} and V_L bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. Minimize feedback input track lengths to avoid switching noise pick-up.

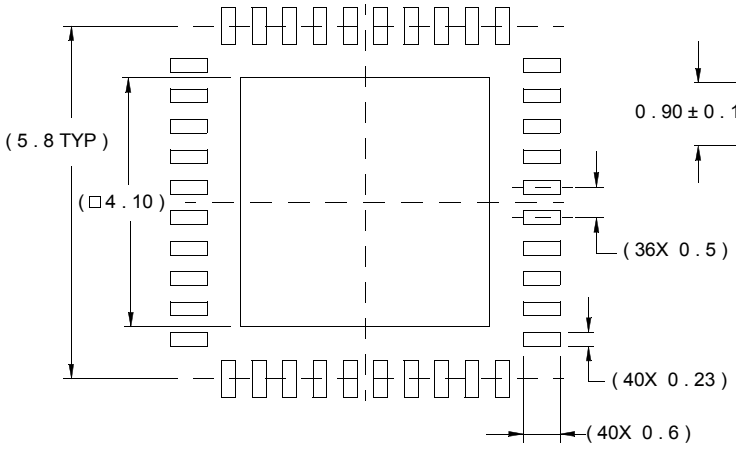
A demo board is available to illustrate the proper layout implementation.

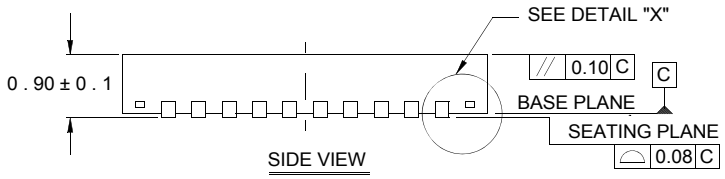
Package Outline Drawing

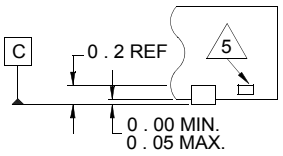
L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 10/06









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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