

Digital Green-Mode Synchronous Rectifier Controller

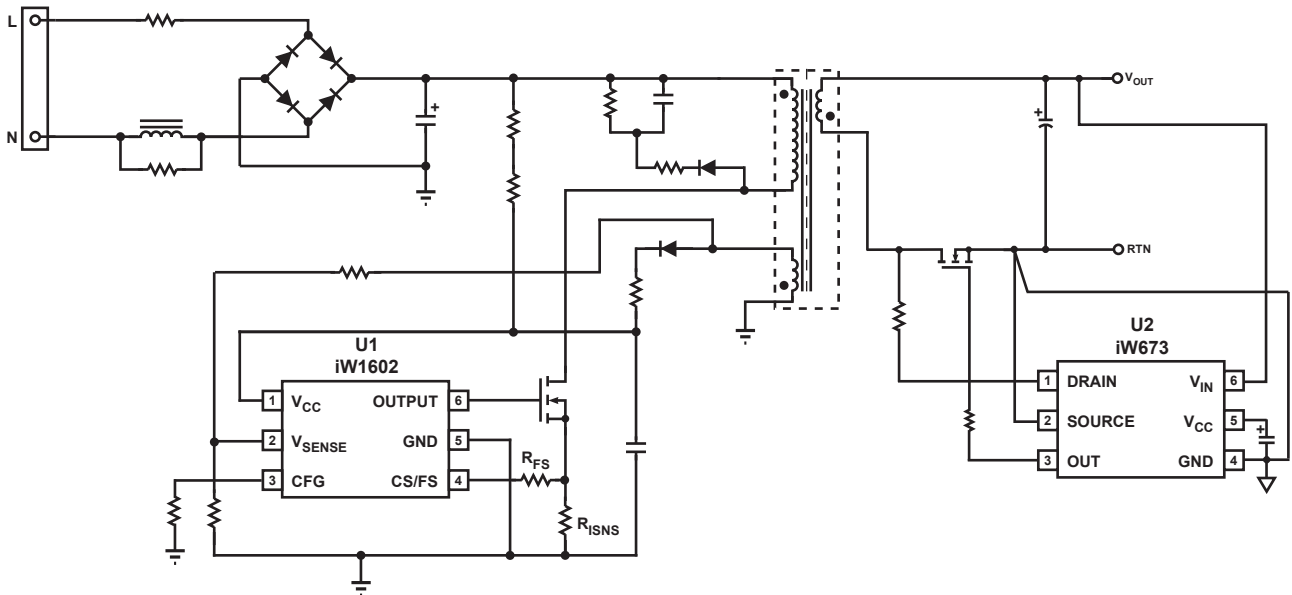


Figure 3.2 : iW673 Typical Application Circuit Using iW1602 as the Primary-Side Controller (Achieving <75mW No-Load Power Consumption in 5V, 2.5A Adapter Designs with Fast Dynamic Load Response, and Supporting Constant Current Operation down to 2.4V System Output)

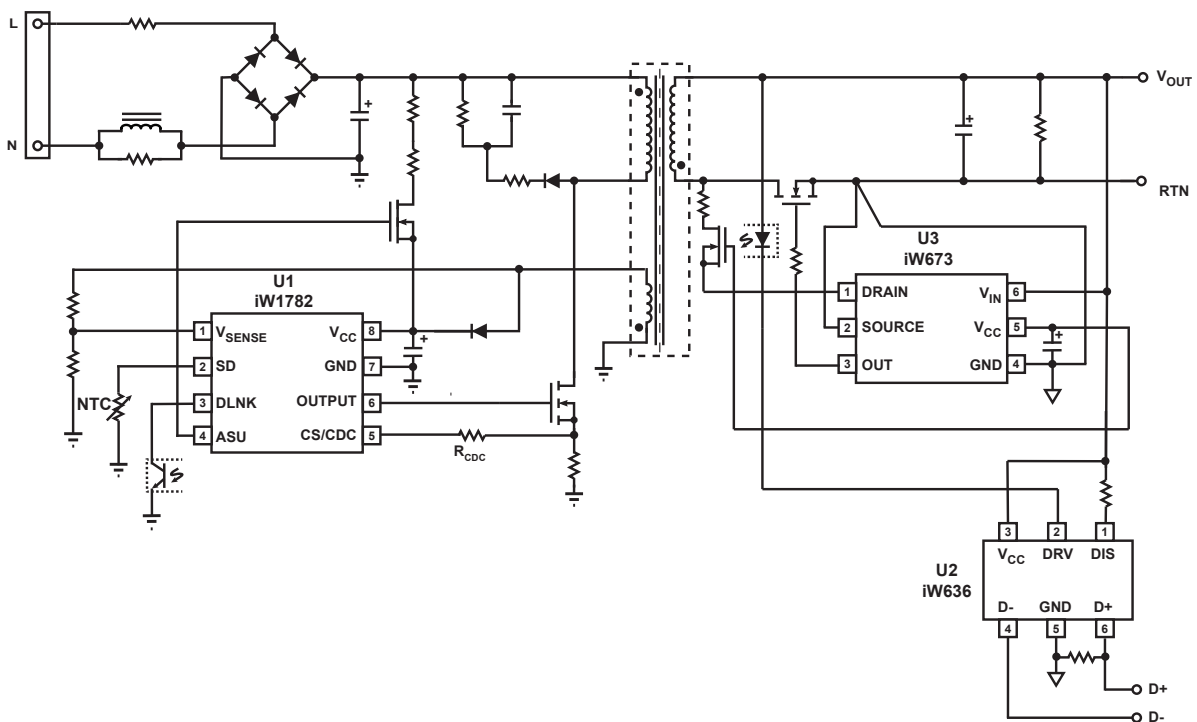


Figure 3.3 : iW673 Typical Application Circuit for Multi-Level Output Voltage and Current (Using iW1782 as Primary-Side Controller and iW636 as Secondary-Side Controller) for Qualcomm® Quick Charge™ 3.0 (Achieving <20mW No-Load Power Consumption)

Note: The DFET clamping circuit at the DRAIN pin of iW673 is not needed if the maximum voltage on the drain of the SR MOSFET is lower 60V.

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4 Pinout Description

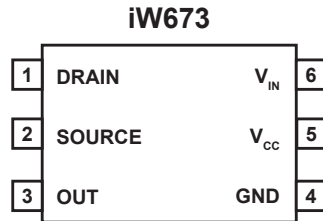


Figure 4.1 : 6-Pin SOT23 Package

Pin No.	Pin Name	Type	Pin Description
1	DRAIN	Analog Input	Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.
2	SOURCE	Analog input	Synchrnous rectifier MOSFET source voltage sensing input.
3	OUT	Output	Synchronous rectifier MOSFET driver.
4	GND	Ground	Ground.
5	V_{CC}	Power Input	Output of internal LDO and PLR. It provides bias voltage for the internal logic circuit and the MOSFET driver. Connect this pin to a capacitor.
6	V_{IN}	Analog Input	Input of internal LDO and system output voltage sensing circuit. Connect to adapter/charger output for bias voltage. The internal LDO clamps the V_{CC} voltage at 5V when $V_{IN} > 5V$. The V_{IN} is also the input for the PLR enable comparator and the SR enable comparator.

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5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

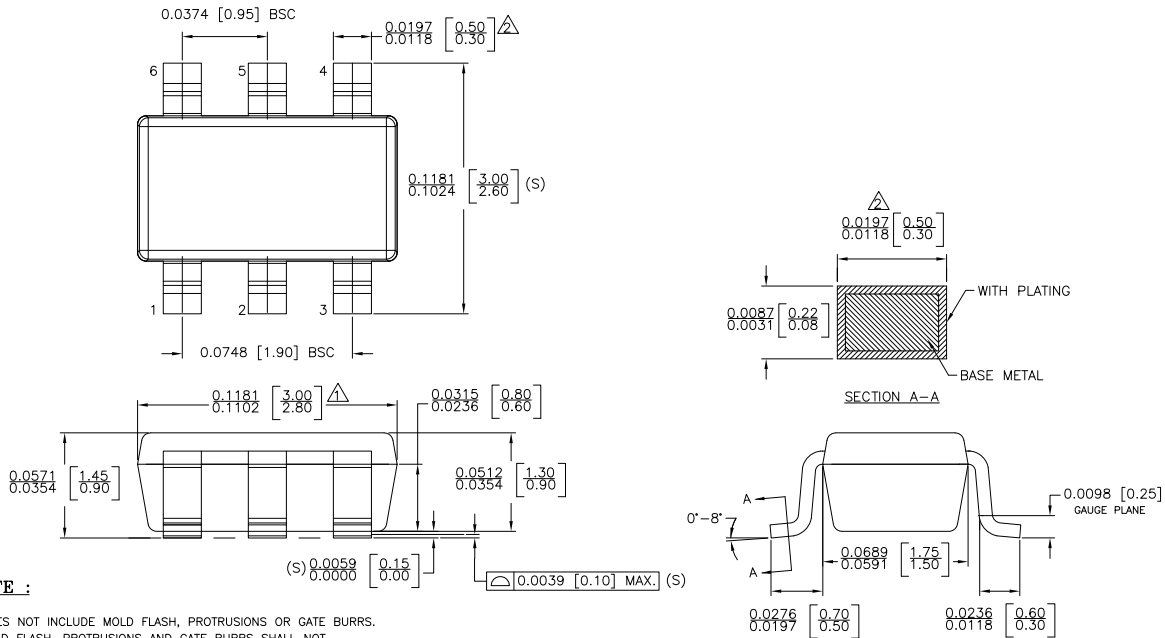
Parameter	Symbol	Value	Units
V_{IN} DC supply voltage range (pin 6, $I_{CC} = 15\text{mA}$ max)	V_{IN}	-0.3 to 33	V
Continuous DC supply current at V_{IN} pin ($V_{IN} = 30\text{V}$)	I_{VO}	15	mA
Continuous DC supply current at V_{CC} pin ($V_{CC} = 5.5\text{V}$)	I_{VCC}	15	mA
Gate peak output current	I_G	± 3	A
DRAIN pin voltage (Note 1)	V_D	-1.5 to 60	V
DRAIN pin peak current	I_{DRAIN}	-40 to 300	mA
SOURCE pin voltage	V_{SOURCE}	-0.6 to 1	V
V_{CC} pin voltage	V_{CC}	-0.6 to 6	V
Junction temperature	T_J	-40 to 150	$^{\circ}\text{C}$
Storage temperature		-65 to 150	$^{\circ}\text{C}$
Thermal resistance junction-to-ambient	θ_{JA}	190	$^{\circ}\text{C}/\text{W}$
ESD rating per JEDEC JESD22-A114		2,000	V

Notes:

Note 1: The DRAIN pin voltage should not be below -0.6V for more than 500 ns.

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6 Physical Dimensions



NOTE :

- △ DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.127 MM PER SIDE.
- △ DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.127 MM PER SIDE.
- 3. DIE IS FACING UP FOR MOLD. DIE IS FACING DOWN FOR TRIM/FORM.
- 4. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION SC74A AND JEDEC SPECIFICATION MO-178AB.
- 5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
- 6. CONTROLLING DIMENSIONS IN INCHES. [mm]

SIATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 6 SOT23 PACKAGE OUTLINE	
REV: A	DATE: 02-MAR-2015
REVISION NOTE: NEW DRAWING	

7 Ordering Information

Part no.	Options	Package	Description
iW673-00	$V_{OUT} < 16V$. $I_{OUT} < 4A$. Not recommended for new designs	SOT23	Tape & Reel ¹
iW673-01	$V_{OUT} < 25V$. $I_{OUT} > 4A$ or when SR MOSFET with large package inductance (TO-220 or similar) is used.	SOT23	Tape & Reel ¹
iW673-10	$V_{OUT} < 25V$. $I_{OUT} < 4A$. PLR circuit is disabled until UVLO once V_{OUT} reaches PLR disable threshold ($V_{LR_DISABLE}$).	SOT23	Tape & Reel ¹
iW673-20	$V_{OUT} < 25V$. $I_{OUT} < 4A$.	SOT23	Tape & Reel ¹

Note 1: Tape and reel packing quantity is 3,000/reel. Minimum packing quantity is 3,000.

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8 Top Marking

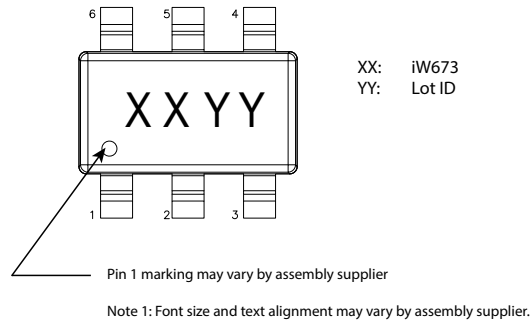


Figure 8.1 : Top Marking for iW673

Part Number	Top Mark Product and Product Option Code (YY)
iW673-00	N/A
iW673-01	5LYY
iW673-10	6EYY
iW673-20	6GY Y

Table 8.1 : Product Option Code Table

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(Rev.1.0 Mar 2020)

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