1. Overview

1.1 Features

The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M32C/80 Series CPU core. The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) is housed in 144-pin and 100-pin plastic molded LQFP/QFP packages.
With a 16-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.
The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, etc.

1.1.2 Specifications

Tables 1.1 to 1.4 lists the specifications of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

Table 1.1 Specifications (144-Pin Package) (1)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 9, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

Table 1.2 Specifications (144-Pin Package) (2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5, UART6	Clock synchronous/asynchronous × 2
A/D Converter		10-bit resolution × 34 channels (in single-chip mode) 10-bit resolution × 18 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 16 channels • Communication function: Clock synchronous serial interface, clock asynchronous serial interface, HDLC data processing, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 121 with selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		144-pin LQFP (PLQP0144KA-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

Table 1.3 Specifications (100-Pin Package) (1)

Item	Function	Specification
CPU	Central processing unit	M32C/80 core (multiplier: 16 bits × 16 bits → 32 bits multiply-addition operation instructions: 16 × 16 + 48 → 48 bits) • Basic instructions: 108 • Minimum instruction execution time: 31.3 ns (f(CPU) = 32 MHz, VCC1 = 4.2 to 5.5 V) 41.7 ns (f(CPU) = 24 MHz, VCC1 = 3.0 to 5.5 V) • Operating mode: Single-chip mode, memory expansion mode, and microprocessor mode
Memory	ROM, RAM, data flash	See **Tables 1.5 to 1.7 Product List**.
Power Supply Voltage Detection		Vdet3 detection function, Vdet4 detection function, cold start/warm start determination function
External Bus Expansion	Bus/memory expansion function	• Address space: 16 Mbytes • External bus interface: 1 to 7 wait states can be inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Switchable between separate bus and multiplexed bus formats, switchable data bus width (8-bit or 16-bit)
Clock	Clock generation circuits	• 4 circuits: Main clock, sub clock, on-chip oscillator, PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection function • Frequency divider circuit: Dividing ratio selectable among 1, 2, 3, 4, 6, 8, 10, 12, 14, 16 • Low power consumption features: Wait mode, stop mode
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit × 1 channel (with prescaler)
DMA	DMAC	• 4 channels, cycle steal method • Trigger sources: 43 • Transfer modes: 2 (single transfer and repeat transfer)
	DMACII	• Can be activated by all peripheral function interrupt sources • Transfer modes: 2 (single transfer and burst transfer) • Immediate transfer, calculation transfer, and chain transfer functions
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one shot timer mode, pulse width modulation (PWM) mode, Event counter 2-phase pulse signal processing (2-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Timer function for 3-phase motor control	3-phase inverter control × 1 (using timer A1, timer A2, timer A4, and timer B2) On-chip dead time timer

Table 1.4 Specifications (100-Pin Package) (2)

Item	Function	Specification
Serial Interface	UART0 to UART4	Clock synchronous/asynchronous × 5 I^2C bus, special mode 2, GCI mode, SIM mode, IrDA mode(2), IEBus (optional)(1)(3)
	UART5	Clock synchronous/asynchronous × 1
A/D Converter		10-bit resolution × 26 channels (in single-chip mode) 10-bit resolution × 10 channels (in memory expansion mode and microprocessor mode) Including sample and hold function
D/A Converter		8-bit resolution × 2 channels
CRC Calculation Circuit		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) compliant
X/Y Converter		16 bits x 16 bits
Intelligent I/O		16-bit timer × 2 • Time measurement function (input capture): 8 channels • Waveform generation function (output compare): 10 channels • Communication function: Clock synchronous serial interface, clock asynchronous serial interface, HDLC data processing, IEBus (optional)(1)(3) • 2-phase pulse signal processing (2-phase encoder input) × 1
ROM Correction Function		Address match interrupt × 8
CAN modules		Supporting CAN 2.0B specification M32C/87: 16 slots × 2 channels, M32C/87A: 16 slots × 1 channel M32C/87B: none
I/O Ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 85, selectable pull-up resistor • N channel open drain ports: 2
Flash Memory		• Erase and program voltage: 3.3 V ± 0.3 V or 5.0 V ± 0.5 V • Erase and program endurance: 100 times (all areas) • Program security: ROM code protect and ID code check • Debug functions: On-chip debug and on-board flash reprogram
Operating Frequency/Supply Voltage		32 MHz: VCC1 = 4.2 to 5.5 V, VCC2 = 3.0 V to VCC1 24 MHz: VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current Consumption		32 mA (32 MHz, VCC1 = VCC2 = 5 V) 23 mA (24 MHz, VCC1 = VCC2 = 3.3 V) 45 μA (approx. 1 MHz, VCC1 = VCC2 = 3.3 V, on-chip oscillator low-power consumption mode → wait mode) 0.8 μA (VCC1 = VCC2 = 3.3 V, stop mode)
Operating Ambient Temperature (°C)		-20 to 85°C, -40 to 85°C (optional)(3)
Package		100-pin LQFP (PLQP0100KB-A) 100-pin QFP (PRQP0100JB-A)

NOTES:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. Available in UART0.
3. Please contact a Renesas sales office for optional features.

1.2 Product List

Tables 1.5 to 1.7 list product information. Figure 1.1 shows product numbering system.

Table 1.5 M32C/87 Group (1) (M32C/87: 2-channel CAN module) Current as of Oct. 2007

Type Number	RENESAS Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLFP	PRQP0100JB-A (100P6S-A)			
M30879FLGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKGP	PLQP0100KB-A (100P6Q-A)			
M30878FJGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJGP	PLQP0100KB-A (100P6Q-A)			
M30875FHGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHGP	PLQP0100KB-A (100P6Q-A)			
M30878MJ-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJ-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJ-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MH-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MH-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

Table 1.6 M32C/87 Group (2) (M32C/87A: 1-channel CAN module) Current as of Oct. 2007

Type Number	RENESAS Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLAGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLAFP	PRQP0100JB-A (100P6S-A)			
M30879FLAGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKAGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKAGP	PLQP0100KB-A (100P6Q-A)			
M30878FJAGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJAGP	PLQP0100KB-A (100P6Q-A)			
M30875FHAGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHAGP	PLQP0100KB-A (100P6Q-A)			
M30878MJA-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJA-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJA-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHA-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHA-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

Table 1.7 M32C/87 Group (3) (M32C/87B: no CAN module) Current as of Oct. 2007

Type Number	RENESAS Code	ROM Capacity	RAM Capacity	Remarks
M3087BFLBGP	PLQP0144KA-A (144P6Q-A)	1 MB + 4 KB(1)	48 KB	Flash memory
M30879FLBFP	PRQP0100JB-A (100P6S-A)			
M30879FLBGP	PLQP0100KB-A (100P6Q-A)			
M3087BFKBGP	PLQP0144KA-A (144P6Q-A)	768 KB + 4 KB(1)		
M30879FKBGP	PLQP0100KB-A (100P6Q-A)			
M30878FJBGP	PLQP0144KA-A (144P6Q-A)	512 KB + 4 KB(1)	31 KB	
M30876FJBGP	PLQP0100KB-A (100P6Q-A)			
M30875FHBGP	PLQP0144KA-A (144P6Q-A)	384 KB + 4 KB(1)	24 KB	
M30873FHBGP	PLQP0100KB-A (100P6Q-A)			
M30878MJB-XXXGP	PLQP0144KA-A (144P6Q-A)	512 KB	31 KB	Mask ROM
M30876MJB-XXXFP	PRQP0100JB-A (100P6S-A)			
M30876MJB-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30875MHB-XXXGP	PLQP0144KA-A (144P6Q-A)	384 KB	24 KB	
M30873MHB-XXXGP	PLQP0100KB-A (100P6Q-A)			

NOTE:
1. Additional 4-Kbyte space is available for data flash memory.

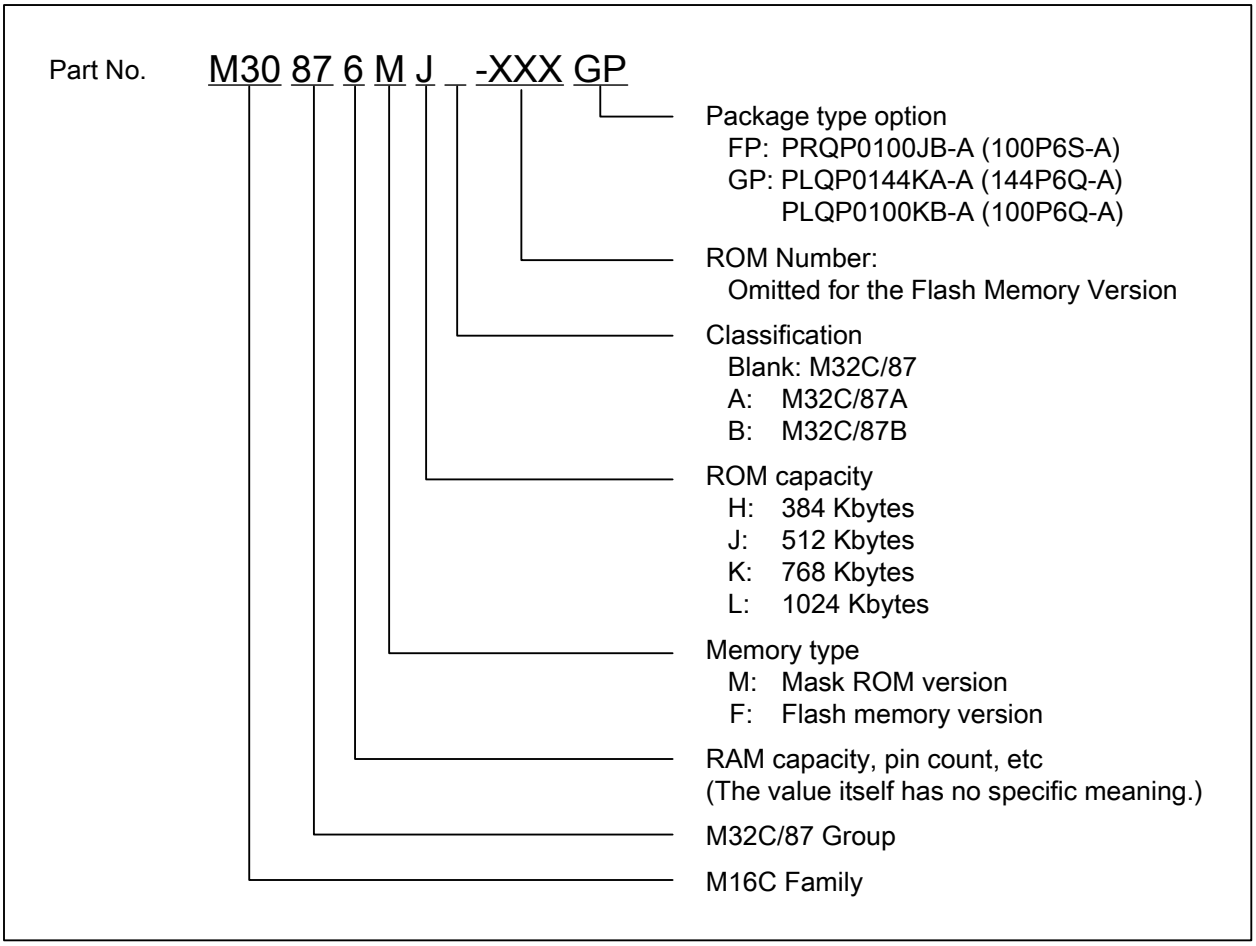
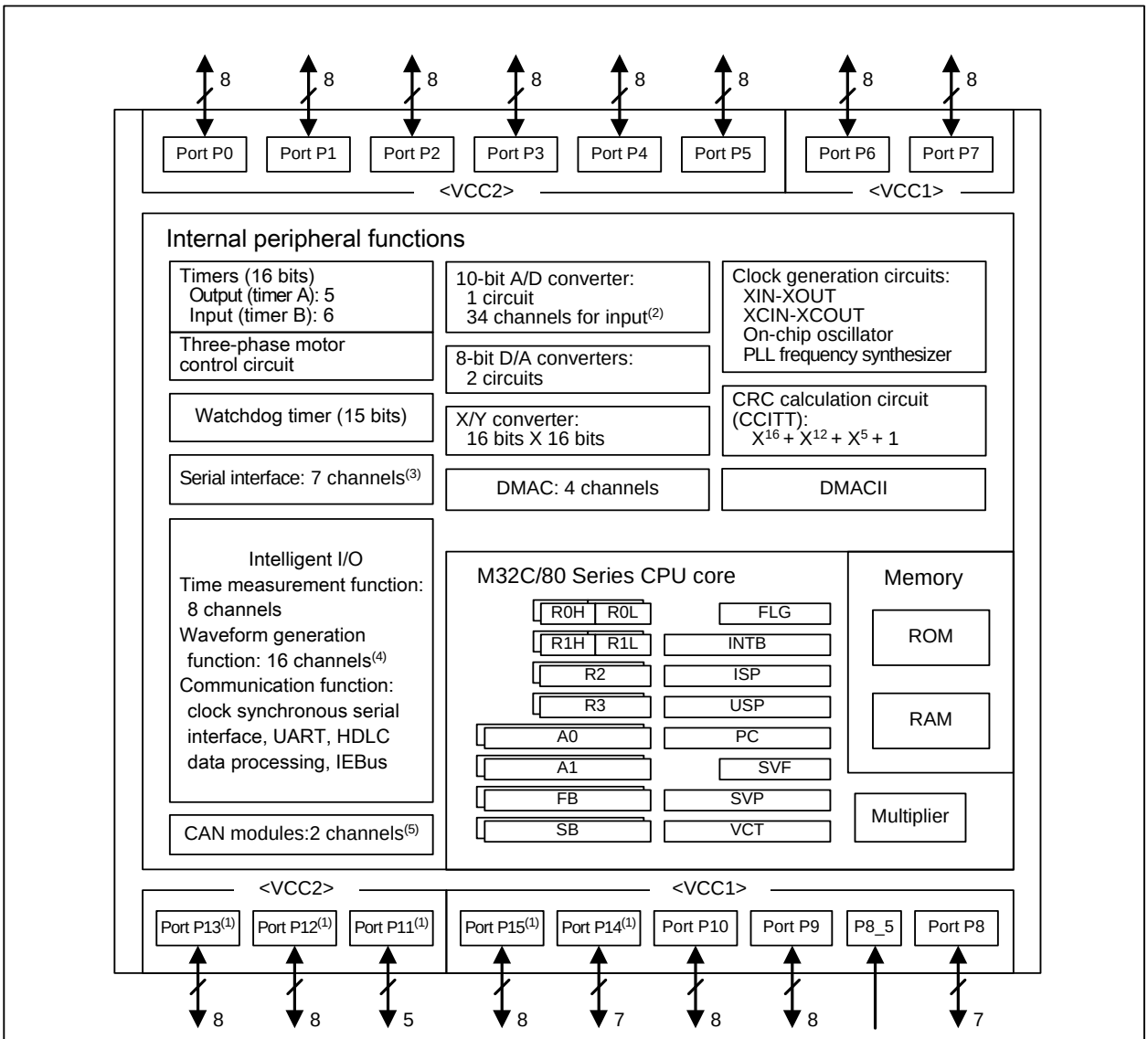


Figure 1.1 Product Numbering System

1.3 Block Diagram

Figure 1.2 shows a block diagram of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).

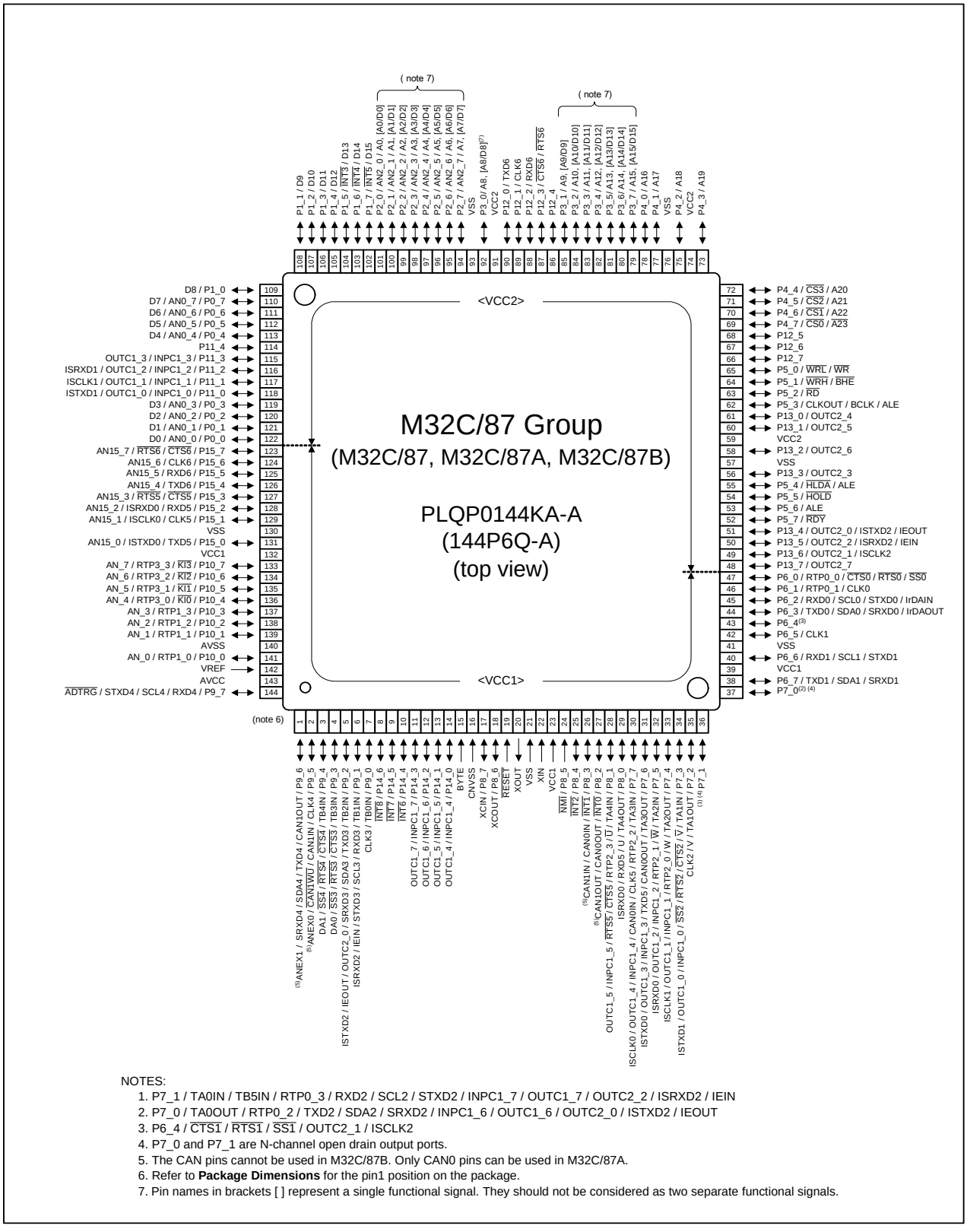


NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. 34 channels are available in the 144-pin package. 26 channels are available in the 100-pin package.
3. 6 channels are available in the 100-pin package.
4. 10 channels are available in the 100-pin package.
5. M32C/87A has 1 channel. M32C/87B has no CAN module.

Figure 1.2 M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Block Diagram

1.4 Pin Assignments

Figures 1.3 to 1.5 show pin assignments (top view).



NOTES:
1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P6_4 / CTS1 / RTS1 / SS1 / OUTC2_1 / ISCLK2
4. P7_0 and P7_1 are N-channel open drain output ports.
5. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
6. Refer to **Package Dimensions** for the pin1 position on the package.
7. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.8 144-Pin Package List of Pin Names (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
1		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2		P9_5			CLK4/CAN1IN/$\overline{\text{CAN1WU}}$		ANEX0	
3		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$		DA1	
4		P9_3		TB3IN	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		DA0	
5		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7		P9_0		TB0IN	CLK3			
8		P14_6	$\overline{\text{INT8}}$					
9		P14_5	$\overline{\text{INT7}}$					
10		P14_4	$\overline{\text{INT6}}$					
11		P14_3				INPC1_7/OUTC1_7		
12		P14_2				INPC1_6/OUTC1_6		
13		P14_1				INPC1_5/OUTC1_5		
14		P14_0				INPC1_4/OUTC1_4		
15	BYTE							
16	CNVSS							
17	XCIN	P8_7						
18	XCOUT	P8_6						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P8_5	$\overline{\text{NMI}}$					
25		P8_4	$\overline{\text{INT2}}$					
26		P8_3	$\overline{\text{INT1}}$		CAN0IN/CAN1IN			
27		P8_2	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT			
28		P8_1		TA4IN/$\overline{\text{U}}$/RTP2_3	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	INPC1_5/OUTC1_5		
29		P8_0		TA4OUT/U	RXD5	ISRXD0		
30		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
31		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
32		P7_5		TA2IN/$\overline{\text{W}}$/RTP2_1		INPC1_2/OUTC1_2/ ISRXD1		
33		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
34		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	INPC1_0/OUTC1_0/ ISTXD1		
35		P7_2		TA1OUT/V	CLK2			
36		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
37		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
38		P6_7			TXD1/SDA1/SRXD1			
39	VCC1							
40		P6_6			RXD1/SCL1/STXD1			

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.9 144-Pin Package List of Pin Names (2)

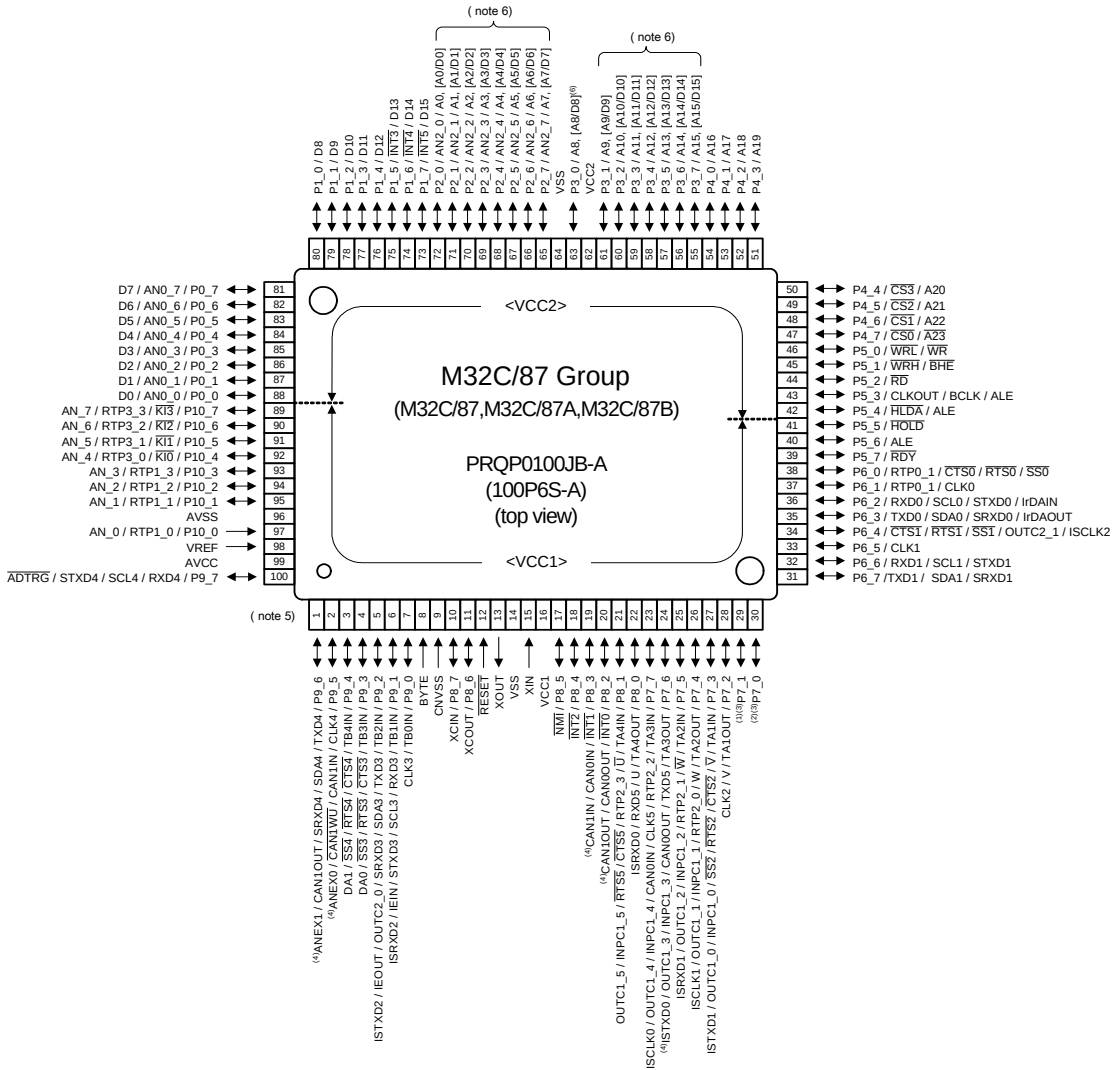
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
41	VSS							
42		P6_5			CLK1			
43		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	OUTC2_1/ISCLK2		
44		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
45		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
46		P6_1		RTP0_1	CLK0			
47		P6_0		RTP0_0	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$			
48		P13_7				OUTC2_7		
49		P13_6				OUTC2_1/ISCLK2		
50		P13_5				OUTC2_2/ISRXD2/IEIN		
51		P13_4				OUTC2_0/ISTXD2/ IEOUT		
52		P5_7						$\overline{\text{RDY}}$
53		P5_6						ALE
54		P5_5						$\overline{\text{HOLD}}$
55		P5_4						$\overline{\text{HLDA}}$/ALE
56		P13_3				OUTC2_3		
57	VSS							
58		P13_2				OUTC2_6		
59	VCC2							
60		P13_1				OUTC2_5		
61		P13_0				OUTC2_4		
62	CLKOUT	P5_3						BCLK/ALE
63		P5_2						$\overline{\text{RD}}$
64		P5_1						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P5_0						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P12_7						
67		P12_6						
68		P12_5						
69		P4_7						$\overline{\text{CS0}}$/$\overline{\text{A23}}$
70		P4_6						$\overline{\text{CS1}}$/A22
71		P4_5						$\overline{\text{CS2}}$/A21
72		P4_4						$\overline{\text{CS3}}$/A20
73		P4_3						A19
74	VCC2							
75		P4_2						A18
76	VSS							
77		P4_1						A17
78		P4_0						A16
79		P3_7						A15,[A15/D15]
80		P3_6						A14,[A14/D14]

Table 1.10 144-Pin Package List of Pin Names (3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
81		P3_5						A13,[A13/D13]
82		P3_4						A12,[A12/D12]
83		P3_3						A11,[A11/D11]
84		P3_2						A10,[A10/D10]
85		P3_1						A9,[A9/D9]
86		P12_4						
87		P12_3			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$			
88		P12_2			RXD6			
89		P12_1			CLK6			
90		P12_0			TXD6			
91	VCC2							
92		P3_0						A8,[A8/D8]
93	VSS							
94		P2_7					AN2_7	A7,[A7/D7]
95		P2_6					AN2_6	A6,[A6/D6]
96		P2_5					AN2_5	A5,[A5/D5]
97		P2_4					AN2_4	A4,[A4/D4]
98		P2_3					AN2_3	A3,[A3/D3]
99		P2_2					AN2_2	A2,[A2/D2]
100		P2_1					AN2_1	A1,[A1/D1]
101		P2_0					AN2_0	A0,[A0/D0]
102		P1_7	$\overline{\text{INT5}}$					D15
103		P1_6	$\overline{\text{INT4}}$					D14
104		P1_5	$\overline{\text{INT3}}$					D13
105		P1_4						D12
106		P1_3						D11
107		P1_2						D10
108		P1_1						D9
109		P1_0						D8
110		P0_7					AN0_7	D7
111		P0_6					AN0_6	D6
112		P0_5					AN0_5	D5
113		P0_4					AN0_4	D4
114		P11_4						
115		P11_3				INPC1_3/OUTC1_3		
116		P11_2				INPC1_2/OUTC1_2/ ISRXD1		
117		P11_1				INPC1_1/OUTC1_1/ ISCLK1		
118		P11_0				INPC1_0/OUTC1_0/ ISTXD1		
119		P0_3					AN0_3	D3
120		P0_2					AN0_2	D2

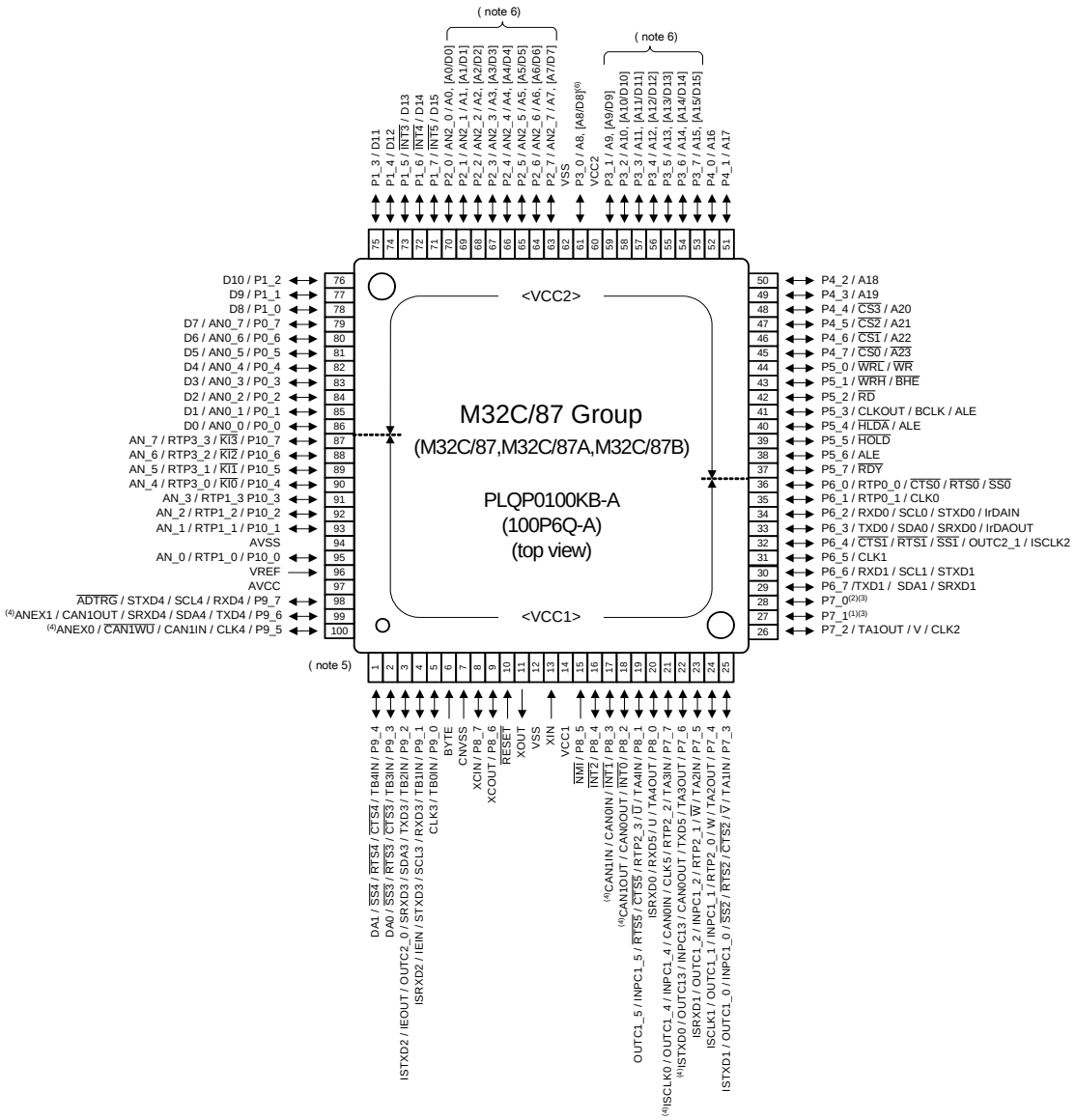
Table 1.11 144-Pin Package List of Pin Names (4)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
121		P0_1					AN0_1	D1
122		P0_0					AM0_0	D0
123		P15_7			$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$		AN15_7	
124		P15_6			CLK6		AN15_6	
125		P15_5			RXD6		AN15_5	
126		P15_4			TXD6		AN15_4	
127		P15_3			$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		AN15_3	
128		P15_2			RXD5	ISRXD0	AN15_2	
129		P15_1			CLK5	ISCLK0	AN15_1	
130	VSS							
131		P15_0			TXD5	ISTXD0	AN15_0	
132	VCC1							
133		P10_7	$\overline{\text{KI3}}$	RTP3_3			AN_7	
134		P10_6	$\overline{\text{KI2}}$	RTP3_2			AN_6	
135		P10_5	$\overline{\text{KI1}}$	RTP3_1			AN_5	
136		P10_4	$\overline{\text{KI0}}$	RTP3_0			AN_4	
137		P10_3		RTP1_3			AN_3	
138		P10_2		RTP1_2			AN_2	
139		P10_1		RTP1_1			AN_1	
140	AVSS							
141		P10_0		RTP1_0			AN_0	
142	VREF							
143	AVCC							
144		P9_7			RXD4/SCL4/STXD4		$\overline{\text{ADTRG}}$	



NOTES:
1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P7_0 and P7_1 are N-channel open drain output ports.
4. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
5. Refer to **Package Dimensions** for the pin1 position on the package.
6. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.4 Pin Assignment for 100-Pin Package



NOTES:
1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P7_0 and P7_1 are N-channel open drain output ports.
4. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
5. Refer to **Package Dimensions** for the pin1 position on the package.
6. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.12 100-Pin Package List of Pin Names (1)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin(1)	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
1	99		P9_6			TXD4/SDA4/SRXD4/ CAN1OUT		ANEX1	
2	100		P9_5			CLK4/CAN1IN/ CAN1WU		ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9_3		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/SRXD3	OUTC2_0/IEOUT/ISTXD2		
6	4		P9_1		TB1IN	RXD3/SCL3/STXD3	IEIN/ISRXD2		
7	5		P9_0		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVSS							
10	8	XCIN	P8_7						
11	9	XCOUT	P8_6						
12	10	RESET							
13	11	XOUT							
14	12	VSS							
15	13	XIN							
16	14	VCC1							
17	15		P8_5	NMI					
18	16		P8_4	INT2					
19	17		P8_3	INT1		CAN0IN/CAN1IN			
20	18		P8_2	INT0		CAN0OUT/CAN1OUT			
21	19		P8_1		TA4IN/U/RTP2_3	CTS5/RTS5	INPC1_5/OUTC1_5		
22	20		P8_0		TA4OUT/U	RXD5	ISRXD0		
23	21		P7_7		TA3IN/RTP2_2	CLK5/CAN0IN	INPC1_4/OUTC1_4/ ISCLK0		
24	22		P7_6		TA3OUT	TXD5/CAN0OUT	INPC1_3/OUTC1_3/ ISTXD0		
25	23		P7_5		TA2IN/W/RTP2_1		INPC1_2/OUTC1_2 ISRXD1		
26	24		P7_4		TA2OUT/W/ RTP2_0		INPC1_1/OUTC1_1/ ISCLK1		
27	25		P7_3		TA1IN/V	CTS2/RTS2/SS2	INPC1_0/OUTC1_0/ ISTXD1		
28	26		P7_2		TA1OUT/V	CLK2			
29	27		P7_1		TA0IN/TB5IN/ RTP0_3	RXD2/SCL2/STXD2	INPC1_7/OUTC1_7/ OUTC2_2/ISRXD2/IEIN		
30	28		P7_0		TA0OUT/RTP0_2	TXD2/SDA2/SRXD2	INPC1_6/OUTC1_6/ OUTC2_0/ISTXD2/IEOUT		
31	29		P6_7			TXD1/SDA1/SRXD1			
32	30		P6_6			RXD1/SCL1/STXD1			
33	31		P6_5			CLK1			
34	32		P6_4			CTS1/RTS1/SS1	OUTC2_1/ISCLK2		
35	33		P6_3			TXD0/SDA0/SRXD0/ IrDAOUT			
36	34		P6_2			RXD0/SCL0/STXD0/ IrDAIN			
37	35		P6_1		RTP0_1	CLK0			
38	36		P6_0		RTP0_0	CTS0/RTS0/SS0			
39	37		P5_7						RDY
40	38		P5_6						ALE

NOTE:
1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.13 100-Pin Package List of Pin Names (2)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
41	39		P5_5						$\overline{\text{HOLD}}$
42	40		P5_4						$\overline{\text{HLDA}}$/ALE
43	41	CLKOUT	P5_3						BCLK/ALE
44	42		P5_2						$\overline{\text{RD}}$
45	43		P5_1						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7						$\overline{\text{CS0}}$/A23
48	46		P4_6						$\overline{\text{CS1}}$/A22
49	47		P4_5						$\overline{\text{CS2}}$/A21
50	48		P4_4						$\overline{\text{CS3}}$/A20
51	49		P4_3						A19
52	50		P4_2						A18
53	51		P4_1						A17
54	52		P4_0						A16
55	53		P3_7						A15,[A15/D15]
56	54		P3_6						A14,[A14/D14]
57	55		P3_5						A13,[A13/D13]
58	56		P3_4						A12,[A12/D12]
59	57		P3_3						A11,[A11/D11]
60	58		P3_2						A10,[A10/D10]
61	59		P3_1						A9,[A9/D9]
62	60	VCC2							
63	61		P3_0						A8,[A8/D8]
64	62	VSS							
65	63		P2_7					AN2_7	A7,[A7/D7]
66	64		P2_6					AN2_6	A6,[A6/D6]
67	65		P2_5					AN2_5	A5,[A5/D5]
68	66		P2_4					AN2_4	A4,[A4/D4]
69	67		P2_3					AN2_3	A3,[A3/D3]
70	68		P2_2					AN2_2	A2,[A2/D2]
71	69		P2_1					AN2_1	A1,[A1/D1]
72	70		P2_0					AN2_0	A0,[A0/D0]
73	71		P1_7	$\overline{\text{INT5}}$					D15
74	72		P1_6	$\overline{\text{INT4}}$					D14
75	73		P1_5	$\overline{\text{INT3}}$					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8

Table 1.14 100-Pin Package List of Pin Names (3)

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
81	79		P0_7					AN0_7	D7
82	80		P0_6					AN0_6	D6
83	81		P0_5					AN0_5	D5
84	82		P0_4					AN0_4	D4
85	83		P0_3					AN0_3	D3
86	84		P0_2					AN0_2	D2
87	85		P0_1					AN0_1	D1
88	86		P0_0					AN0_0	D0
89	87		P10_7	$\overline{KI3}$	RTP3_3			AN_7	
90	88		P10_6	$\overline{KI2}$	RTP3_2			AN_6	
91	89		P10_5	$\overline{KI1}$	RTP3_1			AN_5	
92	90		P10_4	$\overline{KI0}$	RTP3_0			AN_4	
93	91		P10_3		RTP1_3			AN_3	
94	92		P10_2		RTP1_2			AN_2	
95	93		P10_1		RTP1_1			AN_1	
96	94	AVSS							
97	95		P10_0		RTP1_0			AN_0	
98	96	VREF							
99	97	AVCC							
100	98		P9_7			RXD4/SCL4/STXD4		$\overline{ADTRG}$	

1.5 Pin Descriptions

Table 1.15 Pin Functions (100-Pin and 144-Pin Packages) (1)

Type	Symbol	I/O Type	Supply Voltage	Description
Power supply	VCC1,VCC2 VSS	–	–	Apply 3.0 to 5.5 V to pins VCC1 and VCC2, and 0 V to the VSS pin. The input condition of VCC1 ≥ VCC2 must be met.
Analog power supply input	AVCC AVSS	–	VCC1	Power supply input pins to the A/D converter and D/A converter. Connect the AVCC pin to VCC1, and the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The MCU is placed in a reset state while applying an “L” signal to the $\overline{\text{RESET}}$ pin.
CNVSS	CNVSS	I	VCC1	This pin switches processor mode. Apply an “L” to the CNVSS pin to start up in single-chip mode, or an “H” to start up in microprocessor mode (mask ROM, flash memory version) and boot mode (flash memory version).
External data bus width select input	BYTE	I	VCC1	Switches a data bus width in external memory space 3. A data bus is 16 bits wide when the BYTE pin is held “L” and 8 bits wide when it is held “H”. Fix to either “L” or “H”. Apply an “L” to the BYTE pin in single-chip mode.
Bus control Pins	D0 to D7	I/O	VCC2	Data (D0 to D7) input/output pins while accessing an external memory space with separate bus.
	D8 to D15	I/O	VCC2	Data (D8 to D15) input/output pins while accessing an external memory space with 16-bit separate bus.
	A0 to A22	O	VCC2	Address bits (A0 to A22) output pins.
	$\overline{\text{A23}}$	O	VCC2	Inverted address bit (A23) output pin.
	A0/D0 to A7/D7	I/O	VCC2	Data (D0 to D7) input/output and 8 low-order address bits (A0 to A7) output are performed by time-sharing these pins while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Data (D8 to D15) input/output and 8 middle-order address bits (A8 to A15) output are performed by time-sharing these pins while accessing an external memory space with 16-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Chip-select signal output pins used to specify external devices.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	$\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$) and $\overline{\text{RD}}$ signal output pins. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{WR}}$ and $\overline{\text{BHE}}$ by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected: If external data bus is 16 bits wide, data is written to an even address in external memory space while an “L” is output from the $\overline{\text{WRL}}$ pin. Data is written to an odd address while an “L” is output from the $\overline{\text{WRH}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected: Data is written while an “L” is output from the $\overline{\text{WR}}$ pin. Data is read while an “L” is output from the $\overline{\text{RD}}$ pin. Data in odd address is accessed while an “L” is output from the $\overline{\text{BHE}}$ pin. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ when an external data bus is 8 bits wide.
	ALE	O	VCC2	ALE signal is used for the external devices to latch address signals when the multiplexed bus is selected.
	$\overline{\text{HOLD}}$	I	VCC2	The MCU is placed in a hold state while an “L” signal is applied to the $\overline{\text{HOLD}}$ pin.
	$\overline{\text{HLDA}}$	O	VCC2	The $\overline{\text{HLDA}}$ pin outputs an “L” while the MCU is placed in a hold state.
	$\overline{\text{RDY}}$	I	VCC2	Bus is placed in a wait state while an “L” signal is applied to the $\overline{\text{RDY}}$ pin.

I: Input O: Output I/O: Input and output

Table 1.16 Pin Description (100-Pin and 144-Pin Packages) (2)

Type	Symbol	I/O Type	Supply Voltage	Description
Main clock input	XIN	I	VCC1	Input/output pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply an external clock, apply it to XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	Input/output pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply an external clock, apply it to XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Bus clock output pin.
Clock output	CLKOUT	O	VCC2	The CLKOUT pin outputs the clock having the same frequency as fC, f8, or f32
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
	$\overline{\text{NT3}}$ to $\overline{\text{INT5}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	$\overline{\text{NMI}}$ interrupt input pin. Connect the $\overline{\text{NMI}}$ pin to VCC1 via a resistor when the $\overline{\text{NMI}}$ interrupt is not used.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	Timer A0 to A4 input/output pins. (TA0OUT is N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Timer A0 to A4 input pins.
Timer B	TB0IN to TB5IN	I	VCC1	Timer B0 to B5 input pins.
Three-phase motor control timer output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Three-phase motor control timer output pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS5}}$	I	VCC1	Input pins to control data transmission.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS5}}$	O	VCC1	Output pins to control data reception.
	CLK0 to CLK5	I/O	VCC1	Serial clock input/output pins.
	RXD0 to RXD5	I	VCC1	Serial data input pins.
	TXD0 to TXD5	O	VCC1	Serial data output pins. (TXD2 is N-channel open drain output.)
I^2C mode	SDA0 to SDA4	I/O	VCC1	Serial data input/output pins. (SDA2 is N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Serial clock input/output pins. (SCL2 is N-channel open drain output.)
Serial interface special function	STXD0 to STXD4	O	VCC1	Serial data output pins when slave mode is selected. (STXD2 is N-channel open drain output.)
	SRXD0 to SRXD4	I	VCC1	Serial data input pins when slave mode is selected.
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	VCC1	Control input pins used in the serial interface special mode.
IrDA	IrDAIN	I	VCC1	IrDA serial data input pin.
	IrDAOUT	O	VCC1	IrDA serial data output pin.
CAN(1)	CAN0IN, CAN1IN	I	VCC1	Received data input pins for the CAN communication function.
	CAN0OUT, CAN1OUT	O	VCC1	Transmit data output pins for the CAN communication function.
	$\overline{\text{CAN1WU}}$	I	VCC1	CAN wake-up interrupt input pin.

I: Input O: Output I/O: Input and output

NOTE:

1. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.

Table 1.17 Pin Description (100-Pin and 144-Pin Package) (3)

Type	Symbol	I/O Type	Supply Voltage	Description
Intelligent I/O	INPC1_0 to INPC1_3	I	VCC1/ VCC2(1)	Input pins for the time measurement function.
	INPC1_4 to INPC1_7	I	VCC1	
	OUTC1_0 to OUTC1_3	O	VCC1/ VCC2(1)	Output pins for the waveform generation function. (OUTC1_6/OUTC2_0 and OUTC1_7/OUTC2_2 assigned to ports 7_0 and 7_1 are N-channel open drain output.)
	OUTC1_4 to OUTC1_7	O	VCC1	
	OUTC2_0 to OUTC2_2	O	VCC1/ VCC2(1)	
	ISCLK0	I/O	VCC1	Clock input/output pins for the intelligent I/O communication function.
	ISCLK1, ISCLK2	I/O	VCC1/ VCC2(1)	
	ISRXD0	I	VCC1	Data input pins for the intelligent I/O communication function.
	ISRXD1, ISRXD2	I	VCC1/ VCC2(1)	
	ISTXD0	O	VCC1	Data output pins for the intelligent I/O communication function. (ISTXD2 assigned to port 7_0 is N-channel open drain output.)
	ISTXD1, ISTXD2	O	VCC1/ VCC2(1)	
	IEIN	I	VCC1/ VCC2(1)	Data input pin for the intelligent I/O communication function.
	IEOUT	O	VCC1/ VCC2(1)	Data output pin for the intelligent I/O communication function. (IEOUT assigned to port 7_0 is N-channel open drain output.)
Reference voltage input	VREF	I	–	The VREF pin supplies the reference voltage to the A/D converter and D/A converter.
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	VCC1	Analog input pins for the A/D converter.
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input pin for the A/D converter.
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter or output pin in external op-amp connection mode.
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	VCC1	Output pins for the D/A converter.
Real-time port	RTP0_0 to RTP0_3 RTP1_0 to RTP1_3 RTP2_0 to RTP2_3 RTP3_0 to RTP3_3	O	VCC1	These pins function as real-time ports. (RTP0_2 and RTP0_3 are N-channel open drain output.)

I: Input O: Output I/O: Input and output

NOTE:

1. Only VCC1 can be used in the 100-pin package.

Table 1.18 Pin Description (100-Pin and 144-Pin Package) (4)

Type	Symbol	I/O Type	Supply Voltage	Description
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. The Port Pi Direction Register (i = 0 to 15) determines if each pin is used as an input port or an output port. The Pull-Up Control Resisters determine if the input ports, divided into groups of four, are pulled up or not.
	P6_0 to P6_7, P7_0 to P7_7, P9_0 to P9_7, P10_0 to P10_7	I/O	VCC1	These 8-bit I/O ports are functionally equivalent to P0. (P7_0 and P7_1 are N-channel open drain output.)
	P8_0 to P8_4 P8_6, P8_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.
Input port	P8_5	I	VCC1	Shares the pin with $\overline{\text{NMI}}$. Input port to read $\overline{\text{NMI}}$ pin level.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Key input interrupt input pins.

I: Input O: Output I/O: Input and output

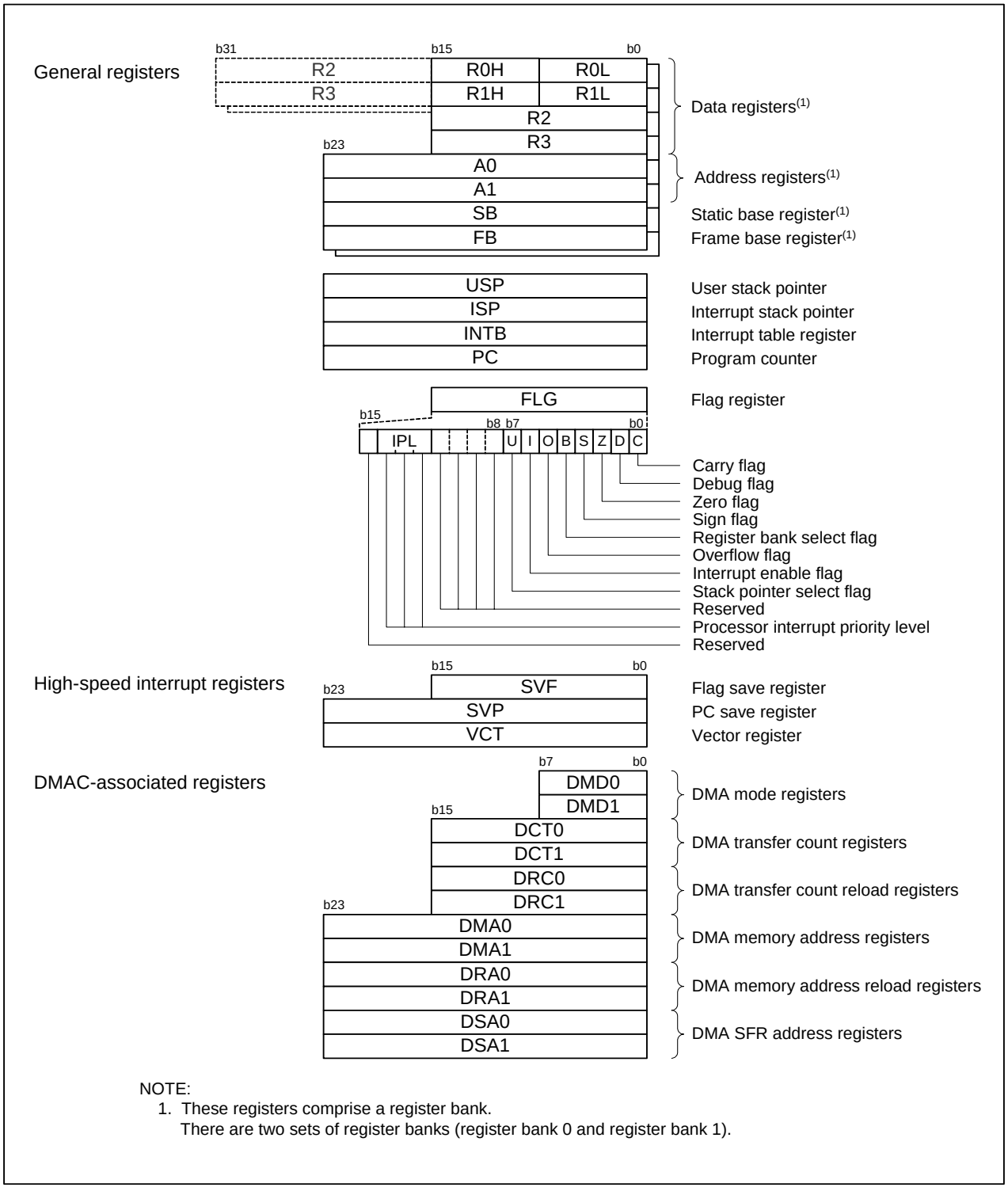
Table 1.19 Pin Description (144-Pin Package Only)

Type	Symbol	I/O Type	Supply Voltage	Description
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT6}}$ to $\overline{\text{INT8}}$	I	VCC1	$\overline{\text{INT}}$ interrupt input pins.
Serial interface	$\overline{\text{CTS6}}$	I	VCC1/ VCC2	Input pin to control data transmission.
	$\overline{\text{RTS6}}$	O	VCC1/ VCC2	Output pin to control data reception.
	CLK6	I/O	VCC1/ VCC2	Serial clock input/output pin.
	RXD6	I	VCC1/ VCC2	Serial data input pin.
	TXD6	O	VCC1/ VCC2	Serial data output pin.
Intelligent I/O	OUTC2_3 to OUTC2_7	O	VCC2	Output pins for the waveform generation function.
A/D converter	AN15_0 to AN15_7	I	VCC1	Analog input pins for the A/D converter.
I/O port	P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7	I/O	VCC2	These I/O ports are functionally equivalent to P0.
	P14_0 to P14_6, P15_0 to P15_7	I/O	VCC1	These I/O ports are functionally equivalent to P0.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
The register bank is comprised of eight registers (R0, R1, R2, R3, A0, A1, SB, and FB) out of 28 CPU registers. There are two sets of register banks.



NOTE:
1. These registers comprise a register bank.
There are two sets of register banks (register bank 0 and register bank 1).

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order (R0H/R1H) and low-order bits (R0L/R1L) to be used separately as 8-bit data registers.
R0 can be combined with R2 and used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers used for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register used for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register used for FB-relative addressing.

2.1.5 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of a relocatable interrupt vector table.

2.1.7 Program Counter (PC)

PC is 24 bits wide and indicates the address of the next instruction to be executed.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating the CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether or not carry or borrow has been generated after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.1.8.3 Zero Flag (Z)

The Z flag becomes 1 when an arithmetic operation results in 0; otherwise becomes 0.

2.1.8.4 Sign Flag (S)

The S flag becomes 1 when an arithmetic operation results in a negative value; otherwise becomes 0.

2.1.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is set to 0. Register bank 1 is selected when this flag is set to 1.

2.1.8.6 Overflow Flag (O)

The O flag becomes 1 when an arithmetic operation results in an overflow; otherwise becomes 0.

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0 and enabled when it is set to 1. The I flag becomes 0 when an interrupt request is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0. USP is selected when the U flag is set to 1.
The U flag becomes 0 when a hardware interrupt request is acknowledged or the INT instruction specifying software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority level than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

Only write 0 to bits assigned to the reserved space. When read, the bits return undefined values.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with the DMAC are as follows:

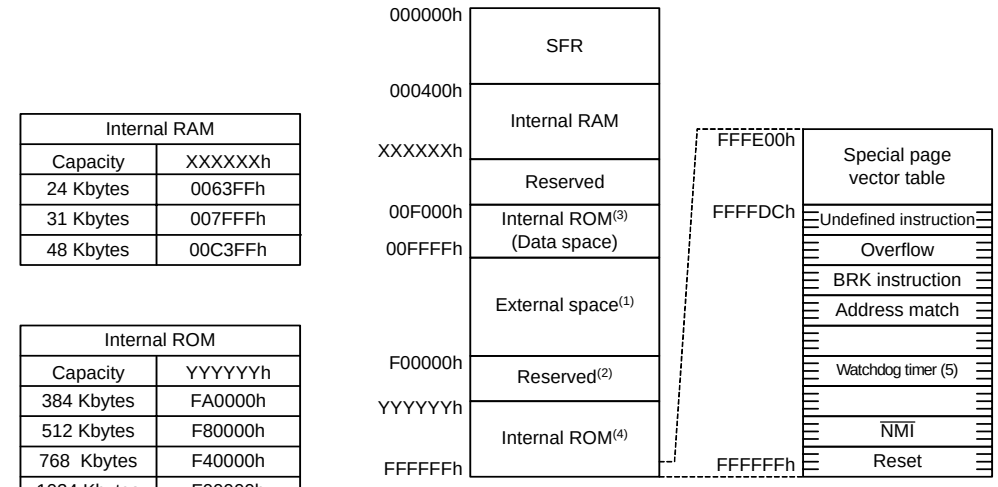
- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA memory address reload register (DRA0, DRA1)
- DMA SFR address register (DSA0, DSA1)

3. Memory

Figure 3.1 is a memory map of the M32C/87 Group (M32C/87, M32C/87A, M32C/87B).
The M32C/87 Group (M32C/87, M32C/87A, M32C/87B) has 16-Mbyte address space from addresses 000000h to FFFFFFh.
The internal ROM is allocated in lower addresses, beginning with address FFFFFFh. For example, a 512-Kbyte internal ROM area is allocated in addresses F80000h to FFFFFFh.
The fixed interrupt vectors are allocated in addresses FFFFDCh to FFFFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 000400h. For example, a 48-Kbyte internal RAM area is allocated in addresses 000400h to 00C3FFh. The internal RAM is used not only for storing data but for the stacks when subroutines are called or when interrupt requests are acknowledged.
SFRs are allocated in addresses 000000h to 0003FFh. The peripheral function control registers such as for I/O ports, A/D converters, serial interfaces, timers are allocated here. All blank spaces within SFRs are reserved and cannot be accessed by users.
The special page vectors are allocated addresses FFFE00h to FFFFDBh. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

Internal RAM	
Capacity	XXXXXXh
24 Kbytes	0063FFh
31 Kbytes	007FFFh
48 Kbytes	00C3FFh

Internal ROM	
Capacity	YYYYYYh
384 Kbytes	FA0000h
512 Kbytes	F80000h
768 Kbytes	F40000h
1024 Kbytes	F00000h



NOTES:
1. The space is used as the external space in memory expansion mode and in microprocessor mode.
2. The space is reserved in memory expansion mode. It is used as the external space in microprocessor mode.
3. Additional 4-Kbyte space is provided in the flash memory version to store data. This space is used in single chip mode and memory expansion mode. It is reserved in microprocessor mode.
4. This space is used in single chip mode and memory expansion mode. It is used as the external space in microprocessor mode.
5. The watchdog timer interrupt, oscillation stop detection interrupt, and Vdet4 detection interrupt use the same vector.

Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

Special Function Registers (SFRs) are the control registers of peripheral functions. Tables 4.1 to 4.20 list SFR address maps.

Table 4.1 SFR Address Map (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0(1)	PM0	1000 0000b(CNVSS="L") 0000 0011b(CNVSS="H")
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	0000 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	XXXX 0000b
000Bh	External Data Bus Width Control Register	DS	XXXX 1000b(BYTE="L") XXXX 0000b(BYTE="H")
000Ch	Main Clock Division Register	MCD	XXX0 1000b
000Dh	Oscillation Stop Detection Register	CM2	00h
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0010h	Address Match Interrupt Register 0	RMAD0	000000h
0011h			
0012h			
0013h	Processor Mode Register 2	PM2	00h
0014h	Address Match Interrupt Register 1	RMAD1	000000h
0015h			
0016h			
0017h	Voltage Detection Register 2	VCR2	00h
0018h	Address Match Interrupt Register 2	RMAD2	000000h
0019h			
001Ah			
001Bh	Voltage Detection Register 1	VCR1	0000 1000b
001Ch	Address Match Interrupt Register 3	RMAD3	000000h
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	PLL Control Register 0	PLC0	0001 X010b
0027h	PLL Control Register 1	PLC1	000X 0000b
0028h	Address Match Interrupt Register 4	RMAD4	000000h
0029h			
002Ah			
002Bh			
002Ch	Address Match Interrupt Register 5	RMAD5	000000h
002Dh			
002Eh			
002Fh	Vdet4 Detection Interrupt Register	D4INT	XX00 0000b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. Bits PM01 and PM00 in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.2 SFR Address Map (2)

Address	Register	Symbol	After Reset
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h	Address Match Interrupt Register 6	RMAD6	000000h
0039h			
003Ah			
003Bh			
003Ch	Address Match Interrupt Register 7	RMAD7	000000h
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	External Space Wait Control Register 0	EWCR0	X0X0 0011b
0049h	External Space Wait Control Register 1	EWCR1	X0X0 0011b
004Ah	External Space Wait Control Register 2	EWCR2	X0X0 0011b
004Bh	External Space Wait Control Register 3	EWCR3	X0X0 0011b
004Ch			
004Dh			
004Eh			
004Fh			
0050h			
0051h			
0052h			
0053h			
0054h			
0055h	Flash Memory Control Register 1	FMR1	0000 0X0Xb
0056h			
0057h	Flash Memory Control Register 0	FMR0	0000 0001b(Flash Memory) XXXX XXX0b(Mask ROM)
0058h			
0059h			
005Ah			
005Bh			
005Ch			
005Dh			
005Eh			
005Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.3 SFR Address Map (3)

Address	Register	Symbol	After Reset
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
0069h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
006Ah	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Bh	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
006Dh	UART3 Receive/ACK Interrupt Control Register	S3RIC	XXXX X000b
006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
006Fh	UART4 Receive/ACK Interrupt Control Register	S4RIC	XXXX X000b
0070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
0071h	UART0/UART3 Bus Conflict Detection Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000b
0072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
0073h	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000b
0074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
0075h	II/O Interrupt Control Register 0 / CAN1 interrupt Control Register 0	IIO0IC/CAN3IC	XXXX X000b
0076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
0077h	II/O Interrupt Control Register 2	IIO2IC	XXXX X000b
0078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
0079h	II/O Interrupt Control Register 4	IIO4IC	XXXX X000b
007Ah	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
007Bh	II/O Interrupt Control Register 6	IIO6IC	XXXX X000b
007Ch	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
007Dh	II/O Interrupt Control Register 8	IIO8IC	XXXX X000b
007Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
007Fh	II/O Interrupt Control Register 10 / CAN0 Interrupt Control Register 1	IIO10IC/CAN1IC	XXXX X000b
0080h			
0081h	II/O Interrupt Control Register 11 / CAN0 Interrupt Control Register 2	IIO11IC/CAN2IC	XXXX X000b
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0089h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
008Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
008Bh	UART3 Transmit/NACK Interrupt Control Register	S3TIC	XXXX X000b
008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
008Dh	UART4 Transmit/NACK Interrupt Control Register	S4TIC	XXXX X000b
008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
008Fh	UART2 Bus Conflict Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.4 SFR Address Map (4)

Address	Register	Symbol	After Reset
0090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
0091h	UART1/UART4 Bus Conflict Detection Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000b
0092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
0093h	Key Input Interrupt Control Register	KUPIC	XXXX X000b
0094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
0095h	II/O Interrupt Control Register 1 / CAN1 Interrupt Control Register 1	IIO1IC/CAN4IC	XXXX X000b
0096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0097h	II/O Interrupt Control Register 3	IIO3IC	XXXX X000b
0098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0099h	II/O Interrupt Control Register 5 / CAN1 Interrupt Control Register 2	IIO5IC/CAN5IC	XXXX X000b
009Ah	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
009Bh	II/O Interrupt Control Register 7	IIO7IC	XXXX X000b
009Ch	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
009Dh	II/O Interrupt Control Register 9 / CAN0 Interrupt Control Register 0	IIO9IC/CAN0IC	XXXX X000b
009Eh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
009Fh	Exit Priority Register	RLVL	XXXX 0000b
00A0h	Interrupt Request Register 0	IIO0IR	0000 000Xb
00A1h	Interrupt Request Register 1	IIO1IR	0000 000Xb
00A2h	Interrupt Request Register 2	IIO2IR	0000 000Xb
00A3h	Interrupt Request Register 3	IIO3IR	0000 000Xb
00A4h	Interrupt Request Register 4	IIO4IR	0000 000Xb
00A5h	Interrupt Request Register 5	IIO5IR	0000 000Xb
00A6h	Interrupt Request Register 6	IIO6IR	0000 000Xb
00A7h	Interrupt Request Register 7	IIO7IR	0000 000Xb
00A8h	Interrupt Request Register 8	IIO8IR	0000 000Xb
00A9h	Interrupt Request Register 9	IIO9IR	0000 000Xb
00AAh	Interrupt Request Register 10	IIO10IR	0000 000Xb
00ABh	Interrupt Request Register 11	IIO11IR	0000 000Xb
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	Interrupt Enable Register 0	IIO0IE	00h
00B1h	Interrupt Enable Register 1	IIO1IE	00h
00B2h	Interrupt Enable Register 2	IIO2IE	00h
00B3h	Interrupt Enable Register 3	IIO3IE	00h
00B4h	Interrupt Enable Register 4	IIO4IE	00h
00B5h	Interrupt Enable Register 5	IIO5IE	00h
00B6h	Interrupt Enable Register 6	IIO6IE	00h
00B7h	Interrupt Enable Register 7	IIO7IE	00h
00B8h	Interrupt Enable Register 8	IIO8IE	00h
00B9h	Interrupt Enable Register 9	IIO9IE	00h
00BAh	Interrupt Enable Register 10	IIO10IE	00h
00BBh	Interrupt Enable Register 11	IIO11IE	00h
00BCh			
00BDh			
00BEh			
00BFh to 00DFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.5 SFR Address Map (5)

Address	Register	Symbol	After Reset
00E0h			
00E1h			
00E2h			
00E3h			
00E4h			
00E5h			
00E6h			
00E7h			
00E8h	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXXb
00E9h			XXX0 XXXXb
00EAh	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XXh
00EBh			
00ECh	Group 0 Receive Input Register	G0RI	XXh
00EDh	Group 0 SI/O Communication Mode Register	G0MR	00h
00EEh	Group 0 Transmit Output Register	G0TO	XXh
00EFh	Group 0 SI/O Communication Control Register	G0CR	0000 X011b
00F0h	Group 0 Data Compare Register 0	G0CMP0	XXh
00F1h	Group 0 Data Compare Register 1	G0CMP1	XXh
00F2h	Group 0 Data Compare Register 2	G0CMP2	XXh
00F3h	Group 0 Data Compare Register 3	G0CMP3	XXh
00F4h	Group 0 Data Mask Register 0	G0MSK0	XXh
00F5h	Group 0 Data Mask Register 1	G0MSK1	XXh
00F6h	Communication Clock Select Register	CCS	XXXX 0000b
00F7h			
00F8h	Group 0 Receive CRC Code Register	G0RCRC	XXXXh
00F9h			
00FAh	Group 0 Transmit CRC Code Register	G0TCRC	0000h
00FBh			
00FCh	Group 0 SI/O Expansion Mode Register	G0EMR	00h
00FDh	Group 0 SI/O Extended Receive Control Register	G0ERC	00h
00FEh	Group 0 SI/O Special Communication Interrupt Detection Register	G0IRF	0000 XXXXb
00FFh	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXXb
0100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
0101h			
0102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
0103h			
0104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
0105h			
0106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
0107h			
0108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
0109h			
010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
010Bh			
010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
010Dh			
010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
010Fh			
0110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
0111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
0112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
0113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
0114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
0115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
0116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
0117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
0118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
0119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.6 SFR Address Map (6)

Address	Register	Symbol	After Reset
011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
0120h 0121h	Group 1 Base Timer Register	G1BT	XXXXh
0122h	Group 1 Base Timer Control Register 0	G1BCR0	00h
0123h	Group 1 Base Timer Control Register 1	G1BCR1	X000 000Xb
0124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
0125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
0126h	Group 1 Function Enable Register	G1FE	00h
0127h	Group 1 Function Select Register	G1FS	00h
0128h 0129h	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXXb X000 XXXXb
012Ah	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XXh
012Bh			
012Ch	Group 1 Receive Input Register	G1RI	XXh
012Dh	Group 1 SI/O Communication Mode Register	G1MR	00h
012Eh	Group 1 Transmit Output Register	G1TO	XXh
012Fh	Group 1 SI/O Communication Control Register	G1CR	0000 X011b
0130h	Group 1 Data Compare Register 0	G1CMP0	XXh
0131h	Group 1 Data Compare Register 1	G1CMP1	XXh
0132h	Group 1 Data Compare Register 2	G1CMP2	XXh
0133h	Group 1 Data Compare Register 3	G1CMP3	XXh
0134h	Group 1 Data Mask Register 0	G1MSK0	XXh
0135h	Group 1 Data Mask Register 1	G1MSK1	XXh
0136h			
0137h			
0138h 0139h	Group 1 Receive CRC Code Register	G1RCRC	XXXXh
013Ah 013Bh	Group 1 Transmit CRC Code Register	G1TCRC	0000h
013Ch	Group 1 SI/O Expansion Mode Register	G1EMR	00h
013Dh	Group 1 SI/O Extended Receive Control Register	G1ERC	00h
013Eh	Group 1 SI/O Special Communication Interrupt Detection Register	G1IRF	0000 XXXXb
013Fh	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXXb
0140h 0141h	Group 2 Waveform Generation Register 0	G2PO0	XXXXh
0142h 0143h	Group 2 Waveform Generation Register 1	G2PO1	XXXXh
0144h 0145h	Group 2 Waveform Generation Register 2	G2PO2	XXXXh
0146h 0147h	Group 2 Waveform Generation Register 3	G2PO3	XXXXh
0148h 0149h	Group 2 Waveform Generation Register 4	G2PO4	XXXXh
014Ah 014Bh	Group 2 Waveform Generation Register 5	G2PO5	XXXXh
014Ch 014Dh	Group 2 Waveform Generation Register 6	G2PO6	XXXXh
014Eh 014Fh	Group 2 Waveform Generation Register 7	G2PO7	XXXXh

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.7 SFR Address Map (7)

Address	Register	Symbol	After Reset
0150h	Group 2 Waveform Generation Control Register 0	G2POCR0	00h
0151h	Group 2 Waveform Generation Control Register 1	G2POCR1	00h
0152h	Group 2 Waveform Generation Control Register 2	G2POCR2	00h
0153h	Group 2 Waveform Generation Control Register 3	G2POCR3	00h
0154h	Group 2 Waveform Generation Control Register 4	G2POCR4	00h
0155h	Group 2 Waveform Generation Control Register 5	G2POCR5	00h
0156h	Group 2 Waveform Generation Control Register 6	G2POCR6	00h
0157h	Group 2 Waveform Generation Control Register 7	G2POCR7	00h
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	Group 2 Base Timer Register	G2BT	XXXXh
0161h			
0162h	Group 2 Base Timer Control Register 0	G2BCR0	00h
0163h	Group 2 Base Timer Control Register 1	G2BCR1	00h
0164h	Base Timer Start Register	BTSR	XXXX 0000b
0165h			
0166h	Group 2 Function Enable Register	G2FE	00h
0167h	Group 2 RTP Output Buffer Register	G2RTP	00h
0168h			
0169h			
016Ah	Group 2 SI/O Communication Mode Register	G2MR	00XX X000b
016Bh	Group 2 SI/O Communication Control Register	G2CR	0000 X000b
016Ch	Group 2 SI/O Transmit Buffer Register	G2TB	XXXXh
016Dh			
016Eh	Group 2 SI/O Receive Buffer Register	G2RB	XXXXh
016Fh			
0170h	Group 2 IEBus Address Register	IEAR	XXXXh
0171h			
0172h	Group 2 IEBus Control Register	IECR	00XX X000b
0173h	Group 2 IEBus Transmit Interrupt Source Detection Register	IETIF	XXX0 0000b
0174h	Group 2 IEBus Receive Interrupt Source Detection Register	IERIF	XXX0 0000b
0175h			
0176h			
0177h	Input Function Select Register B	IPSB	00h
0178h	Input Function Select Register	IPS	00h
0179h	Input Function Select Register A	IPSA	00h
017Ah			
017Bh			
017Ch			
017Dh to 01BFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.8 SFR Address Map (8)

Address	Register	Symbol	After Reset
01C0h	UART5 Transmit/Receive Mode Register	U5MR	00h
01C1h	UART5 Baud Rate Register	U5BRG	XXh
01C2h	UART5 Transmit Buffer Register	U5TB	XXXXh
01C3h			
01C4h	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
01C5h	UART5 Transmit/Receive Control Register 1	U5C1	XXXX 0010b
01C6h	UART5 Receive Buffer Register	U5RB	XXXXh
01C7h			
01C8h	UART6 Transmit/Receive Mode Register	U6MR	00h
01C9h	UART6 Baud Rate Register	U6BRG	XXh
01CAh	UART6 Transmit Buffer Register	U6TB	XXXXh
01CBh			
01CCh	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
01CDh	UART6 Transmit/Receive Control Register 1	U6C1	XXXX 0010b
01CEh	UART6 Receive Buffer Register	U6RB	XXXXh
01CFh			
01D0h	UART5, UART6 Transmit/Receive Control Register	U56CON	X000 0000b
01D1h	UART5, UART6 Input Pin Function Select Register	U56IS	X000 X000b
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h	RTP Output Buffer Register 0	RTP0R	XXh
01D9h	RTP Output Buffer Register 1	RTP1R	XXh
01DAh	RTP Output Buffer Register 2	RTP2R	XXh
01DBh	RTP Output Buffer Register 3	RTP3R	XXh
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	CAN0 Message Slot Buffer 0 Standard ID0(1)(2)	C0SLOT0_0	XXh
01E1h	CAN0 Message Slot Buffer 0 Standard ID1(1)(2)	C0SLOT0_1	XXh
01E2h	CAN0 Message Slot Buffer 0 Extended ID0(1)(2)	C0SLOT0_2	XXh
01E3h	CAN0 Message Slot Buffer 0 Extended ID1(1)(2)	C0SLOT0_3	XXh
01E4h	CAN0 Message Slot Buffer 0 Extended ID2(1)(2)	C0SLOT0_4	XXh
01E5h	CAN0 Message Slot Buffer 0 Data Length Code(1)(2)	C0SLOT0_5	XXh
01E6h	CAN0 Message Slot Buffer 0 Data 0(1)(2)	C0SLOT0_6	XXh
01E7h	CAN0 Message Slot Buffer 0 Data 1(1)(2)	C0SLOT0_7	XXh
01E8h	CAN0 Message Slot Buffer 0 Data 2(1)(2)	C0SLOT0_8	XXh
01E9h	CAN0 Message Slot Buffer 0 Data 3(1)(2)	C0SLOT0_9	XXh
01EAh	CAN0 Message Slot Buffer 0 Data 4(1)(2)	C0SLOT0_10	XXh
01EBh	CAN0 Message Slot Buffer 0 Data 5(1)(2)	C0SLOT0_11	XXh
01ECh	CAN0 Message Slot Buffer 0 Data 6(1)(2)	C0SLOT0_12	XXh
01EDh	CAN0 Message Slot Buffer 0 Data 7(1)(2)	C0SLOT0_13	XXh
01EEh	CAN0 Message Slot Buffer 0 Time Stamp High-Order(1)(2)	C0SLOT0_14	XXh
01EFh	CAN0 Message Slot Buffer 0 Time Stamp Low-Order(1)(2)	C0SLOT0_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
2. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.9 SFR Address Map (9)

Address	Register[2][3]	Symbol	After Reset
01F0h	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XXh
01F1h	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XXh
01F2h	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XXh
01F3h	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XXh
01F4h	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XXh
01F5h	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XXh
01F6h	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XXh
01F7h	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XXh
01F8h	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XXh
01F9h	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XXh
01FAh	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XXh
01FBh	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XXh
01FCh	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XXh
01FDh	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XXh
01FEh	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XXh
01FFh	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XXh
0200h	CAN0 Control Register 0	C0CTLR0	XX01 0X01b[1]
0201h			XXXX 0000b[1]
0202h	CAN0 Status Register	C0STR	0000 0000b[1]
0203h			X000 0X01b[1]
0204h	CAN0 Extended ID Register	C0IDR	0000h[1]
0205h			
0206h	CAN0 Configuration Register	C0CONR	0000 XXXXb[1]
0207h			0000 0000b[1]
0208h	CAN0 Time Stamp Register	C0TSR	0000h[1]
0209h			
020Ah	CAN0 Transmit Error Count Register	C0TEC	00h[1]
020Bh	CAN0 Receive Error Count Register	C0REC	00h[1]
020Ch	CAN0 Slot Interrupt Status Register	C0SISTR	0000h[1]
020Dh			
020Eh			
020Fh			
0210h	CAN0 Slot Interrupt Mask Register	C0SIMKR	0000h[1]
0211h			
0212h			
0213h			
0214h	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000b[1]
0215h	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000b[1]
0216h	CAN0 Error Source Register	C0EFR	00h[1]
0217h	CAN0 Baud Rate Prescaler	C0BRP	0000 0001b[1]
0218h			
0219h	CAN0 Mode Register	C0MDR	XXXX XX00b[1]
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.10 SFR Address Map (10)

Address	Register[3][4]	Symbol	After Reset
0220h	CAN0 Single Shot Control Register	C0SSCTLR	0000h[1][2]
0221h			
0222h			
0223h			
0224h	CAN0 Single Shot Status Register	C0SSSTR	0000h[1][2]
0225h			
0226h			
0227h			
0228h	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000b[1][2]
0229h	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000b[1][2]
022Ah	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000b[1][2]
022Bh	CAN0 Global Mask Register Extended ID1	C0GMR3	00h[1][2]
022Ch	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000b[1][2]
022Dh			
022Eh			
022Fh			
0230h	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0 / C0LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0231h	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1 / C0LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
0232h	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2 / C0LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
0233h	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3 / C0LMAR3	00h[1][2]/ 00h[1][2]
0234h	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4 / C0LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
0235h	CAN0 Message Slot 5 Control Register	C0MCTL5	00h[1][2]
0236h	CAN0 Message Slot 6 Control Register	C0MCTL6	00h[1][2]
0237h	CAN0 Message Slot 7 Control Register	C0MCTL7	00h[1][2]
0238h	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8 / C0LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
0239h	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9 / C0LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
023Ah	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10 / C0LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
023Bh	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11 / C0LMBR3	00h[1][2]/ 00h[1][2]
023Ch	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12 / C0LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
023Dh	CAN0 Message Slot 13 Control Register	C0MCTL13	00h[1][2]
023Eh	CAN0 Message Slot 14 Control Register	C0MCTL14	00h[1][2]
023Fh	CAN0 Message Slot 15 Control Register	C0MCTL15	00h[1][2]
0240h	CAN0 Slot Buffer Select Register	C0SBS	00h[2]
0241h	CAN0 Control Register 1	C0CTLR1	X000 00XXb[2]
0242h	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0b
0243h			
0244h	CAN0 Acceptance Filter Support Register	C0AFS	0000 0000b[2]
0245h			0000 0001b[2]
0246h			
0247h			
0248h			
0249h			
024Ah to 024Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:

1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 0220h to 023Fh.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.11 SFR Address Map (11)

Address	Register[2][3]	Symbol	After Reset
0250h	CAN1 Slot Buffer Select Register	C1SBS	00h[1]
0251h	CAN1 Control Register 1	C1CTLR1	X000 00XXb[1]
0252h	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0b[1]
0253h			
0254h	CAN1 Acceptance Filter Support Register	C1AFS	0000 0000b[1]
0255h			0000 0001b[1]
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XXh
0261h	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XXh
0262h	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XXh
0263h	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XXh
0264h	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XXh
0265h	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XXh
0266h	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XXh
0267h	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XXh
0268h	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XXh
0269h	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XXh
026Ah	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XXh
026Bh	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XXh
026Ch	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XXh
026Dh	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XXh
026Eh	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XXh
026Fh	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XXh
0270h	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XXh
0271h	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XXh
0272h	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XXh
0273h	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XXh
0274h	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XXh
0275h	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XXh
0276h	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XXh
0277h	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XXh
0278h	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XXh
0279h	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XXh
027Ah	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XXh
027Bh	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XXh
027Ch	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XXh
027Dh	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XXh
027Eh	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XXh
027Fh	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XXh

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
2. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
3. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.12 SFR Address Map (12)

Address	Register[3][4]	Symbol	After Reset
0280h	CAN1 Control Register 0	C1CTLR0	XX01 0X01b[2]
0281h			XXXX 0000b[2]
0282h	CAN1 Status Register	C1STR	0000 0000b[2]
0283h			X000 0X01b[2]
0284h	CAN1 Extended ID Register	C1IDR	0000h[2]
0285h			
0286h	CAN1 Configuration Register	C1CONR	0000 XXXXb[2]
0287h			0000 0000b[2]
0288h	CAN1 Time Stamp Register	C1TSR	0000h[2]
0289h			
028Ah	CAN1 Transmit Error Count Register	C1TEC	00h[2]
028Bh	CAN1 Receive Error Count Register	C1REC	00h[2]
028Ch	CAN1 Slot Interrupt Status Register	C1SISTR	0000h[2]
028Dh			
028Eh			
028Fh			
0290h	CAN1 Slot Interrupt Mask Register	C1SIMKR	0000h[2]
0291h			
0292h			
0293h			
0294h	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X000b[2]
0295h	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X000b[2]
0296h	CAN1 Error Source Register	C1EFR	00h[2]
0297h	CAN1 Baud Rate Prescaler	C1BRP	0000 0001b[2]
0298h			
0299h	CAN1 Mode Register	C1MDR	XXXX XX00b[2]
029Ah			
029Bh			
029Ch			
029Dh			
029Eh			
029Fh			
02A0h	CAN1 Single Shot Control Register	C1SSCTLR	0000h[1][2]
02A1h			
02A2h			
02A3h			
02A4h	CAN1 Single Shot Status Register	C1SSSTR	0000h[1][2]
02A5h			
02A6h			
02A7h			
02A8h	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 0000b[1][2]
02A9h	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 0000b[1][2]
02AAh	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 0000b[1][2]
02ABh	CAN1 Global Mask Register Extended ID1	C1GMR3	00h[1][2]
02ACh	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 0000b[1][2]
02ADh			
02AEh			
02AFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The BANKSEL bit in the C0CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.13 SFR Address Map (13)

Address	Register[3][4]	Symbol	After Reset
02B0h	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0 / C1LMAR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
02B1h	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1 / C1LMAR1	0000 0000b[1][2]/ XX00 0000b[1][2]
02B2h	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2 / C1LMAR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
02B3h	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3 / C1LMAR3	00h[1][2]/ 00h[1][2]
02B4h	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4 / C1LMAR4	0000 0000b[1][2]/ XX00 0000b[1][2]
02B5h	CAN1 Message Slot 5 Control Register	C1MCTL5	00h[1][2]
02B6h	CAN1 Message Slot 6 Control Register	C1MCTL6	00h[1][2]
02B7h	CAN1 Message Slot 7 Control Register	C1MCTL7	00h[1][2]
02B8h	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8 / C1LMBR0	0000 0000b[1][2]/ XXX0 0000b[1][2]
02B9h	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9 / C1LMBR1	0000 0000b[1][2]/ XX00 0000b[1][2]
02BAh	CAN1 Message Slot 10 Control Register / CAN1 Local Mask Register B Extended ID0	C1MCTL10 / C1LMBR2	0000 0000b[1][2]/ XXXX 0000b[1][2]
02BBh	CAN1 Message Slot 11 Control Register / CAN1 Local Mask Register B Extended ID1	C1MCTL11 / C1LMBR3	00h[1][2]/ 00h[1][2]
02BCh	CAN1 Message Slot 12 Control Register / CAN1 Local Mask Register B Extended ID2	C1MCTL12 / C1LMBR4	0000 0000b[1][2]/ XX00 0000b[1][2]
02BDh	CAN1 Message Slot 13 Control Register	C1MCTL13	00h[1][2]
02BEh	CAN1 Message Slot 14 Control Register	C1MCTL14	00h[1][2]
02BFh	CAN1 Message Slot 15 Control Register	C1MCTL15	00h[1][2]

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. The BANKSEL bit in the C1CTLR1 register can switch functions for addresses 02A0h to 02BFh.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to “1” (sleep mode exited) after reset and supplying a clock to the CAN module.
3. The CAN-associated registers (allocated in addresses 01E0h to 02BFh) cannot be used in M32C/87B. In M32C/87A, only CAN0-associated registers can be used.
4. Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.

Table 4.14 SFR Address Map (14)

Address	Register	Symbol	After Reset
02C0h	X0 Register, Y0 Register	X0R, Y0R	XXXXh
02C1h			
02C2h	X1 Register, Y1 Register	X1R, Y1R	XXXXh
02C3h			
02C4h	X2 Register, Y2 Register	X2R, Y2R	XXXXh
02C5h			
02C6h	X3 Register, Y3 Register	X3R, Y3R	XXXXh
02C7h			
02C8h	X4 Register, Y4 Register	X4R, Y4R	XXXXh
02C9h			
02CAh	X5 Register, Y5 Register	X5R, Y5R	XXXXh
02CBh			
02CCh	X6 Register, Y6 Register	X6R, Y6R	XXXXh
02CDh			
02CEh	X7 Register, Y7 Register	X7R, Y7R	XXXXh
02CFh			
02D0h	X8 Register, Y8 Register	X8R, Y8R	XXXXh
02D1h			
02D2h	X9 Register, Y9 Register	X9R, Y9R	XXXXh
02D3h			
02D4h	X10 Register, Y10 Register	X10R, Y10R	XXXXh
02D5h			
02D6h	X11 Register, Y11 Register	X11R, Y11R	XXXXh
02D7h			
02D8h	X12 Register, Y12 Register	X12R, Y12R	XXXXh
02D9h			
02DAh	X13 Register, Y13 Register	X13R, Y13R	XXXXh
02DBh			
02DCh	X14 Register, Y14 Register	X14R, Y14R	XXXXh
02DDh			
02DEh	X15 Register, Y15 Register	X15R, Y15R	XXXXh
02DFh			
02E0h	X/Y Control Register	XYC	XXXX XX00b
02E1h			
02E2h			
02E3h			
02E4h	UART1 Special Mode Register 4	U1SMR4	00h
02E5h	UART1 Special Mode Register 3	U1SMR3	00h
02E6h	UART1 Special Mode Register 2	U1SMR2	00h
02E7h	UART1 Special Mode Register	U1SMR	00h
02E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
02E9h	UART1 Baud Rate Register	U1BRG	XXh
02EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
02EBh			
02ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
02EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
02EEh	UART1 Receive Buffer Register	U1RB	XXXXh
02EFh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.15 SFR Address Map (15)

Address	Register	Symbol	After Reset
02F0h			
02F1h			
02F2h			
02F3h			
02F4h	UART4 Special Mode Register 4	U4SMR4	00h
02F5h	UART4 Special Mode Register 3	U4SMR3	00h
02F6h	UART4 Special Mode Register 2	U4SMR2	00h
02F7h	UART4 Special Mode Register	U4SMR	00h
02F8h	UART4 Transmit/Receive Mode Register	U4MR	00h
02F9h	UART4 Baud Rate Register	U4BRG	XXh
02FAh	UART4 Transmit Buffer Register	U4TB	XXXXh
02FBh			
02FCh	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
02FDh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
02FEh	UART4 Receive Buffer Register	U4RB	XXXXh
02FFh			
0300h	Timer B3, B4, B5 Count Start Register	TBSR	000X XXXXb
0301h			
0302h	Timer A11 Register	TA11	XXXXh
0303h			
0304h	Timer A21 Register	TA21	XXXXh
0305h			
0306h	Timer A41 Register	TA41	XXXXh
0307h			
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh			
030Fh			
0310h	Timer B3 Register	TB3	XXXXh
0311h			
0312h	Timer B4 Register	TB4	XXXXh
0313h			
0314h	Timer B5 Register	TB5	XXXXh
0315h			
0316h			
0317h			
0318h			
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh	External Interrupt Source Select Register 1(1)	IFSRA	00h
031Fh	External Interrupt Source Select Register	IFSR	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The IFSRA register is included in the 144-pin package only.

Table 4.16 SFR Address Map (16)

Address	Register	Symbol	After Reset
0320h			
0321h			
0322h			
0323h			
0324h	UART3 Special Mode Register 4	U3SMR4	00h
0325h	UART3 Special Mode Register 3	U3SMR3	00h
0326h	UART3 Special Mode Register 2	U3SMR2	00h
0327h	UART3 Special Mode Register	U3SMR	00h
0328h	UART3 Transmit/Receive Mode Register	U3MR	00h
0329h	UART3 Baud Rate Register	U3BRG	XXh
032Ah	UART3 Transmit Buffer Register	U3TB	XXXXh
032Bh			
032Ch	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
032Dh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
032Eh	UART3 Receive Buffer Register	U3RB	XXXXh
032Fh			
0330h			
0331h			
0332h			
0333h			
0334h	UART2 Special Mode Register 4	U2SMR4	00h
0335h	UART2 Special Mode Register 3	U2SMR3	00h
0336h	UART2 Special Mode Register 2	U2SMR2	00h
0337h	UART2 Special Mode Register	U2SMR	00h
0338h	UART2 Transmit/Receive Mode Register	U2MR	00h
0339h	UART2 Baud Rate Register	U2BRG	XXh
033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
033Bh			
033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
033Fh			
0340h	Count Start Register	TABSR	00h
0341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
0342h	One-Shot Start Register	ONSF	00h
0343h	Trigger Select Register	TRGSR	00h
0344h	Up/Down Select Register	UDF	00h
0345h			
0346h	Timer A0 Register	TA0	XXXXh
0347h			
0348h	Timer A1 Register	TA1	XXXXh
0349h			
034Ah	Timer A2 Register	TA2	XXXXh
034Bh			
044Ch	Timer A3 Register	TA3	XXXXh
034Dh			
034Eh	Timer A4 Register	TA4	XXXXh
034Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.17 SFR Address Map (17)

Address	Register	Symbol	After Reset
0350h	Timer B0 Register	TB0	XXXXh
0351h			
0352h	Timer B1 Register	TB1	XXXXh
0353h			
0354h	Timer B2 Register	TB2	XXXXh
0355h			
0356h	Timer A0 Mode Register	TA0MR	00h
0357h	Timer A1 Mode Register	TA1MR	00h
0358h	Timer A2 Mode Register	TA2MR	00h
0359h	Timer A3 Mode Register	TA3MR	00h
035Ah	Timer A4 Mode Register	TA4MR	00h
035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
035Fh	Count Source Prescaler Register(1)	TCSPR	0XXX 0000b
0360h			
0361h			
0362h			
0363h			
0364h	UART0 Special Mode Register 4	U0SMR4	00h
0365h	UART0 Special Mode Register 3	U0SMR3	00h
0366h	UART0 Special Mode Register 2	U0SMR2	00h
0367h	UART0 Special Mode Register	U0SMR	00h
0368h	UART0 Transmit/Receive Mode Register	U0MR	00h
0369h	UART0 Baud Rate Register	U0BRG	XXh
036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
036Bh			
036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
036Fh			
0370h			
0371h			
0372h	IrDA Control Register	IRCON	X000 0000b
0373h			
0374h			
0375h			
0376h			
0377h			
0378h	DMA0 Request Source Select Register	DM0SL	0X00 0000b
0379h	DMA1 Request Source Select Register	DM1SL	0X00 0000b
037Ah	DMA2 Request Source Select Register	DM2SL	0X00 0000b
037Bh	DMA3 Request Source Select Register	DM3SL	0X00 0000b
037Ch	CRC Data Register	CRCD	XXXXh
037Dh			
037Eh	CRC Input Register	CRCIN	XXh
037Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTE:
1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Table 4.18 SFR Address Map (18)

Address	Register	Symbol	After Reset
0380h	A/D0 Register 0	AD00	00XXh
0381h			
0382h	A/D0 Register 1	AD01	00XXh
0383h			
0384h	A/D0 Register 2	AD02	00XXh
0385h			
0386h	A/D0 Register 3	AD03	00XXh
0387h			
0388h	A/D0 Register 4	AD04	00XXh
0389h			
038Ah	A/D0 Register 5	AD05	00XXh
038Bh			
038Ch	A/D0 Register 6	AD06	00XXh
038Dh			
038Eh	A/D0 Register 7	AD07	00XXh
038Fh			
0390h			
0391h			
0392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
0393h			
0394h	A/D0 Control Register 2	AD0CON2	XX0X X000b
0395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
0396h	A/D0 Control Register 0	AD0CON0	00h
0397h	A/D0 Control Register 1	AD0CON1	00h
0398h	D/A Register 0	DA0	XXh
0399h			
039Ah	D/A Register 1	DA1	XXh
039Bh			
039Ch	D/A Control Register	DACON	XXXX XX00b
039Dh	D/A Control Register 1	DACON1	XXXX 0000b
039Eh			
039Fh			

X: Undefined
Blank spaces are all reserved. No access is allowed.

Table 4.19 SFR Address Map (19)

Address	Register	Address	Register
03A0h	Function Select Register A8(1)	PS8	X000 0000b
03A1h	Function Select Register A9(1)	PS9	00h
03A2h			
03A3h	Function Select Register B9(1)	PSL9	XXX0 XX00b
03A4h	Function Select Register E2	PSE2	XXXX XX0Xb
03A5h			
03A6h			
03A7h	Function Select Register D1	PSD1	00X0 XX00b
03A8h	Function Select Register D2	PSD2	XXXX XX0Xb
03A9h			
03AAh	Function Select Register C6(1)	PSC6	XXXX 0X00b
03ABh	Function Select Register E1	PSE1	00XX XX00b
03ACh	Function Select Register C2	PSC2	XXXX X00Xb
03ADh	Function Select Register C3	PSC3	X0XX XXXXb
03AEh			
03AFh	Function Select Register C	PSC	00h
03B0h	Function Select Register A0	PS0	00h
03B1h	Function Select Register A1	PS1	00h
03B2h	Function Select Register B0	PSL0	00h
03B3h	Function Select Register B1	PSL1	00h
03B4h	Function Select Register A2	PS2	00X0 0000b
03B5h	Function Select Register A3	PS3	00h
03B6h	Function Select Register B2	PSL2	00X0 0000b
03B7h	Function Select Register B3	PSL3	00h
03B8h	Function Select Register A4	PS4	00h
03B9h	Function Select Register A5(1)	PS5	XXX0 0000b
03BAh			
03BBh	Function Select Register B5(1)	PSL5	XXX0 0000b
03BCh	Function Select Register A6(1)	PS6	00h
03BDh	Function Select Register A7(1)	PS7	00h
03BEh	Function Select Register B6(1)	PSL6	00h
03BFh	Function Select Register B7(1)	PSL7	00h
03C0h	Port P6 Register	P6	XXh
03C1h	Port P7 Register	P7	XXh
03C2h	Port P6 Direction Register	PD6	00h
03C3h	Port P7 Direction Register	PD7	00h
03C4h	Port P8 Register	P8	XXh
03C5h	Port P9 Register	P9	XXh
03C6h	Port P8 Direction Register	PD8	00X0 0000b
03C7h	Port P9 Direction Register	PD9	00h
03C8h	Port P10 Register	P10	XXh
03C9h	Port P11 Register(1)	P11	XXh
03CAh	Port P10 Direction Register	PD10	00h
03CBh	Port P11 Direction Register(1)(2)	PD11	XXX0 0000b
03CCh	Port P12 Register(1)	P12	XXh
03CDh	Port P13 Register(1)	P13	XXh
03CEh	Port P12 Direction Register(1)(2)	PD12	00h
03CFh	Port P13 Direction Register(1)(2)	PD13	00h

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.

Table 4.20 SFR Address Map (20)

Address	Register	Address	Register
03D0h	Port P14 Register(1)	P14	XXh
03D1h	Port P15 Register(1)	P15	XXh
03D2h	Port P14 Direction Register(1)(2)	PD14	X000 0000b
03D3h	Port P15 Direction Register(1)(2)	PD15	00h
03D4h			
03D5h			
03D6h			
03D7h			
03D8h			
03D9h			
03DAh	Pull-Up Control Register 2	PUR2	00h
03DBh	Pull-Up Control Register 3	PUR3	00h
03DCh	Pull-Up Control Register 4(1)(3)	PUR4	XXXX 0000b
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh			
03EDh			
03EEh			
03EFh			
03F0h	Pull-Up Control Register 0	PUR0	00h
03F1h	Pull-Up Control Register 1	PUR1	XXXX 0000b
03F2h			
03F3h			
03F4h			
03F5h			
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blank spaces are all reserved. No access is allowed.
NOTES:
1. These registers cannot be used in the 100-pin package.
2. Set to FFh in the 100-pin package.
3. Set to 00h in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
VCC1, VCC2	Supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VCC2	Supply voltage		–	-0.3 to VCC1 + 0.1	V
AVCC	Analog supply voltage		VCC1 = AVCC	-0.3 to 6.0	V
VI	Input voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1), VREF, XIN		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
VO	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P14_0 to 14_6, P15_0 to P15_7(1), XOUT		-0.3 to VCC1 + 0.3	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)		-0.3 to VCC2 + 0.3	
		P7_0, P7_1		-0.3 to 6.0	
Pd	Power consumption		-40°C≤Topr≤85°C	500	mW
Topr	Operating ambient temperature	during CPU operation		-20 to 85/ -40 to 85(2)	°C
		during programming or erasing Flash memory		0 to 60	°C
Tstg	Storage temperature			-65 to 150	°C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact a Renesas sales office if temperature range of -40 to 85°C is required.

Table 5.2 Recommended Operating Conditions (1)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
VCC1, VCC2	Supply voltage (VCC1 ≥ VCC2)		3.0	5.0	5.5	V
AVCC	Analog supply voltage			VCC1		V
VSS	Supply voltage			0		V
AVSS	Analog supply voltage			0		V
VIH	Input high “H” voltage	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(2)	0.8VCC2		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7(1), P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(2), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0.8VCC1		VCC1	
		P7_0, P7_1	0.8VCC1		6.0	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0.8VCC2		VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0.5VCC2		VCC2	
VIL	Input low “L” voltage	P2_0 to P2_7,P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(2)	0		0.2VCC2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7(1), P9_0 to P9_7, P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(2), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	0		0.2VCC1	
		P0_0 to P0_7, P1_0 to P1_7 (in single-chip mode)	0		0.2VCC2	
		P0_0 to P0_7, P1_0 to P1_7 (in memory expansion mode and microprocessor mode)	0		0.16VCC2	

NOTES:
1. VIH and VIL reference for P8_7 apply when P8_7 is used as a programmable input port. It does not apply when P8_7 is used as XCIN.
2. P11 to P15 are provided in the 144-pin package only.

Table 5.3 Recommended Operating Conditions (2)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
IOH(peak)	Peak output high "H" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-10.0	mA
IOH(avg)	Average output high "H" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			-5.0	mA
IOL(peak)	Peak output low "L" current(2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			10.0	mA
IOL(avg)	Average output low "L" current(1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(3)			5.0	mA

NOTES:
1. Average output current is the average value within 100 ms.
2. A total IOL(peak) of P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14, and P15 must be 80 mA or less.
   A total IOL(peak) of P3, P4, P5, P6, P7,P8_0 to P8_4, P12, and P13 must be 80 mA or less.
   A total IOH(peak) of P0, P1, P2, and P11 must be -40 mA or less.
   A total IOH(peak) of P8_6 to P8_7, P9, P10, P14, and P15 must be -40 mA or less.
   A total IOH(peak) of P3, P4, P5, P12, and P13 must be -40 mA or less.
   A total IOH(peak) of P6, P7, and P8_0 to P8_4 must be -40 mA or less.
3. P11 to P15 are provided in the 144-pin package only.

Table 5.4 Recommended Operating Conditions (3)
(VCC1 = VCC2 = 3.0 to 5.5 V, Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(CPU)	CPU clock frequency (same frequency as f(BCLK))	VCC1 = 4.2 to 5.5V	0		32	MHz
		VCC1 = 3.0 to 5.5V	0		24	MHz
f(XIN)	Main clock input oscillation frequency	VCC1 = 4.2 to 5.5V	0		32	MHz
		VCC1 = 3.0 to 5.5V	0		24	MHz
f(XCIN)	Sub clock frequency			32.768	50	kHz
f(Ring)	On-chip oscillator frequency			1		MHz
f(VCO)	VCO clock frequency (PLL frequency synthesizer)		20		80	MHz
f(PLL)	PLL clock frequency	VCC1 = 4.2 to 5.5V	10		32	MHz
		VCC1 = 3.0 to 5.5V	10		24	MHz
tsu(PLL)	Wait time to stabilize PLL frequency synthesizer	VCC1 = 5.0V			5	ms
		VCC1 = 3.3V			10	ms

VCC1 = VCC2 = 5V

Table 5.5 Electrical Characteristics (1)
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high “H” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -5 mA	VCC2 - 2.0		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOH = -5 mA	VCC1 - 2.0		VCC1	
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7 P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -200 µA	VCC2 - 0.3		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOH = -200 µA	VCC1 - 0.3		VCC1	
		XOUT	IOH = -1 mA	3.0		VCC1	V
		XCOUT — High drive capability	No load applied		2.5		V
		XCOUT — Low drive capability	No load applied		1.6		V
VOL	Output low “L” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 200 µA			0.45	V
		XOUT	IOL = 1 mA			2.0	V
		XCOUT — High drive capability	No load applied		0		V
		XCOUT — Low drive capability	No load applied		0		V
VT+ - VT-	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, $\overline{TB0IN}$ to $\overline{TB5IN}$, $\overline{INT0}$ to $\overline{INT8}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS6}$, CLK0 to $\overline{CLK6}$, TA0OUT to TA4OUT, $\overline{NMI}$, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, $\overline{ISRXD0}$ to $\overline{ISRXD2}$, IEIN, CAN0IN, CAN1IN, $\overline{CAN1WU}$		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V

NOTE:
1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.6 Electrical Characteristics (2)
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
IIH	Input high "H" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 5 V			5.0	µA
IIL	Input low "L" current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 0V			-5.0	µA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	VI = 0V	30	50	167	kΩ
RfXIN	Feedback resistance	XIN			1.5		MΩ
RfXCIN	Feedback resistance	XCIN			10		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:
1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Table 5.7 Electrical Characteristics (3)
(VCC1 = VCC2 = 5.5 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 32 MHz		32	45	mA
			f(CPU) = 16 MHz		19		mA
			f(CPU) = 8 MHz		12		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		50		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 5V

Table 5.8 A/D Conversion Characteristics
(VCC1 = VCC2 = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
–	Resolution	VREF = VCC1				10	Bits
INL	Integral nonlinearity error	VREF = VCC1 = VCC2 = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential nonlinearity error					±1	LSB
–	Offset error					±3	LSB
–	Gain error					±3	LSB
RLADDER	Resistor ladder	VREF = VCC1		8		40	kΩ
tCONV	10-bit conversion time(1)(2)			2.06			µs
tCONV	8-bit conversion time(1)(2)			1.75			µs
tSAMP	Sampling time(1)			0.188			µs
VREF	Reference voltage			2		VCC1	V
VIA	Analog input voltage			0		VREF	V

NOTES:
1. The value is obtained when ϕAD frequency is at 16 MHz. Keep ϕAD frequency at 16 MHz or lower.
2. With using the sample and hold function

Table 5.9 D/A Conversion Characteristics
(VCC1 = VCC2 = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.5	mA

NOTE:
1. Measured when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if the VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

VCC1 = VCC2 = 5V

Table 5.10 Flash Memory Electrical Characteristics (VCC1 = 4.5 V to 5.5 V, 3.0 to 3.6 V, Topr = 0 to 60°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Erase and program endurance(1)		100			times
–	Word program time (16 bits) (VCC1 = 5.0 V, Topr = 25°C)			25	300	µs
–	Lock bit program time			25	300	µs
–	Block erase time (VCC1 = 5.0 V, Topr = 25°C)	4-Kbyte block		0.3	4	s
		8-Kbyte block		0.3	4	s
		32-Kbyte block		0.5	4	s
		64-Kbyte block		0.8	4	s
tps	Wait time to stabilize flash memory circuit				15	µs
–	Data hold time (Topr = -40 to 85°C)		10			years

NOTE:
1. If erase and program endurance is n times (n = 100), each block can be erased n times. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one erase and program time. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited)

VCC1 = VCC2 = 5V

Table 5.11 Voltage Detection Circuit Electrical Characteristics (VCC1 = VCC2 = 3.0 to 5.5 V, VSS = 0 V, Topr = 25°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Vdet4 detection voltage	VCC1 = 3.0 V to 5.5 V	3.3	3.8	4.4	V
Vdet3	Vdet3 detection voltage			3.0		V
Vdet3s	Hardware reset 2 hold voltage				2.0	V
Vdet3r	Hardware reset 2 release voltage			3.1		V

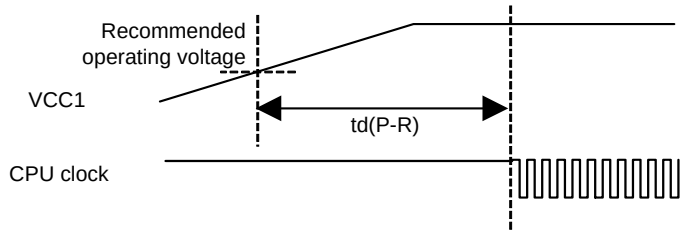
NOTES:
1. Vdet4 > Vdet3
2. Vdet3r > Vdet3 is not guaranteed.

Table 5.12 Power Supply Circuit Timing Characteristics

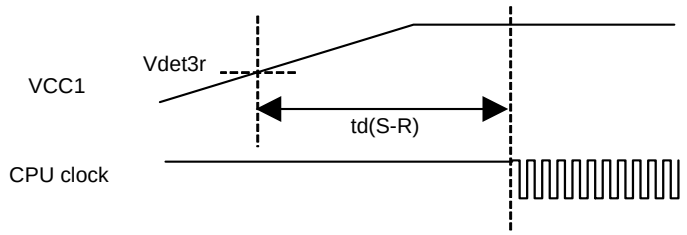
Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait time to stabilize internal supply voltage when power-on	VCC1 = 3.0 to 5.5 V			2	ms
td(S-R)	Wait time to release hardware reset 2	VCC1 = Vdet3r to 5.5 V		6(1)	20	ms
td(E-A)	Start-up time for Vdet3 and Vdet4 detection circuit	VCC1 = 3.0 to 5.5 V			20	µs

NOTE:
1. When VCC1 = 5 V

td(P-R)
Wait time to stabilize internal supply voltage when power-on



td(S-R)
Wait time to release hardware reset 2



td(E-A)
Start-up time for Vdet3 and Vdet4 detection circuit

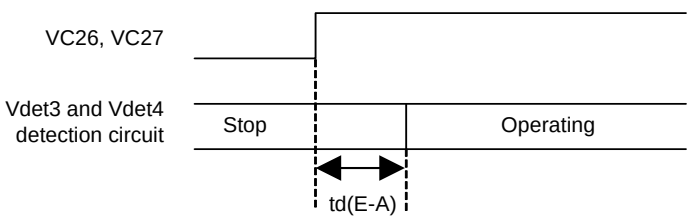


Figure 5.1 Power Supply Timing Diagram

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.13 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	31.25		ns
tw(H)	External clock input high (“H”) pulse width	13.75		ns
tw(L)	External clock input low (“L”) pulse width	13.75		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.14 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.15 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.16 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.17 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.18 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.19 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	800		ns
tsu(TAIN-TAOUT)	TAiOUT input setup time	200		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	200		ns

i = 0 to 4

Table 5.20 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.21 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.22 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.23 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.25 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.26 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.27 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

VCC1 = VCC2 = 5V

Timing Requirements
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Memory Expansion mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	26		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) + 1$)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = a + b$)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $p = \{(a + b - 1) \times 2\} + 1$)

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.29 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15\ [ns]$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10\ [ns]$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10\ [ns]$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $m = b$)

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15\ [ns]$$ (if external bus cycle is $a\phi + b\phi$, $n = (b \times 2) - 1$)

3. tc [ns] is added when recovery cycle is inserted.

VCC1 = VCC2 = 5V

Switching Characteristics
(VCC1 = VCC2 = 4.2 to 5.5 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.30 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space with multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(5)		(note 1)		ns
th(WR-AD)	Address output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(5)		(note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-5		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(note 3)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(note 4)		ns
tdz(RD-AD)	Address output float start time			8	ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(RD\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(RD\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

3. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(AD\text{-}ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

4. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$th(ALE\text{-}AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

5. tc [ns] is added when recovery cycle is inserted.

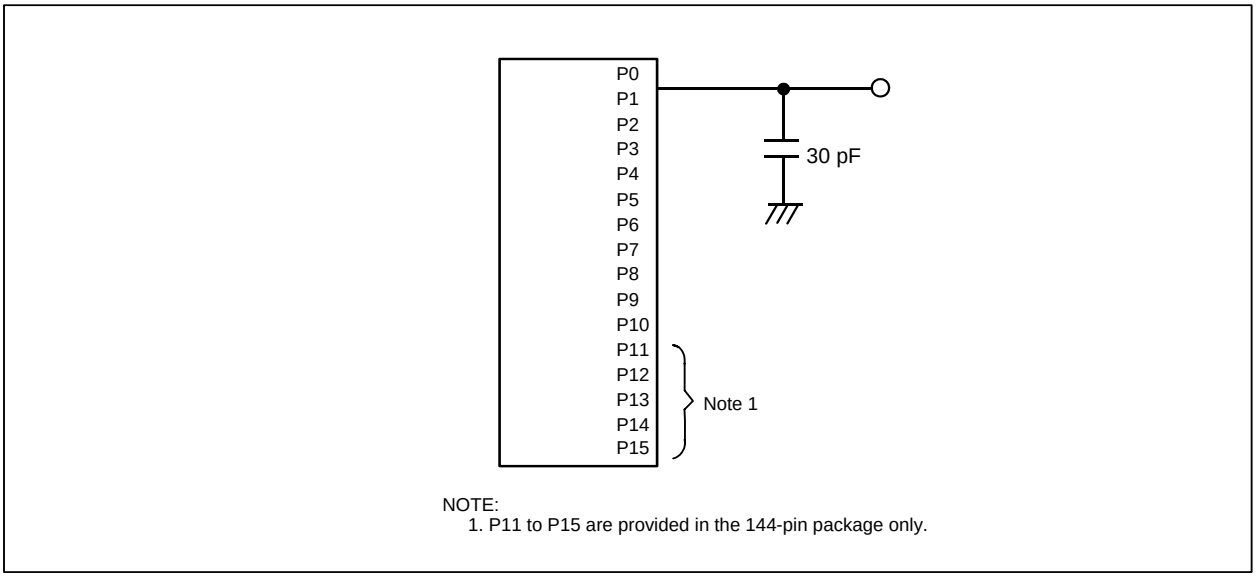


Figure 5.2 P0 to P15 Measurement Circuit

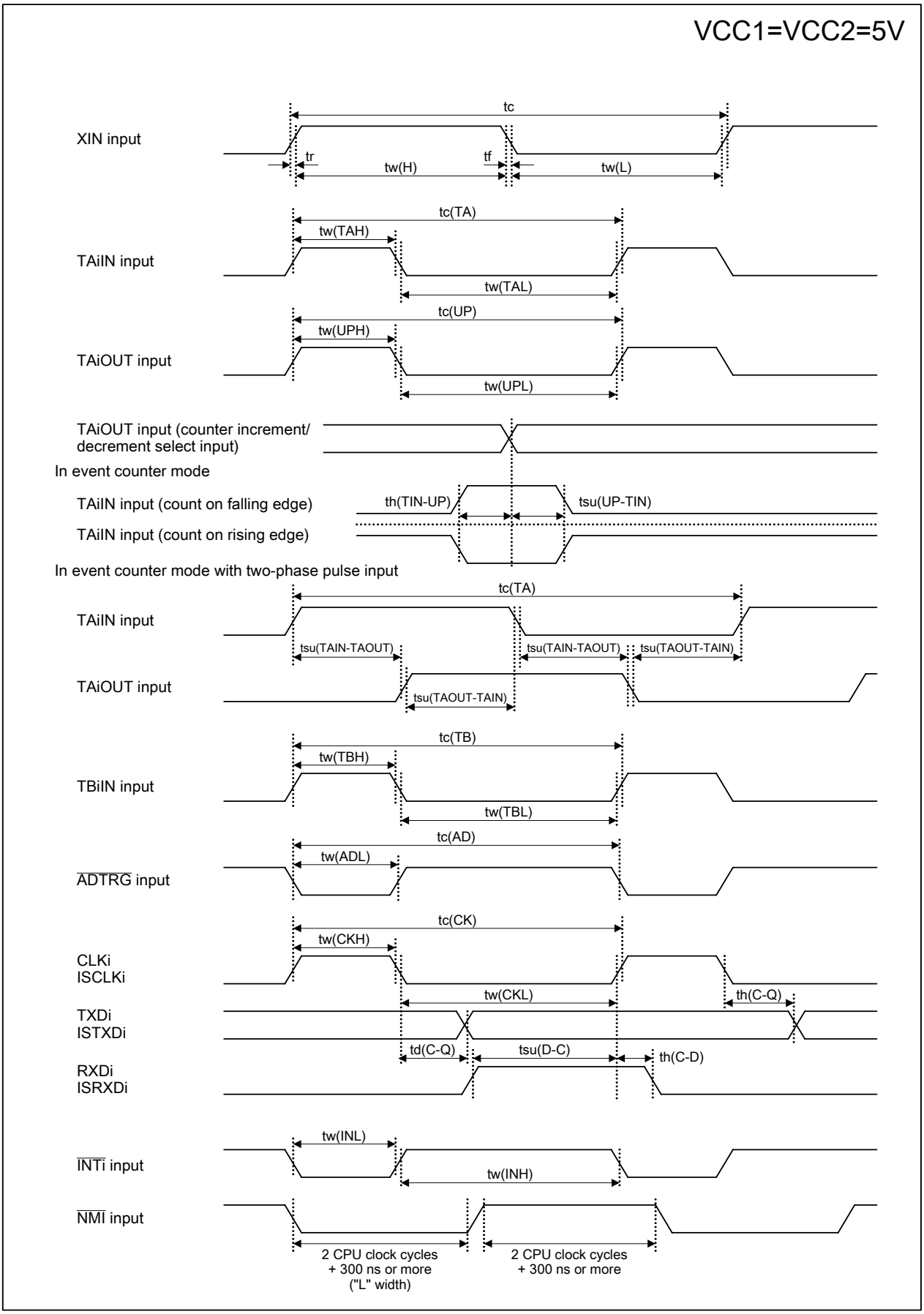


Figure 5.3 VCC1 = VCC2 = 5 V Timing Diagram (1)

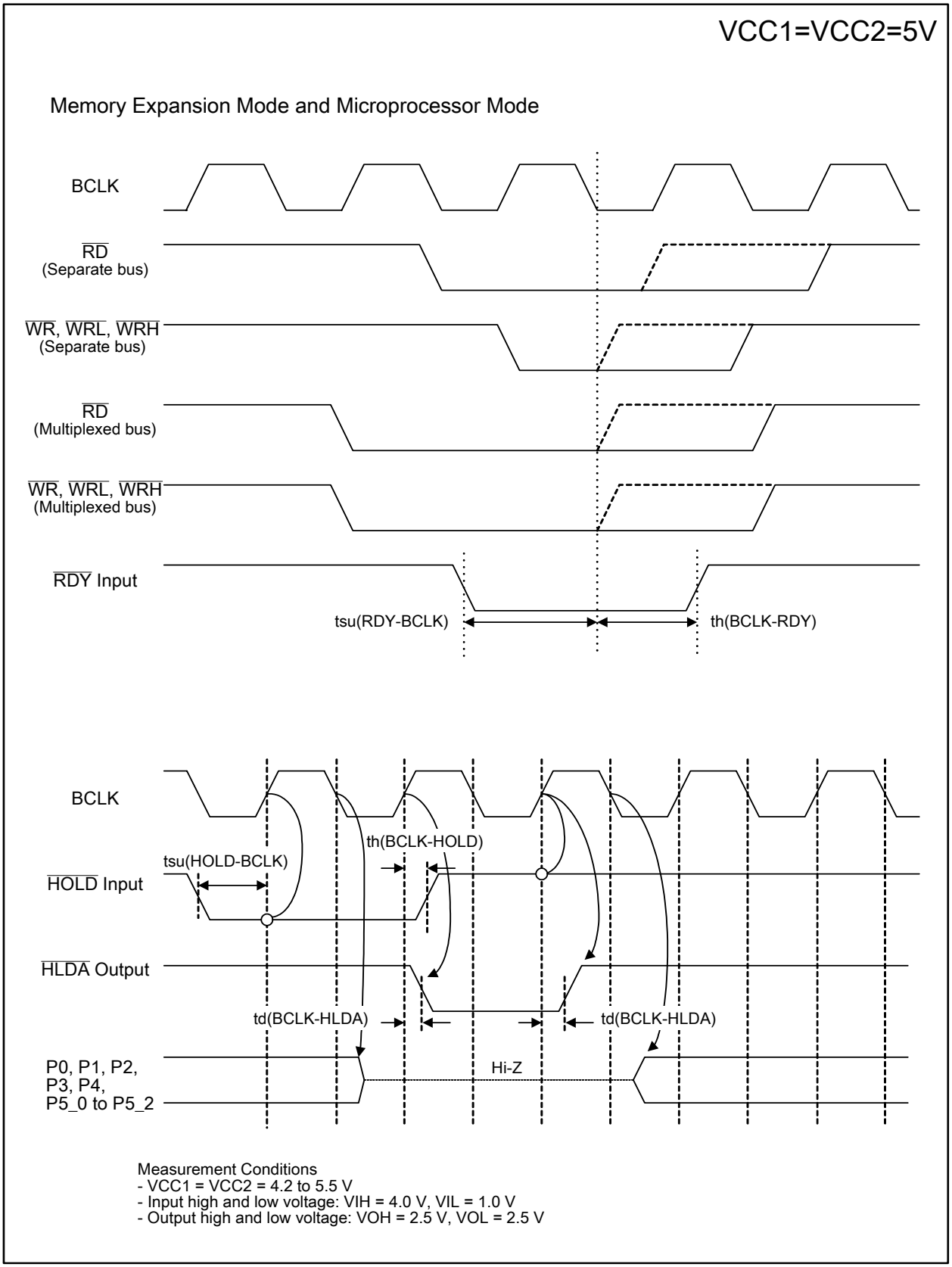
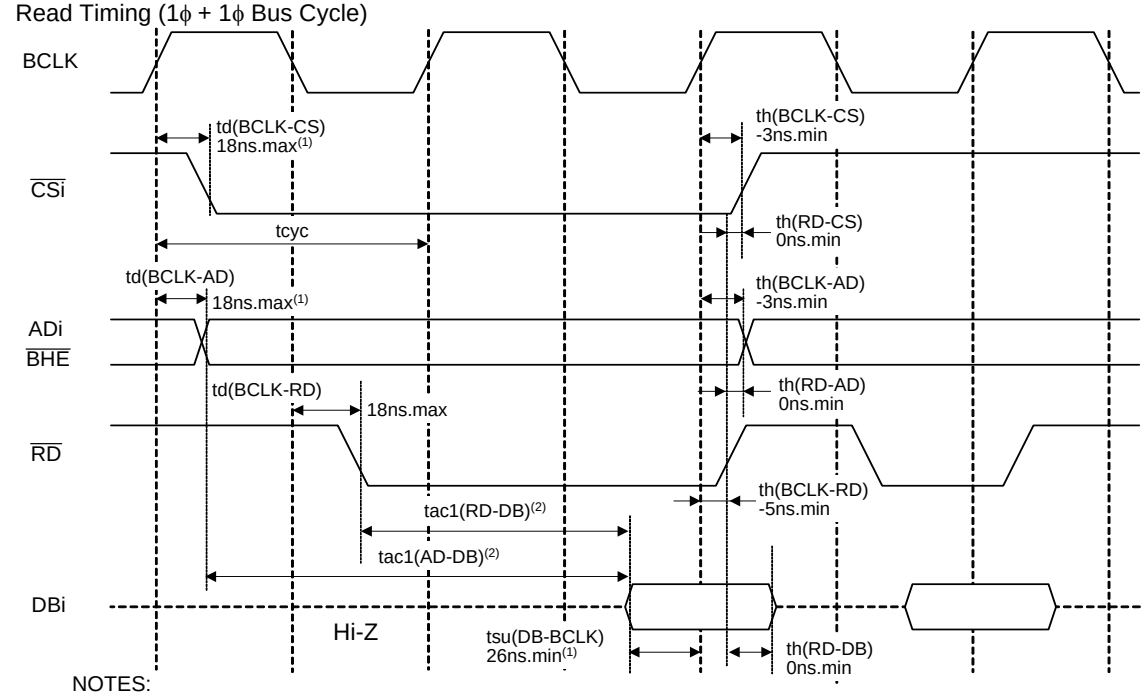


Figure 5.4 VCC1 = VCC2 = 5 V Timing Diagram (2)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

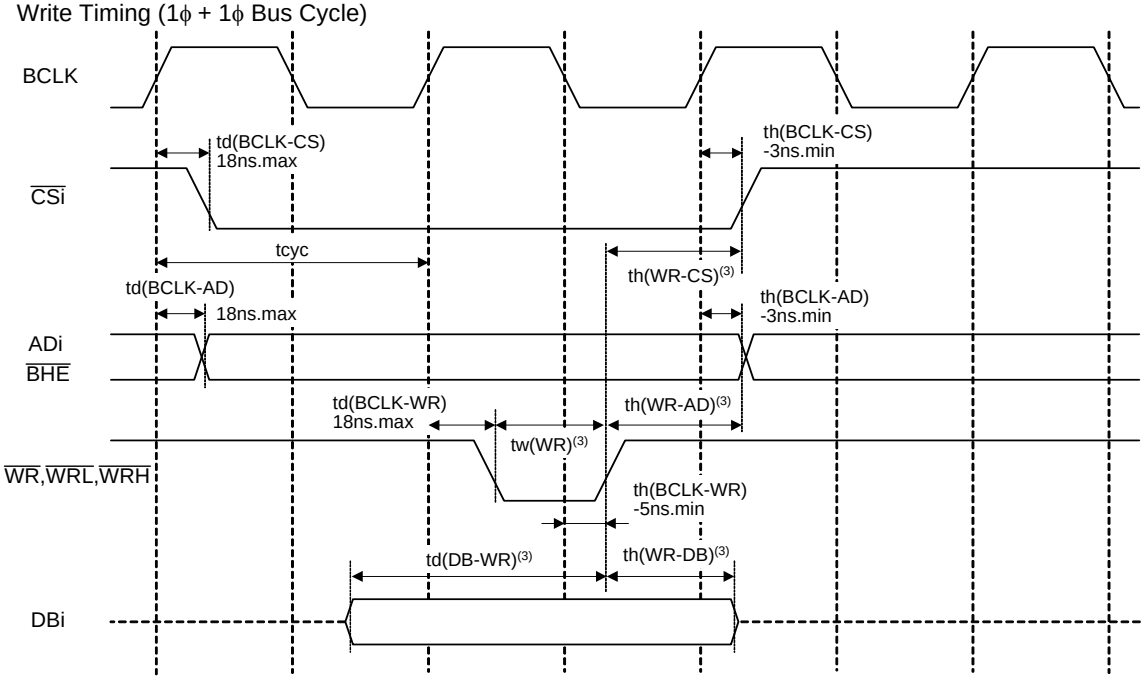
VCC1=VCC2=5V

Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 15) ns.min
   th(WR-AD) = (tcyc / 2 - 10) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

Measurement Conditions:
- VCC1 = VCC2 = 4.2 to 5.5 V
- Input high and low voltage: VIH = 2.5 V, VIL = 0.8 V
- Output high and low voltage: VOH = 2.0 V, VOL = 0.8 V

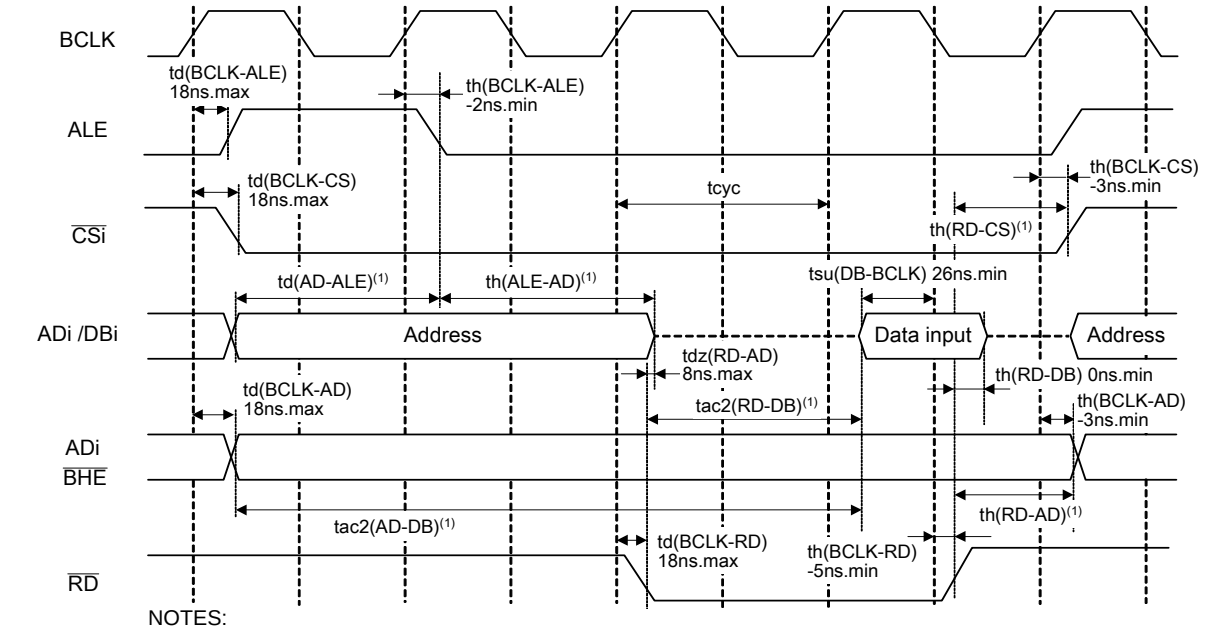
$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.5 VCC1 = VCC2 = 5 V Timing Diagram (3)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

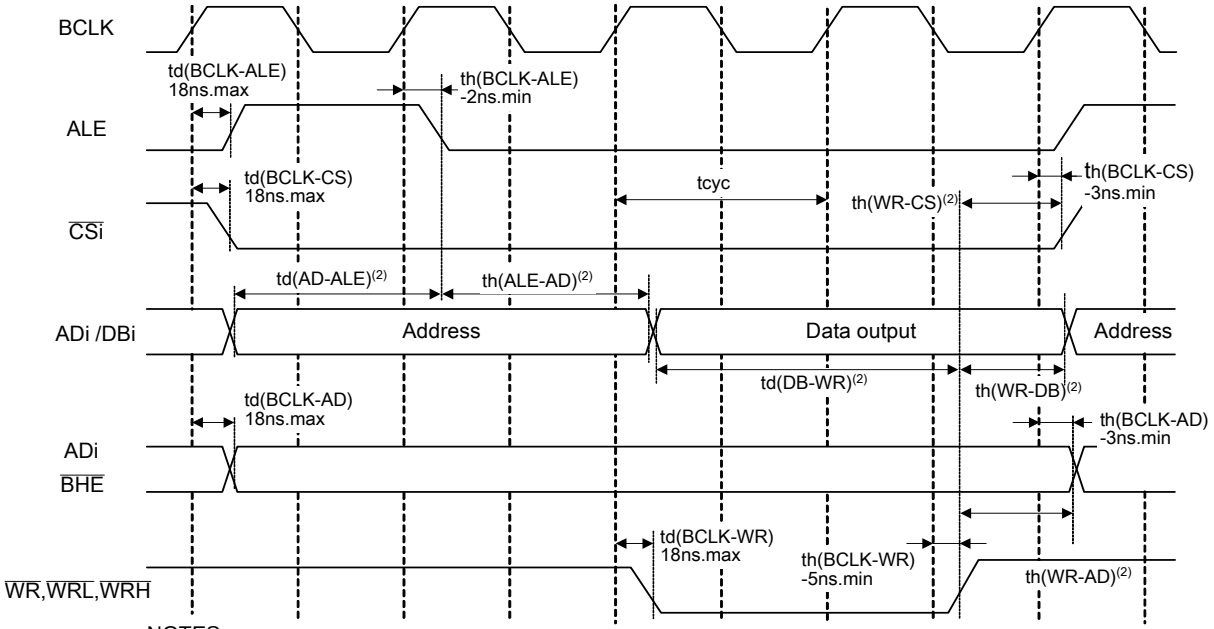
VCC1=VCC2=5V

Read Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(RD-AD) = (tcyc / 2 - 10) ns.min, th(RD-CS) = (tcyc / 2 - 10) ns.min
tac2(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)
tac2(AD-DB) = (tcyc / 2 x p - 35) ns.max (if external bus cycle aϕ + bϕ, p = {(a + b - 1) x 2} + 1)

Write Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(WR-AD) = (tcyc / 2 - 10) ns.min, th(WR-CS) = (tcyc / 2 - 10) ns.min
th(WR-DB) = (tcyc / 2 - 15) ns.min
td(DB-WR) = (tcyc / 2 x m - 25) ns.min (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)

$$tcyc = \frac{10^9}{f(BCLK)}$$

Measurement Conditions:
- VCC1 = VCC2 = 4.2 to 5.5 V
- Input high and low voltage VIH = 2.5 V, VIL = 0.8 V
- Output high and low voltage VOH = 2.0 V, VOL = 0.8 V

Figure 5.6 VCC1 = VCC2 = 5 V Timing Diagram (4)

VCC1 = VCC2 = 3.3 V

Table 5.31 Electrical Characteristics (1)

(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output high “H” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7(1)	IOH = -1 mA	VCC2 - 0.6		VCC2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P14_0 to P14_6, P15_0 to P15_7(1)		VCC1 - 0.6		VCC1	
		XOUT	IOH = -0.1 mA	2.7		VCC1	V
		XCOUT High drive capability	No load applied		2.5		V
		XCOUT Low drive capability	No load applied		1.6		V
VOL	Output low “L” voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	IOL = 1 mA			0.5	V
		XOUT	IOL = 0.1 mA			0.5	V
		XCOUT High drive capability	No load applied		0		V
		XCOUT Low drive capability	No load applied		0		V
VT+ - VT-	Hysteresis	$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, TA0IN to TA4IN, $\overline{\text{TB0IN}}$ to $\overline{\text{TB5IN}}$, $\overline{\text{INT0}}$ to $\overline{\text{INT8}}$, $\overline{\text{ADTRG}}$, $\overline{\text{CTS0}}$ to $\overline{\text{CTS6}}$, CLK0 to CLK6, TA0OUT to TA4OUT, $\overline{\text{NMI}}$, $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, RXD0 to RXD6, SCL0 to SCL4, SDA0 to SDA4, INPC1_0 to INPC1_7, ISCLK0 to ISCLK2, ISRXD0 to ISRXD2, IEIN, CAN0IN, CAN1IN, $\overline{\text{CAN1WU}}$		0.2		1.0	V
		$\overline{\text{RESET}}$		0.2		1.8	V

NOTE:

1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 3.3 V

Table 5.32 Electrical Characteristics (2)
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24 MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
IIH	Input high “H” current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 3 V			4.0	µA
IIL	Input low “L” current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1), XIN, $\overline{\text{RESET}}$, CNVSS, BYTE	VI = 0V			-4.0	µA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7,P10_0 to P10_7, P11_0 to P11_4, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_6, P15_0 to P15_7(1)	VI=0V	40	90	500	kΩ
RfXIN	Feedback resistance	XIN			3.0		MΩ
RfXCIN	Feedback resistance	XCIN			20.0		MΩ
VRAM	RAM data retention voltage	In stop mode		2.0			V

NOTE:
1. P11 to P15 are provided in the 144-pin package only.

VCC1 = VCC2 = 3.3 V

Table 5.33 Electrical Characteristics (3)
(VCC1 = VCC2 = 3.3 V, VSS = 0 V, Topr = 25°C)

Symbol	Parameter	Measurement Condition(1)		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current	Flash memory version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		2.6		mA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is operating		430		µA
			f(CPU) = 32 kHz In low-power consumption mode While flash memory is stopped(2)		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA
		Mask ROM version	f(CPU) = 24 MHz		23	33	mA
			f(CPU) = 16 MHz		17		mA
			f(CPU) = 8 MHz		11		mA
			f(CPU) = f(Ring) In on-chip oscillator low-power consumption mode		1		mA
			f(CPU) = 32 kHz In low-power consumption mode		30		µA
			Wait mode: f(CPU) = f(Ring) After entering wait mode from on-chip oscillator low-power consumption mode		45		µA
			Stop mode (while clock is stopped)		0.8	5	µA
			Stop mode (while clock is stopped) Topr = 85°C			50	µA

NOTES:
1. In single-chip mode, leave the output pins open and connect the input pins to VSS.
2. Value is obtained when setting the FMSTP bit in the FMR0 register to 1 (flash memory stopped) and running the program on RAM.

VCC1 = VCC2 = 3.3 V

Table 5.34 A/D Conversion Characteristics (VCC1 = VCC2 = AVCC = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution	VREF = VCC1			10	Bits
INL	Integral nonlinearity error (8-bit)	VREF = VCC1 = VCC2 = 3.3 V			±2	LSB
DNL	Differential nonlinearity error (8-bit)				±1	LSB
–	Offset error (8-bit)				±2	LSB
–	Gain error (8-bit)				±2	LSB
RLADDER	Resistor ladder	VREF = VCC1	8		40	kΩ
tCONV	8-bit conversion time(1)(2)		4.9			µs
VREF	Reference voltage		3		VCC1	V
VIA	Analog input voltage		0		VREF	V

NOTES:
1. The value when ϕAD frequency is at 10 MHz. Keep ϕAD frequency at 10 MHz or lower. If f(CPU) (=fAD) is 24 MHz, divide f(CPU) by 3 to make it 8 MHz. The conversion time in this case is 6.1 µs.
2. Sample and hold function is not available.

Table 5.35 D/A Conversion Characteristics (VCC1 = VCC2 = VREF = 3.0 to 3.6 V, VSS = AVSS = 0 V, Topr = -20 to 85°C, f(CPU) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(note 1)			1.0	mA

NOTE:
1. Measurement when one D/A converter is used, and the DAi register (i = 0, 1) of the unused D/A converter is set to 00h. The current flown into the resistor ladder in the A/D converter is excluded. IVREF flows even if VCUT bit in the AD0CON1 register is set to 0 (VREF not connected)

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.36 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External clock input cycle time	41		ns
tw(H)	External clock input high (“H”) pulse width	18		ns
tw(L)	External clock input low (“L”) pulse width	18		ns
tr	External clock rise time		5	ns
tf	External clock fall time		5	ns

Table 5.37 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	100		ns
tw(TAH)	TAiIN input high (“H”) pulse width	40		ns
tw(TAL)	TAiIN input low (“L”) pulse width	40		ns

i = 0 to 4

Table 5.38 Timer A Input (Gate Signal Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	400		ns
tw(TAH)	TAiIN input high (“H”) pulse width	200		ns
tw(TAL)	TAiIN input low (“L”) pulse width	200		ns

i = 0 to 4

Table 5.39 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	200		ns
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

Table 5.40 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high (“H”) pulse width	100		ns
tw(TAL)	TAiIN input low (“L”) pulse width	100		ns

i = 0 to 4

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.41 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high (“H”) pulse width	1000		ns
tw(UPL)	TAiOUT input low (“L”) pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

i = 0 to 4

Table 5.42 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAiIN input setup time	500		ns

i = 0 to 4

Table 5.43 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high (“H”) pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low (“L”) pulse width (counted on both edges)	80		ns

i = 0 to 5

Table 5.44 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

Table 5.45 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high (“H”) pulse width	200		ns
tw(TBL)	TBiIN input low (“L”) pulse width	200		ns

i = 0 to 5

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.46 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(AD)	$\overline{\text{ADTRG}}$ input cycle time (required for trigger)	1000		ns
tw(ADL)	$\overline{\text{ADTRG}}$ input low (“L”) pulse width	125		ns

Table 5.47 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input high (“H”) pulse width	100		ns
tw(CKL)	CLKi input low (“L”) pulse width	100		ns
td(C-Q)	TXDi output delay time		80	ns
th(C-Q)	TXDi output hold time	0		ns
tsu(D-C)	RXDi input setup time	70		ns
th(C-D)	RXDi input hold time	90		ns

i = 0 to 6

Table 5.48 Intelligent I/O Communication Function (Groups 0 and 1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLKi input cycle time	600		ns
tw(CKH)	ISCLKi input high (“H”) pulse width	300		ns
tw(CKL)	ISCLKi input low (“L”) pulse width	300		ns
td(C-Q)	ISTXDi output delay time		100	ns
th(C-Q)	ISTXDi output hold time	0		ns
tsu(D-C)	ISRXDi input setup time	100		ns
th(C-D)	ISRXDi input hold time	100		ns

i = 0, 1

Table 5.49 Intelligent I/O Communication Function (Group 2)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	ISCLK2 input cycle time	600		ns
tw(CKH)	ISCLK2 input high (“H”) pulse width	300		ns
tw(CKL)	ISCLK2 input low (“L”) pulse width	300		ns
td(C-Q)	ISTXD2 output delay time		180	ns
th(C-Q)	ISTXD2 output hold time	0		ns
tsu(D-C)	ISRXD2 input setup time	150		ns
th(C-D)	ISRXD2 input hold time	100		ns

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.50 External Interrupt $\overline{INTi}$ Input (Edge Sensitive)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INTi}$ input high (“H”) pulse width	250		ns
tw(INL)	$\overline{INTi}$ input low (“L”) pulse width	250		ns

i = 0 to 8(1)

NOTE:
1. $\overline{INT6}$ to $\overline{INT8}$ are provided in the 144-pin package only.

VCC1 = VCC2 = 3.3 V

Timing Requirements
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.51 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data input access time (RD standard)		(note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard)		(note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, when accessing a space with the multiplexed bus)		(note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	$\overline{\text{RDY}}$ input setup time	40		ns
tsu(HOLD-BCLK)	$\overline{\text{HOLD}}$ input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	$\overline{\text{RDY}}$ input hold time	0		ns
th(BCLK-HOLD)	$\overline{\text{HOLD}}$ input hold time	0		ns
td(BCLK-HLDA)	$\overline{\text{HLDA}}$ output delay time		25	ns

NOTE:
1. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations. Insert wait states or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$\text{tac1(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is aϕ + bϕ, m = (b × 2) + 1)

$$\text{tac1(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35\ [ns]$$ (if external bus cycle is aϕ + bϕ, n = a + b)

$$\text{tac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is aϕ + bϕ, m = (b × 2) - 1)

$$\text{tac2(AD-DB)} = \frac{10^9 \times p}{f(BCLK) \times 2} - 35\ [ns]$$ (if external bus cycle is aϕ + bϕ, p = {(a + b - 1) × 2} + 1)

VCC1 = VCC2 = 3.3 V

Switching Characteristics
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.52 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(3)		0		ns
th(WR-AD)	Address output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(3)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(3)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(3)		(note 1)		ns
tw(WR)	WR output width		(note 2)		ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 20\ [ns]$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 15\ [ns]$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10\ [ns]$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equations.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK)} - 20\ [ns]\ (\text{if external bus cycle is } a\phi + b\phi,\ m = b)$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15\ [ns]\ (\text{if external bus cycle is } a\phi + b\phi,\ n = (b \times 2) - 1)$$

3. tc [ns] is added when recovery cycle is inserted.

VCC1 = VCC2 = 3.3 V

Switching Characteristics
(VCC1 = VCC2 = 3.0 to 3.6 V, VSS = 0 V, Topr = -20 to 85°C unless otherwise specified)

Table 5.53 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space with multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address output delay time	See Figure 5.2		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)(5)		(note 1)		ns
th(WR-AD)	Address output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)(5)		(note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(note 2)		ns
th(WR-DB)	Data output hold time (WR standard)(5)		(note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(note 3)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(note 4)		ns
tdz(RD-AD)	Address output float start time			8	ns

NOTES:

1. Values, which depend on BCLK frequency, can be obtained from the following equations.

$$th(RD\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}AD) = \frac{10^9}{f(BCLK) \times 2} - 15 \text{ [ns]}$$

$$th(RD\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \text{ [ns]}$$

$$th(WR\text{-}DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \text{ [ns]}$$

2. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(DB\text{-}WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $m = (b \times 2) - 1$)

3. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$td(AD\text{-}ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

4. Values, which depend on BCLK frequency and external bus cycles, can be obtained from the following equation.

$$th(ALE\text{-}AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \text{ [ns]}$$ (if external bus cycle is $a\phi + b\phi$, $n = a$)

5. tc [ns] is added when recovery cycle is inserted.

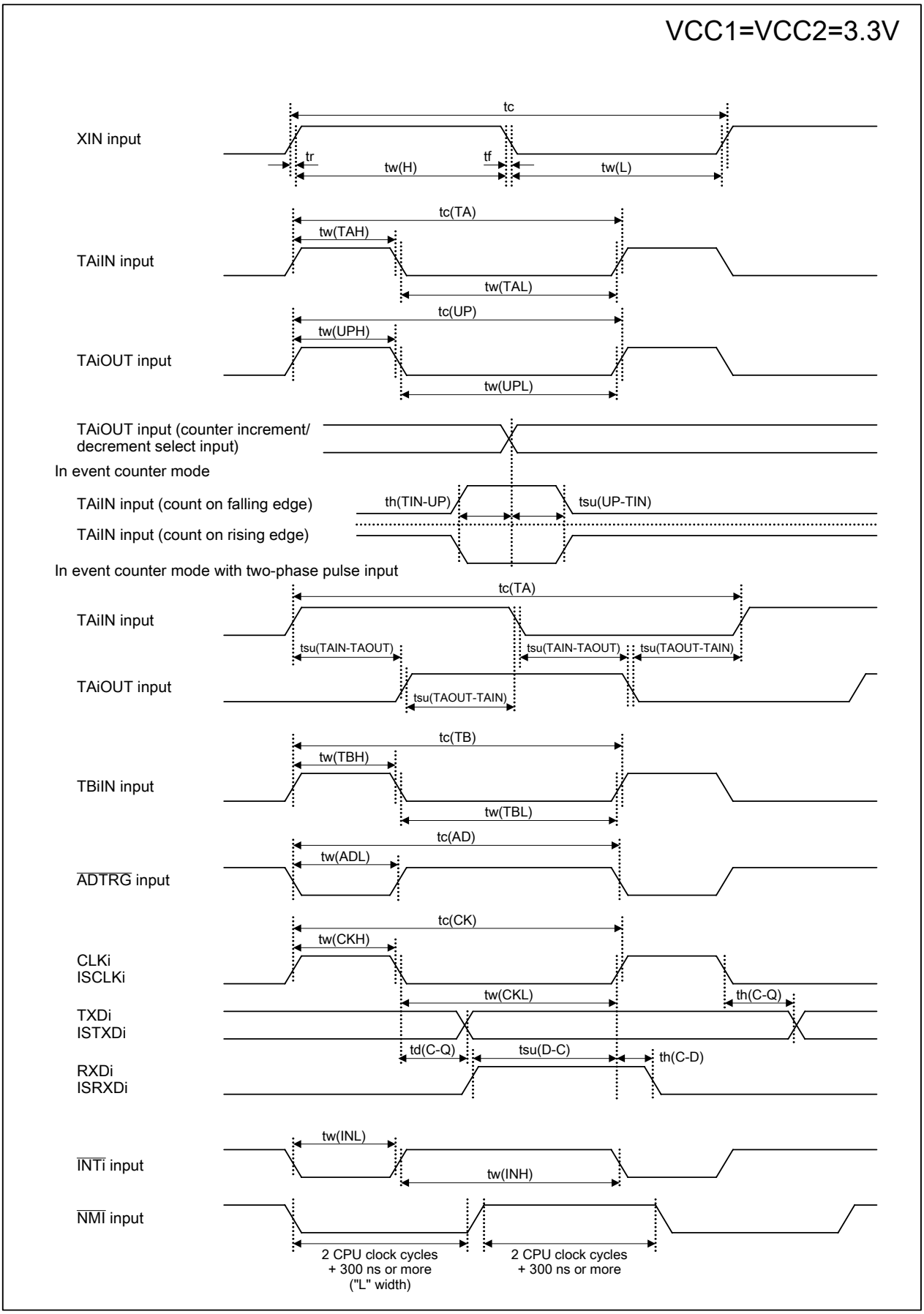


Figure 5.7 VCC1 = VCC2 = 3.3 V Timing Diagram (1)

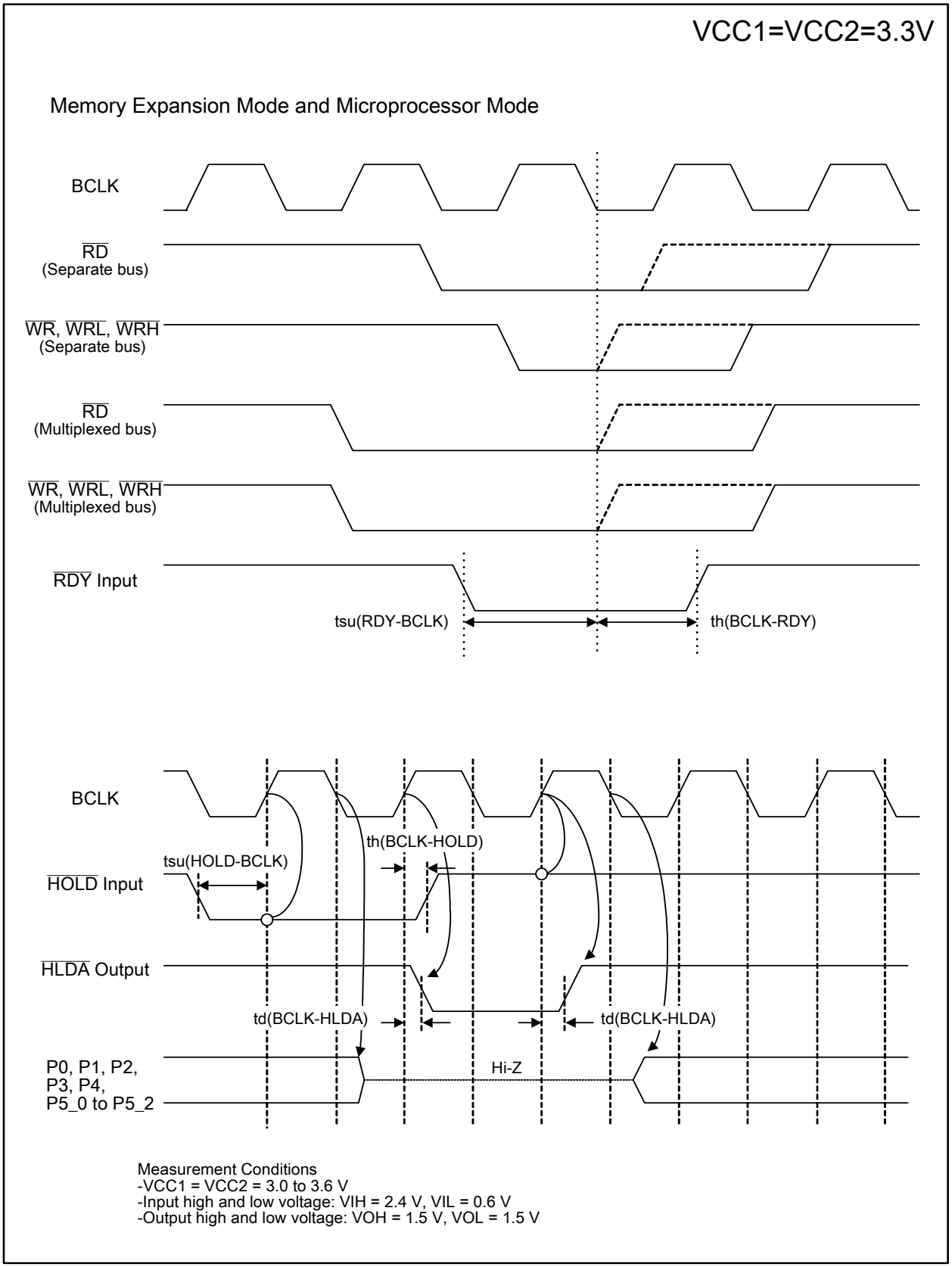
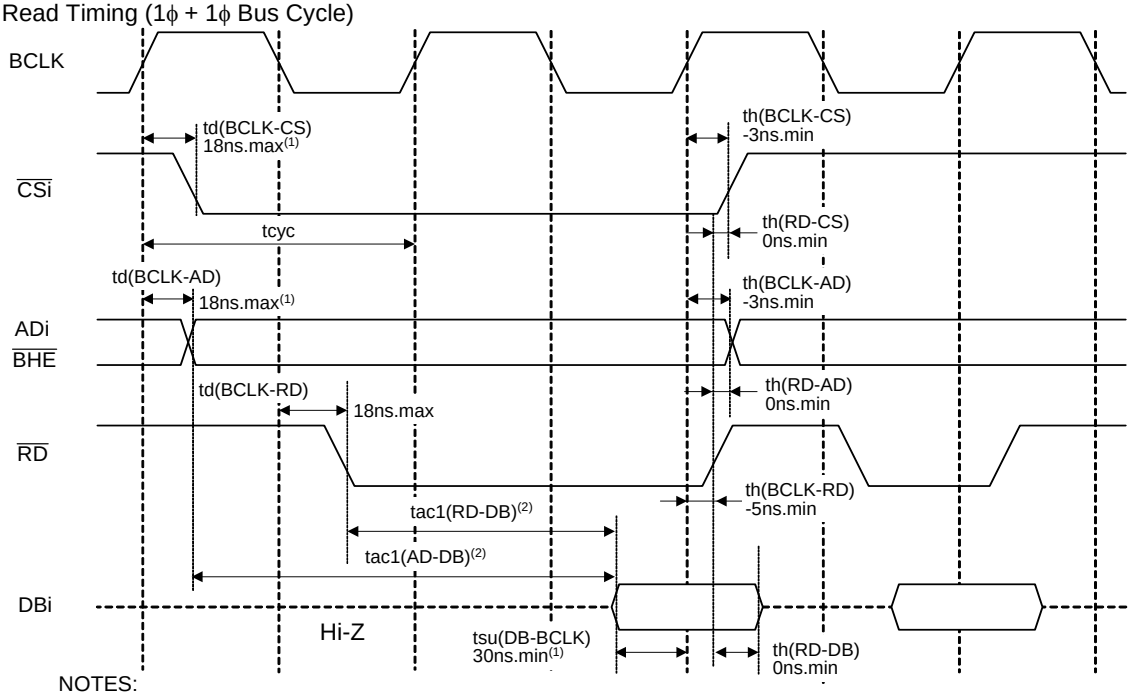


Figure 5.8 VCC1 = VCC2 = 3.3 V Timing Diagram (2)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space)

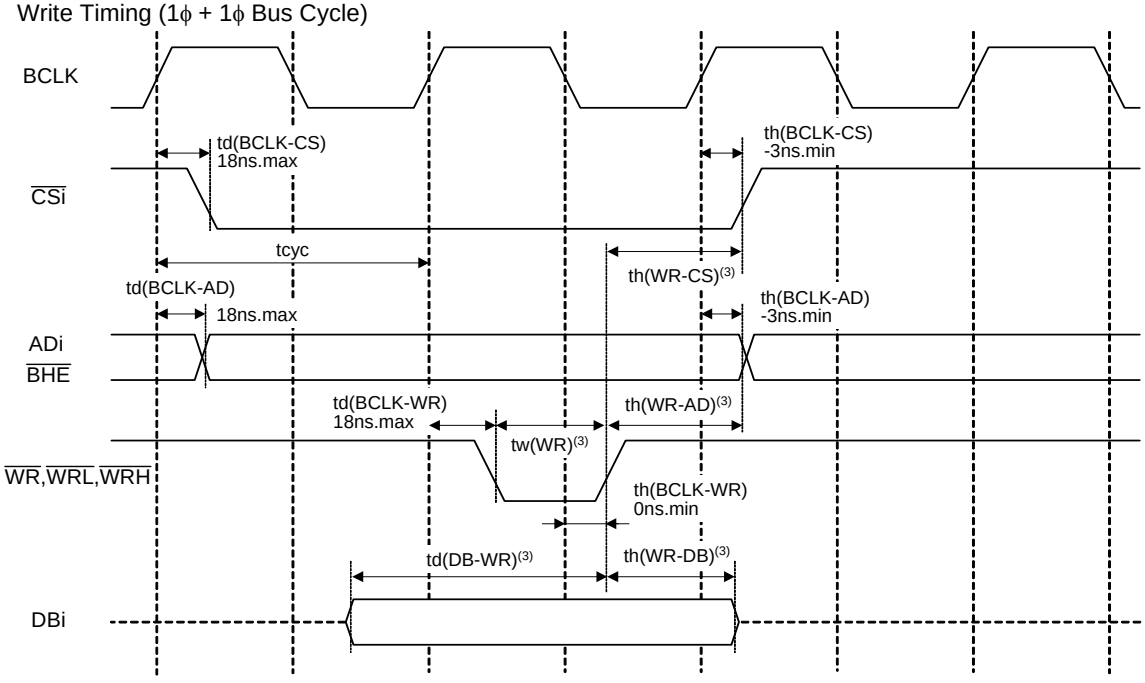
VCC1=VCC2=3.3V

Read Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
1. Values guaranteed only when the MCU is used stand-alone.
   A maximum of 35 ns is guaranteed for td(BCLK-AD) + tsu(DB-BCLK).
2. Varies with operation frequency:
   tac1(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) + 1)
   tac1(AD-DB) = (tcyc x n - 35) ns.max (if external bus cycle aϕ + bϕ, n = a + b)

Write Timing (1ϕ + 1ϕ Bus Cycle)



NOTES:
3. Varies with operation frequency:
   td(DB-WR) = (tcyc x m - 20) ns.min
   (if external bus cycle aϕ + bϕ, m = b)
   th(WR-DB) = (tcyc / 2 - 20) ns.min
   th(WR-AD) = (tcyc / 2 - 15) ns.min
   th(WR-CS) = (tcyc / 2 - 10) ns.min
   tw(WR) = (tcyc / 2 x n - 15) ns.min
   (if external bus cycle aϕ + bϕ, n = (b x 2) - 1)

Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage: VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage: VOH = 1.5 V, VOL = 1.5 V

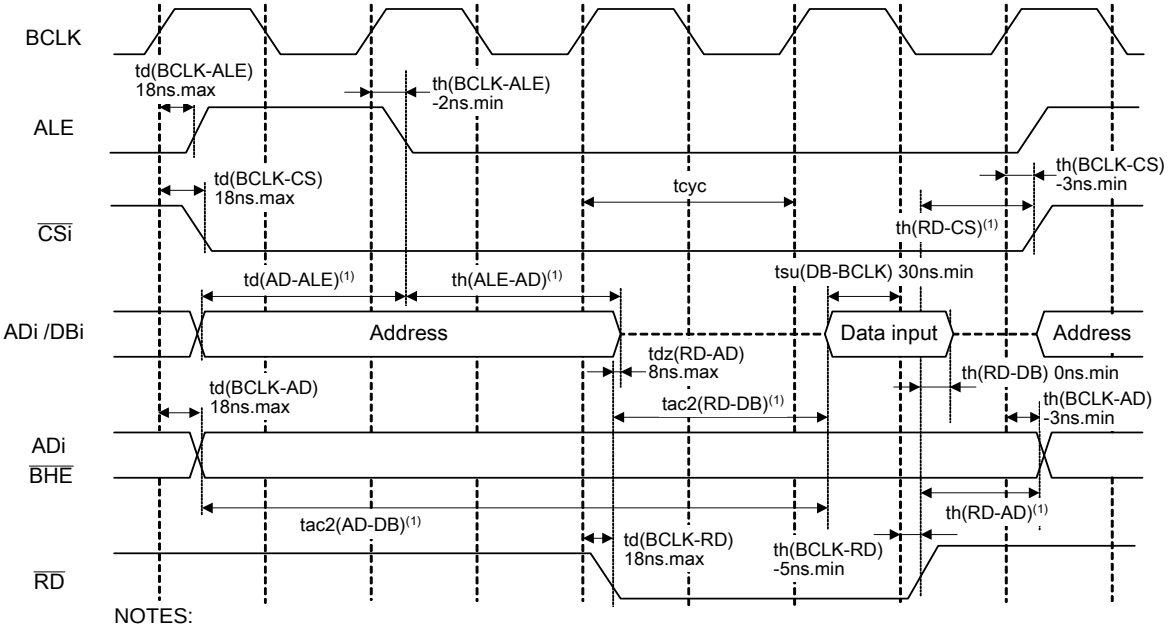
$$tcyc = \frac{10^9}{f(BCLK)}$$

Figure 5.9 VCC1 = VCC2 = 3.3 V Timing Diagram (3)

Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

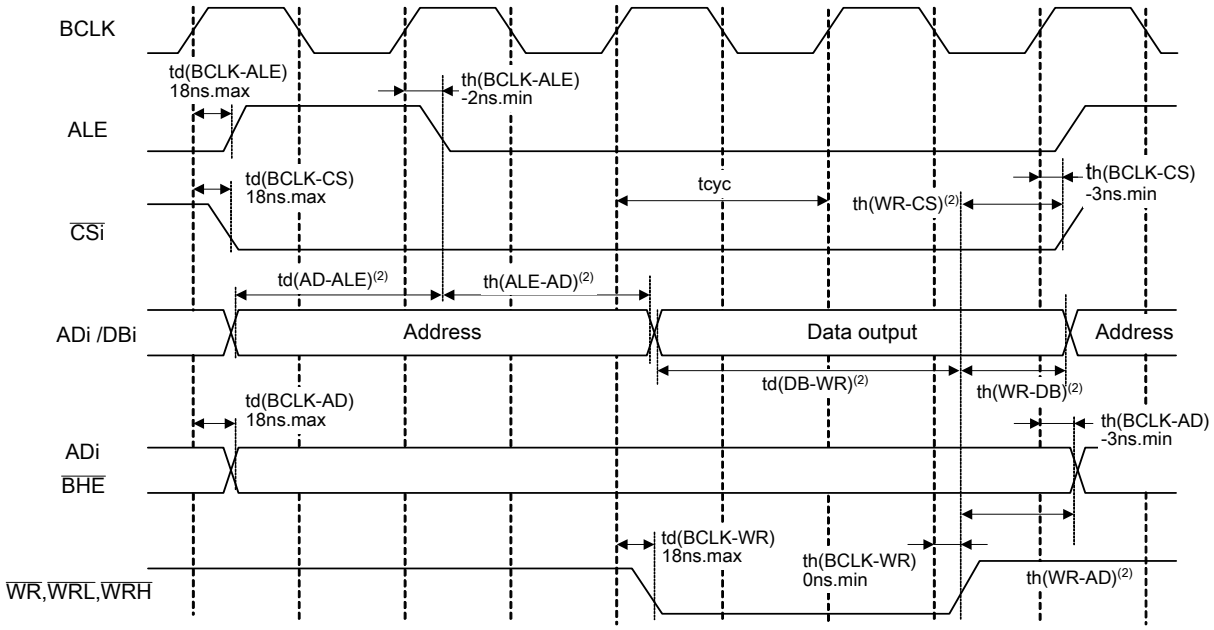
VCC1=VCC2=3.3V

Read Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(RD-AD) = (tcyc / 2 - 10) ns.min, th(RD-CS) = (tcyc / 2 - 10) ns.min
tac2(RD-DB) = (tcyc / 2 x m - 35) ns.max (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)
tac2(AD-DB) = (tcyc / 2 x p - 35) ns.max (if external bus cycle aϕ + bϕ, p = {(a + b - 1) x 2} + 1)

Write Timing (2ϕ + 2ϕ Bus Cycle)



NOTES:
1. Varies with operation frequency:
td(AD-ALE) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(ALE-AD) = (tcyc / 2 x n - 20) ns.min (if external bus cycle aϕ + bϕ, n = a)
th(WR-AD) = (tcyc / 2 - 15) ns.min, th(WR-CS) = (tcyc / 2 - 10) ns.min
th(WR-DB) = (tcyc / 2 - 20) ns.min
td(DB-WR) = (tcyc / 2 x m - 25) ns.min (if external bus cycle aϕ + bϕ, m = (b x 2) - 1)

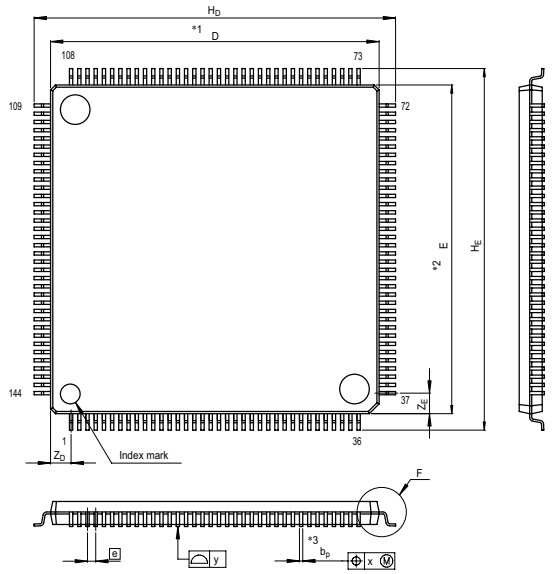
$$tcyc = \frac{10^9}{f(BCLK)}$$

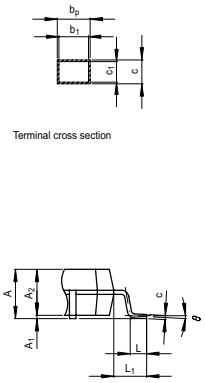
Measurement Conditions:
- VCC1 = VCC2 = 3.0 to 3.6 V
- Input high and low voltage VIH = 1.5 V, VIL = 0.5 V
- Output high and low voltage VOH = 1.5 V, VOL = 1.5 V

Figure 5.10 VCC1 = VCC2 = 3.3 V Timing Diagram (4)

Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g

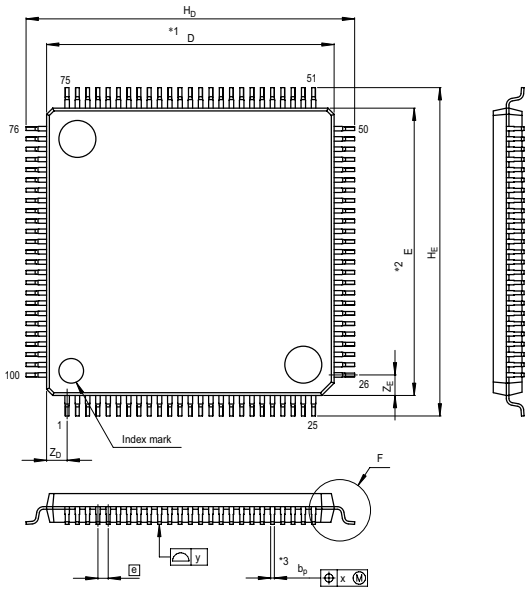


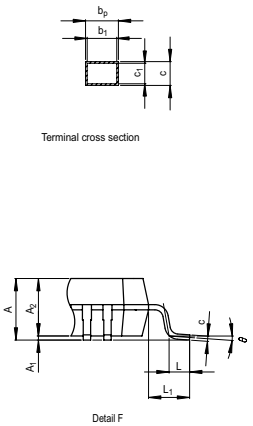


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

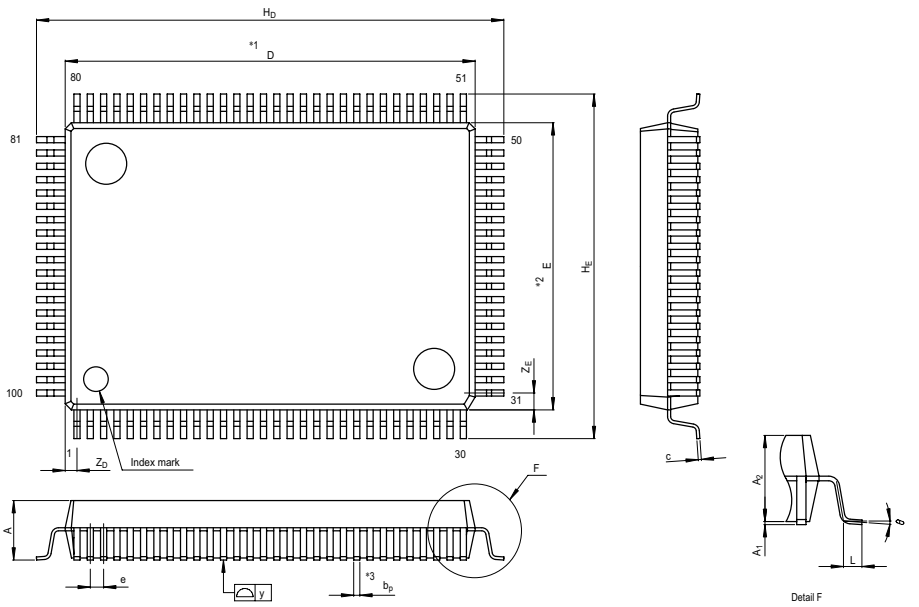




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec.16, 04	–	New Document
1.00	Jul.14, 05	–	**M32C/87A and M32C/87B** added
		–	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		–	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Overview
		2	• **Table 1.2 M32C/87 Group Performance (144-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		3	• **Table 1.2 M32C/87 Group Performance (100-Pin Package)** M32C/87A and M32C/87B performance added to the CAN module performance; Power Consumption performance released
		4	• **Figure 1.1 M32C/87 Group Block Diagram** Note 4 deleted; note 5 added
		7	• **Figure 1.3 Pin Assignment for 144-Pin Package** Note 15 added
		8	• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
		11	• **Figure 1.4 Pin Assignment for 100-Pin Package** Note 19 added
		12	• **Figure 1.5 Pin Assignment for 100-Pin Package** Note 15 added
		13	• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
		17	• **Table 1.6 Pin Description** Note 2 added
			Memory
		22	• **Figure 3.1 Memory Map** Note 3 changed
			Special Function Register (SFR)
		26	• The RLVL register Value after reset modified
		26	• The IIO0IR to IIO11IR registers Value after reset modified
		27 to 30	• Name of the registers assosiated to Intelligent I/O changed
		27	• The G0RB register Value after reset modified
		27	• The G1BCR0 and G1BCR1 registers Value after reset modified
		29	• The G0CR register Value after reset modified
		32 to 37	• Note added to the CAN-associated registers
		40	• The TCSPR register Value after reset modified; note 1 added
		41	• The AD00 register Value after reset modified
		42	• The PSC register Value after reset modified
		42	• The PS2 register Value after reset modified
		43	• The PCR register Value after reset modified
		44	• The PSD1 register Value after reset modified
		45	• The PCR register Value after reset modified
			Electrical Characteristics
		48	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added; min. and max. values for f(RING) added
		49	• **Table 5.3 Electrical Characteristics** V_{OH} values modified**;** R_{PULLUP} value modified
		50	• **Table 5.3 Electrical Characteristics (Continued)** Measurement Condition and standard values for ICC added and some released
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Word Program Time and Lock bit Program Time values modified; parameter All-Unlocked-Block-Erase Time deleted; note 1 deleted
		54	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added

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Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		57	• **Table 5.22 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified
		58	• **Table 5.23 Memory Expansion Mode and Microprocessor Mode** *th(WR-DB)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		60	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)** *tac1(RD-DB)* expression on note 2 modified; *th(WR-DB)* and *tw(ER)* expressions on note 3 modified; *tcyc* expression added
		61	• **Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)** *tac2(RD-DB) and tac2(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(DB-WR)* expression on note 2 modified; *tcyc* expression added
		62	• **Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
		64	• **Table 5.24 Electrical Characteristics** V_{OH} values changed**;** R_{PULLUP} and Icc values modified
		65	• **Table 5.25 A/D Conversion Characteristics** tCONV value modified
		66	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on note 1 modified; *tac2(RD-DB)* expression on note 1 added
		69	• **Table 5.40 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified
		70	• **Table 5.41 Memory Expansion Mode and Microprocessor Mode** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *th(WR-AD)* expression on note 1 modified; *th(ALE-AD)* expression on note 4 modified
		71	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)** *th(BCLK-AD), th(BCLK-CS)* and *th(BCLK-RD)* values modified; *tac1(AD-DB)* expression on note 2 modified; *th(WR-DB)*, *th(WR-AD) and tw(WR)* expression on note 3 modified; *tcyc* expression added
		72	• **Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)** *tac2(RD-DB) and tac1(AD-DB)* expressions on note 1 modified; *th(ALE-AD)* expressions on notes 1 and 2 modified; *td(WR-AD)*, *td(DB-WR) and th(WR-DB)* expressions on note 2 modified; *tcyc* expression added
		73	• **Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)** $\overline{\text{NMI}}$ input diagram added
1.01	Aug. 29, 05		Overview
		17	• **Tables 1.6 Pin Description** Intelligent I/O functions modified
			Special Function Register (SFR)
		29	• The G1BCR0 register Value after reset modified
		29	• The G1BCR1 register Value after reset modified
			Electrical Characteristics
		49	• **Table 5.3 Electrical Characteristics** Icc standard value modified

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.50	Oct 20, 2007	All	**All in this manual** • Descriptions and formats unified • Notation of numbers changed (e.g. 00_2 → 00b, FF_{16} → FFh) • Notation of pin name changed (e.g. RTP00 → RTP_0, A15(/D15) → [A15/D15]) • [Term changed] Serial I/O → Serial interface Clock synchronous serial I/O mode → Clock synchronous mode Clock asynchronous serial I/O mode → Clock asynchronous mode Clock synchronous variable length → Variable data length clock synchronous Voltage detection circuit → Power supply voltage detection function Low voltage detection interrupt → Vdet4 detection interrupt Brown-out detection reset → Vdet3 detection function
			Overview
		1	• Header **SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER → RENESAS MCU**
			• **1.1 Features** title added; **1.1 Applications** changed to **1.1.1 Applications**
		2	• **1.2 Performance Overview** changed to **1.1.2 Specifications**
		2-5	• **Tables 1.1** to **1.4** Structure, descriptions in Specification field, NOTE, and value partially revised or deleted
			• **Real-Time Port** Item deleted; **ROM Correction Function** Item added
		8	• **1.3 Block Diagram** moved following the **1.2 Product List**
		6-7	• **1.2 Product List** Tables revised; NOTE 1 added
		9, 14, 15	• **Figures 1.3** to **1.5** Arrows for VSS and VCC deleted; NOTES partially modified
		11,17	• **Tables 1.9** and **1.13** CLKOUT pin moved from Bus Control Pin column to Control Pin column
		19-22	• **Tables 1.15** to **1.19** Descriptions revised; NOTE 1 added
			Memory
		26	• Text partially modified
			SFR
		34-39	• **Tables 4.8** to **4.13** NOTE “Set the PM13 bit in the PM1 register to 1 (2 wait states for SFR area) before accessing the CAN-associated registers.” added
		45	• **Table 4.19** The PSL5 register added to the Address field of 03BBh item; the PSL7 register added to the Address field of 03BFh item
			• [Register names changed]
		27	002Fh Low Voltage Detection Interrupt Register → Vdet4 Detection Interrupt Register
		34	01C1h UART5 Bit Rate Register → UART5 Baud Rate Register 01C9h UART6 Bit Rate Register → UART6 Baud Rate Register 01D0h UART5, UART6 Transmit/Receive Control Register 2 → UART5, UART6 Transmit/Receive Control Register 01DBh to 01D8h Pulse Output Data Register → RTP Output Buffer Register
		41	0303h to 0302h Timer A1-1 Register → Timer A11 Register 0305h to 0304h Timer A2-1 Register → Timer A21 Register 0307h to 0306h Timer A4-1 Register → Timer A41 Register
		42	0340h Count Start Flag → Count Start Register 0341h Clock Prescaler Reset Flag → Clock Prescaler Reset Register

REVISION HISTORY	M32C/87 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			SFR
		42	• [Register names changed] 0342h One-Shot Start Flag → One-Shot Start Register 0344h Up-Down Flag → Up/Down Select Register
			• [Value After Reset changed]
		27	000Fh WDC 000X XXX$_2$ → 00XX XXXXb
		27	002Fh D4INT 00$_{16}$ → XX00 0000b
		29	007Bh IIO6IC XX00 X000$_2$ → XXXX X000b
		31	00EFh G0CR XX00 X011$_2$ → 0000 X011b
		31	00FEh G0IRF 00$_{16}$ → 0000 XXXXb
		32	013Eh G1IRF 00$_{16}$ → 0000 XXXXb
		34	01C7h to 01C6h U5RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		34	01CFh to 01CEh U6RB XXXX XXXX XXXX 0XXX$_2$ → XXXXh
		44	038Fh to 0382h AD07 to AD01 XXXX$_{16}$ → 00XXh
			Electrical Characteristics
			• [Term changed] Low Voltage Reset → Hardware Reset 2 Low Voltage Detection → Vdet3 and Vdet4 detection circuit
		47	• **Table 5.1** Description in Condition field of Pd (Power consumption) partially modified
		50-53	• **Tables 5.2** to **5.9** f(BCLK) is changed to f(CPU)
		50	• **Table 5.4** Description added in Parameter field of f(CPU); f(VCO) added
		51,69	• **Tables 5.5** to **5.7** and **Tables 5.31** to **5.33** Description in XCOUT and Hysteresis in Parameter fields partially modified
		53,71	• **Table 5.7** and **5.33** Structure and standard values revised; items in Measurement Condition and NOTE added
		54	• **Table 5.8** Description in Parameter field and NOTE partially modified
		54,55	• **Table 5.9** and **5.10** Description in Parameter field and NOTE partially modified
		56,73	• **Tables 5.11** and **5.36** Description in Parameter field and standard value partially modified
		58,74	• **Tables 5.19** and **5.42** added
		59	• **Table 5.24** Values revised; **Table 5.25** and **5.26 added**
		60	• **Table 5.27** Titles modified; NOTE added
		61	• **Table 5.28** moved to the last table in Timing Requirements
		62-63	• **Table 5.29** NOTE 3 added; **Table 26.30** NOTE 5 added
		65-68	• **Figures 5.3** to **5.6** Order rearranged; measurement condition modified
		69-72	• **Table 5.31** to **5.35** f(BCLK) revised to f(CPU)
		75	• **Table 5.47** Values revised; **Table5.48** and **5.49** added
		76	• **Table 5.50** Titles modified; NOTE added
		77	• **Table 5.51** Table moved to the last table in Timing Requirements
		78-79	• **Table 5.52** NOTE 3 added**; Table 5.53** NOTE 5 added
		80-83	• **Figures 5.7** to **5.10** Order rearranged

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