

Description

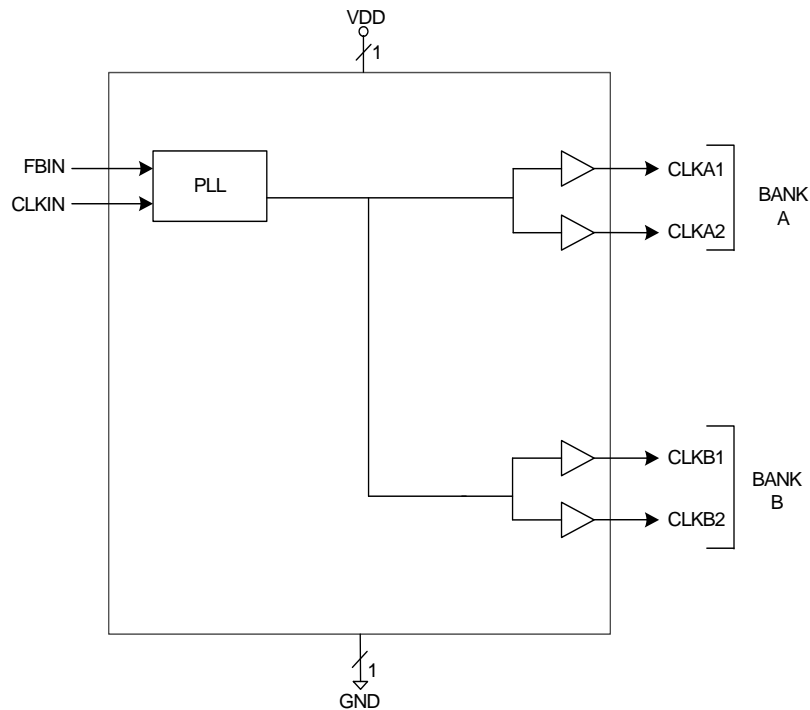
The MK2304-1 is a low jitter, low skew, high performance Phase Lock Loop (PLL) based zero delay buffer for high speed applications. Based on IDT's proprietary low jitter PLL techniques, the device provides four low skew outputs at speeds up to 133 MHz at 3.3 V. The MK2304-1 includes two banks of two outputs each 1X. In the zero delay mode, the rising edge of the input clock is aligned with the rising edges of all 4 outputs. Compared to competitive CMOS devices, the MK2304-1 has the lowest jitter.

IDT manufactures the largest variety of clock generators and buffers and is the largest clock supplier in the world.

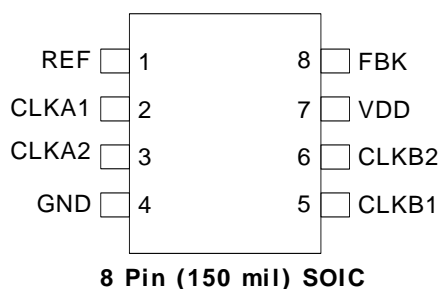
Features

- Packaged in 8-pin SOIC
- Zero input-output delay
- 2 banks of two 1X outputs
- Output to output skew is less than 200 ps
- Output clocks up to 133 MHz at 3.3 V
- Full CMOS outputs with 8 mA output drive capability at TTL levels at 3.3 V
- Spread Smart™ technology Works with Spread Spectrum clock generators
- Advanced, low power, sub micron CMOS process
- Operating voltage of 3.3 V
- Available in industrial temperature range

Block Diagram



Pin Assignment



Feedback Configuration Table

| Feedback From | CLKA1:A2 | CLKB1:B2 |
|---------------|----------|----------|
| Bank A | CLKIN | CLKIN |
| Bank B | CLKIN | CLKIN |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | REF | Input | Clock input. Connect to input clock source. 5 V tolerant input. |
| 2 | CLKA1 | Output | Clock A1 output. |
| 3 | CLKA2 | Output | Clock A2 output. |
| 4 | GND | Power | Connect to ground. |
| 5 | CLKB1 | Output | Clock B1 output. |
| 6 | CLKB1 | Output | Clock B2 output. |
| 7 | VDD | Power | 3.3 V Power Supply. |
| 8 | FBK | Input | PLL feedback input. |

External Components

The Mk2304-1 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1 μ F should be connected between VDD and GND, as close to the part as possible. A 33 Ω series terminating resistor should be used on each clock output to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2304-1. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs, except CLKIN | -0.5 V to VDD+0.5 V |
| CLKIN | -0.5 V to +5.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70 °C |
| Ambient Operating Temperature (industrial) | -40 to +85 °C |
| Storage Temperature | -65 to +150 °C |
| Junction Temperature | 175 °C |
| Soldering Temperature | 260 °C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature (commercial) | 0 | | +70 | °C |
| Ambient Operating Temperature (industrial) | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |

DC Electrical Characteristics

VDD=3.3 V ±10%, Commercial temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|-------------------------|------|------|------|-------|
| Operating Voltage | VDD | | 3.0 | | 3.6 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -8 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 8 mA | | | 0.4 | V |
| Operating Supply Current 100 MHz, CLKIN | IDD | No Load | | 45 | | mA |
| Short Circuit Current | I _{OS} | Each output | | TBD | | mA |
| Input Capacitance | C _{IN} | FBIN | | 7 | | pF |

VDD=3.3 V ±10%, Industrial temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|-------------------------|------|------|------|-------|
| Operating Voltage | VDD | | 3.0 | | 3.6 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -8 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 8 mA | | | 0.4 | V |
| Operating Supply Current 100 MHz, CLKIN | IDD | No Load | | 45 | | mA |
| Short Circuit Current | I _{OS} | Each output | | TBD | | mA |
| Input Capacitance | C _{IN} | FBIN | | 7 | | pF |

AC Electrical Characteristics

VDD = 3.3 V ±10%, Commercial Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|-------------------|--|------|------|------|-------|
| Output Frequency | | FBIN to CLKA1, 30 pF Load | 10 | | 100 | MHz |
| Output Frequency | | FBIN to CLKA1, 15 pF Load | 10 | | 133 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =30 pF | | | 2.2 | ns |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =15 pF | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =30 pF | | | 2.2 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =15 pF | | | 1.5 | ns |
| Output Clock Duty Cycle | | At 1.4 V, CL=30 pf | 40 | 50 | 60 | % |
| Output Clock Duty Cycle | | At 1.4 V, CL=15 pf | 45 | 50 | 55 | % |
| Device to Device skew, equally loaded | | Rising edges at VDD/2 | | | 500 | ps |
| Output to Output skew, equally loaded, On same bank | | Rising edges at VDD/2 | | | 200 | ps |
| Skew from Output Bank A to Output Bank B | | All outputs equally loaded | | | 400 | ps |
| Delay CLKIN Rising Edge to FBIN Rising Edge | | Measured at VDD/2 | | | ±250 | ps |
| Maximum Absolute Jitter | | | | 300 | | ps |
| Cycle to Cycle Jitter | | 30 pF loads 66.67 MHz outputs | | | 200 | ps |
| | | 15pF loads 66.67 MHz outputs | | | 175 | ps |
| PLL Lock Time | t _{LOCK} | Stable power supply, valid clocks on CLKIN, FBIN | | | 1 | ms |

VDD = 3.3V ±10%, Industrial Temperature -40 to +85° C

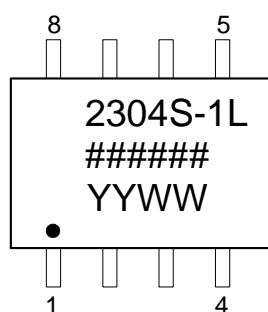
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------|-----------------|-------------------------------------|------|------|------|-------|
| Output Frequency | | FBIN to CLKA1, 30 pF Load | 10 | | 100 | MHz |
| Output Frequency | | FBIN to CLKA1, 15 pF Load | 10 | | 133 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =30 pF | | | 2.5 | ns |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =15 pF | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =30 pF | | | 2.5 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =15 pF | | | 1.5 | ns |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|------------|--|------|------|------|-------|
| Output Clock Duty Cycle | | At 1.4 V, CL=30 pf | 40 | 50 | 60 | % |
| Output Clock Duty Cycle | | At 1.4 V, CL=15 pf | 40 | 50 | 60 | % |
| Device to Device skew, equally loaded | | Rising edges at VDD/2 | | | 500 | ps |
| Output to Output skew, equally loaded, On same bank | | Rising edges at VDD/2 FIN=100 MHz | | | 200 | ps |
| Skew from Output Bank A to Output Bank B | | All outputs equally loaded | | | 400 | ps |
| Delay CLKIN Rising Edge to FBIN Rising Edge | | Measured at VDD/2 | | | ±250 | ps |
| Maximum Absolute Jitter | | | | 300 | | ps |
| Cycle to Cycle Jitter | | 30 pF loads 66.67 MHz outputs | | | 200 | ps |
| | | 15 pF loads 66.67 MHz outputs | | | 175 | ps |
| PLL Lock Time | t_{LOCK} | Stable power supply, valid clocks on CLKIN, FBIN | | | 1 | ms |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 120 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 115 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 105 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 58 | | °C/W |

Marking Diagram (MK2304S-1LF)

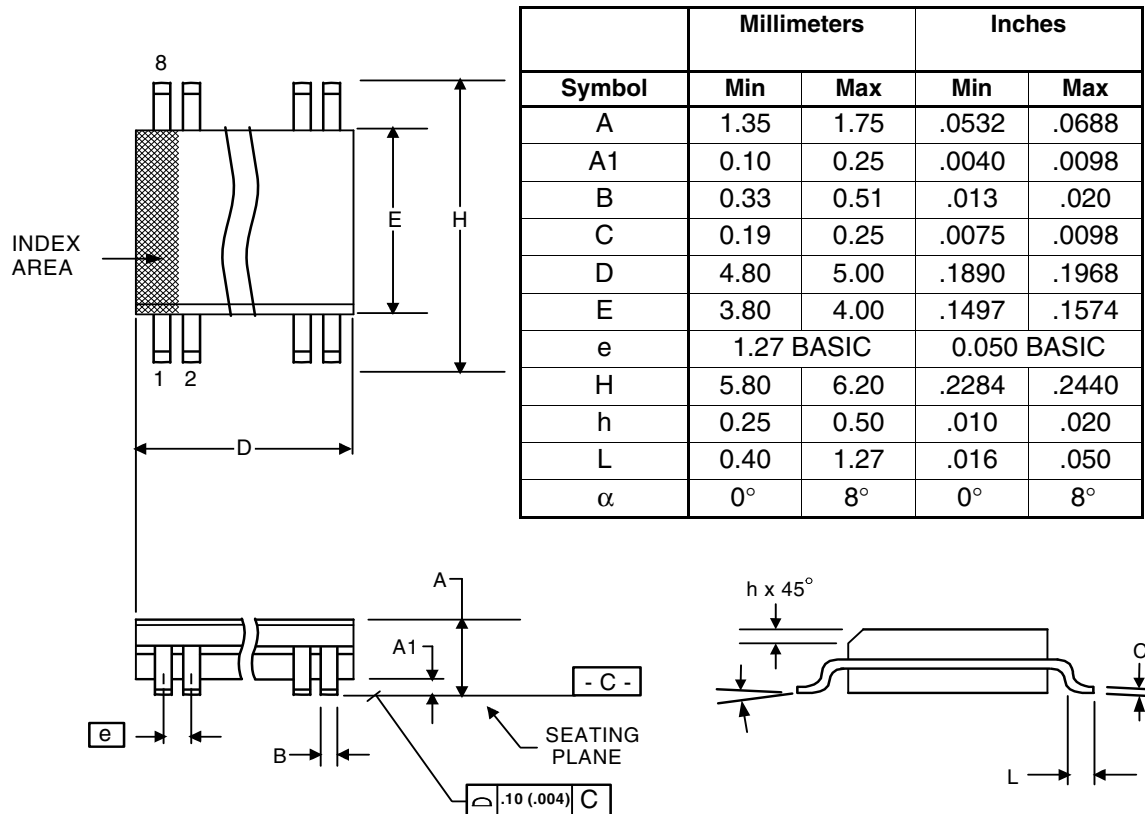


Notes:

- Line 1: part number
- Line 2: ##### = lot number
- Line 3: YYWW = date code.

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|------------|---------------|
| MK2304S-1LF | 2304S-1L | Tubes | 8-pin SOIC | 0 to 70° C |
| MK2304S-1LFT | 2304S-1L | Tape and Reel | 8-pin SOIC | 0 to 70° C |
| MK2304S-1ILF | 2304S1IL | Tubes | 8-pin SOIC | -40° to 85° C |
| MK2304S-1ILFT | 2304S1IL | Tape and Reel | 8-pin SOIC | -40° to 85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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